Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

CS61584A

Dual T1/E1 Line Interface

Features

- Dual T1/E1 Line Interface
- 3.3 Volt and 5 Volt Versions
- Crystal-less Jitter Attenuator Meets European CTR 12 and ETSI ETS 300 011 Specifications
- Matched Impedance Transmit Drivers
- Transmitter Tri-state Capability
- Common Transmit and ReceiveTransformers for all Modes
- Serial and Parallel Host Mode Operation
- User-customizable Pulse Shapes
- Supports JTAG Boundary Scan
- Compliant with:
  - ITU-T Recommendations: G.703, G.704, G.706, G.732, G.775 and I.431
  - American National Standards (ANSI): T1.102, T1.105, T1.403, T1.408, and T1.231
  - FCC Rules and Regulations: Part 68 and Part 15
  - AT&T Publication 62411
  - ETSI ETS 300 011, 300 233, CTR 12, TBR 13
- TR-NET-00499

Description

The CS61584A is a dual line interface for T1/E1 applications, designed for high-volume cards where low power and high density are required. The device is optimized for flexible microprocessor control through a serial or parallel Host mode interface. Hardware mode operation is also available.

Matched impedance drivers reduce power consumption and provide substantial transmitter return loss. The transmitter pulse shapes are customizable to allow non-standard line loads. Crystalless jitter attenuation complies with most stringent standards. Support of JTAG boundary scan enhances system testability and reliability.

ORDERING INFORMATION

See page 53.

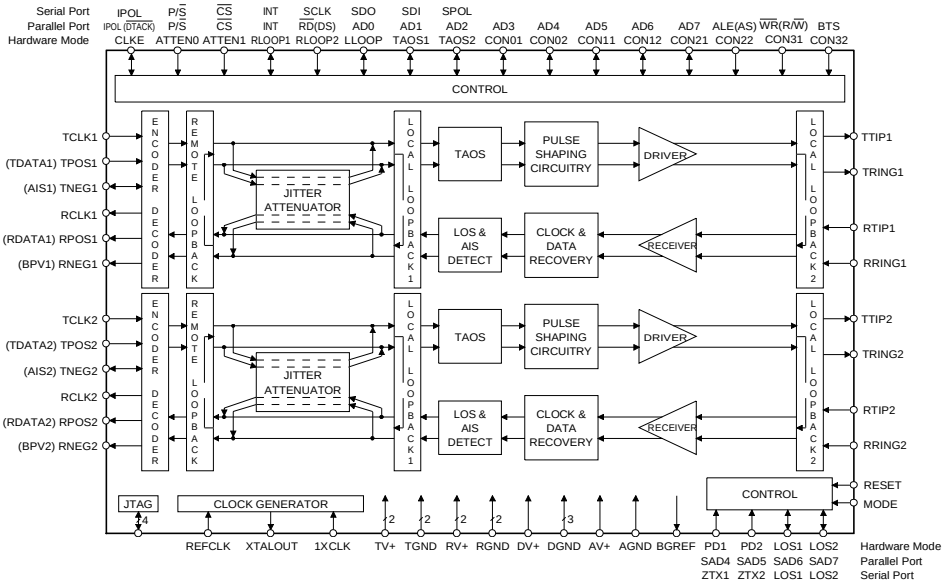

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
DC Supply (TV+1, TV+2, RV+1, RV+2, AV+, DV+) (Note 1)		-	6.0	V
Input Voltage (Any Pin)	V_{in}	RGND - 0.3	(RV+) + 0.3	V
Input Current (Any Pin) (Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C

Notes: 1. Referenced to RGND1, RGND2, TGND1, TGND2, AGND, DGND at 0 V.

2. Transient currents of up to 100 mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter			Symbol	Min	Typ	Max	Unit
DC Supply (TV+1, TV+2, RV+1, RV+2, AV+, DV+)		(Note 3)					V
		3.3 V		3.135	3.3	3.465	
		5.0 V		4.75	5.0	5.25	
Ambient Operating Temperature			T_A	-40	25	85	°C
Power Consumption Per Channel (3.3 V)		(Note 4)	P_C				mW
	T1	(Note 5)		-	310	-	
	T1	(Note 6)		-	190	-	
	E1, 75 Ω	(Note 5)		-	250	-	
	E1, 120 Ω	(Note 5)		-	230	-	
Power Consumption Per Channel (5.0 V)		(Note 4)	P_C				mW
	T1	(Note 5)		-	350	-	
	T1	(Note 6)		-	250	-	
	E1, 75 Ω	(Note 5)		-	320	-	
	E1, 120 Ω	(Note 5)		-	310	-	
REFCLK Frequency	T1	1XCLK = 1		(1.544 - 100 ppm)	1.544	(1.544 + 100 ppm)	MHz
	T1	1XCLK = 0		(12.352 - 100 ppm)	12.352	(12.352 + 100 ppm)	MHz
REFCLK Frequency	E1	1XCLK = 1		(2.048 - 100 ppm)	2.048	(2.048 + 100 ppm)	MHz
	E1	1XCLK = 0		(16.384 - 100 ppm)	16.384	(16.384 + 100 ppm)	MHz

Notes: 3. TV+1, TV+2, AV+, DV+, RV+1, RV+2 should be connected together. TGND1, TGND2, RGND1, GND2, DGND1, DGND2, DGND3 should be connected together.

4. Per channel power consumption while driving line load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.

5. Assumes 100% ones density and maximum line length at maximum supply voltage (3.465 V or 5.25 V).

6. Assumes 50% ones density and 300 ft. line length at typical supply voltage (3.3 V or 5.0 V).

Specifications are subject to change without notice

ANALOG CHARACTERISTICS (T_A = -40 to 85 °C; power supply pins within ±5% of nominal.)

Parameter	Symbol	Min	Typ	Max	Unit
Receiver					
RTIP/RRING Differential Input Impedance		-	20	-	kΩ
Sensitivity Below DSX-1 (0 dB = 2.4 V)		-	-13.6	-	dB
Loss of Signal Threshold		-	0.3	-	V
Data Decision Threshold T1, DSX-1 (Note 7) (Note 8) T1, FCC Part 68 and E1 (Note 9) (Note 10)		60 55 45 40	65 - 50 -	70 75 55 60	% of Peak
Allowable Consecutive Zeros before LOS		160	175	190	bits
Receiver Input Jitter Tolerance (DSX-1, E1) 10 Hz and below (Note 11) 2 kHz 10 kHz - 100 kHz		 300 6.0 0.4	 - - -	 - - -	UI
Receiver Return Loss (Notes 12, 13, and 14) 51 kHz - 102 kHz 102 kHz - 2.048 MHz 2.048 MHz - 3.072 MHz		 12 18 14	 22 24 22	 - - -	dB
Jitter Attenuator					
Jitter Attenuator Corner Frequency T1 (Notes 12 and 15) E1		 1.25 -	 4.0 1.25	 - -	Hz
Attenuation at 10 kHz Jitter Frequency (Notes 12 and 15)		-	60	-	dB
Attenuator Input Jitter Tolerance (Note 12) (Before Onset of FIFO Overflow or Underflow Protection)		28	43	-	UI_{pk-pk}
Transmitter					
Arbitrary Pulse Amplitude at Transformer Secondary T1, DSX-1 T1, DS1 E1, 75 Ω E1, 120 Ω		 - - - -	 73 52 43 52	 - - - -	mV/LSB

Notes:
7. For input amplitude of 1.2 V_{pk} to 4.14 V_{pk}.
8. For input amplitude of 0.5 V_{pk} to 1.2 V_{pk}, and 4.14 V_{pk} to 5.0 V_{pk}.
9. For input amplitude of 1.07 V_{pk} to 4.14 V_{pk}.
10. For input amplitude of 4.14 V_{pk} to 5.0 V_{pk}.
11. Jitter tolerance increases at lower frequencies. Refer to the Receiver section.
12. Not production tested. Parameters guaranteed by design and characterization.
13. Typical performance using the line interface circuitry recommended in the Applications section.
14. Return loss = 20 $\log_{10}$ ABS((z_1 + z_0) / (z_1 - z_0)) where z_1 = impedance of the transmitter or receiver, and z_0 = cable impedance.
15. Attenuation measured with sinusoidal input jitter equal to 3/4 of measured jitter tolerance. Circuit attenuates jitter at 20 dB/decade above the corner frequency. Output jitter can increase significantly when more than 28 UI's are input to the attenuator. The jitter attenuator -3 dB knee in T1 mode is selectable for 4.0 Hz or 1.25 Hz. Refer to the Jitter Attenuator section.

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
Transmitter (Continued)					
AMI Output Pulse Amplitudes (Note 16)					V
E1, 75 Ω (Note 17)		2.14	2.37	2.6	
E1, 120 Ω (Note 18)		2.7	3.0	3.3	
T1, DSX-1 (Note 19)		2.4	3.0	3.6	
Recommended Transmitter Output Load (3.3 V) (Note 16)					Ω
T1		-	24.8	-	
E1, 75 Ω		-	18.6	-	
E1, 120 Ω		-	30.0	-	
Recommended Transmitter Output Load (5.0 V) (Note 16)					Ω
T1		-	76.6	-	
E1, 75 Ω		-	57.4	-	
E1, 120 Ω		-	90.6	-	
Jitter Added During Remote Loopback					UI
10 Hz - 8 kHz		-	0.020	-	
8 kHz - 40 kHz		-	0.015	-	
10 Hz - 40 kHz		-	0.015	-	
Broad Band (Note 20)		-	0.045	-	
Power in 2 kHz band about 772 kHz (Notes 12 and 13) (DSX-1 only)		12.6	15	17.9	dBm
Power in 2 kHz band about 1.544 MHz (Note 12 and 13) (referenced to power in 2 kHz band at 772 kHz, DSX-1 only)		-29	-38	-	dB
Positive to Negative Pulse Imbalance (Notes 12 and 13)					
T1, DSX-1		-	0.2	0.5	dB
E1, amplitude at center fo pulse interval		-5	-	5	%
E1, width at 50% of nominal amplitude		-5	-	5	%
Transmitter Return Loss (Notes 12, 13, and 14)					dB
51 kHz - 102 kHz		8	25	-	
102 kHz - 2.048 MHz		14	18	-	
2.048 MHz - 3.072 MHz		10	12	-	
E1 Short Circuit Current 5.0 V (Note 21)		-	-	50	mA_{rms}
3.3 V		-	70	-	mA_{rms}
E1 and DSX-1 Output Pulse Rise/Fall Times (Note 22)		-	50	-	ns
E1 Pulse Width (at 50% of peak amplitude)		-	244	-	ns
E1 Pulse Amplitude for a space E1, 75 Ω		-0.237	-	0.237	V
E1, 120 Ω		-0.3	-	0.3	V

Notes: 16. Using a transformer that meets the specifications in the Applications section.

17. Measured across 75 Ω at the output of the transmit transformer for CON3/2/1/0 = 0/0/0/0.

18. Measured across 120 Ω at the output of the transmit transformer for CON3/2/1/0 = 0/0/0/1.

19. Measured at the DSX-1 Cross-Connect for line length settings CON3/2/1/0 = 0/0/1/0, 0/0/1/1, 0/1/0/0, 0/1/0/1, and 0/1/1/0 after the length of #22 ABAM cable specified in Table 1.

20. Input signal to RTIP/RRING is jitter free. Values will reduce slightly if jitter free clock is input to TCLK.

21. Transformer secondary shorted with 0.5 Ω resistor during the transmission of 100% ones.

22. At transformer secondary and measured from 10% to 90% of amplitude.

DIGITAL CHARACTERISTICS (T_A = -40 to 85 °C; power supply pins within ±5% of nominal.)

Parameter		Symbol	Min	Max	Unit
High-Level Input Voltage	(Note 23)	V_{IH}	(DV+) - 0.5	-	V
Low-Level Input Voltage	(Note 23)	V_{IL}	-	0.5	V
High-Level Output Voltage (I_{out} = -40 µA)	(Note 24)	V_{OH}	(DV+) - 0.3	-	V
Low-Level Output Voltage (I_{out} = 1.6 mA)	(Note 24)	V_{OL}	-	0.3	V
Input Leakage Current (Digital pins except J-TMS and J-TDI)			-	±10	µA

Notes: 23. Digital inputs are designed for CMOS logic levels.

24. Digital outputs are TTL compatible and drive CMOS levels into a CMOS load.

SWITCHING CHARACTERISTICS (T_A = -40 to 85 °C; power supply pins within ±5% of nominal; Inputs: Logic 0 = 0 V, Logic 1 = DV+.)

Parameter		Symbol	Min	Typ	Max	Unit
T1 Clock/Data						
TCLK Frequency	(Note 25)	f_{tclk}	-	1.544	-	MHz
TCLK Duty Cycle		t_{pwh2}/t_{pw2}	20	50	80	%
RCLK Duty Cycle	(Note 26)	t_{pwh1}/t_{pw1}	45	50	55	%
Rise Time (All Digital Outputs)	(Note 27)	t_r	-	-	65	ns
Fall Time (All Digital Outputs)	(Note 27)	t_f	-	-	65	ns
RPOS/RNEG (RDATA) to RCLK Rising Setup Time		t_{su1}	-	274	-	ns
RCLK Rising to RPOS/RNEG (RDATA) Hold Time		t_{h1}	-	274	-	ns
TPOS/TNEG (TDATA) to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG (TDATA) Hold Time		t_{h2}	25	-	-	ns
E1 Clock/Data						
TCLK Frequency	(Note 25)	f_{tclk}	-	2.048	-	MHz
TCLK Duty Cycle		t_{pwh2}/t_{pw2}	20	50	80	%
RCLK Duty Cycle	(Note 26)	t_{pwh1}/t_{pw1}	45	50	55	%
Rise Time (All Digital Outputs)	(Note 27)	t_r	-	-	65	ns
Fall Time (All Digital Outputs)	(Note 27)	t_f	-	-	65	ns
RPOS/RNEG (RDATA) to RCLK Rising Setup Time		t_{su1}	-	194	-	ns
RCLK Rising to RPOS/RNEG (RDATA) Hold Time		t_{h1}	-	194	-	ns
TPOS/TNEG (TDATA) to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG (TDATA) Hold Time		t_{h2}	25	-	-	ns

Notes: 25. The maximum burst rate of a gapped TCLK input clock is 8.192 MHz. For the gapped clock to be tolerated by the CS61584A, the jitter attenuator must be switched to the transmit path of the line interface. The maximum gap size that can be tolerated on TCLK is 28 UIp-p.

26. RCLK duty cycle may be outside the specified limits when the jitter attenuator is in the transmit path and when the jitter attenuator is employing the overflow/underflow protection mechanism.

27. At max load of 50 pF.

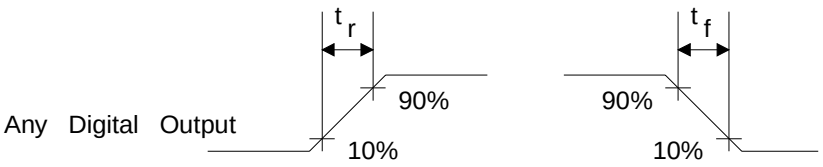

Figure 1. Signal Rise And Fall Characteristics

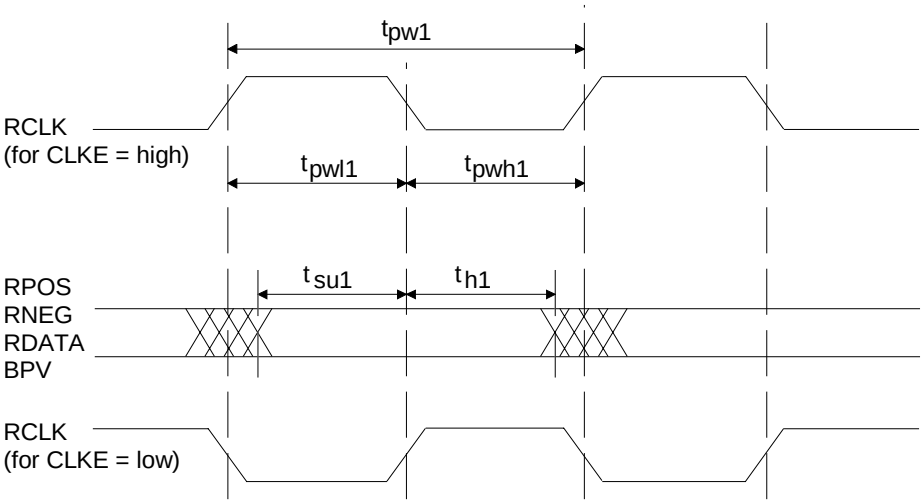

Figure 2. Recovered Clock and Data Switching Characteristics

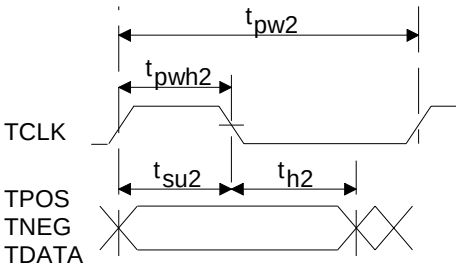

Figure 3. Transmit Clock and Data Switching Characteristics

SWITCHING CHARACTERISTICS - SERIAL PORT (T_A = -40 to 85 °C; DV+, TV+, RV+ = nominal ± 0.3 V; Inputs: Logic 0 = 0 V, Logic 1 = RV+)

Parameter		Symbol	Min	Typ	Max	Unit
SDI to SCLK Setup Time		t_{dc}	25	-	-	ns
SCLK to SDI Hold Time		t_{cdh}	25	-	-	ns
SCLK Low Time		t_{cl}	50	-	-	ns
SCLK High Time		t_{ch}	50	-	-	ns
SCLK Rise and Fall Time		t_r, t_f	-	-	15	ns
$\overline{CS}$ to SCLK Setup Time		t_{cc}	20	-	-	ns
SCLK to $\overline{CS}$ Hold Time	(Note 28)	t_{cch}	20	-	-	ns
$\overline{CS}$ Inactive Time		t_{cwh}	100	-	-	ns
SDO Valid to SCLK	(Note 29)	t_{cdv}	-	-	50	ns
$\overline{CS}$ to SDO High Z		t_{cdz}	-	50	-	ns

Notes: 28. If SPOL = 0, then $\overline{CS}$ should return high no sooner than 20 ns after the 16th rising edge of SCLK during a serial port read.

29. Output load capacitance = 50 pF.

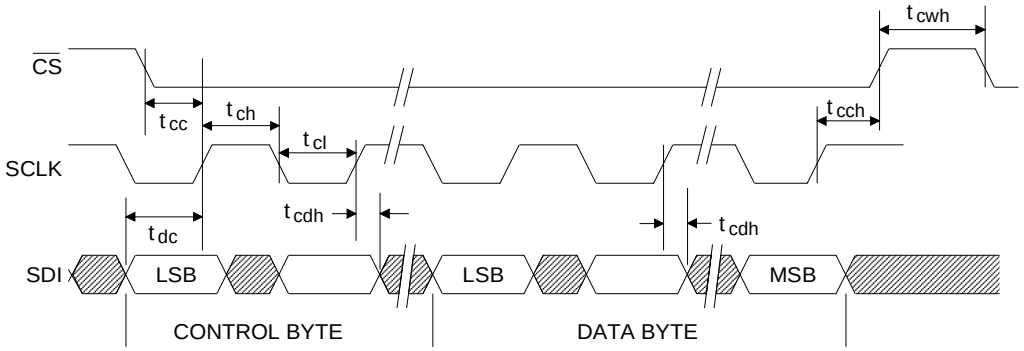

Figure 4. Serial Port Write Timing Diagram

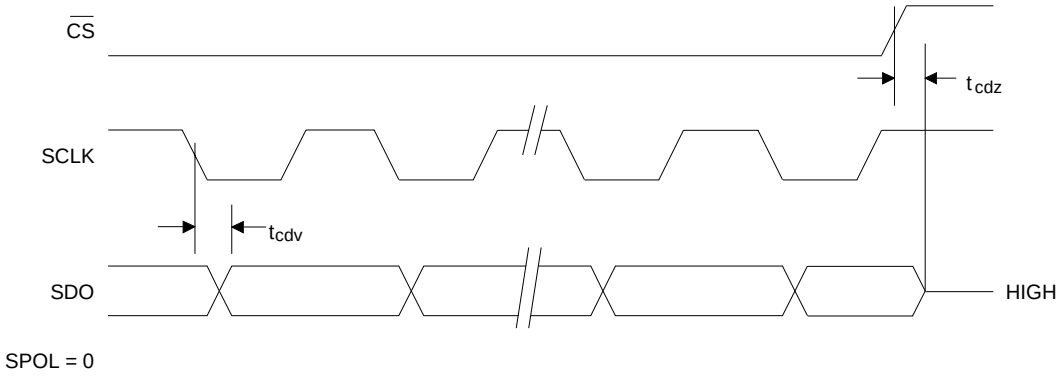

Figure 5. Serial Port Read Timing Diagram

SWITCHING CHARACTERISTICS - PARALLEL PORT (T_A = -40 to 85 °C;

TV+, RV+ = nominal ± 0.3 V; Inputs: Logic 0 = 0 V, Logic 1 = RV+)

Parameter	Symbol	Min	Max	Unit
Cycle Time	t_{cyc}	250	-	ns
Pulse Width, DS Low or $\overline{RD}$ High	PW_{el}	150	-	ns
Pulse Width, DS High or $\overline{RD}$ Low	PW_{eh}	150	-	ns
Input Rise/Fall Times	t_r, t_f	-	30	ns
R/$\overline{W}$ Hold Time	t_{rwh}	10	-	ns
R/$\overline{W}$ Setup Time Before DS High	t_{rws}	50	-	ns
$\overline{CS}$ Setup Time Before DS, $\overline{WR}$, or $\overline{RD}$ Active	t_{cs}	50	-	ns
$\overline{CS}$ Setup Time Before DS, $\overline{WR}$, or $\overline{RD}$ Active for RAM/ROM	t_{csr}	130	-	ns
$\overline{CS}$ Hold Time	t_{ch}	20	-	ns
Read Data Hold Time	t_{dhr}	10	80	ns
Write Data Hold Time	t_{dhw}	5	-	ns
Muxed Address Valid to AS or ALE Fall	t_{asl}	15	-	ns
Muxed Address Hold Time	t_{ahl}	10	-	ns
Delay Time DS, $\overline{WR}$, or $\overline{RD}$ to AS or ALE Rise	t_{asd}	25	-	ns
Pulse Width AS or ALE High		40	-	ns
Delay Time AS or ALE to DS, $\overline{WR}$, or $\overline{RD}$	t_{ased}	40	-	ns
Output Data Delay Time from DS or $\overline{RD}$	t_{ddr}	20	120	ns
Data Setup Time	t_{dsw}	80	-	ns
$\overline{DTACK}$ Delay	t_{dkd}	5	-	ns
$\overline{DTACK}$ Hold Time	t_{dkh}	5	-	ns
AS/ALE Min Low Interval for RAM/ROM	t_{aamir}	50	-	ns

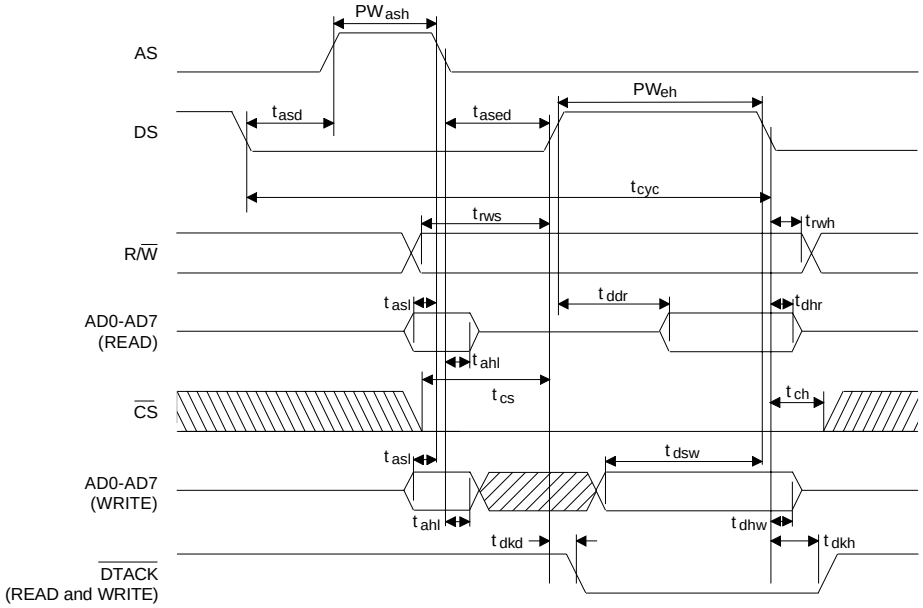

Figure 6. Parallel Port Timing - Motorola Mode

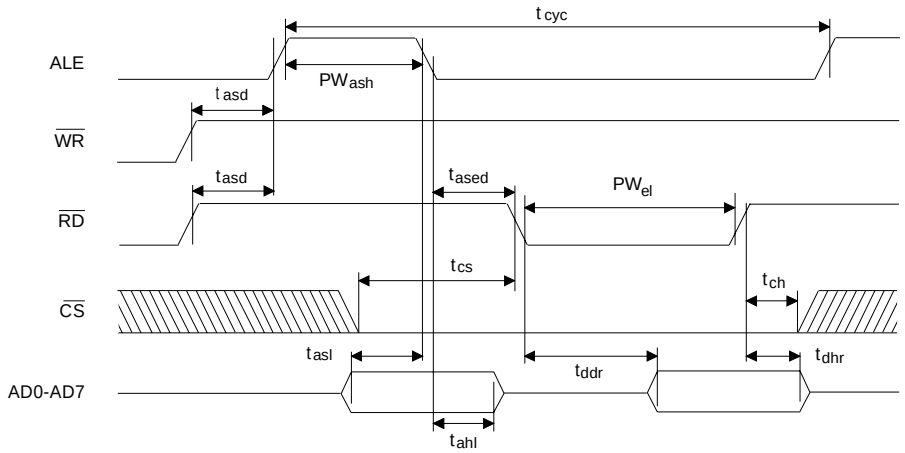

Figure 7. Parallel Port Timing - Intel Read Mode

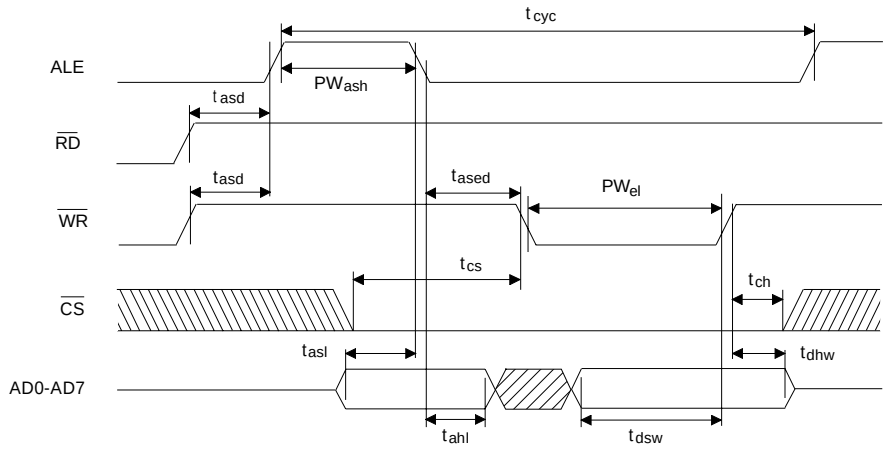

Figure 8. Parallel Port Timing - Intel Write Mode

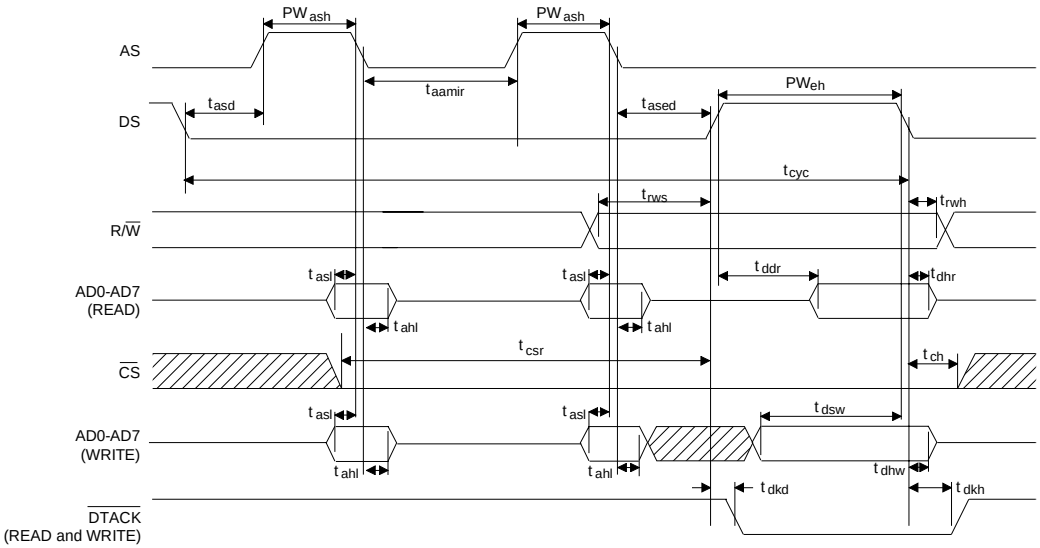

Figure 9. Parallel Port Timing - Motorola Mode to RAM

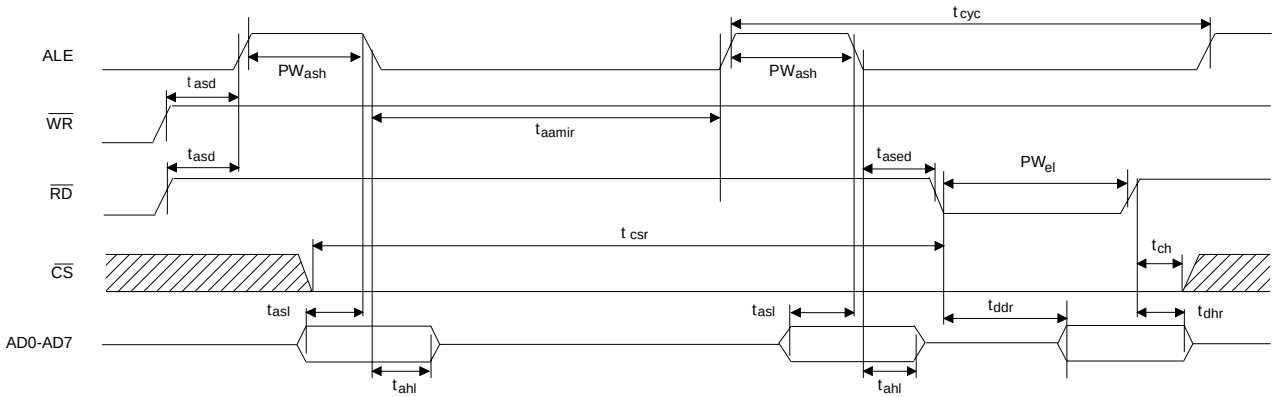

Figure 10. Parallel Port Timing - Intel Read Mode from RAM or ROM

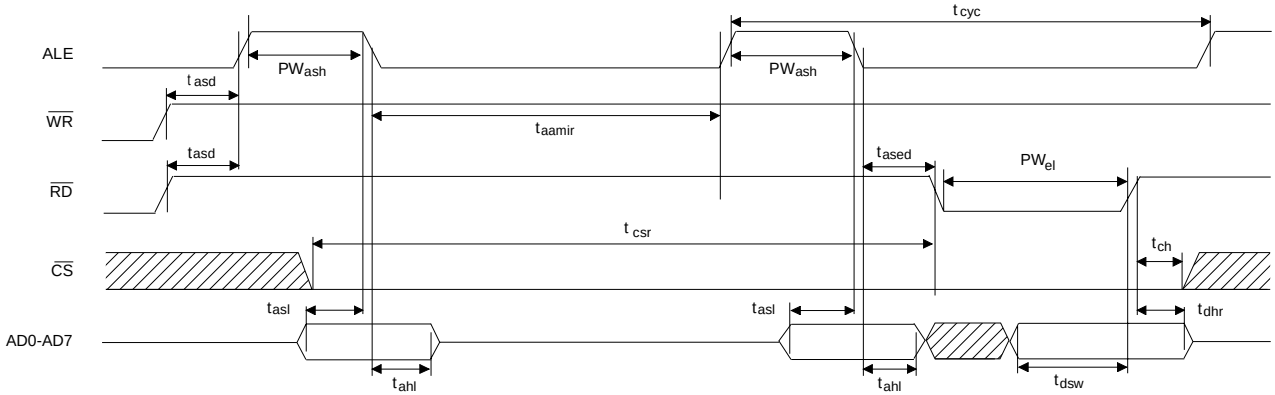

Figure 11. Parallel Port Timing - Intel Write Mode to RAM

SWITCHING CHARACTERISTICS - JTAG (T_A = -40 to 85 °C; TV+, RV+ = nominal ± 0.3 V; Inputs: Logic 0 = 0 V, Logic 1 = RV+)

Parameter	Symbol	Min	Max	Unit
Cycle Time	t_{cyc}	200	-	ns
J-TMS/J-TDI to J-TCK Rising Setup Time	t_{su}	50	-	ns
J-TCK Rising to J-TMS/J-TDI Hold Time	t_h	50	-	ns
J-TCK Falling to J-TDO Valid	t_{dv}	-	60	ns

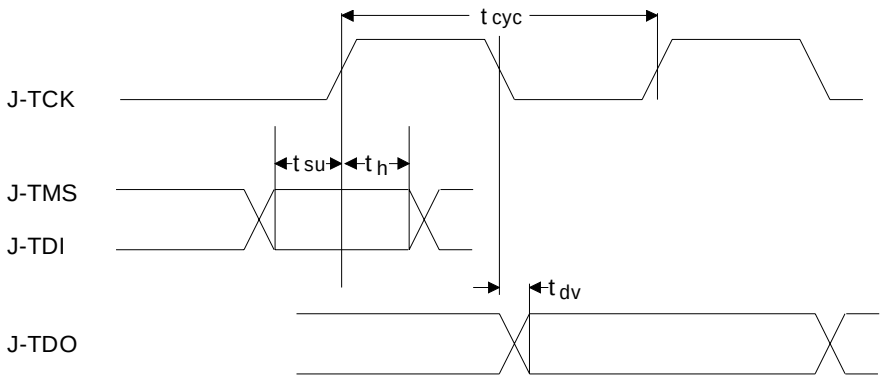

Figure 12. JTAG Switching Characteristics

2. OVERVIEW

The CS61584A is a dual line interface for T1/E1 applications, designed for high-volume cards where low power and high density are required. The device can be operated in either Hardware mode using control pins or in Host mode using an internal register set. One board design can support all T1/E1 short-haul modes by only changing component values in the receive and transmit paths (if REFCLK and TCLK are connected externally). Figure 13 illustrates applications of the CS61584A in various environments.

The line driver generates waveforms compatible with E1 (CCITT G.703), T1 short haul (DSX-1) and T1 FCC Part 68 Option A (DS1). A single transformer turns ratio is used for all waveform types. The driver internally matches the impedance of the load, providing excellent return loss to insure superior T1/E1 pulse quality. An additional benefit of the internal impedance matching is a 50 percent reduction in power consumption compared to implementing return loss using external resistors that causes the transmitter to drive the equivalent of two line loads.

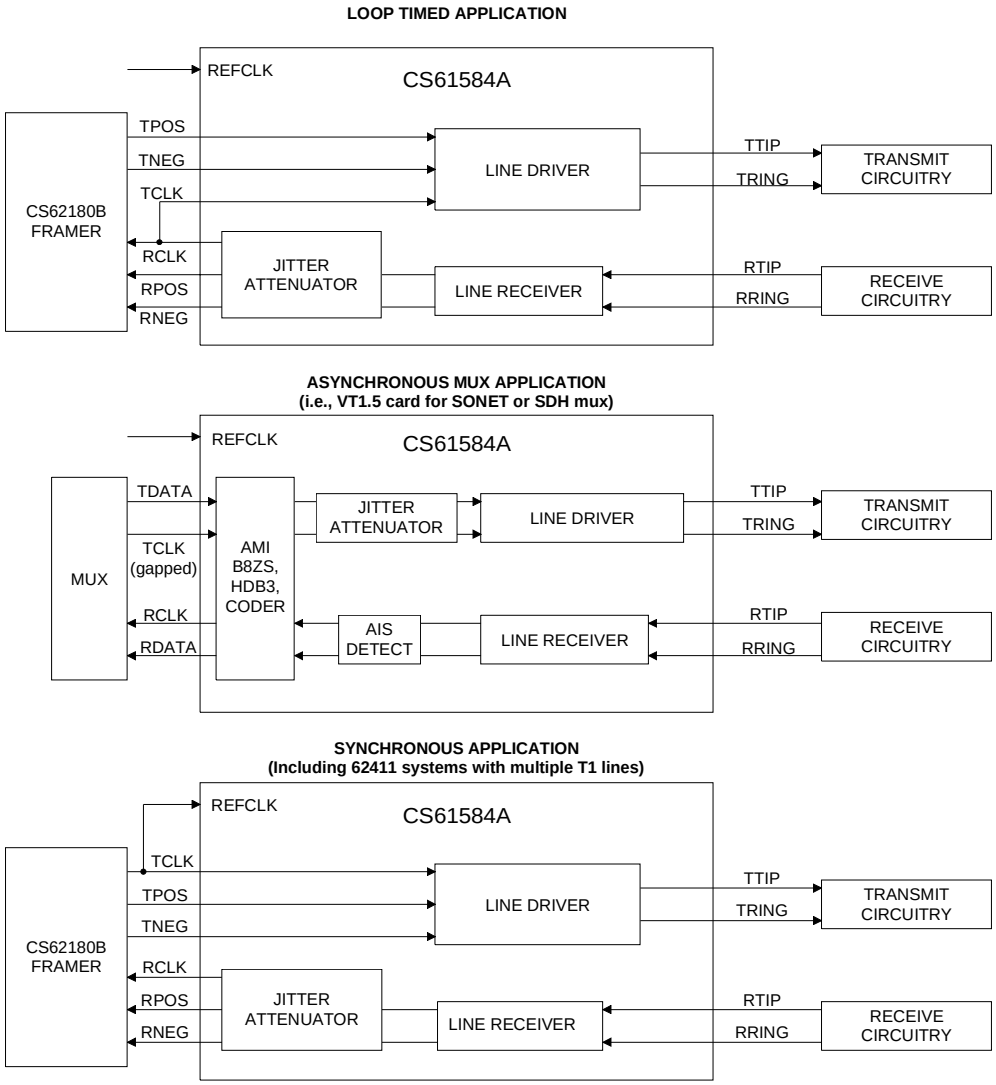

Figure 13. Examples of CS61584A Applications

The line receiver contains all the necessary clock and data recovery circuits.

The jitter attenuator meets AT&T 62411 requirements when using either a 1X or 8X reference clock supplied by either a quartz crystal, crystal oscillator, or external reference at the REFCLK input pin.

2.1 AT&T 62411 Customer Premises Application

The AT&T 62411 specification applies to the T1 interface between the customer premises and the carrier, and must be implemented by the customer premises equipment in order to connect to the AT&T network.

In 62411 applications, the management of jitter is a very important design consideration. Typically, the jitter attenuator is placed in the receive path of the CS61584A to reduce the jitter input to the system synchronizer. The jitter attenuated recovered clock is used as the input to the transmit clock to implement a loop-timed system. A Stratum 4 (±32 ppm) quality clock or better should be input to REFCLK. Note that any jitter present on the reference clock will not be filtered by the jitter attenuator.

2.2 Asynchronous Multiplexer Application

Asynchronous multiplexers accept multiple T1/E1 lines (which are asynchronous to each other), and combine them into a higher speed transmission rate (e.g. M13 muxes and SONET muxes). In these systems, the jitter attenuator is placed in the transmit path of the CS61584A to remove the gapped clock jitter input by the multiplexer to TCLK. Because the transmit clock is jittered, the reference clock to the CS61584A is provided by an external source operating at 1X or 8X the data rate. Because T1/E1 framers are not usually required in asynchronous multiplexers, the B8ZS/AMI/HDB3 coders in the CS61584A are activated to provide data interfaces on TDATA and RDATA.

2.3 Synchronous Application

A typical example of a synchronous application is a T1 card in a central office switch or a 0/1 digital cross-connect system. These systems place the jitter attenuator in the receive path to reduce the jitter presented to the system. A Stratum 3 or better system clock is input to the CS61584A transmit and reference clocks.

3. TRANSMITTER

The transmitter accepts data from a T1 or E1 system and outputs pulses of appropriate shape to the line. The transmit clock (TCLK) and transmit data (TPOS and TNEG, or TDATA) are supplied synchronously. Data is sampled on the falling edge of the TCLK input.

During Hardware mode operation, the configuration pins (CON[3:0]) control transmitted pulse shapes, transmitter source impedance, receiver slicing level, and driver tristate as shown in Table 1. During Host mode operation, the configuration is established by the CON[3:0] bits in the Control B registers. Typical output pulses are shown in Figures 14 and 15. These pulse shapes are fully pre-defined by circuitry in the CS61584A, and are fully compliant with appropriate standards when used with our application guidelines in standard installations. Both channels must be operated at the same line rate (both T1 or both E1).

Host mode operation permits arbitrary transmit pulse shapes to be created and downloaded to the CS61584A. These custom pulse shapes can be used to compensate for waveform degradation caused by non-standard cables, transformers, or protection circuitry (refer to the Arbitrary Waveform Registers section).

Note that the pulse width for Part 68 Option A (324 ns) is narrower than the optimal pulse width for DSX-1 (350 ns). The CS61584A automatically adjusts the pulse width based on the configuration selection.

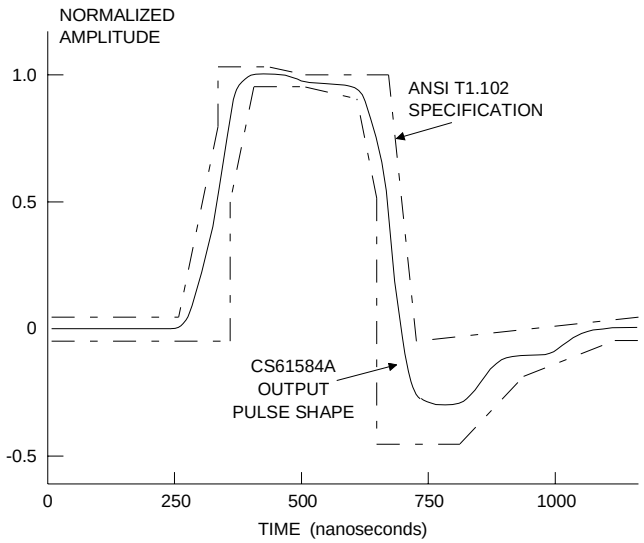

Figure 14. Typical Pulse Shape at DSX-1 Cross Connect

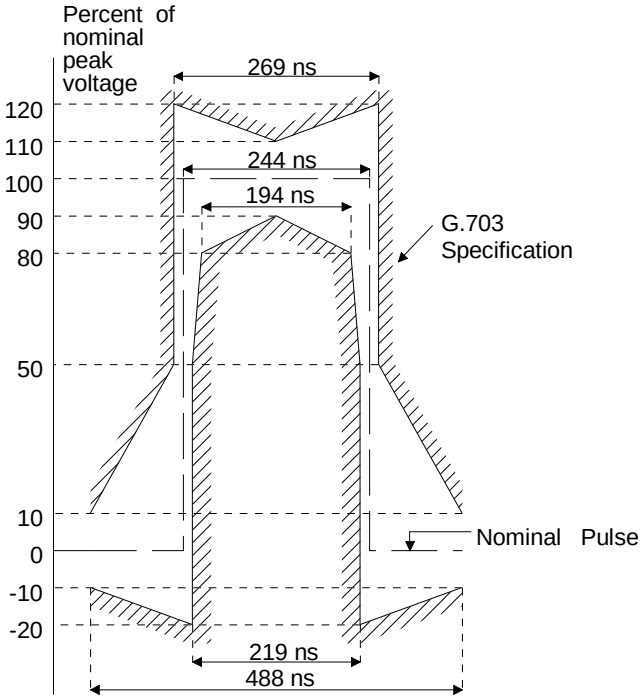

Figure 15. Mask of the Pulse at the 2048 kbps Interface

CON3	CON2	CON1	CON0	Transmit Pulse Width at 50% Amplitude	Transmit Pulse Shape	Receiver Slicing Level	Line Code Encoder / Decoder
0	0	0	0	244 ns (50%)	E1: square, 2.37 V into 75 Ω	50%	AMI/HDB3
1	0	0	0	244 ns (50%)	Arbitrary E1 Wave into 75 Ω	50%	AMI/HDB3
0	0	0	1	244 ns (50%)	E1: square, 2.37 V into 75 Ω	50%	AMI/HDB3
1	0	0	1	244 ns (50%)	Arbitrary E1 Wave into 120 Ω	50%	AMI/HDB3
0	0	1	0	350 ns (54%)	DSX-1: 0-133 ft.	65%	AMI/B8ZS
0	0	1	1	350 ns (54%)	DSX-1: 133-266 ft.	65%	AMI/B8ZS
0	1	0	0	350 ns (54%)	DSX-1: 266-399 ft.	65%	AMI/B8ZS
0	1	0	1	350 ns (54%)	DSX-1: 399-533 ft.	65%	AMI/B8ZS
0	1	1	0	350 ns (54%)	DSX-1: 533-655 ft.	65%	AMI/B8ZS
1	0	1	0	350 ns (54%)	Arbitrary DSX-1 Waveform	65%	AMI/B8ZS
0	1	1	1	324 ns (50%)	DS1: FCC Part 68 Option A with undershoot	65%	AMI/B8ZS
1	1	0	0	324 ns (50%)	DS1: FCC Part 68 Option A (0 dB)	65%	AMI/B8ZS
1	0	1	1	324 ns (50%)	Arbitrary DS1 Waveform	65%	AMI/B8ZS
1	1	0	1	Reserved			
1	1	1	0	Transmit Hi Z	Tristate TTIP/TRING Driver Outputs	50%	AMI/HDB3
1	1	1	1	Transmit Hi Z	Tristate TTIP/TRING Driver Outputs	65%	AMI/B8ZS

Table 1. Line Configuration Selections

The transmitter impedance changes with the line length options in order to match the load impedance (75 Ω for E1 coax, 100 Ω for T1, 120 Ω for E1 shielded twisted pair), providing a minimum of 14 dB return loss for T1 and E1 frequencies during the transmission of both marks and spaces. This improves signal quality by minimizing reflections from the transmitter. Impedance matching also reduces load power consumption by a factor of two when compared to the return loss achieved by using external resistors.

The CS61584A driver will automatically detect an inactive TLCK (i.e., no data clocked to the driver) or REFCLK input. When either of these conditions are detected the driver is forced to the tristate (high-impedance) condition. If the jitter attenuator is in the transmit path, the driver will tristate after 170 to 182 TCLK clock cycles. If the attenuator is not in the transmit path, the driver will tristate after 4 to 12 TCLK clock cycles. During Host mode operation, the CLKLOST bit in the Status register goes high to indicate when the driver is tristated due to the absence of TCLK or REFCLK. The driver exits the tristate condition when four clock cycles are input to TCLK. On power-up or reset, the driver is tristated until REFCLK is present and four clock cycles are input to TCLK. In Host mode the driver will have to be taken out of the tristate condition by writing the CON[3:0]. The driver is not forced to the tristate condition during remote loopback if TCLK is absent.

When the transmit configuration established by CON[3:0], TAOS, or LLOOP changes state, the transmitter stabilizes within 22 TCLK bit periods. The transmitter takes longer to stabilize when RLOOP1 or RLOOP2 is selected because the timing circuitry must adjust to the new frequency from RCLK.

When the transmitter transformer secondaries are shorted through a 0.5 Ω resistor, the transmitter will output a maximum of 50 mA-rms, as required by the European specification BS6450. This spec is met for 5.0 V operation only.

4. RECEIVER

The input signal is connected to the receiver through a step down transformer (1.15:1 for 5 V and 2:1 for 3.3 V). Data and clock are extracted from the T1/E1 signal input to the line interface and to the system. The signal is detected differentially across the receive transformer and can be recovered over the entire range of short haul cable lengths. The transmit and receive transformer specifications are identical and are presented in the Applications section. As shown in Table 1, the receiver slicing level is set at 65% for DS1/DSX-1 short-haul and at 50% for all other applications.

The clock recovery circuit is a second-order phase locked loop that can tolerate up to 0.4 UI of jitter from 10 kHz to 100 kHz without generating errors (Figure 13). The clock and data recovery circuit is tolerant of long strings of consecutive zeros and will successfully recover a 1-in-175 jitter-free line input signal.

Recovered data at RPOS and RNEG (or RDATA) is stable and may be sampled using the recovered clock RCLK. During Hardware mode operation,

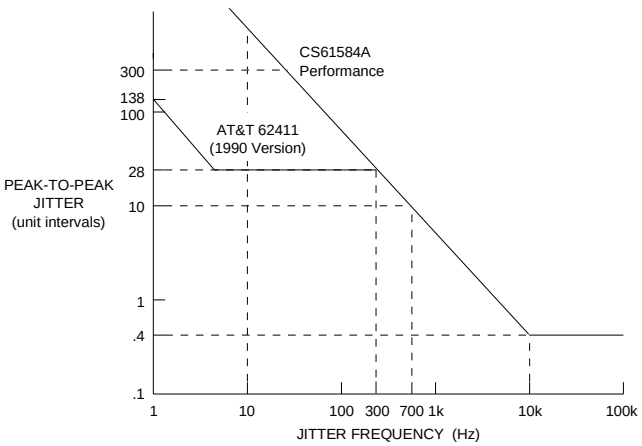

Figure 16. Minimum Input Jitter Tolerance of Receiver (Clock Recovery Circuit and jitter Attenuator)

the CLKE pin determines the clock polarity where the output data is stable and valid as shown in Table 2. During Host mode operation, the polarity is established by the CLKE bit in the Control A register. When CLKE is low, RPOS and RNEG (or RDATA) are valid on the rising edge of RCLK. When CLKE is high, RPOS and RNEG (or RDATA) are valid on the falling edge of RCLK

During Host mode operation, the data at RPOS and RNEG (or RDATA) may be forced to output an unframed all-ones pattern by setting both the LLOOP1 and LLOOP2 bits in the Control B register to "1".

CLKE	DATA	CLOCK	Clock edge for valid data
LOW	RPOS, RNEG or RDATA	RCLK RCLK	Rising Rising
HIGH	RPOS, RNEG or RDATA	RCLK RCLK	Falling Falling

Table 2. Recovered Data/Clock Options

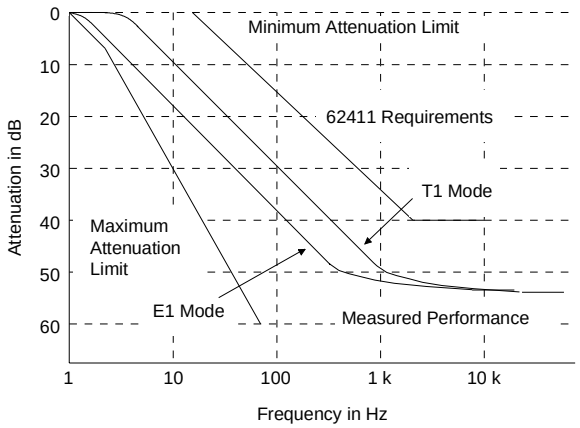

Figure 17. Typical Jitter Transfer Function

5. JITTER ATTENUATOR

The jitter attenuator can be switched into either the receive or transmit paths. Alternatively, it can also be removed from both paths to reduce the propagation delay. Figure 14 illustrates the typical jitter attenuation curves.

During Hardware mode operation, the location of the jitter attenuators for both channels is controlled by the ATTEN0 and ATTEN1 pins. During Host mode operation, the location of the jitter attenuators are independent and are controlled by the ATTEN[1:0] bits in the Control A registers. Table 3 shows how these pins are decoded.

The attenuator consists of a 64-bit FIFO, a narrowband monolithic PLL, and control logic. Signal jitter is absorbed in the FIFO which is designed to neither overflow nor underflow. If overflow or underflow is imminent, the jitter transfer function is altered to ensure that no bit-errors occur. Under this condition, jitter gain may occur and external provisions may be required. The jitter attenuator will typically tolerate 43 UIs before the overflow/underflow mechanism occurs. If the jitter attenuator has not had time to "lock" to the average incoming frequency (e.g. following a device reset) the attenuator will tolerate a minimum of 22 UIs before the overflow/underflow mechanism occurs.

The jitter attenuator -3 dB knee frequency is 4.0 Hz for T1 mode and 1.25 Hz for E1 mode as selected by the CON[3:0] pins or register bits. A 1.25 Hz knee for the E1 mode guarantees jitter attenuation compliance to European specifications CTR 12 and ETSI ETS 300 011. Setting ATTEN[1:0] = 11 will place the jitter attenuator in the receive path with a 1.25 Hz knee for both T1 and E1 modes of operation.

For T1/E1 line cards used in high-speed mutiplexers (e.g., SONET and SDH), the jitter attenuator is typically used in the transmit path. The attenuator can accept a transmit clock with gaps ≤ 28 UIs and a transmit clock burst rate of ≤ 8 MHz.

ATTEN1	ATTEN0	Location of Jitter Attenuator
0	0	Receiver
0	1	Disabled
1	0	Transmitter
1	1	Receiver w/ 1.25 Hz knee

Table 3. Jitter Attenuation Control

6. REFERENCE CLOCK

The CS61584A requires a reference clock with a minimum accuracy of ±100 ppm for T1 and E1 applications. This clock can be either a 1X clock (i.e., 1.544 MHz or 2.048 MHz), or can be a 8X clock (i.e., 12.352 MHz or 16.384 MHz) as selected by the 1XCLK pin. This clock may be supplied from internal system timing or a CMOS crystal oscillator and input to the REFCLK pin. An 8X quartz crystal may be connected across the REFCLK and XTALOUT pins and the 1XCLK pin set low. The quartz crystal and CMOS crystal oscillator specifications and are presented in the Applications section.

In systems with a jittered transmit clock, the reference clock should not be tied to the transmit clock and a separate external quartz crystal or crystal oscillator should drive the reference clock input. Any jitter present on the reference clock will not be filtered by the jitter attenuator.

7. POWER-UP RESET

On power-up, the device is held in a static state until the power supply achieves approximately 60% of the power supply voltage. When this threshold is crossed, the device waits another 10 ms to allow the power supply to reach operating voltage and then calibrates the transmit and receive circuitry. This initial calibration takes less than 20 ms but can occur only if REFCLK and TCLK are present.

Power-up reset initializes the control logic and register set and performs the same functions as the RESET pin. During Host mode operation, a reset event is indicated by the Latched-Reset bit in the Status register.

8. LINE CONTROL AND MONITORING

Line control and monitoring of the CS61584A may be implemented in either Hardware or Host mode. Hardware mode is selected when the MODE pin is set low and allows the device to be configured and monitored using control pins. Host mode is selected when the MODE pin is set high and allows the device to be configured and monitored using an internal register set.

The following controls and indications are available in Hardware mode: line length selection, receive clock edge, jitter attenuator location, loss of signal, transmit all ones, local loopback, remote loopback, and power down. Host mode operation offers several additional control options (refer to the Host Mode section).

Note: Please refer to the Loop Selection Equations in the Applications section.

8.1 Line Code Encoder/Decoder

Hardware mode supports only transparent operation to permit the line code to be encoded and decoded by an external T1/E1 framing device. Recovered data is output on the RNEG and RPOS pins in NRZ format and transmitted data is input on the TNEG and TPOS pins.

Host mode supports transparent, AMI, B8ZS, or HDB3 line encoding and decoding for applications not using an external T1/E1 framer (i.e. multiplexers). The CODER, AMI-T, and AMI-R bits in the Control A registers select the coder mode for a given channel. The selection of the transmit encoder is independent from the selection of the receive decoder. When CODER = 1, the transmit data is input to the encoder on TDATA and the receive data is output from the decoder on RDATA in NRZ format.

8.2 Alarm Indication Signal

During Host mode operation, the alarm indication signal (AIS) is detected by the receiver and reported using the AIS and Latched-AIS bits in the Status registers. The receiver detects the AIS condition on observation of 99.9% ones density in a 5.3 ms period (< 9 zeros in 8192 bits). If CODER = 1 in the Control A registers, the TNEG pin becomes the AIS output pin that is set high on detection of AIS. The AIS condition is exited when ≥ 9 zeros are detected in 8192 bits.

8.3 Bipolar Violation Detection

During Host mode operation, a bipolar violation (BPV) is detected by the receiver and reported using the Latched-BPV bit in the Status registers. If CODER = 1 in the Control A registers, the RNEG pin becomes the BPV output strobe pin that is set high for one bit period on detection of a BPV. Note that B8ZS (or HDB3) zero substitutions are not flagged as bipolar violations if the B8ZS (or HDB3) decoder has been enabled (CODER = 1 and AMI-R = 0 in the Control A registers).

8.4 Excessive Zeros Detection

During Host mode operation if CODER = 1 and EXZ = 1 in the Control A register, the BPV output pin is OR'ed with receive excessive zero events. In AMI mode when AMI-Rx = 1, the BPV pin is set high for one bit period when 16 or more consecutive zeros are received. In B8ZS mode when AMI-Rx = 0, the BPV pin is set high for one bit period when 8 or more consecutive zeros are received. This is in accordance with the ANSI T1.231 specification. For E1 operation with HDB3 disabled, the excessive zeros detection is also disabled. For E1 with HDB3 enabled the BPV pin goes high for every set of 4 consecutively received zeros.

8.5 Loss of Signal

During Hardware mode and Host mode operation, the loss of signal (LOS) condition is detected by the receiver and reported when the LOS pin is set high. Loss of signal is indicated when 175 ±15 consecutive zeros are received, or when the receive (RTIP/RRING) signal level drops below the receiver sensitivity of the device. The LOS condition is exited according to the ANSI T1.231-1993 criteria that requires a minimum 12.5% ones density signal over 175 ±75 bit periods with no more than 100 consecutive zeros. During LOS, recovered data is squelched and zeroes are output on RPOS/RNEG (RDATA).

During Host mode operation, LOS is reported using the LOS and Latched-LOS bits in the Status registers. Note that both the LOS pin and register indications are available in Host mode operation. The LOS pin and/or bit is set high when the device is reset, in power-up, or a channel is powered-down and returns low when data is recovered by the receiver.

During LOS condition the RPOS (RDATA), RNEG pins are forced low, except when LLOOP1 (digital loopback) is enabled, or when the AAO (Automatic All Ones) bit is set in the channel 1 mask register. Setting the AAO bit high forces unframed all ones pattern out on the RPOS (RDATA), RNEG pins when LOS condition occurs.

When the jitter attenuator is in the receive path and LOS occurs, the frequency of the last valid recovered signal is held at RCLK. When the jitter attenuator is not in the receive path, the output frequency becomes the frequency of the reference clock.

8.6 Transmit All Ones

During Hardware mode operation, transmit all ones (TAOS) is selected by setting the TAOS pin high. During Host mode, TAOS is controlled using the TAOS bit in the Control B registers.

Selecting TAOS causes continuous ones to be transmitted to the line on TTIP and TRING at the frequency of REFCLK. In this mode, the transmit data inputs TPOS and TNEG (or TDATA) are ignored. A TAOS request overrides the data transmitted to the line interface during local and remote loopbacks. Note that the CLKLOST interrupt is not available for TCLK in the TAOS mode.

8.7 Receive All Ones

During Host mode operation, the data at RPOS and RNEG (or RDATA) may be forced to output an unframed all-ones pattern by setting both the LLOOP1 and LLOOP2 bits in the Control B register to "1". An automatic Receive All Ones (AAO)

response to a Loss of Signal condition for either channel is activated by setting bit 1 of the channel 1 Mask register to 1.

8.8 Local Loopback

Selecting LLOOP causes the TCLK, TPOS, and TNEG (or TDATA) inputs to be looped back through the jitter attenuator (if enabled) to the RCLK, RPOS, and RNEG (or RDATA) outputs. The receive line interface is ignored, but data at TPOS and TNEG (or TDATA) continues to be transmitted to the line interface at TTIP and TRING. During Hardware mode operation, simultaneous local loopback 2 of both channels is selected by setting the LLOOP pin high. During Host mode operation, local loopback 1 on a per channel basis is controlled using the LLOOP1 bit in the Control B registers.

During Hardware mode operation, a per channel local loopback 1 is performed when both the RLOOP and TAOS pins are high. The data at TPOS and TNEG is overridden with an all-ones pattern (TAOS) and the receive input at RTIP and RRING is ignored.

During Host mode operation, local loopback 2 can also be selected using the LLOOP2 bit in the Control B registers. Selecting LLOOP2 causes the TCLK, TPOS, and TNEG (or TDATA) inputs to be looped back to the RCLK, RPOS, and RNEG (or RDATA) outputs. The line driver, line receiver, and jitter attenuator (if enabled) are also included. The receive line interface is ignored, but data at TPOS and TNEG (or TDATA) continues to be transmitted to the line interface at TTIP and TRING.

A TAOS request overrides the data transmitted to the line interface during both local loopbacks. A TAOS request also overrides the data received at RPOS and RNEG (or RDATA) during local loopback 2. Note that simultaneous selection of local and remote loopback modes is not valid.

8.9 Remote Loopback

During Hardware mode operation, remote loopbacks of either channel is selected by setting the RLOOP pin high. During Host mode operation, remote loopback of each channel is controlled using the RLOOP bit in the Control B registers.

Selecting RLOOP causes the data received from the line interface at RTIP and RRING to be looped back through the jitter attenuator (if enabled) and retransmitted on TTIP and TRING. Data input to TPOS and TNEG (or TDATA) is ignored, but data recovered from RTIP and RRING continues to be output on RPOS and RNEG (or RDATA).

Remote loopback is functional if TCLK is absent. A TAOS request overrides the data transmitted to the line interface during a remote loopback. Note that simultaneous selection of local and remote loopback modes is not valid.

8.10 Driver Tristate

The drivers may be independently tristated in all modes of operation. During Hardware mode operation, setting the CON[3:0] pins of a channel to "111X" will tristate the driver. During Host mode serial port operation, the ZTX1 and ZTX2 pins perform the driver tristate function and setting the CON[3:0] bits in the Control B registers to "111X" will also tristate the driver. During Host mode parallel port operation, setting the CON[3:0] bits in the Control B register to "111X" tristates the driver. In host mode, the CS61584A powers up with CON[3:0] set to 1110, which tristates the transmitter.

8.11 Power Down

During Hardware mode operation, channel power down is selected by setting the PD1 or PD2 pin high. During Host mode operation, channel power down is controlled using the PD bit in the Control A registers. Power down places the transmitter, receiver, and jitter attenuator in reset. The RCLK, RPOS, RNEG, RDATA, AIS, BPV, TTIP, and TRING output pins are placed in a high-impedance

state. LOS will go high, and the status register will be reset, but the Control, Mask, and Arbitrary Waveform registers remain unchanged. The channel not in power down and the processor port will still to operate normally.

Simultaneously selecting PD1 and PD2 will place all the above-mentioned pins in high impedance state and power down additional analog circuitry that is shared by both channels. The status registers are reset. In the hardware mode all output pins are tri-stated and internally pulled up to the positive supply rail. After exiting the power down state, the channel will be fully operational in less than 20 ms.

8.12 Reset Pin

The CS61584A is continuously calibrated during operation to insure the performance of the device over power supply and temperature. This continuous calibration function eliminates the need to reset the line interface during operation.

During Hardware and Host modes of operation, a device reset is selected by setting the RESET pin high for a minimum of 200 ns. The reset function initiates on the falling edge of RESET and requires less than 20 ms to complete. The control logic and register set are initialized and the transmit and receive circuitry is calibrated if REFCLK and TCLK are present. During Host mode operation, a reset event is indicated by the Latched-Reset bit in the Status register.

9. HOST MODE

Host mode allows the CS61584A to be configured and monitored using an internal register set. This option is selected when the MODE pin is set high. Using the P/$\overline{S}$ pin, serial or 8-bit parallel interface ports are available in Host mode. During serial port operation, the registers are specified by a 6-bit address in the range of 0x10 to 0x19. During parallel port operation, the registers are specified by an 8-bit address. The four most significant bits of the address selects one of 16 devices on the board, established by the SAD[7:4] pins. The four least significant bits of the address specify the register address in the range of 0x00 to 0x09 for the selected device. Parallel port option is compatible with Motorola and Intel 8-bit, multiplexed address/data bus.

9.1 Register Set

The register set available during Host mode operation is presented in Table 4.

Serial Port Address	Parallel Port Address*	Description
0x10	0xY0	Ch 1 Status
0x11	0xY1	Ch 2 Status
0x12	0xY2	Ch 1 Mask
0x13	0xY3	Ch 2 Mask
0x14	0xY4	Ch 1 Control A
0x15	0xY5	Ch 2 Control A
0x16	0xY6	Ch 1 Control B
0x17	0xY7	Ch 2 Control B
0x18	0xY8	Ch 1 Arbitrary Pulse Shape
0x19	0xY9	Ch 2 Arbitrary Pulse Shape

*Y denotes the SAD[7:4] address of the CS61584A device.

Table 4. CS61584A Register Set

9.1.1 Status Registers

The Status registers are read-only registers and are shown in Table 5. The CS61584A generates an interrupt on the $\overline{INT}$ pin any time an unmasked Status register bit changes. When BTS is low (Intel mode), the IPOL pin determines the polarity of the $\overline{INT}$ pin. When BTS is high (Motorola mode), $\overline{INT}$ polarity is active low (IPOL becomes $\overline{DTACK}$). Reading both Status register clears the interrupt and deactivates the $\overline{INT}$ pin.

LOS: Set high while the loss of signal condition is detected. Reading the Status register does not clear the LOS bit. A LOS interrupt is generated only on the falling edge of the LOS alarm condition. The Latched-LOS bit generates an interrupt on the rising edge of LOS. Refer to the timing diagram in Figure 18.

Latched-LOS: Set high on the rising edge of the loss of signal condition. Reading the Status register clears the Latched-LOS bit and deactivates the $\overline{INT}$ pin. Refer to the timing diagram in Figure 18.

AIS: Set high while the alarm indication signal is detected. Reading the Status register does not clear the AIS bit. An AIS interrupt is generated only on the falling edge of the AIS alarm condition. The Latched-AIS bit generates an interrupt on the rising edge of AIS. Refer to the timing diagram in Figure 18.

Status Register (Channel 1) Serial Port Address: 0x10; Parallel Port Address: 0xY0				
Bit	**Description**	**Definition**		**Reset Value**
		1	**0**	
7	LOS1	LOS currently detected	no LOS	1
6	Latched-LOS1	LOS event since last read	no LOS	1
5	AIS1	AIS currently detected	no AIS	0
4	Latched-AIS1	AIS event since last read	no AIS	0
3	Latched-BPV1	BPV event since last read	no BPV	0
2	Latched-Overflow1	Pulse overflow since last read	no overflow	0
1	Latched-Reset	Reset event since last read	no reset	1
0	Interrupt1	Interrupt event since last read	no interrupt	1

Status Register (Channel 2) Serial Port Address: 0x11; Parallel Port Address: 0xY1				
Bit	**Description**	**Definition**		**Reset Value**
		1	**0**	
7	LOS2	LOS currently detected	no LOS	1
6	Latched-LOS2	LOS event since last read	no LOS	1
5	AIS2	AIS currently detected	no AIS	0
4	Latched-AIS2	AIS event since last read	no AIS	0
3	Latched-BPV2	BPV event since last read	no BPV	0
2	Latched-Overflow2	Pulse overflow since last read	no overflow	0
1	Latched-CLKLOST	TCLK or REFCLK absent	TCLK and REFCLK present	0
0	Interrupt2	Interrupt event since last read	no interrupt	1

Table 5. Status Registers

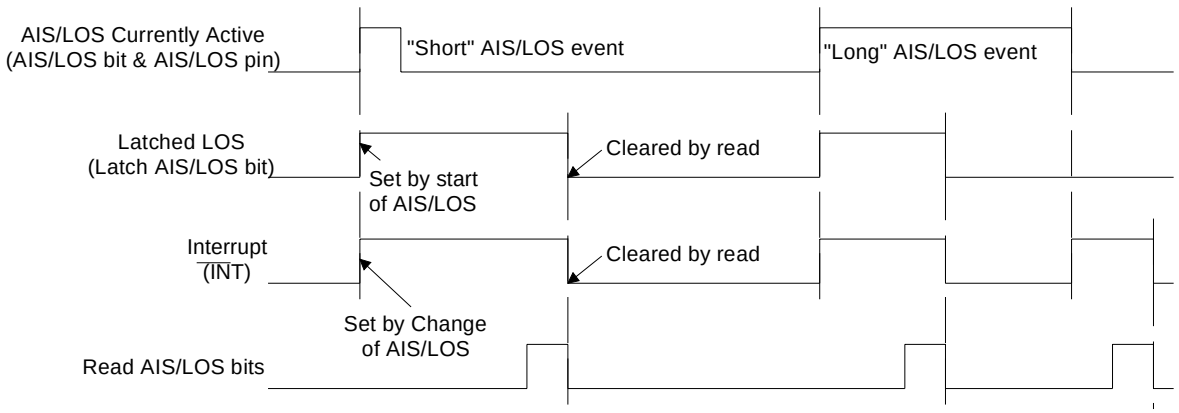

Figure 18. Alarm Indication Event Relationships

Latched-AIS: Set high on the rising edge of the alarm indication signal condition. Reading the Status register clears the Latched-AIS bit and deactivates the $\overline{INT}$ pin. Refer to the timing diagram in Figure 18.

Latched-BPV: Indicates a bipolar violation has been received since the last read of the Status register. Reading the Status register clears the Latched-BPV bit and deactivates the $\overline{INT}$ pin. This bit is set only when the line code decoder is enabled in the Control A register.

Latched-Overflow: Indicates a waveform generated using the Arbitrary Waveform register has exceeded full scale since the last read of the Status register. Reading the Status register clears the Latched-Overflow bit and deactivates the $\overline{INT}$ pin.

Latched-Reset: Indicates a reset event (power-up or RESET pin) has occurred since the last read of the Status register. Reading the Status register clears the Latched-Reset bit and deactivates the $\overline{INT}$ pin. This bit is not maskable.

Latched-CLKLOST: Set high when TCLK or REFCLK are absent. Reading the Status register clears the Latched-CLKLOST bit and deactivates the $\overline{INT}$ pin.

Interrupt: Indicates a change in the Status register since the last read. Reading the Status register clears the Interrupt bit and deactivates the $\overline{INT}$ pin.

9.1.2 Mask Registers

The Mask registers are read-write registers and are shown in Table 6. The Mask registers disables the interrupts in the corresponding Status register on a per-bit basis. Masking a Status register bit forces it to remain at zero and prevents the $\overline{INT}$ pin from activating on the condition.

Mask Register (Channel 1) Serial Port Address: 0x12; Parallel Port Address: 0xY2				
Bit	**Description**	**Definition**		**Reset Value**
		1	**0**	
7	Mask LOS1	Mask Interrupt	Enable Interrupt	0
6	Mask Latched-LOS1	Mask Interrupt	Enable Interrupt	0
5	Mask AIS1	Mask Interrupt	Enable Interrupt	0
4	Mask Latched-AIS1	Mask Interrupt	Enable Interrupt	0
3	Mask Latched-BPV1	Mask Interrupt	Enable Interrupt	0
2	Mask Latched-Overflow1	Mask Interrupt	Enable Interrupt	0
1	Automatic All Ones, AAO	Ones at RPOS/NEG on LOS	Zeros at RPOS/NEG on LOS	0
0	Mask Interrupt1	Mask Interrupt	Enable Interrupt	0

Mask Register (Channel 2) Serial Port Address: 0x13; Parallel Port Address: 0xY3				
Bit	**Description**	**Definition**		**Reset Value**
		1	**0**	
7	Mask LOS2	Mask Interrupt	Enable Interrupt	0
6	Mask Latched-LOS2	Mask Interrupt	Enable Interrupt	0
5	Mask AIS2	Mask Interrupt	Enable Interrupt	0
4	Mask Latched-AIS2	Mask Interrupt	Enable Interrupt	0
3	Mask Latched-BPV2	Mask Interrupt	Enable Interrupt	0
2	Mask Latched-Overflow2	Mask Interrupt	Enable Interrupt	0
1	Mask Latched-CLKLOST	Mask Interrupt	Enable Interrupt	0
0	Mask Interrupt2	Mask Interrupt	Enable Interrupt	0

Table 6. Mask Registers