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CS61880

Octal E1 Line Interface Unit

Features

- **Octal E1 Short-haul Line Interface Unit**
- **Low Power**
- **No External Component Changes for 120 Ω / 75 Ω Operation**
- **Pulse Shapes can be customized by the user**
- **Internal AMI, or HDB3 Encoding/Decoding**
- **LOS Detection per ITU G.775 or ETSI 300- 233**
- **G.772 Non-Intrusive Monitoring**
- **G.703 BITS Clock Recovery**
- **Crystal-less Jitter Attenuation**
- **Serial/Parallel Microprocessor Control Interfaces**
- **Transmitter Short Circuit Current Limiter (<50 mA)**
- **TX Drivers with Fast High-Z and Power Down**
- **JTAG Boundary Scan compliant to IEEE 1149.1**
- **144-Pin LQFP or 160-Pin FBGA Package**

ORDERING INFORMATION

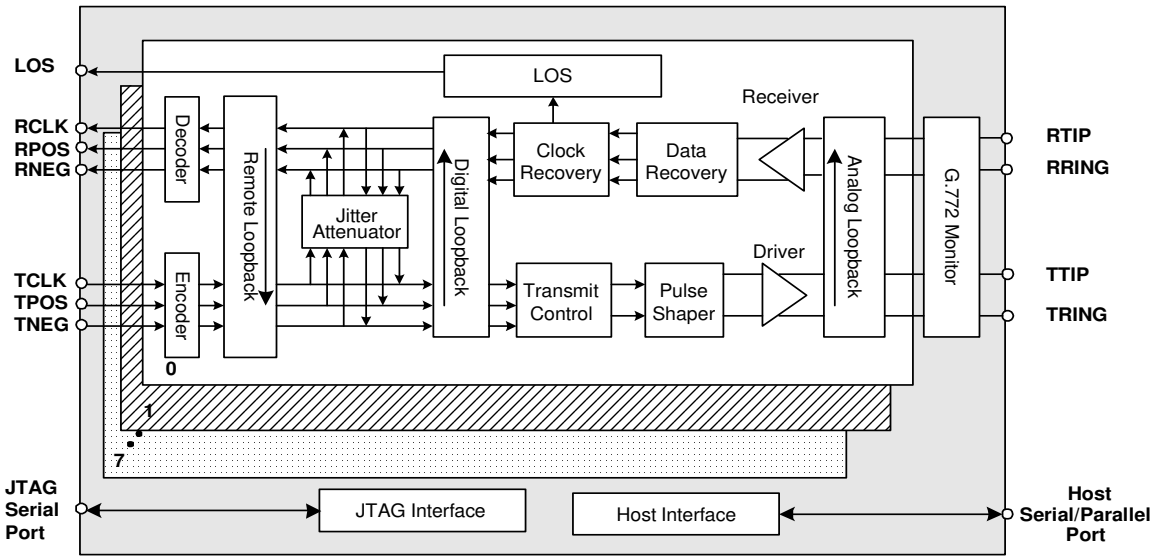
CS61880-IQ	144-pin LQFP
CS61880-IB	160-pin FBGA

Description

The CS61880 is a full-featured Octal E1 short-haul LIU that supports 2.048 Mbps data transmission for both E1 75 Ω and E1 120 Ω applications. Each channel provides crystal-less jitter attenuation that complies with the most stringent standards. Each channel also provides internal AMI/HDB3 encoding/decoding. To support enhanced system diagnostics, channel zero can be configured for G.772 non-intrusive monitoring of any of the other 7 channels' receive or transmit paths.

The CS61880 makes use of ultra low power matched impedance transmitters and receivers to reduce power beyond that achieved by traditional driver designs. By achieving a more precise line match, this technique also provides superior return loss characteristics. Additionally, the internal line matching circuitry reduces the external component count. All transmitters have controls for independent power down and High-Z.

Each receiver provides reliable data recovery with over 12 dB of cable attenuation. The receiver also incorporates LOS detection compliant to the most recent specifications.



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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Contacting Cirrus Logic Support

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To find the one nearest to you go to: **http://www.cirrus.com/**

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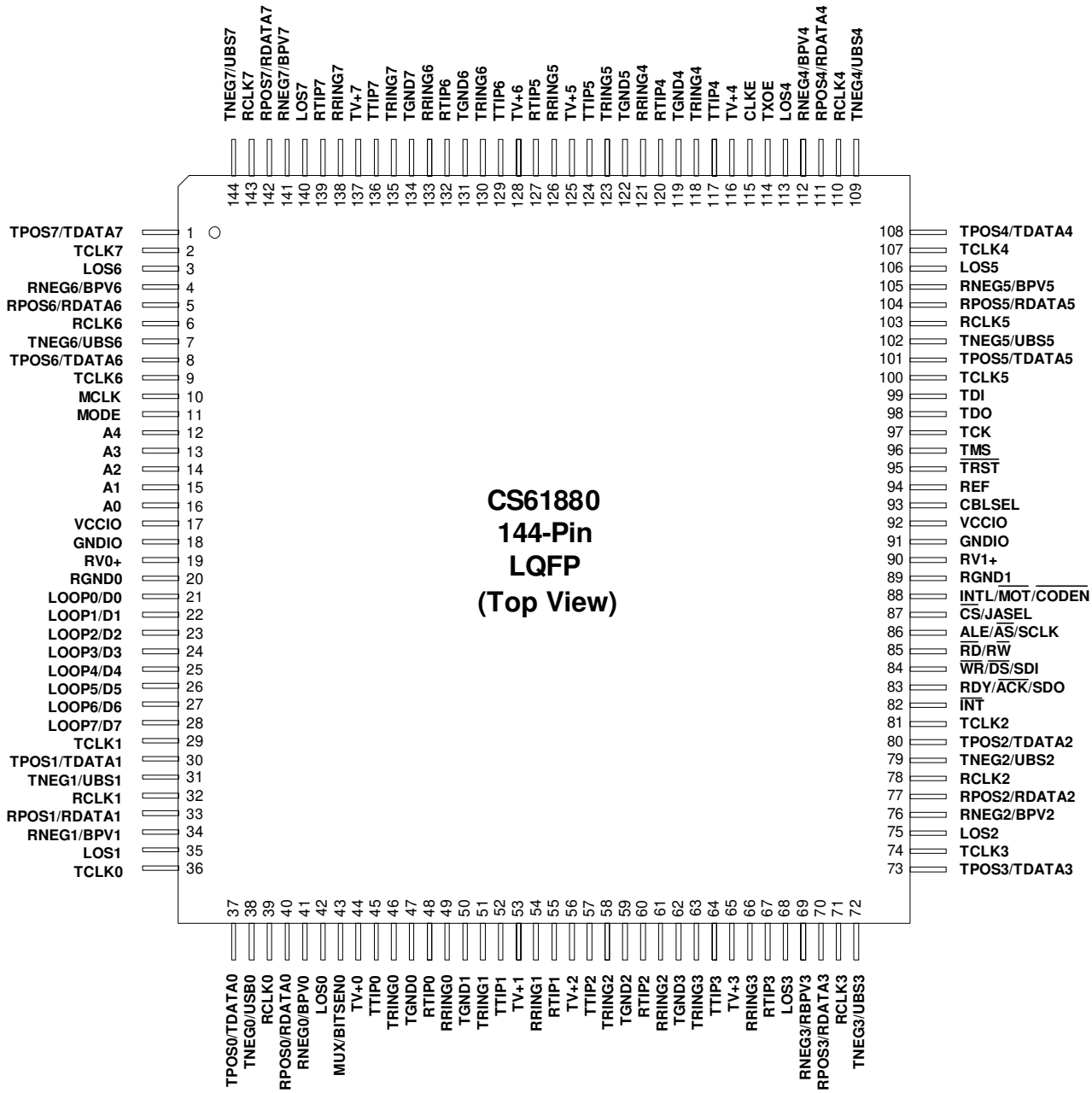

Figure 1. CS61880 144-Pin LQFP Package Pin Outs

2. PIN OUT - 160-BALL FBGA PACKAGE

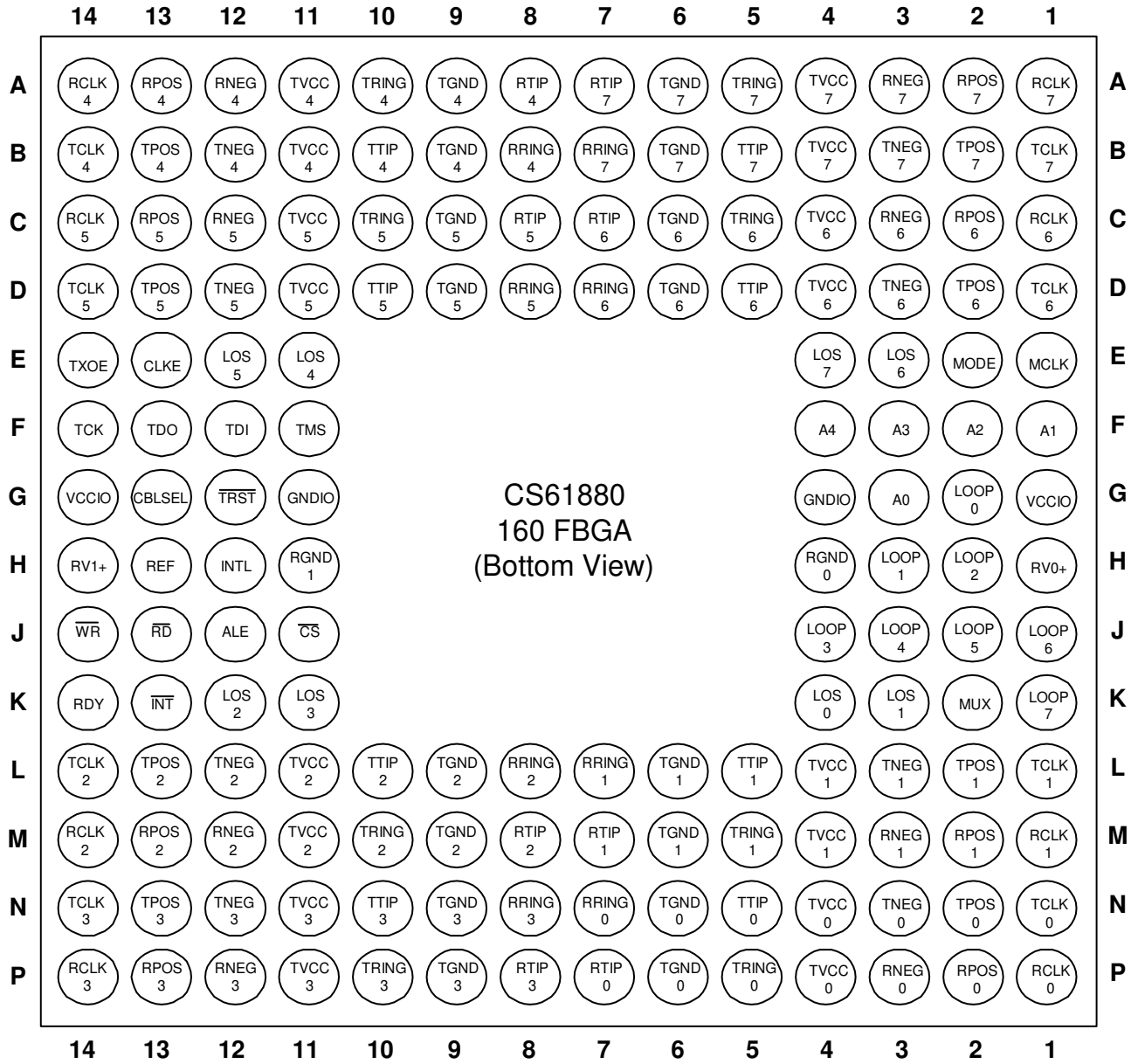

Figure 2. CS61880 160-Ball FBGA Package Pin Outs

3. PIN DESCRIPTIONS

3.1 Power Supplies

SYMBOL	LQFP	FBGA	TYPE	DESCRIPTION
VCCIO	17 92	G1 G14		**Power Supply, Digital Interface:** Power supply for digital interface pins; typically 3.3 V
GNDIO	18 91	G4 G11		**Ground, Digital Interface:** Power supply ground for the digital interface; typically 0 V
RV0+ RV1+	19 90	H1 H14		**Power Supply, Core Circuitry:** Power supply for all sub-circuits except the transmit driver; typically +3.3 V
RGND0 RGND1	20 89	H4 H11		**Ground, Core Circuitry:** Ground for sub-circuits except the TX driver; typically 0 V
TV+0	44	N4, P4		**Power Supply, Transmit Driver 0** Power supply for transmit driver 0; typically +3.3 V
TGND0	47	N6, P6		**Ground, Transmit Driver 0** Power supply ground for transmit driver 0; typically 0 V
TV+1	53	L4, M4		**Power Supply, Transmit Driver 1**
TGND1	50	L6, M6		**Ground, Transmit Driver 1**
TV+2	56	L11 M11		**Power Supply, Transmit Driver 2**
TGND2	59	L9, M9		**Ground, Transmit Driver 2**
TV+3	65	N11 P11		**Power Supply, Transmit Driver 3**
TGND3	62	N9, P9		**Ground, Transmit Driver 3**
TV+4	116	A11 B11		**Power Supply, Transmit Driver 4**
TGND4	119	A9, B9		**Ground, Transmit Driver 4**
TV+5	125	C11 D11		**Power Supply, Transmit Driver 5**
TGND5	122	C9, D9		**Ground, Transmit Driver 5**
TV+6	128	C4, D4		**Power Supply, Transmit Driver 6**
TGND6	131	C6, D6		**Ground, Transmit Driver 6**
TV+7	137	A4, B4		**Power Supply, Transmit Driver 7**
TGND7	134	A6, B6		**Ground, Transmit Driver 7**

3.2 Control

<table>
<tr><th>SYMBOL</th><th>LQFP</th><th>FBGA</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>MCLK</td><td>10</td><td>E1</td><td>I</td><td>Master Clock Input
This pin is a free running reference clock that should be 2.048 MHz. This timing reference is used as follows:
- Timing reference for the clock recovery and jitter attenuation circuitry.
- RCLK reference during Loss of Signal (LOS) conditions
- Transmit clock reference during Transmit all Ones (TAOS) condition
- Wait state timing for microprocessor interface
- When this pin is held “High”, the PLL clock recovery circuit is disabled. In this mode, the CS61880 receivers function as simple data slicers.
- When this pin is held “Low”, the receiver paths are powered down and the output pins RCLK, RPOS, and RNEG are High-Z.</td></tr>
<tr><td>MODE</td><td>11</td><td>E2</td><td>I</td><td>Mode Select
This pin is used to select whether the CS61880 operates in Serial host, Parallel host or Hardware mode.
<u>Host Mode</u> - The CS61880 is controlled through either a serial or a parallel microprocessor interface (Refer to HOST MODE (See Section 13 on page 32).
<u>Hardware Mode</u> - The microprocessor interface is disabled and the device control/status are provided through the pins on the device.

Table 1. Operation Mode Selection
<table><tr><th>Pin State</th><th>OPERATING Mode</th></tr><tr><td>LOW</td><td>Hardware Mode</td></tr><tr><td>HIGH</td><td>Parallel Host Mode</td></tr><tr><td>VCCIO/2</td><td>Serial Host Mode</td></tr></table>
NOTE: For serial host mode connect this pin to a resistor divider consisting of two 10 kΩ resistors between VCCIO and GNDIO.</td></tr>
</table>

<table>
<tr><th>SYMBOL</th><th>LQFP</th><th>FBGA</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>MUX/BITSEN0</td><td>43</td><td>K2</td><td>I</td><td>Multiplexed Interface/Bits Clock Select
<u>Host Mode</u> -This pin configures the microprocessor interface for multiplexed or non-multiplexed operation.
<u>Hardware mode</u> - This pin is used to enable channel 0 as a G.703 BITS Clock recovery channel (Refer to BUILDING INTEGRATED TIMING SYSTEMS (BITS) CLOCK MODE (See Section 8 on page 23). Channel 1 through 7 are not affected by this pin during hardware mode. During host mode the G.703 BITS Clock recovery function is enabled by the Bits Clock Enable Register (1Eh) (See Section 14.31 on page 40).

Table 2. Mux/Bits Clock Selection
<table><tr><th>Pin State</th><th>Parallel Host Mode</th><th>Hardware Mode</th></tr><tr><td>HIGH</td><td>multiplexed</td><td>BITS Clock ON</td></tr><tr><td>LOW</td><td>non multiplexed</td><td>BITS Clock OFF</td></tr></table>
NOTE: The MUX pin only controls the BITS Clock function in Hardware Mode</td></tr>
<tr><td>$\overline{INT}$</td><td>82</td><td>K13</td><td>O</td><td>Interrupt Output
This active low output signals the host processor when one of the CS61880's internal status register bits has changed state. When the status register is read, the interrupt is cleared. The various status changes that would force $\overline{INT}$ active are maskable via internal interrupt enable registers.

NOTE: This pin is an open drain output and requires a 10 kΩ pull-up resistor.</td></tr>
<tr><td>RDY/$\overline{ACK}$/SDO</td><td>83</td><td>K14</td><td>O</td><td>Ready/Data Transfer Acknowledge/Serial Data Output
<u>Intel Parallel Host Mode</u> - During a read or write register access, RDY is asserted “Low” to acknowledge that the device has been accessed. An asserted “High” acknowledges that data has been written or read. Upon completion of the bus cycle, this pin High-Z.
<u>Motorola Parallel Host Mode</u> - During a data bus read operation this pin, “ACK”, is asserted “High” to indicate that data on the bus is valid. An asserted “Low” on this pin during a write operation acknowledges that a data transfer to the addressed register has been accepted. Upon completion of the bus cycle, this pin High-Z.
NOTE: Wait state generation via RDY/$\overline{ACK}$ is disabled in RZ mode (No Clock Recovery).
<u>Serial Host Mode</u> - When the microprocessor interface is configured for serial bus operation, “SDO” is used as a serial data output. This pin is forced into a high impedance state during a serial write access. The CLKE pin controls whether SDO is valid on the rising or falling edge of SCLK. Upon completion of the bus cycle, this pin High-Z.
<u>Hardware Mode</u> - This pin is not used and should be left open.</td></tr>
</table>

SYMBOL	LQFP	FBGA	TYPE	DESCRIPTION
$\overline{WR}/\overline{DS}$/SDI	84	J14	I	**Write Enable/Data Strobe/Serial Data** **Intel Parallel Host Mode - This pin, "$\overline{WR}$", functions as a write enable.** **Motorola Parallel Host Mode -** This pin, "$\overline{DS}$", functions as a data strobe input. **Serial Host Mode -** This pin, "SDI", functions as the serial data input. **Hardware Mode -** This pin is not used and should be connected to ground.
$\overline{RD}$/R$\overline{W}$	85	J13	I	**Read Enable/Read/Write** **Intel Parallel Host Mode - This pin, "$\overline{RD}$", functions as a read enable.** **Motorola Parallel Host Mode -** This pin, "R/$\overline{W}$", functions as the read/write input signal. **Hardware Mode -** This pin is not used and should be connected to ground.
ALE/$\overline{AS}$/SCLK	86	J12	I	**Address Latch Enable/Address Strobe/Serial Clock** **Intel Parallel Host Mode -** This pin, "ALE", functions as the Address Latch Enable when configured for multiplexed address/data operation. **Motorola Parallel Host Mode -** This pin, "$\overline{AS}$", functions as the active "low" address strobe when configured for multiplexed address/data operation. **Serial Host Mode -** This pin, "SCLK", is the serial clock used for data I/O on SDI and SDO. **Hardware Mode -** This pin is not used and should be connected to ground.
$\overline{CS}$/JASEL	87	J11	I	**Chip Select Input/Jitter Attenuator Select** **Host Mode -** This active low input is used to enable accesses to the microprocessor interface in either serial or parallel mode. **Hardware Mode -** This pin controls the position of the Jitter Attenuator. **Table 3. Jitter Attenuation Selection** Pin State: LOW — Jitter Attenuation Position: Transmit Path Pin State: HIGH — Jitter Attenuation Position: Receive Path Pin State: OPEN — Jitter Attenuation Position: Disabled

SYMBOL	LQFP	FBGA	TYPE	DESCRIPTION
INTL/$\overline{\text{MOT}}$/$\overline{\text{CODEN}}$	88	H12	I	**Intel/Motorola/Coder Mode Select Input** **Parallel Host Mode -** When this pin is "Low" the microprocessor interface is configured for operation with Motorola processors. When this pin is "High" the microprocessor interface is configured for operation with Intel processors. **Hardware Mode -** When the CS61880 is configured for unipolar operation, this pin, $\overline{\text{CODEN}}$, configures the line encoding/decoding function. When $\overline{\text{CODEN}}$ is low, HDB3 encoders/decoders are enabled. When $\overline{\text{CODEN}}$ is high, AMI encoding/decoding is activated. This is done for all eight channels.
TXOE	114	E14	I	**Transmitter Output Enable** **Host mode -** Operates the same as in hardware mode. Individual drivers can be set to a high impedance state via the **Output Disable Register (12h)** (See Section 14.19 on page 38). **Hardware Mode -** When TXOE pin is asserted Low, all the TX drivers are forced into a high impedance state. All other internal circuitry remains active.
CLKE	115	E13	I	**Clock Edge Select** In clock/data recovery mode, setting CLKE "high" will cause RPOS/RNEG to be valid on the falling edge of RCLK and SDO to be valid on the rising edge of SCLK. When CLKE is set "low", RPOS/RNEG is valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK. When the part is operated in data recovery mode, the RPOS/RNEG output polarity is active "high" when CLKE is set "high" and active "low" when CLKE is set "low".

3.3 Address Inputs/Loopbacks

SYMBOL	LQFP	FBGA	TYPE	DESCRIPTION
A4	12	F4	I	**Address Selector Input** **Parallel Host Mode -** During non-multiplexed parallel host mode operation, this pin function as the address 4 input for the parallel interface. **Hardware Mode -** The A4 pin must be tied low at all times.
A3 A2 A1 A0	13 14 15 16	F3 F2 F1 G3	I I I I	**Non-Intrusive Monitoring/Address Selector Inputs** **Parallel Host Mode -** During non-multiplexed parallel host mode operation, these pins function as address A[3:0] inputs for the parallel interface. **Hardware Mode -** The A[3:0] pins are used for port selection during non-intrusive monitoring. In non-intrusive monitoring mode, receiver 0's input is internally connected to the transmit or receive ports on one of the other 7 channels. The recovered clock and data from the selected port are output on RPOS0/RNEG0 and RCLK0. Additionally, the data from the selected port can be output on TTIP0/TRING0 by activating the remote loopback function for channel 0 (Refer to **Performance Monitor Register (0Bh)** (See Section 14.12 on page 36).
LOOP0/D0 LOOP1/D1 LOOP2/D2 LOOP3/D3 LOOP4/D4 LOOP5/D5 LOOP6/D6 LOOP7/D7	21 22 23 24 25 26 27 28	G2 H3 H2 J4 J3 J2 J1 K1	I/O I/O I/O I/O I/O I/O I/O I/O	**Loopback Mode Selector/Parallel Data Input/Output** **Parallel Host Mode -** In non-multiplexed microprocessor interface mode, these pins function as the bi-directional 8-bit data port. When operating in multiplexed microprocessor interface mode, these pins function as the address and data inputs/outputs. **Hardware Mode** - No Loopback - The CS61880 is in a normal operating state when LOOP is left open (unconnected) or tied to VCCIO/2. - Local Loopback - When LOOP is tied High, data transmitted on TTIP and TRING is looped back into the analog input of the corresponding channel's receiver and output on RPOS and RNEG. Input Data present on RTIP and RRING is ignored. - Remote Loopback - When LOOP is tied Low the recovered clock and data received on RTIP and RRING is looped back for transmission on TTIP and TRING. Data on TPOS and TNEG is ignored.

3.4 Cable Select

SYMBOL	LQFP	FBGA	TYPE	DESCRIPTION
CBLSEL	93	G13	I	**Cable Impedance Select** **Host Mode -** The input voltage to this pin does not effect normal operation. **Hardware Mode -** This pin is used to select the transmitted pulse shape and set the line impedance for all eight receivers and transmitters. This pin also selects whether or not all eight receivers use an internal or external line matching network (Refer to the Table 4 below for proper settings). **Table 4. Cable Impedance Selection** CBLSEL: No Connect — Transmitters: 120 Ω Internal — Receivers: 120 Ω Internal or External CBLSEL: HIGH — Transmitters: 75 Ω Internal — Receivers: 75 Ω Internal CBLSEL: LOW — Transmitters: 75 Ω Internal — Receivers: 75 Ω External **NOTE:** Refer to Figure 16 on page 50 and Figure 17 on page 51 for appropriate external line matching components. All transmitters use internal matching networks.

3.5 Status

SYMBOL	LQFP	FBGA	TYPE	DESCRIPTION
LOS0	42	K4	O	**Loss of Signal Output** The LOS output pins can be configured to indicate a loss of signal (LOS) state that is compliant to either ITU G.775 or ETSI 300 233. These pins are asserted “High” to indicate LOS. The LOS output returns low when an input signal is present for the time period dictated by the associated specification (Refer to **Loss-of-Signal (LOS)** (See Section 10.5 on page 27)).
LOS1	35	K3	O	
LOS2	75	K12	O	
LOS3	68	K11	O	
LOS4	113	E11	O	
LOS5	106	E12	O	
LOS6	3	E3	O	
LOS7	140	E4	O	

3.6 Digital Rx/Tx Data I/O

SYMBOL	LQFP	FBGA	TYPE	DESCRIPTION
TCLK0	36	N1	I	**Transmit Clock Input Port 0** - When TCLK is active, the TPOS and TNEG pins function as NRZ inputs that are sampled on the falling edge of TCLK. - If MCLK is active, TAOS will be generated when TCLK is held High for 16 MCLK cycles. **NOTE:** MCLK is used as the timing reference during TAOS and must have the appropriate stability. - If TCLK is held High in the absence of MCLK, the TPOS and TNEG inputs function as RZ inputs. In this mode, the transmit pulse width is set by the pulse-width of the signal input on TPOS and TNEG. To enter this mode, TCLK must be held high for at least 12 µs. - If TCLK is held Low, the output drivers enter a low-power, high impedance state.
TPOS0/TDATA0 TNEG0/UBS	37 38	N2 N3	I I	**Transmit Positive Pulse/Transmit Data Input Port 0** **Transmit Negative Pulse/Unipolar-Bipolar Select Port 0** The function of the TPOS/TDATA and TNEG/UBS inputs are determined by whether Unipolar, Bipolar or RZ input mode has been selected. **Bipolar Mode -** In this mode, NRZ data on TPOS and TNEG are sampled on the falling edge of TCLK and transmitted onto the line at TTIP and TRING respectively. A "High" input on TPOS results in transmission of a positive pulse; a "High" input on TNEG results in a transmission of a negative pulse. The translation of TPOS/TNEG inputs to TTIP/TRING outputs is as follows: **Table 5. Bipolar Mode Translations** TPOS / TNEG / OUTPUT 0 / 0 / Space 1 / 0 / Positive Mark 0 / 1 / Negative Mark 1 / 1 / Space **Unipolar mode -** Unipolar mode is activated by holding TNEG/UBS "High" for more than 16 TCLK cycles, when MCLK is present. The falling edge of TCLK samples a unipolar data steam on TPOS/TDATA. **RZ Mode -** To activate RZ mode tie TCLK "High" in the absence of MCLK. In this mode, the duty cycle of the TPOS and TNEG inputs determine the pulse width of the output signal on TTIP and TRING.

SYMBOL	LQFP	FBGA	TYPE	DESCRIPTION
RCLK0	39	P1	O	**Receive Clock Output Port 0** - When MCLK is active, this pin outputs the recovered clock from the signal input on RTIP and RRING. In the event of LOS, the RCLK output transitions from the recovered clock to MCLK. - If MCLK is held "High", the clock recovery circuitry is disabled and the RCLK output is driven by the XOR of RNEG and RPOS. - If MCLK is held "Low", this output is in a high-impedance state.
RPOS0/RDATA0 RNEG0/BPV0	40 41	P2 P3	O O	**Receive Positive Pulse/ Receive Data Output Port 0** **Receive Negative Pulse/Bipolar Violation Output Port 0** The function of the RPOS/RDATA and RNEG/BPV outputs are determined by whether Unipolar, Bipolar, or RZ input mode has been selected. During LOS, the RPOS/RNEG outputs will remain active. **NOTE:** The RPOS/RNEG outputs can be High-Z by holding MCLK Low. **Bipolar Output Mode -** When configured for Bipolar operation, NRZ Data is recovered from RTIP/RRING and output on RPOS/RNEG. A high signal on RPOS or RNEG correspond to the receipt of a positive or negative pulse on RTIP/RRING respectively. The RPOS/RNEG outputs are valid on the falling or rising edge of RCLK as configured by CLKE. **Unipolar Output Mode -** When unipolar mode is activated, the recovered data is output on RDATA. The decoder signals bipolar violations are output on the RNEG/BPV pin. **RZ Output Mode -** In this mode, the RPOS/RNEG pins output RZ data recovered by slicing the signal present on RTIP/RRING. A positive pulse on RTIP with respect to RRING generates a logic 1 on RPOS; a positive pulse on RRING with respect to RTIP generates a logic 1 on RNEG. The polarity of the output on RPOS/RNEG is selectable using the CLKE pin. In this mode, external circuitry is used to recover clock from the received signal.
TCLK1	29	L1	I	**Transmit Clock Input Port 1**
TPOS1/TDATA1	30	L2	I	**Transmit Positive Pulse/Transmit Data Input Port 1**
TNEG1/UBS1	31	L3	I	**Transmit Negative Pulse/Unipolar-Bipolar Select Port 1**
RCLK1	32	M1	O	**Receive Clock Output Port 1**
RPOS1/RDATA1	33	M2	O	**Receive Positive Pulse/ Receive Data Output Port 1**
RNEG1/BPV1	34	M3	O	**Receive Negative Pulse/Bipolar Violation Output Port 1**
TCLK2	81	L14	I	**Transmit Clock Input Port 2**
TPOS2/TDATA2	80	L13	I	**Transmit Positive Pulse/Transmit Data Input Port 2**
TNEG2/UBS2	79	L12	I	**Transmit Negative Pulse/Unipolar-Bipolar Select Port 2**

SYMBOL	LQFP	FBGA	TYPE	DESCRIPTION
RCLK2	78	M14	O	**Receive Clock Output Port 2**
RPOS2/RDATA2	77	M13	O	**Receive Positive Pulse/ Receive Data Output Port 2**
RNEG2/BPV2	76	M12	O	**Receive Negative Pulse/Bipolar Violation Output Port 2**
TCLK3	74	N14	I	**Transmit Clock Input Port 3**
TPOS3/TDATA3	73	N13	I	**Transmit Positive Pulse/Transmit Data Input Port 3**
TNEG3/UBS3	72	N12	I	**Transmit Negative Pulse/Unipolar-Bipolar Select Port 3**
RCLK3	71	P14	O	**Receive Clock Output Port 3**
RPOS3/RDATA3	70	P13	O	**Receive Positive Pulse/ Receive Data Output Port 3**
RNEG3/BPV3	69	P12	O	**Receive Negative Pulse/Bipolar Violation Output Port 3**
TCLK4	107	B14	I	**Transmit Clock Input Port 4**
TPOS4/TDATA4	108	B13	I	**Transmit Positive Pulse/Transmit Data Input Port 4**
TNEG4/UBS4	109	B12	I	**Transmit Negative Pulse/Unipolar-Bipolar Select Port 4**
RCLK4	110	A14	O	**Receive Clock Output Port 4**
RPOS4/RDATA4	111	A13	O	**Receive Positive Pulse/ Receive Data Output Port 4**
RNEG4/BPV4	112	A12	O	**Receive Negative Pulse/Bipolar Violation Output Port 4**
TCLK5	100	D14	I	**Transmit Clock Input Port 5**
TPOS5/TDATA5	101	D13	I	**Transmit Positive Pulse/Transmit Data Input Port 5**
TNEG5/UBS5	102	D12	I	**Transmit Negative Pulse/Unipolar-Bipolar Select Port 5**
RCLK5	103	C14	O	**Receive Clock Output Port 5**
RPOS5/RDATA5	104	C13	O	**Receive Positive Pulse/ Receive Data Output Port 5**
RNEG5/BPV5	105	C12	O	**Receive Negative Pulse/Bipolar Violation Output Port 5**
TCLK6	9	D1	I	**Transmit Clock Input Port 6**
TPOS6/TDATA6	8	D2	I	**Transmit Positive Pulse/Transmit Data Input Port 6**
TNEG6/UBS6	7	D3	I	**Transmit Negative Pulse/Unipolar-Bipolar Select Port 6**
RCLK6	6	C1	O	**Receive Clock Output Port 6**
RPOS6/RDATA6	5	C2	O	**Receive Positive Pulse/ Receive Data Output Port 6**
RNEG6/BPV6	4	C3	O	**Receive Negative Pulse/Bipolar Violation Output Port 6**
TCLK7	2	B1	I	**Transmit Clock Input Port 7**
TPOS7/TDATA7	1	B2	I	**Transmit Positive Pulse/Transmit Data Input Port 7**
TNEG7/UBS7	144	B3	I	**Transmit Negative Pulse/Unipolar-Bipolar Select Port 7**

SYMBOL	LQFP	FBGA	TYPE	DESCRIPTION
RCLK7	143	A1	O	**Receive Clock Output Port 7**
RPOS7/RDATA7	142	A2	O	**Receive Positive Pulse/ Receive Data Output Port 7**
RNEG7/BPV7	141	A3	O	**Receive Negative Pulse/Bipolar Violation Output Port 7**

3.7 Analog RX/TX Data I/O

SYMBOL	LQFP	FBGA	TYPE	DESCRIPTION
TTIP0 TRING0	45 46	N5 P5	O O	**Transmit Tip Output Port 0** **Transmit Ring Output Port 0** These pins are the differential outputs of the transmit driver. The driver internally matches impedances for E1 75 Ω or E1 120 Ω lines requiring only a 1:1.15 transformer. The CBLSEL pin is used to select the appropriate line matching impedance only in “Hardware” mode. In host mode, the appropriate line matching impedance is selected by the **Line Length Data Register (11h)** (See Section 14.18 on page 38). **NOTE:** TTIP and TRING are forced to a high impedance state when the TCLK or the TXOE pin is forced “Low”.
RTIP0 RRING0	48 49	P7 N7	I I	**Receive Tip Input Port 0** **Receive Ring Input Port 0** These pins are the differential line inputs to the receiver. The receiver uses either Internal Line Impedance or External Line Impedance modes to match the line impedances for E1 75Ω or E1 120Ω modes. **Internal Line Impedance Mode -** The receiver uses the same external resistors to match the line impedance (Refer to Figure 16 on page 50). **External Line Impedance Mode -** The receiver uses different external resistors to match the line impedance (Refer to Figure 17 on page 51). - In host mode, the appropriate line impedance is selected by the **Line Length Data Register (11h)** (See Section 14.18 on page 38). - In hardware mode, the CBLSEL pin selects the appropriate line impedance. (Refer to Table 4 on page 15 for proper line impedance settings). **NOTE:** Data and clock recovered from the signal input on these pins are output via RCLK, RPOS, and RNEG.
TTIP1	52	L5	O	**Transmit Tip Output Port 1**
TRING1	51	M5	O	**Transmit Ring Output Port 1**
RTIP1	55	M7	I	**Receive Tip Input Port 1**
RRING1	54	L7	I	**Receive Ring Input Port 1**
TTIP2	57	L10	O	**Transmit Tip Output Port 2**

SYMBOL	LQFP	FBGA	TYPE	DESCRIPTION
TRING2	58	M10	O	**Transmit Ring Output Port 2**
RTIP2	60	M8	I	**Receive Tip Input Port 2**
RRING2	61	L8	I	**Receive Ring Input Port 2**
TTIP3	64	N10	O	**Transmit Tip Output Port 3**
TRING3	63	P10	O	**Transmit Ring Output Port 3**
RTIP3	67	P8	I	**Receive Tip Input Port 3**
RRING3	66	N8	I	**Receive Ring Input Port 3**
TTIP4	117	B10	O	**Transmit Tip Output Port 4**
TRING4	118	A10	O	**Transmit Ring Output Port 4**
RTIP4	120	A8	I	**Receive Tip Input Port 4**
RRING4	121	B8	I	**Receive Ring Input Port 4**
TTIP5	124	D10	O	**Transmit Tip Output Port 5**
TRING5	123	C10	O	**Transmit Ring Output Port 5**
RTIP5	127	C8	I	**Receive Tip Input Port 5**
RRING5	126	D8	I	**Receive Ring Input Port 5**
TTIP6	129	D5	O	**Transmit Tip Output Port 6**
TRING6	130	C5	O	**Transmit Ring Output Port 6**
RTIP6	132	C7	I	**Receive Tip Input Port 6**
RRING6	133	D7	I	**Receive Ring Input Port 6**
TTIP7	136	B5	O	**Transmit Tip Output Port 7**
TRING7	135	A5	O	**Transmit Ring Output Port 7**
RTIP7	139	A7	I	**Receive Tip Input Port 7**
RRING7	138	B7	I	**Receive Ring Input Port 7**

3.8 JTAG Test Interface

SYMBOL	LQFP	FBGA	TYPE	DESCRIPTION
$\overline{\text{TRST}}$	95	G12	I	**JTAG Reset** This active Low input resets the JTAG controller. This input is pulled up internally and may be left as a NC when not used.
TMS	96	F11	I	**JTAG Test Mode Select Input** This input enables the JTAG serial port when active High. This input is sampled on the rising edge of TCK. This input is pulled up internally and may be left as a NC when not used.
TCK	97	F14	I	**JTAG Test Clock** Data on TDI is valid on the rising edge of TCK. Data on TDO is valid on the falling edge of TCK. When TCK is stopped high or low, the contents of all JTAG registers remain unchanged. Tie pin low through a 10 kΩ resistor when not used.
TDO	98	F13	O	**JTAG Test Data Output** JTAG test data is shifted out of the device on this pin. Data is output on the falling edge of TCK. Leave as NC when not used.
TDI	99	F12	I	**JTAG Test Data Input** JTAG test data is shifted into the device using this pin. The pin is sampled on the rising edge of TCK. TDI is pulled up internally and may be left as a NC when not used.

3.9 Miscellaneous

SYMBOL	LQFP	FBGA	TYPE	DESCRIPTION
REF	94	H13	I	**Reference Input** This pin must be tied to ground through 13.3 kΩ 1% resistor. This pin is used to set the internal current level.

4. OPERATION

The CS61880 is a full featured line interface unit for up to eight E1 75 Ω or E1 120 Ω lines. The device provides an interface to twisted pair or co-axial media. A matched impedance technique is employed that reduces power and eliminates the need for matching resistors. As a result, the device can interface directly to the line through a transformer without the need for matching resistors on the transmit side. The receive side uses the same resistor values for all E1 settings.

5. POWER-UP

On power-up, the device is held in a static state until the power supply achieves approximately 70% of the power supply voltage. Once the power supply threshold is passed, the analog circuitry is calibrated, the control registers are reset to their default settings, and the various internal state machines are reset. The reset/calibration process completes in about 30 ms.

6. MASTER CLOCK

The CS61880 requires a 2.048 MHz reference clock with a minimum accuracy of ±100 ppm. This clock may be supplied from internal system timing or a CMOS crystal oscillator and input to the MCLK pin.

The receiver uses MCLK as a reference for clock recovery, jitter attenuation, and the generation of RCLK during LOS. The transmitter uses MCLK as the transmit timing reference during a blue alarm transmit all ones condition. In addition, MCLK provides the reference timing for wait state generation.

In systems with a jittered transmit clock, MCLK should not be tied to the transmit clock, a separate crystal oscillator should drive the reference clock input. Any jitter present on the reference clock will not be filtered by the jitter attenuator and can cause the CS61880 to operate incorrectly.

7. G.772 MONITORING

The receive path of channel zero of the CS61880 can be used to monitor the receive or transmit paths of any of the other channels. The signal to be monitored is multiplexed to channel zero through the G.772 Multiplexer. The multiplexer and channel zero then form a G.772 compliant digital Protected Monitoring Point (PMP). When the PMP is connected to the channel, the attenuation in the signal path is negligible across the signal band. The signal can be observed using RPOS, RNEG, and RCLK of channel zero or by putting channel zero in remote loopback, the signal can be observed on TTIP and TRING of channel zero.

The G.772 monitoring function is available during both host mode and hardware mode operation. In host modes, individual channels are selected for monitoring via the **Performance Monitor Register (0Bh)** (See Section 14.12 on page 36)). In hardware mode, individual channels are selected through the A3:A0 pins (Refer to Table 6 below for address settings).

Table 6. G.772 Address Selection

Address [A3:A0]	Channel Selection
0000	Monitoring Disabled
0001	Receiver Channel # 1
0010	Receiver Channel # 2
0011	Receiver Channel # 3
0100	Receiver Channel # 4
0101	Receiver Channel # 5
0110	Receiver Channel # 6
0111	Receiver Channel # 7
1000	Monitoring Disabled
1001	Transmitter Channel # 1
1010	Transmitter Channel # 2
1011	Transmitter Channel # 3
1100	Transmitter Channel # 4
1101	Transmitter Channel # 5
1110	Transmitter Channel # 6
1111	Transmitter Channel # 7

NOTE: In hardware mode the A4 pin must be tied low at all times.

8. BUILDING INTEGRATED TIMING SYSTEMS (BITS) CLOCK MODE

This mode is used to enable one or more channels as a stand-alone timing recovery unit used for G.703 Clock Recovery.

In hardware mode, BITS Clock mode is selected by pulling the MUX pin "HIGH". This enables only channel zero as a stand-alone timing recovery unit, no other channel can be used as a timing recovery unit.

In host mode, each channel can be setup as an independent G.703 timing recovery unit, through the **Bits Clock Enable Register (1Eh)** (See Section 14.31 on page 40), setting the desired bit to "1" enables BITS Clock mode for that channel. The following diagrams show how the BITS clock function operates.

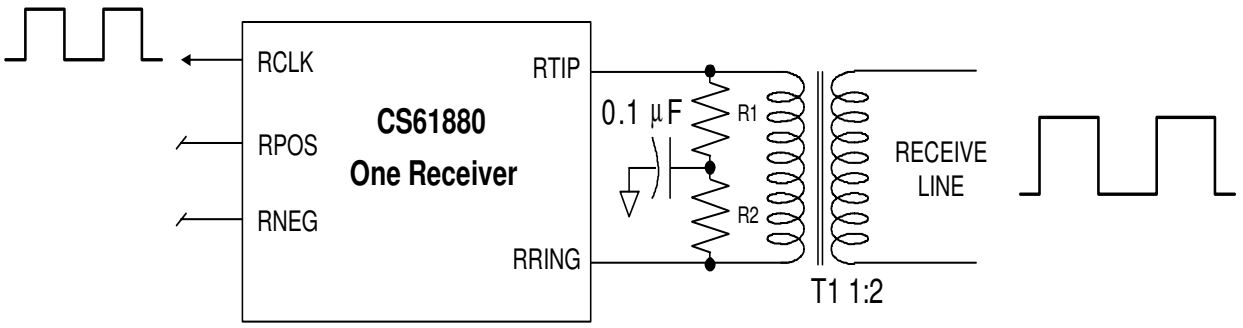

Figure 3. G.703 BITS Clock Mode in NRZ Mode

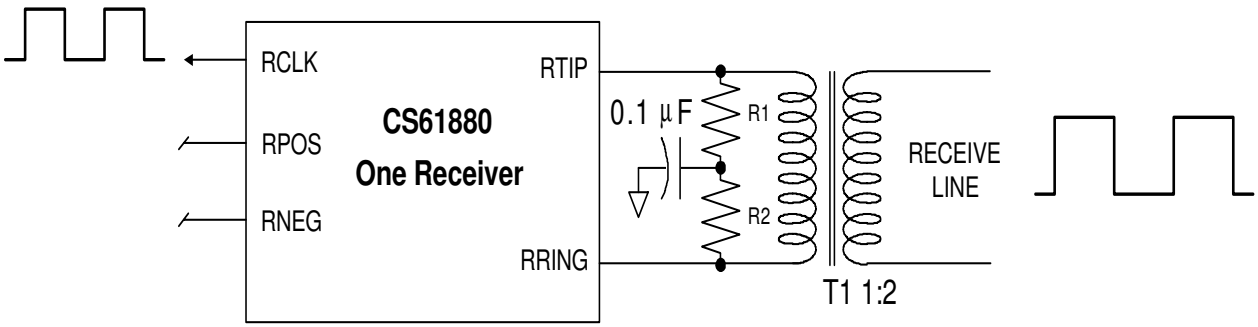

Figure 4. G.703 BITS Clock Mode in RZ Mode

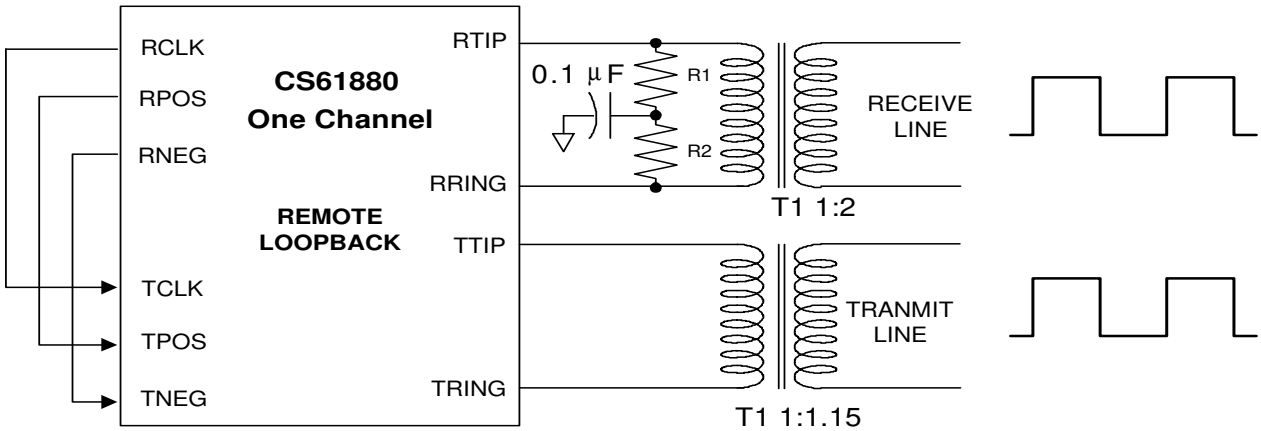

Figure 5. G.703 BITS Clock Mode in Remote Loopback

9. TRANSMITTER

The CS61880 contains eight identical transmitters that each use a low power matched impedance driver to eliminate the need for external load matching resistors, while providing superior return loss. As a result, the TTIP/TRING outputs can be connected directly to the transformer allowing one hardware circuit for E1 120 Ω, and E1 75 Ω applications.

Digital transmit data and clock are input into the CS61880 through the TPOS/TDATA, TNEG and TCLK input pins. These pins accept data in one of three formats: unipolar, bipolar, or RZ. In either unipolar or bipolar mode, the CS61880 internally generates a pulse shape compliant to the G.703 mask for E1 (Refer to Figure 6). The pulse shaping applied to the transmit data can be selected in hardware mode or in host mode.

In hardware mode, the line impedance (75 Ω or 120 Ω) and which prestored pulse shape to transmit (75 Ω or 120 Ω) is selected via the CBLSEL pin for all eight transmitters.

In host mode, each channel is configured independently by writing to the **Line Length Channel ID Register (10h)** (See Section 14.17 on page 38), then writing the desired line length settings to the LEN[3:0] bits in the **Line Length Data Register (11h)** (See Section 14.18 on page 38). The LEN bits select the pulse shape and line impedance of the addressed channel. In host mode, the CBLSEL pin is not used.

NOTE: If one channel is configured for E1 75 Ω mode, another channel can be configured for E1 120 Ω mode at the same time. This operation is only allowed in host mode.

The CS61880 also allows the user to customize the transmit pulse shapes to compensate for non-standard cables, transformers, or protection circuitry. For further information on the AWG Refer to **Arbitrary Waveform Generator** (See Section 15 on page 42).

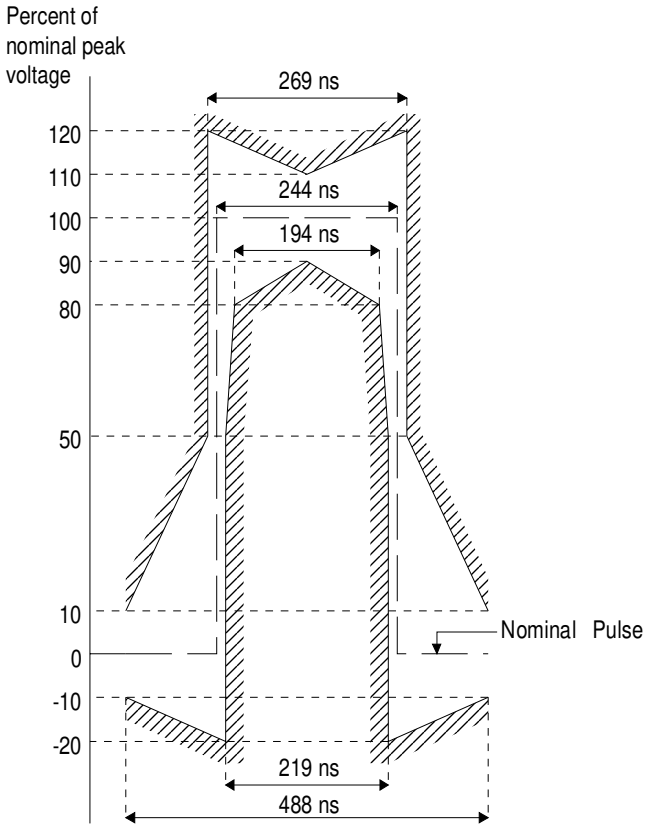

Figure 6. Pulse Mask at E1 Interface

For more information on the host mode registers refer to **Register Descriptions** (See Section 14 on page 35).

9.1 Bipolar Mode

Bipolar mode provides transparent operation for applications in which the line coding function is performed by an external framing device. In this mode, the falling edge of TCLK samples NRZ data on TPOS/TNEG for transmission on TTIP/TRING.

9.2 Unipolar Mode

In unipolar mode, the CS61880 is configured such that transmit data is encoded using HDB3, or AMI line codes. This mode is activated by holding

TNEG/UBS "High" for more than 16 TCLK cycles. Transmit data is input to the part via the TPOS/TDATA pin on the falling edge of TCLK. When operating the part in hardware mode, the CODEN pin is used to select between HDB3 or AMI encoding. During host mode operation, the line coding is selected via the **Line Length Channel ID Register (10h)** (See Section 14.17 on page 38).

NOTE: The encoders/decoders are selected for all eight channels in both hardware and host mode.

9.3 RZ Mode

In RZ mode, the internal pulse shape circuitry is bypassed and RZ data driven into TPOS/TNEG is transmitted on TTIP/TRING. In this mode, the pulse width of the transmitter output is determined by the width of the RZ signal input to TPOS/TNEG pins. This mode is entered when MCLK is inactive and TCLK is held "High" for at least 12 µs.

9.4 Transmitter Powerdown / High-Z

The transmitters can be forced into a high impedance, low power state by holding TCLK of the appropriate channel low for at least 12 µs or 140 MCLK cycles. In hardware and host mode, the TXOE pin forces all eight transmitters into a high impedance state within 1 µs.

In host mode, each transmitter is individually controllable using the **Output Disable Register (12h)** (See Section 14.19 on page 38). The TXOE pin can be used in host mode, but does not effect the contents of the Output Enable Register. This feature is useful in applications that require redundancy.

9.5 Transmit All Ones (TAOS)

When TAOS is activated, continuous ones are transmitted on TTIP/TRING using MCLK as the transmit timing reference. In this mode, the TPOS and TNEG inputs are ignored.

In hardware mode, TAOS is activated by pulling TCLK "High" for more than 16 MCLK cycles.

In host mode, TAOS is generated for a particular channel by asserting the associated bit in the **TAOS Enable Register (03h)** (See Section 14.4 on page 35).

Since MCLK is the reference clock, it should be of adequate stability.

9.6 Automatic TAOS

While a given channel is in the LOS condition, if the corresponding bit in the **Automatic TAOS Register (0Eh)** (See Section 14.15 on page 37) is set, the device will drive that channel's TTIP and TRING with the all ones pattern. This function is only available in host mode. Refer to **Loss-of-Signal (LOS)** (See Section 10.5 on page 27).

9.7 Driver Failure Monitor

In host mode, the Driver Failure Monitor (DFM) function monitors the output of each channel and sets a bit in the **DFM Status Register (05h)** (See Section 14.6 on page 35) if a secondary short circuit is detected between TTIP and TRING. This generates an interrupt if the respective bit in the **DFM Interrupt Enable Register (07h)** (See Section 14.8 on page 36) is also set. Any change in the **DFM Status Register (05h)** (See Section 14.6 on page 35) will result in the corresponding bit in the **DFM Interrupt Status Register (09h)** (See Section 14.10 on page 36) being set. The interrupt is cleared by reading the **DFM Interrupt Status Register (09h)** (See Section 14.10 on page 36).

9.8 Driver Short Circuit Protection

The CS61880 provides driver short circuit protection when current on the secondary exceeds 50 mA RMS.