



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



Octal T1/E1/J1 Line Interface Unit

Features

- ❑ Industry-standard Footprint
- ❑ Octal E1/T1/J1 Short-haul Line Interface Unit
- ❑ Low Power
- ❑ No external component changes for 100 Ω/120 Ω/75 Ω operation.
- ❑ Pulse shapes can be customized by the user.
- ❑ Internal AMI, B8ZS, or HDB3 Encoding/Decoding
- ❑ LOS Detection per T1.231, ITU G.775, ETSI 300-233
- ❑ G.772 Non-Intrusive Monitoring
- ❑ G.703 BITS Clock Recovery
- ❑ Crystal-less Jitter Attenuation
- ❑ Serial/Parallel Microprocessor Control Interfaces
- ❑ Transmitter Short Circuit Current Limiter (<50mA)
- ❑ TX Drivers with Fast High-Z and Power Down
- ❑ JTAG boundary scan compliant to IEEE 1149.1.
- ❑ 144-Pin LQFP & 160-Pin LFBGA Packages

ORDERING INFORMATION

CS61884-IQZ	144-pin LQFP, Lead Free
CS61884-IRZ	160-pin LFBGA, Lead Free

Description

The CS61884 is a full-featured octal E1/T1/J1 short-haul LIU that supports both 1.544 Mbps or 2.048 Mbps data transmission. Each channel provides crystal-less jitter attenuation that complies with the most stringent standards. Each channel also provides internal AMI/B8ZS/HDB3 encoding/decoding. To support enhanced system diagnostics, channel zero can be configured for G.772 non-intrusive monitoring of any of the other 7 channels' receive or transmit paths.

The CS61884 makes use of ultra-low-power, matched-impedance transmitters and receivers to reduce power beyond that achieved by traditional driver designs. By achieving a more precise line match, this technique also provides superior return loss characteristics. Additionally, the internal line matching circuitry reduces the external component count. All transmitters have controls for independent power down and High-Z.

Each receiver provides reliable data recovery with over 12 dB of cable attenuation. The receiver also incorporates LOS detection compliant to the most recent specifications.

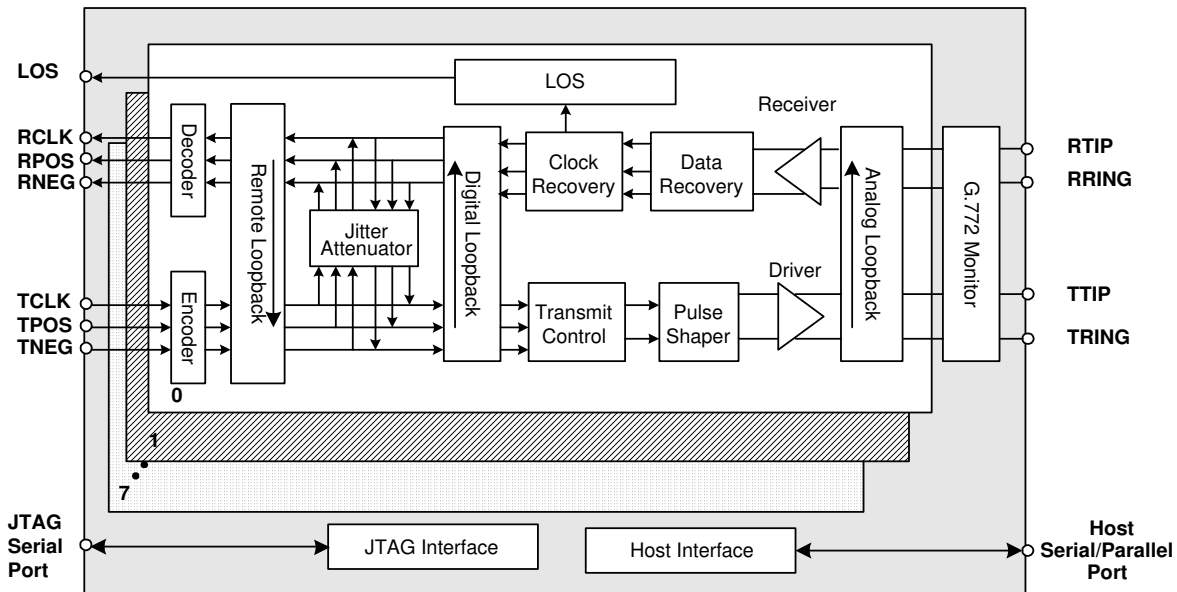


TABLE OF CONTENTS

1. PINOUT - LQFP	7
2. PINOUT - LFBGA	8
3. PIN DESCRIPTIONS	9
3.1 Power Supplies	9
3.2 Control	10
3.3 Address Inputs/Loopbacks	14
3.4 Cable Select	15
3.5 Status	15
3.6 Digital Rx/Tx Data I/O	16
3.7 Analog RX/TX Data I/O	19
3.8 JTAG Test Interface	21
3.9 Miscellaneous	21
4. OPERATION	22
5. POWER-UP	22
6. MASTER CLOCK	22
7. G.772 MONITORING	22
8. BUILDING INTEGRATED TIMING SYSTEMS (BITS) CLOCK MODE	23
9. TRANSMITTER	24
9.1	Bipolar Mode 25
9.2 Unipolar Mode	25
9.3 RZ Mode	25
9.4 Transmitter Powerdown / High-Z	25
9.5 Transmit All Ones (TAOS)	25
9.6 Automatic TAOS	26
9.7 Driver Failure Monitor	26
9.8 Driver Short Circuit Protection	26
10. RECEIVER	26
10.1 Bipolar Output Mode	26
10.2 Unipolar Output Mode	26
10.3 RZ Output Mode	27
10.4 Receiver Powerdown/High-Z	27

Contacting Cirrus Logic Support

Visit the Cirrus Logic web site at:

<http://www.cirrus.com>

IMPORTANT NOTICE

Cirrus Logic, Inc. and its subsidiaries ("Cirrus") believe that the information contained in this document is accurate and reliable. However, the information is subject to change without notice and is provided "AS IS" without warranty of any kind (express or implied). Customers are advised to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, indemnification, and limitation of liability. No responsibility is assumed by Cirrus for the use of this information, including use of this information as the basis for manufacture or sale of any items, or for infringement of patents or other rights of third parties. This document is the property of Cirrus and by furnishing this information, Cirrus grants no license, express or implied under any patents, mask work rights, copyrights, trademarks, trade secrets or other intellectual property rights. Cirrus owns the copyrights associated with the information contained herein and gives consent for copies to be made of the information only for use within your organization with respect to Cirrus integrated circuits or other products of Cirrus. This consent does not extend to other copying such as copying for general distribution, advertising or promotional purposes, or for creating any work for resale.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). CIRRUS PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN PRODUCTS SURGICALLY IMPLANTED INTO THE BODY, AUTOMOTIVE SAFETY OR SECURITY DEVICES, LIFE SUPPORT PRODUCTS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF CIRRUS PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK AND CIRRUS DISCLAIMS AND MAKES NO WARRANTY, EXPRESS, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR PARTICULAR PURPOSE, WITH REGARD TO ANY CIRRUS PRODUCT THAT IS USED IN SUCH A MANNER. IF THE CUSTOMER OR CUSTOMER'S CUSTOMER USES OR PERMITS THE USE OF CIRRUS PRODUCTS IN CRITICAL APPLICATIONS, CUSTOMER AGREES, BY SUCH USE, TO FULLY INDEMNIFY CIRRUS, ITS OFFICERS, DIRECTORS, EMPLOYEES, DISTRIBUTORS AND OTHER AGENTS FROM ANY AND ALL LIABILITY, INCLUDING ATTORNEYS' FEES AND COSTS, THAT MAY RESULT FROM OR ARISE IN CONNECTION WITH THESE USES.

Cirrus Logic, Cirrus, and the Cirrus Logic logo designs are trademarks of Cirrus Logic, Inc. All other brand and product names in this document may be trademarks or service marks of their respective owners.

10.5 Loss-of-Signal (LOS)	27
10.6 Alarm Indication Signal (AIS)	28
11. JITTER ATTENUATOR	28
12. OPERATIONAL SUMMARY	29
12.1 Loopbacks	29
12.2 Analog Loopback	29
12.3 Digital Loopback	30
12.4 Remote Loopback	30
13. HOST MODE	32
13.1 SOFTWARE RESET	32
13.2 Serial Port Operation	32
13.3 Parallel Port Operation	33
13.4 Register Set	34
14. REGISTER DESCRIPTIONS	35
14.1 Revision/IDcode Register (00h)	35
14.2 Analog Loopback Register (01h)	35
14.3 Remote Loopback Register (02h)	35
14.4 TAOS Enable Register (03h)	35
14.5 LOS Status Register (04h)	35
14.6 DFM Status Register (05h)	35
14.7 LOS Interrupt Enable Register (06h)	36
14.8 DFM Interrupt Enable Register (07h)	36
14.9 LOS Interrupt Status Register (08h)	36
14.10 DFM Interrupt Status Register (09h)	36
14.11 Software Reset Register (0Ah)	36
14.12 Performance Monitor Register (0Bh)	36
14.13 Digital Loopback Reset Register (0Ch)	37
14.14 LOS/AIS Mode Enable Register (0Dh)	37
14.15 Automatic TAOS Register (0Eh)	37
14.16 Global Control Register (0Fh)	38
14.17 Line Length Channel ID Register (10h)	38
14.18 Line Length Data Register (11h)	39
14.19 Output Disable Register (12h)	39
14.20 AIS Status Register (13h)	39
14.21 AIS Interrupt Enable Register (14h)	39
14.22 AIS Interrupt Status Register (15h)	40
14.23 AWG Broadcast Register (16h)	40
14.24 AWG Phase Address Register (17h)	40
14.25 AWG Phase Data Register (18h)	40
14.26 AWG Enable Register (19h)	40
14.27 AWG Overflow Interrupt Enable Register (1Ah)	41
14.28 AWG Overflow Interrupt Status Register (1Bh)	41
14.29 Reserved Register (1Ch)	41
14.30 Reserved Register (1Dh)	41
14.31 Bits Clock Enable Register (1Eh)	41
14.32 Reserved Register (1Fh)	41
14.33 Status Registers	42
14.33.1 Interrupt Enable Registers	42
14.33.2 Interrupt Status Registers	42
15. ARBITRARY WAVEFORM GENERATOR	43
16. JTAG SUPPORT	45
16.1 TAP Controller	45
16.1.1 JTAG Reset	45

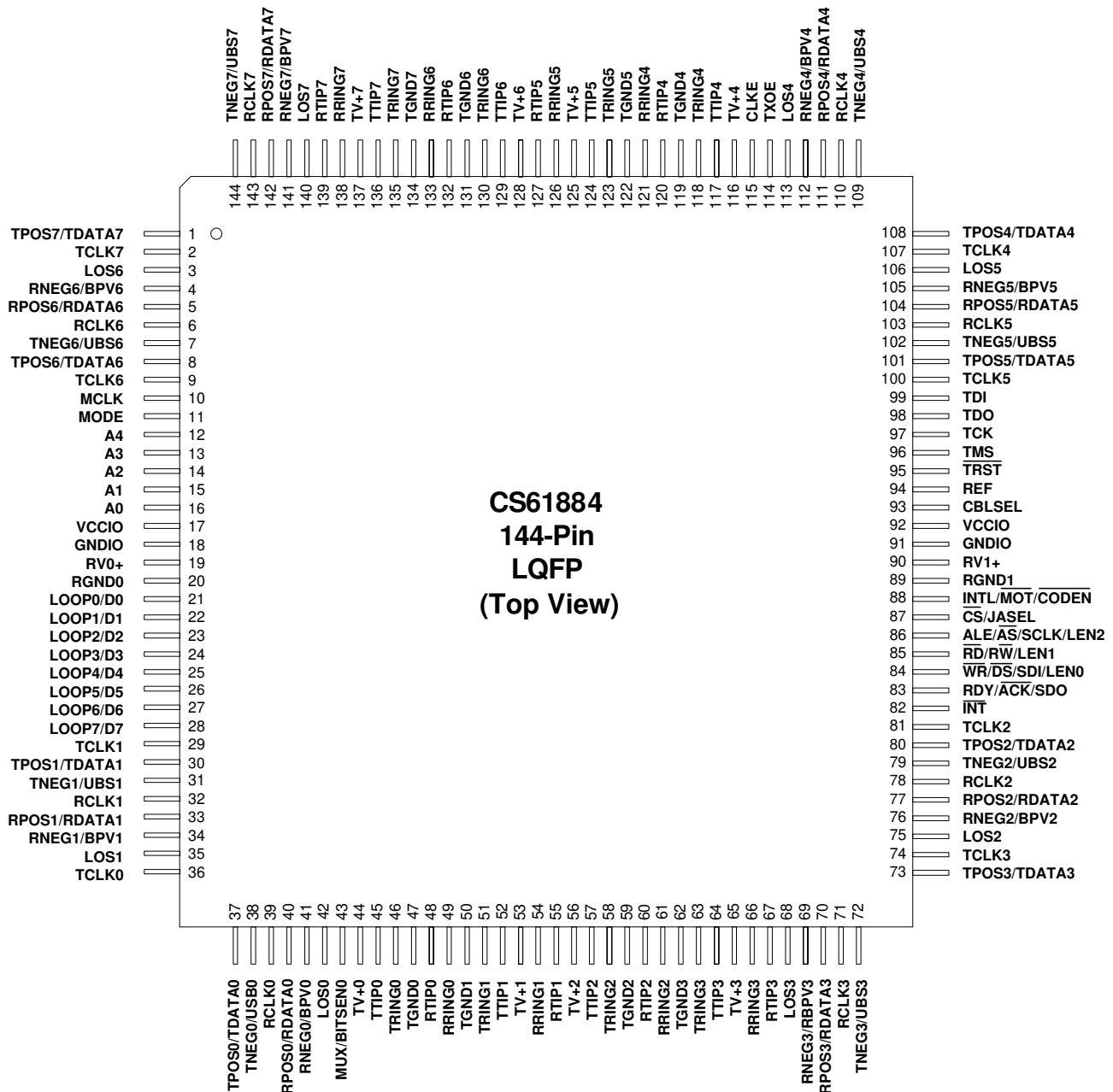
16.1.2 Test-Logic-Reset	45
16.1.3 Run-Test-Idle	45
16.1.4 Select-DR-Scan	46
16.1.5 Capture-DR	46
16.1.6 Shift-DR	46
16.1.7 Exit1-DR	46
16.1.8 Pause-DR	46
16.1.9 Exit2-DR	46
16.1.10 Update-DR	46
16.1.11 Select-IR-Scan	47
16.1.12 Capture-IR	47
16.1.13 Shift-IR	47
16.1.14 Exit1-IR	47
16.1.15 Pause-IR	47
16.1.16 Exit2-IR	47
16.1.17 Update-IR	47
16.2 Instruction Register (IR)	47
16.2.1 EXTEST	47
16.2.2 SAMPLE/PRELOAD	47
16.2.3 IDCODE	47
16.2.4 BYPASS	47
16.3 Device ID Register (IDR)	48
17. BOUNDARY SCAN REGISTER (BSR)	48
18. APPLICATIONS	51
18.1 Transformer specifications	53
18.2 Crystal Oscillator Specifications	53
18.3 Designing for AT&T 62411	53
18.4 Line Protection	53
19. CHARACTERISTICS AND SPECIFICATIONS	54
19.1 Absolute Maximum Ratings	54
19.2 Recommended Operating Conditions	54
19.3 Digital Characteristics	55
19.4 Transmitter Analog Characteristics	55
19.5 Receiver Analog Characteristics	56
19.6 Jitter Attenuator Characteristics	57
19.7 Master Clock Switching Characteristics	59
19.8 Transmit Switching Characteristics	59
19.9 Receive Switching Characteristics	59
19.10 Switching Characteristics - Serial Port	61
19.11 Switching Characteristics - Parallel Port (Multiplexed Mode)	62
19.12 Switching Characteristics- Parallel Port (Non-multiplexed Mode)	65
19.13 Switching Characteristics - JTAG	68
20. COMPLIANT RECOMMENDATIONS AND SPECIFICATIONS	69
21. LFBGA PACKAGE DIMENSIONS	70
22. LQFP PACKAGE DIMENSIONS	71
23. ORDERING INFORMATION	72
24. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION	72
25. REVISION HISTORY	72

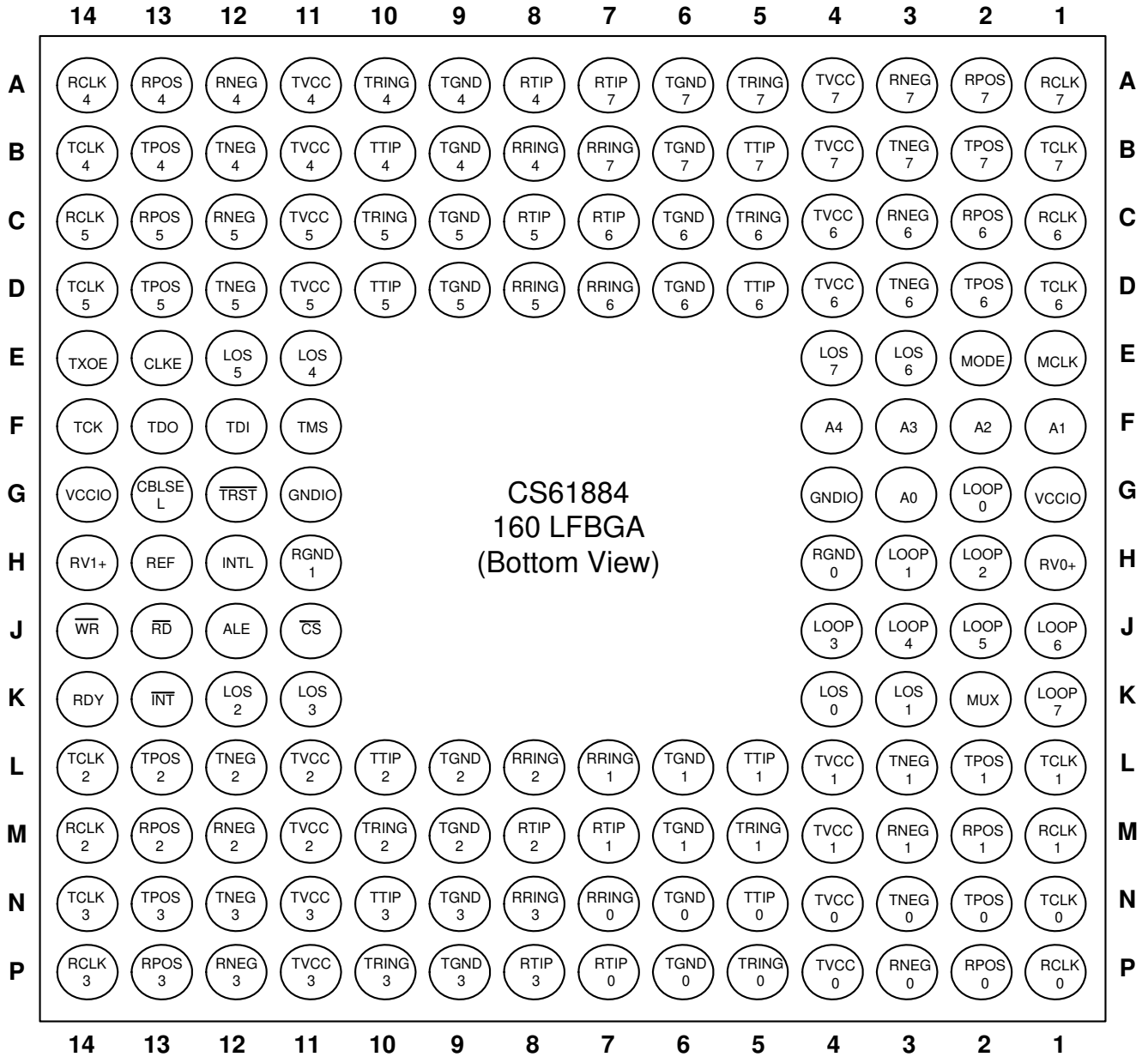
LIST OF FIGURES

Figure 1. CS61884 144-LQFP Pinout	7
Figure 2. CS61884 160-Ball LFBGA Pinout	8
Figure 3. G.703 BITS Clock Mode in NRZ Mode	23
Figure 4. G.703 BITS Clock Mode in RZ Mode	23
Figure 5. G.703 BITS Clock Mode in Remote Loopback	23
Figure 6. Pulse Mask at T1/J1 Interface	24
Figure 7. Pulse Mask at E1 Interface	24
Figure 8. Analog Loopback Block Diagram	30
Figure 9. Analog Loopback with TAOS Block Diagram	30
Figure 10. Digital Loopback Block Diagram	31
Figure 11. Digital Loopback with TAOS	31
Figure 12. Remote Loopback Block Diagram	31
Figure 13. Serial Read/Write Format (SPOL = 0)	33
Figure 14. Arbitrary Waveform UI	43
Figure 15. Test Access Port Architecture	45
Figure 16. TAP Controller State Diagram	46
Figure 17. Internal RX/TX Impedance Matching	51
Figure 18. Internal TX, External RX Impedance Matching	52
Figure 19. Jitter Transfer Characteristic vs. G.736, TBR 12/13 & AT&T 62411	58
Figure 20. Jitter Tolerance Characteristic vs. G.823 & AT&T 62411	58
Figure 21. Recovered Clock and Data Switching Characteristics	60
Figure 22. Transmit Clock and Data Switching Characteristics	60
Figure 23. Signal Rise and Fall Characteristics	60
Figure 24. Serial Port Read Timing Diagram	61
Figure 25. Serial Port Write Timing Diagram	61
Figure 26. Parallel Port Timing - Write; Intel Multiplexed Address / Data Bus Mode	63
Figure 27. Parallel Mode Port Timing - Read; Intel Multiplexed Address / Data Bus Mode	63
Figure 28. Parallel Port Timing - Write in Motorola Multiplexed Address / Data Bus	64
Figure 29. Parallel Port Timing - Read in Motorola Multiplexed Address / Data Bus	64
Figure 30. Parallel Port Timing - Write in Intel Non-Multiplexed Address / Data Bus Mode	66
Figure 31. Parallel Port Timing - Read in Intel Non-Multiplexed Address / Data Bus Mode	66
Figure 32. Parallel Port Timing - Write in Motorola Non-Multiplexed Address / Data Bus Mode	67
Figure 33. Parallel Port Timing - Read in Motorola Non-Multiplexed Address / Data Bus Mode	67
Figure 34. JTAG Switching Characteristics	68

LIST OF TABLES

Table 1. Operation Mode Selection	10
Table 2. Mux/Bits Clock Selection	11
Table 3. Cable Impedance Selection	15
Table 4. G.772 Address Selection	22
Table 5. Hardware Mode Line Length Configuration Selection	25
Table 6. Jitter Attenuator Configurations	28
Table 7. Operational Summary	29
Table 8. Host Control Signal Descriptions	32
Table 9. Host Mode Register Set	34
Table 10. JTAG Instructions	47
Table 11. Boundary Scan Register	48
Table 12. Transformer Specifications	53

1. PINOUT - LQFP

Figure 1. CS61884 144-LQFP Pinout

2. PINOUT - LFBGA

Figure 2. CS61884 160-Ball LFBGA Pinout

3. PIN DESCRIPTIONS

3.1 Power Supplies

SYMBOL	LQFP	LFBGA	TYPE	DESCRIPTION
VCCIO	17 92	G1 G14		Power Supply, Digital Interface: Power supply for digital interface pins; typically 3.3V.
GNDIO	18 91	G4 G11		Ground, Digital Interface: Power supply ground for the digital interface; typically 0 Volts
RV0+ RV1+	19 90	H1 H14		Power Supply, Core Circuitry: Power supply for all sub-circuits except the transmit driver; typically +3.3 Volts
RGND0 RGND1	20 89	H4 H11		Ground, Core Circuitry: Ground for sub-circuits except the TX driver; typically 0 Volts
TV+0	44	N4, P4		Power Supply, Transmit Driver 0 Power supply for transmit driver 0; typically +3.3 Volts
TGND0	47	N6, P6		Ground, Transmit Driver 0 Power supply ground for transmit driver 0; typically 0 Volts
TV+1	53	L4, M4		Power Supply, Transmit Driver 1
TGND1	50	L6, M6		Ground, Transmit Driver 1
TV+2	56	L11 M11		Power Supply, Transmit Driver 2
TGND2	59	L9, M9		Ground, Transmit Driver 2
TV+3	65	N11 P11		Power Supply, Transmit Driver 3
TGND3	62	N9, P9		Ground, Transmit Driver 3
TV+4	116	A11 B11		Power Supply, Transmit Driver 4
TGND4	119	A9, B9		Ground, Transmit Driver 4
TV+5	125	C11 D11		Power Supply, Transmit Driver 5
TGND5	122	C9, D9		Ground, Transmit Driver 5
TV+6	128	C4, D4		Power Supply, Transmit Driver 6
TGND6	131	C6, D6		Ground, Transmit Driver 6
TV+7	137	A4, B4		Power Supply, Transmit Driver 7
TGND7	134	A6, B6		Ground, Transmit Driver 7

3.2 Control

SYMBOL	LQFP	LFBGA	TYPE	DESCRIPTION								
MCLK	10	E1	I	<p>Master Clock Input This pin is a free running reference clock that should be either 1.544 MHz for T1/J1 or 2.048 MHz for E1 operation. This timing reference is used as follows:</p> <ul style="list-style-type: none"> - Timing reference for the clock recovery and jitter attenuation circuitry. - RCLK reference during Loss of Signal (LOS) conditions - Transmit clock reference during Transmit all Ones (TAOS) condition - Wait state timing for microprocessor interface - When this pin is held "High", the PLL clock recovery circuit is disabled. In this mode, the CS61884 receivers function as simple data slicers. - When this pin is held "Low", the receiver paths are powered down and the output pins RCLK, RPOS, and RNEG are High-Z. 								
MODE	11	E2	I	<p>Mode Select This pin is used to select whether the CS61884 operates in Serial host, Parallel host or Hardware mode.</p> <p>Host Mode - The CS61884 is controlled through either a serial or a parallel microprocessor interface (Refer to HOST MODE (See Section 13 on page 32)).</p> <p>Hardware Mode - The microprocessor interface is disabled and the device control/status are provided through the pins on the device.</p> <p style="text-align: center;">Table 1. Operation Mode Selection</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Pin State</th> <th>OPERATING Mode</th> </tr> </thead> <tbody> <tr> <td>LOW</td> <td>Hardware Mode</td> </tr> <tr> <td>HIGH</td> <td>Parallel Host Mode</td> </tr> <tr> <td>VCCIO/2</td> <td>Serial Host Mode</td> </tr> </tbody> </table> <p>NOTE: For serial host mode connect this pin to a resistor divider consisting of two 10KΩ resistors between VCCIO and GNDIO.</p>	Pin State	OPERATING Mode	LOW	Hardware Mode	HIGH	Parallel Host Mode	VCCIO/2	Serial Host Mode
Pin State	OPERATING Mode											
LOW	Hardware Mode											
HIGH	Parallel Host Mode											
VCCIO/2	Serial Host Mode											

SYMBOL	LQFP	LFBGA	TYPE	DESCRIPTION									
MUX/BITSEN0	43	K2	I	<p>Multiplexed Interface/Bits Clock Select Host Mode - This pin configures the microprocessor interface for multiplexed or non-multiplexed operation. Hardware mode - This pin is used to enable channel 0 as a G.703 BITS Clock recovery channel (Refer to BUILDING INTEGRATED TIMING SYSTEMS (BITS) CLOCK MODE (See Section 8 on page 23). Channel 1 through 7 are not affected by this pin during hardware mode. During host mode the G.703 BITS Clock recovery function is enabled by the Bits Clock Enable Register (1Eh) (See Section 14.31 on page 41).</p> <p style="text-align: center;">Table 2. Mux/Bits Clock Selection</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Pin State</th> <th>Parallel Host Mode</th> <th>Hardware Mode</th> </tr> </thead> <tbody> <tr> <td>HIGH</td> <td>multiplexed</td> <td>BITS Clock ON</td> </tr> <tr> <td>LOW</td> <td>non multiplexed</td> <td>BITS Clock OFF</td> </tr> </tbody> </table> <p>NOTE: The MUX pin only controls the BITS Clock function in Hardware Mode</p>	Pin State	Parallel Host Mode	Hardware Mode	HIGH	multiplexed	BITS Clock ON	LOW	non multiplexed	BITS Clock OFF
Pin State	Parallel Host Mode	Hardware Mode											
HIGH	multiplexed	BITS Clock ON											
LOW	non multiplexed	BITS Clock OFF											
$\overline{\text{INT}}$	82	K13	O	<p>Interrupt Output This active low output signals the host processor when one of the CS61884's internal status register bits has changed state. When the status register is read, the interrupt is cleared. The various status changes that would force $\overline{\text{INT}}$ active are maskable via internal interrupt enable registers.</p> <p>NOTE: This pin is an open drain output and requires a 10 kΩ pull-up resistor.</p>									
RDY/ $\overline{\text{ACK}}$ /SDO	83	K14	O	<p>Data Transfer Acknowledge/Ready/Serial Data Output Intel Parallel Host Mode - During a read or write register access, RDY is asserted "Low" to acknowledge that the device has been accessed. An asserted "High" acknowledges that data has been written or read. Upon completion of the bus cycle, this pin High-Z. Motorola Parallel Host Mode - During a data bus read operation this pin "ACK" is asserted "High" to indicate that data on the bus is valid. An asserted "Low" on this pin during a write operation acknowledges that a data transfer to the addressed register has been accepted. Upon completion of the bus cycle, this pin High-Z. NOTE: Wait state generation via RDY/$\overline{\text{ACK}}$ is disabled in RZ mode (No Clock Recovery). Serial Host Mode - When the microprocessor interface is configured for serial bus operation, "SDO" is used as a serial data output. This pin is forced into a high impedance state during a serial write access. The CLKE pin controls whether SDO is valid on the rising or falling edge of SCLK. Upon completion of the bus cycle, this pin High-Z. Hardware Mode - This pin is not used and should be left open.</p>									

SYMBOL	LQFP	LFBGA	TYPE	DESCRIPTION								
$\overline{WR}/\overline{DS}/SDI/LEN0$	84	J14	I	<p>Data Strobe/ Write Enable/Serial Data/Line Length Input Intel Parallel Host Mode - This pin "\overline{WR}" functions as a write enable. Motorola Parallel Host Mode - This pin "\overline{DS}" functions as a data strobe input. Serial Host Mode - This pin "SDI" functions as the serial data input. Hardware Mode - As LEN0, this pin controls the transmit pulse shapes for both E1 and T1/J1 modes. This pin also selects which mode is used E1 or T1/J1 (Refer to Table 5 on page 25).</p>								
$\overline{RD}/\overline{RW}/LEN1$	85	J13	I	<p>Read/Write/ Read Enable/Line Length Input Intel Parallel Host Mode - This pin "\overline{RD}" functions as a read enable. Motorola Parallel Host Mode - This pin "$\overline{R}/\overline{W}$" functions as the read/write input signal. Hardware Mode - As LEN1, this pin controls the transmit pulse shapes for both E1 and T1/J1 modes. This pin also selects which mode is used E1 or T1/J1 (Refer to Table 5 on page 25).</p>								
$ALE/\overline{AS}/SCLK/LEN2$	86	J12	I	<p>Address Latch Enable/Serial Clock/Address Strobe/Line Length Input Intel Parallel Host Mode - This pin "ALE" functions as the Address Latch Enable when configured for multiplexed address/data operation. Motorola Parallel Host Mode - This pin "\overline{AS}" functions as the active "low" address strobe when configured for multiplexed address/data operation. Serial Host Mode - This pin "SCLK" is the serial clock used for data I/O on SDI and SDO. Hardware Mode - As LEN2, this pin controls the transmit pulse shapes for both E1 and T1/J1 modes. This pin also selects which mode is used E1 or T1/J1 (Refer to Table 5 on page 25).</p>								
$\overline{CS}/JASEL$	87	J11	I	<p>Chip Select Input/Jitter Attenuator Select Host Mode - This active low input is used to enable accesses to the microprocessor interface in either serial or parallel mode. Hardware Mode - This pin controls the position of the Jitter Attenuator.</p> <table border="1" data-bbox="821 1587 1383 1730"> <thead> <tr> <th>Pin State</th> <th>Jitter Attenuation Position</th> </tr> </thead> <tbody> <tr> <td>LOW</td> <td>Transmit Path</td> </tr> <tr> <td>HIGH</td> <td>Receive Path</td> </tr> <tr> <td>OPEN</td> <td>Disabled</td> </tr> </tbody> </table>	Pin State	Jitter Attenuation Position	LOW	Transmit Path	HIGH	Receive Path	OPEN	Disabled
Pin State	Jitter Attenuation Position											
LOW	Transmit Path											
HIGH	Receive Path											
OPEN	Disabled											

SYMBOL	LQFP	LFBGA	TYPE	DESCRIPTION
INTL/ $\overline{\text{MOT}}/\overline{\text{CODE}}/\overline{\text{N}}$	88	H12	I	<p>Motorola/Intel/Coder Mode Select Input</p> <p>Parallel Host Mode - When this pin is “Low” the microprocessor interface is configured for operation with Motorola processors. When this pin is “High” the microprocessor interface is configured for operation with Intel processors.</p> <p>Hardware Mode - When the CS61884 is configured for unipolar operation, this pin, CODEN, configures the line encoding/decoding function. When CODEN is low, B8ZS/HDB3 encoders/decoders are enabled for T1/J1 or E1 operation respectively. When CODEN is high, AMI encoding/decoding is activated. This is done for all eight channels.</p>
TXOE	114	E14	I	<p>Transmitter Output Enable</p> <p>Host mode - Operates the same as in hardware mode. Individual drivers can be set to a high impedance state via the Output Disable Register (12h) (See Section 14.19 on page 39).</p> <p>Hardware Mode - When TXOE pin is asserted Low, all the TX drivers are forced into a high impedance state. All other internal circuitry remains active.</p>
CLKE	115	E13	I	<p>Clock Edge Select</p> <p>In clock/data recovery mode, setting CLKE “high” will cause RPOS/RNEG to be valid on the falling edge of RCLK and SDO to be valid on the rising edge of SCLK. When CLKE is set “low”, RPOS/RNEG is valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK. When the part is operated in data recovery mode, the RPOS/RNEG output polarity is active “high” when CLKE is set “high” and active “low” when CLKE is set “low”.</p>

3.3 Address Inputs/Loopbacks

SYMBOL	LQFP	LFBGA	TYPE	DESCRIPTION
A4	12	F4	I	<p>Address Selector Input</p> <p>Parallel Host Mode - During non-multiplexed parallel host mode operation, this pin function as the address 4 input for the parallel interface.</p> <p>Hardware Mode - The A4 pin must be tied low at all times.</p>
A3	13	F3	I	<p>Non-Intrusive Monitoring/Address Selector Inputs</p> <p>Parallel Host Mode - During non-multiplexed parallel host mode operation, these pins function as address A[3:0] inputs for the parallel interface.</p> <p>Hardware Mode - The A[3:0] pins are used for port selection during non-intrusive monitoring. In non-intrusive monitoring mode, receiver 0's input is internally connected to the transmit or receive ports on one of the other 7 channels. The recovered clock and data from the selected port are output on RPOS0/RNEG0 and RCLK0. Additionally, the data from the selected port can be output on TTIP0/TRING0 by activating the remote loopback function for channel 0 (Refer to Performance Monitor Register (0Bh) (See Section 14.12 on page 36).</p>
A2	14	F2	I	
A1	15	F1	I	
A0	16	G3	I	
LOOP0/D0	21	G2	I/O	<p>Loopback Mode Selector/Parallel Data Input/Output</p> <p>Parallel Host Mode - In non-multiplexed microprocessor interface mode, these pins function as the bi-directional 8-bit data port. When operating in multiplexed microprocessor interface mode, these pins function as the address and data inputs/outputs.</p> <p>Hardware Mode</p> <ul style="list-style-type: none"> - No Loopback - The CS61884 is in a normal operating state when LOOP is left open (unconnected) or tied to VCCIO/2. - Local Loopback - When LOOP is tied High, data transmitted on TTIP and TRING is looped back into the analog input of the corresponding channel's receiver and output on RPOS and RNEG. Input Data present on RTIP and RRING is ignored. - Remote Loopback - When LOOP is tied Low the recovered clock and data received on RTIP and RRING is looped back for transmission on TTIP and TRING. Data on TPOS and TNEG is ignored.
LOOP1/D1	22	H3	I/O	
LOOP2/D2	23	H2	I/O	
LOOP3/D3	24	J4	I/O	
LOOP4/D4	25	J3	I/O	
LOOP5/D5	26	J2	I/O	
LOOP6/D6	27	J1	I/O	
LOOP7/D7	28	K1	I/O	

3.4 Cable Select

SYMBOL	LQFP	LFBGA	TYPE	DESCRIPTION																												
CBLSEL	93	G13	I	<p>Cable Impedance Select</p> <p>Host Mode - The input voltage to this pin does not effect normal operation.</p> <p>Hardware Mode - This pin is used in combination with the LEN control pins (Refer to Table 5, “Hardware Mode Line Length Configuration Selection,” on page 25) to set the line impedance for all eight receivers and transmitters. This pin also selects whether or not all eight receivers use an internal or external line matching network (Refer to the Table below for proper settings).</p> <p style="text-align: center;">Table 3. Cable Impedance Selection</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>E1/T1/J1</th> <th>CBLSEL</th> <th>Transmitters</th> <th>Receivers</th> </tr> </thead> <tbody> <tr> <td>T1/J1</td> <td>No Connect</td> <td>100 Ω Internal</td> <td>Internal</td> </tr> <tr> <td>T1/J1</td> <td>HIGH</td> <td>100 Ω Internal</td> <td>Internal</td> </tr> <tr> <td>T1/J1</td> <td>LOW</td> <td>100 Ω Internal</td> <td>External</td> </tr> <tr> <td>E1</td> <td>No Connect</td> <td>120 Ω Internal</td> <td>Inter or Ext</td> </tr> <tr> <td>E1</td> <td>HIGH</td> <td>75 Ω Internal</td> <td>Internal</td> </tr> <tr> <td>E1</td> <td>LOW</td> <td>75 Ω Internal</td> <td>External</td> </tr> </tbody> </table> <p>NOTE: Refer to Figure 17 on page 51 and Figure 18 on page 52 for appropriate external line matching components. All transmitters use internal matching networks.</p>	E1/T1/J1	CBLSEL	Transmitters	Receivers	T1/J1	No Connect	100 Ω Internal	Internal	T1/J1	HIGH	100 Ω Internal	Internal	T1/J1	LOW	100 Ω Internal	External	E1	No Connect	120 Ω Internal	Inter or Ext	E1	HIGH	75 Ω Internal	Internal	E1	LOW	75 Ω Internal	External
E1/T1/J1	CBLSEL	Transmitters	Receivers																													
T1/J1	No Connect	100 Ω Internal	Internal																													
T1/J1	HIGH	100 Ω Internal	Internal																													
T1/J1	LOW	100 Ω Internal	External																													
E1	No Connect	120 Ω Internal	Inter or Ext																													
E1	HIGH	75 Ω Internal	Internal																													
E1	LOW	75 Ω Internal	External																													

3.5 Status

SYMBOL	LQFP	LFBGA	TYPE	DESCRIPTION
LOS0	42	K4	○	<p>Loss of Signal Output</p> <p>The LOS output pins can be configured to indicate a loss of signal (LOS) state that is compliant to either T1.231, ITU G.775 or ETSI 300 233. These pins are asserted “High” to indicate LOS. The LOS output returns low when an input signal is present for the time period dictated by the associated specification (Refer to Loss-of-Signal (LOS) (See Section 10.5 on page 27)).</p>
LOS1	35	K3	○	
LOS2	75	K12	○	
LOS3	68	K11	○	
LOS4	113	E11	○	
LOS5	106	E12	○	
LOS6	3	E3	○	
LOS7	140	E4	○	

3.6 Digital Rx/Tx Data I/O

SYMBOL	LQFP	LFBGA	TYPE	DESCRIPTION															
TCLK0	36	N1	I	<p>Transmit Clock Input Port 0</p> <ul style="list-style-type: none"> - When TCLK is active, the TPOS and TNEG pins function as NRZ inputs that are sampled on the falling edge of TCLK. - If MCLK is active, TAOS will be generated when TCLK is held High for 16 MCLK cycles. <p>NOTE: MCLK is used as the timing reference during TAOS and must have the appropriate stability.</p> <ul style="list-style-type: none"> - If TCLK is held High in the absence of MCLK, the TPOS and TNEG inputs function as RZ inputs. In this mode, the transmit pulse width is set by the pulse-width of the signal input on TPOS and TNEG. To enter this mode, TCLK must be held high for at least 12 μS. - If TCLK is held Low, the output drivers enter a low-power, high impedance state. 															
TPOS0/TDATA0 TNEG0/UBS	37 38	N2 N3	I I	<p>Transmit Positive Pulse/Transmit Data Input Port 0 Transmit Negative Pulse/Unipolar-Bipolar Select Port 0</p> <p>The function of the TPOS/TDATA and TNEG/UBS inputs are determined by whether Unipolar, Bipolar or RZ input mode has been selected.</p> <p>Bipolar Mode - In this mode, NRZ data on TPOS and TNEG are sampled on the falling edge of TCLK and transmitted onto the line at TTIP and TRING respectively. A "High" input on TPOS results in transmission of a positive pulse; a "High" input on TNEG results in a transmission of a negative pulse. The translation of TPOS/TNEG inputs to TTIP/TRING outputs is as follows:</p> <table border="1" data-bbox="776 1266 1430 1444"> <thead> <tr> <th>TPOS</th> <th>TNEG</th> <th>OUTPUT</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Space</td> </tr> <tr> <td>1</td> <td>0</td> <td>Positive Mark</td> </tr> <tr> <td>0</td> <td>1</td> <td>Negative Mark</td> </tr> <tr> <td>1</td> <td>1</td> <td>Space</td> </tr> </tbody> </table> <p>Unipolar mode - Unipolar mode is activated by holding TNEG/UBS "High" for more than 16 TCLK cycles, when MCLK is present. The falling edge of TCLK samples a unipolar data stream on TPOS/TDATA.</p> <p>RZ Mode - To activate RZ mode tie TCLK "High" with the absence of MCLK. In this mode, the duty cycle of the TPOS and TNEG inputs determine the pulse width of the output signal on TTIP and TRING.</p>	TPOS	TNEG	OUTPUT	0	0	Space	1	0	Positive Mark	0	1	Negative Mark	1	1	Space
TPOS	TNEG	OUTPUT																	
0	0	Space																	
1	0	Positive Mark																	
0	1	Negative Mark																	
1	1	Space																	

SYMBOL	LQFP	LFBGA	TYPE	DESCRIPTION
RCLK0	39	P1	O	<p>Receive Clock Output Port 0</p> <ul style="list-style-type: none"> - When MCLK is active, this pin outputs the recovered clock from the signal input on RTIP and RRING. In the event of LOS, the RCLK output transitions from the recovered clock to MCLK. - If MCLK is held “High”, the clock recovery circuitry is disabled and the RCLK output is driven by the XOR of RNEG and RPOS. - If MCLK is held “Low”, this output is in a high-impedance state.
RPOS0/RDATA0	40	P2	O	<p>Receive Positive Pulse/ Receive Data Output Port 0 Receive Negative Pulse/Bipolar Violation Output Port 0</p> <p>The function of the RPOS/RDATA and RNEG/BPV outputs are determined by whether Unipolar, Bipolar, or RZ input mode has been selected. During LOS, the RPOS/RNEG outputs will remain active.</p> <p>NOTE: The RPOS/RNEG outputs can be High-Z by holding MCLK Low.</p> <p>Bipolar Output Mode - When configured for Bipolar operation, NRZ Data is recovered from RTIP/RRING and output on RPOS/RNEG. A high signal on RPOS or RNEG correspond to the receipt of a positive or negative pulse on RTIP/RRING respectively. The RPOS/RNEG outputs are valid on the falling or rising edge of RCLK as configured by CLKE.</p> <p>Unipolar Output Mode - When unipolar mode is activated, the recovered data is output on RDATA. The decoder signals bipolar Violations on the RNEG/BPV pin.</p> <p>RZ Output Mode - In this mode, the RPOS/RNEG pins output RZ data recovered by slicing the signal present on RTIP/RRING. A positive pulse on RTIP with respect to RRING generates a logic 1 on RPOS; a positive pulse on RRING with respect to RTIP generates a logic 1 on RNEG. The polarity of the output on RPOS/RNEG is selectable using the CLKE pin. In this mode, external circuitry is used to recover clock from the received signal.</p>
RNEG0/BPV0	41	P3	O	
TCLK1	29	L1	I	Transmit Clock Input Port 1
TPOS1/TDATA1	30	L2	I	Transmit Positive Pulse/Transmit Data Input Port 1
TNEG1/UBS1	31	L3	I	Transmit Negative Pulse/Unipolar-Bipolar Select Port 1
RCLK1	32	M1	O	Receive Clock Output Port 1
RPOS1/RDATA1	33	M2	O	Receive Positive Pulse/ Receive Data Output Port 1
RNEG1/BPV1	34	M3	O	Receive Negative Pulse/Bipolar Violation Output Port 1
TCLK2	81	L14	I	Transmit Clock Input Port 2
TPOS2/TDATA2	80	L13	I	Transmit Positive Pulse/Transmit Data Input Port 2
TNEG2/UBS2	79	L12	I	Transmit Negative Pulse/Unipolar-Bipolar Select Port 2

SYMBOL	LQFP	LFBGA	TYPE	DESCRIPTION
RCLK2	78	M14	O	Receive Clock Output Port 2
RPOS2/RDATA2	77	M13	O	Receive Positive Pulse/ Receive Data Output Port 2
RNEG2/BPV2	76	M12	O	Receive Negative Pulse/Bipolar Violation Output Port 2
TCLK3	74	N14	I	Transmit Clock Input Port 3
TPOS3/TDATA3	73	N13	I	Transmit Positive Pulse/Transmit Data Input Port 3
TNEG3/UBS3	72	N12	I	Transmit Negative Pulse/Unipolar-Bipolar Select Port 3
RCLK3	71	P14	O	Receive Clock Output Port 3
RPOS3/RDATA3	70	P13	O	Receive Positive Pulse/ Receive Data Output Port 3
RNEG3/BPV3	69	P12	O	Receive Negative Pulse/Bipolar Violation Output Port 3
TCLK4	107	B14	I	Transmit Clock Input Port 4
TPOS4/TDATA4	108	B13	I	Transmit Positive Pulse/Transmit Data Input Port 4
TNEG4/UBS4	109	B12	I	Transmit Negative Pulse/Unipolar-Bipolar Select Port 4
RCLK4	110	A14	O	Receive Clock Output Port 4
RPOS4/RDATA4	111	A13	O	Receive Positive Pulse/ Receive Data Output Port 4
RNEG4/BPV4	112	A12	O	Receive Negative Pulse/Bipolar Violation Output Port 4
TCLK5	100	D14	I	Transmit Clock Input Port 5
TPOS5/TDATA5	101	D13	I	Transmit Positive Pulse/Transmit Data Input Port 5
TNEG5/UBS5	102	D12	I	Transmit Negative Pulse/Unipolar-Bipolar Select Port 5
RCLK5	103	C14	O	Receive Clock Output Port 5
RPOS5/RDATA5	104	C13	O	Receive Positive Pulse/ Receive Data Output Port 5
RNEG5/BPV5	105	C12	O	Receive Negative Pulse/Bipolar Violation Output Port 5
TCLK6	9	D1	I	Transmit Clock Input Port 6
TPOS6/TDATA6	8	D2	I	Transmit Positive Pulse/Transmit Data Input Port 6
TNEG6/UBS6	7	D3	I	Transmit Negative Pulse/Unipolar-Bipolar Select Port 6
RCLK6	6	C1	O	Receive Clock Output Port 6
RPOS6/RDATA6	5	C2	O	Receive Positive Pulse/ Receive Data Output Port 6
RNEG6/BPV6	4	C3	O	Receive Negative Pulse/Bipolar Violation Output Port 6
TCLK7	2	B1	I	Transmit Clock Input Port 7
TPOS7/TDATA7	1	B2	I	Transmit Positive Pulse/Transmit Data Input Port 7
TNEG7/UBS7	144	B3	I	Transmit Negative Pulse/Unipolar-Bipolar Select Port 7

SYMBOL	LQFP	LFBGA	TYPE	DESCRIPTION
RCLK7	143	A1	O	Receive Clock Output Port 7
RPOS7/RDATA7	142	A2	O	Receive Positive Pulse/ Receive Data Output Port 7
RNEG7/BPV7	141	A3	O	Receive Negative Pulse/Bipolar Violation Output Port 7

3.7 Analog RX/TX Data I/O

SYMBOL	LQFP	LFBGA	TYPE	DESCRIPTION
TTIP0	45	N5	O	Transmit Tip Output Port 0 Transmit Ring Output Port 0 TTIP and TRING pins are the differential outputs of the transmit driver. The driver internally matches impedances for E1 75 Ω, E1 120 Ω and T1/J1 100 Ω lines requiring only a 1:2 transformer. The CBLSEL pin is used to select the appropriate line matching impedance only in “Hardware” mode. In host mode, the appropriate line matching impedance is selected by the Line Length Data Register (11h) (See Section 14.18 on page 39). NOTE: TTIP and TRING are forced to a high impedance state when the TCLK pin is “Low” for over 12μS or the TXOE pin is forced “Low”.
TRING0	46	P5	O	
RTIP0	48	P7	I	Receive Tip Input Port 0 Receive Ring Input Port 0 RTIP and RRING are the differential line inputs to the receiver. The receiver uses either Internal Line Impedance or External Line Impedance modes to match the line impedances for E1 75Ω, E1 120Ω or T1/J1 100Ω modes. Internal Line Impedance Mode - The receiver uses the same external resistors to match the line impedance (Refer to Figure 17 on page 51). External Line Impedance Mode - The receiver uses different external resistors to match the line impedance (Refer to Figure 18 on page 52). - In host mode, the appropriate line impedance is selected by the Line Length Data Register (11h) (See Section 14.18 on page 39). - In hardware mode, the CBLSEL pin in combination with the LEN pins select the appropriate line impedance. (Refer to Table 3 on page 15 for proper line impedance settings). NOTE: Data and clock recovered from the signal input on these pins are output via RCLK, RPOS, and RNEG.
RRING0	49	N7	I	
TTIP1	52	L5	O	Transmit Tip Output Port 1
TRING1	51	M5	O	Transmit Ring Output Port 1
RTIP1	55	M7	I	Receive Tip Input Port 1
RRING1	54	L7	I	Receive Ring Input Port 1

SYMBOL	LQFP	LFBGA	TYPE	DESCRIPTION
TTIP2	57	L10	O	Transmit Tip Output Port 2
TRING2	58	M10	O	Transmit Ring Output Port 2
RTIP2	60	M8	I	Receive Tip Input Port 2
RRING2	61	L8	I	Receive Ring Input Port 2
TTIP3	64	N10	O	Transmit Tip Output Port 3
TRING3	63	P10	O	Transmit Ring Output Port 3
RTIP3	67	P8	I	Receive Tip Input Port 3
RRING3	66	N8	I	Receive Ring Input Port 3
TTIP4	117	B10	O	Transmit Tip Output Port 4
TRING4	118	A10	O	Transmit Ring Output Port 4
RTIP4	120	A8	I	Receive Tip Input Port 4
RRING4	121	B8	I	Receive Ring Input Port 4
TTIP5	124	D10	O	Transmit Tip Output Port 5
TRING5	123	C10	O	Transmit Ring Output Port 5
RTIP5	127	C8	I	Receive Tip Input Port 5
RRING5	126	D8	I	Receive Ring Input Port 5
TTIP6	129	D5	O	Transmit Tip Output Port 6
TRING6	130	C5	O	Transmit Ring Output Port 6
RTIP6	132	C7	I	Receive Tip Input Port 6
RRING6	133	D7	I	Receive Ring Input Port 6
TTIP7	136	B5	O	Transmit Tip Output Port 7
TRING7	135	A5	O	Transmit Ring Output Port 7
RTIP7	139	A7	I	Receive Tip Input Port 7
RRING7	138	B7	I	Receive Ring Input Port 7

3.8 JTAG Test Interface

SYMBOL	LQFP	LFBGA	TYPE	DESCRIPTION
$\overline{\text{TRST}}$	95	G12	I	JTAG Reset This active Low input resets the JTAG controller. This input is pulled up internally and may be left as a NC when not used.
TMS	96	F11	I	JTAG Test Mode Select Input This input enables the JTAG serial port when active High. This input is sampled on the rising edge of TCK. This input is pulled up internally and may be left as a NC when not used.
TCK	97	F14	I	JTAG Test Clock Data on TDI is valid on the rising edge of TCK. Data on TDO is valid on the falling edge of TCK. When TCK is stopped high or low, the contents of all JTAG registers remain unchanged. Tie pin low through a 10 K Ω resistor when not used.
TDO	98	F13	O	JTAG Test Data Output JTAG test data is shifted out of the device on this pin. Data is output on the falling edge of TCK. Leave as NC when not used.
TDI	99	F12	I	JTAG Test Data Input JTAG test data is shifted into the device using this pin. The pin is sampled on the rising edge of TCK. TDI is pulled up internally and may be left as a NC when not used.

3.9 Miscellaneous

SYMBOL	LQFP	LFBGA	TYPE	DESCRIPTION
REF	94	H13	I	Reference Input This pin must be tied to ground through 13.3 K Ω 1% resistor. This pin is used to set the internal current level.

4. OPERATION

The CS61884 is a full featured line interface unit for up to eight E1/T1/J1 lines. The device provides an interface to twisted pair or co-axial media. A matched impedance technique is employed that reduces power and eliminates the need for matching resistors. As a result, the device can interface directly to the line through a transformer without the need for matching resistors on the transmit side. The receive side uses the same resistor values for all E1/T1/J1 settings.

5. POWER-UP

On power-up, the device is held in a static state until the power supply achieves approximately 70% of the power supply voltage. Once the power supply threshold is passed, the analog circuitry is calibrated, the control registers are reset to their default settings, and the various internal state machines are reset. The reset/calibration process completes in about 30 ms.

6. MASTER CLOCK

The CS61884 requires a 2.048 MHz or 1.544 MHz reference clock with a minimum accuracy of ± 100 ppm. This clock may be supplied from internal system timing or a CMOS crystal oscillator and input to the MCLK pin.

The receiver uses MCLK as a reference for clock recovery, jitter attenuation, and the generation of RCLK during LOS. The transmitter uses MCLK as the transmit timing reference during a blue alarm transmit all ones condition. In addition, MCLK provides the reference timing for wait state generation.

In systems with a jittered transmit clock, MCLK should not be tied to the transmit clock, a separate crystal oscillator should drive the reference clock input. Any jitter present on the reference clock will not be filtered by the jitter attenuator and can cause the CS61884 to operate incorrectly.

7. G.772 MONITORING

The receive path of channel zero of the CS61884 can be used to monitor the receive or transmit paths of any of the other channels. The signal to be monitored is multiplexed to channel zero through the G.772 Multiplexer. The multiplexer and channel zero then form a G.772 compliant digital Protected Monitoring Point (PMP). When the PMP is connected to the channel, the attenuation in the signal path is negligible across the signal band. The signal can be observed using RPOS, RNEG, and RCLK of channel zero or by putting channel zero in remote loop-back, the signal can be observed on TTIP and TRING of channel zero.

The G.772 monitoring function is available during both host mode and hardware mode operation. In host modes, individual channels are selected for monitoring via the **Performance Monitor Register (0Bh)** (See Section 14.12 on page 36). In hardware mode, individual channels are selected through the A3:A0 pins (Refer to [Table 4](#) below for address settings).

Table 4. G.772 Address Selection

Address [A3:A0]	Channel Selection
0000	Monitoring Disabled
0001	Receiver Channel # 1
0010	Receiver Channel # 2
0011	Receiver Channel # 3
0100	Receiver Channel # 4
0101	Receiver Channel # 5
0110	Receiver Channel # 6
0111	Receiver Channel # 7
1000	Monitoring Disabled
1001	Transmitter Channel # 1
1010	Transmitter Channel # 2
1011	Transmitter Channel # 3
1100	Transmitter Channel # 4
1101	Transmitter Channel # 5
1110	Transmitter Channel # 6
1111	Transmitter Channel # 7

NOTE: In hardware mode the A4 pin must be tied low at all times.

8. BUILDING INTEGRATED TIMING SYSTEMS (BITS) CLOCK MODE

This mode is used to enable one or more channels as a stand-alone timing recovery unit used for G.703 Clock Recovery.

In hardware mode, BITS Clock mode is selected by pulling the MUX pin “HIGH”. This enables only channel zero as a stand-alone timing recovery unit, no other channel can be used as a timing recovery unit.

In host mode, each channel can be setup as an independent G.703 timing recovery unit, through the **Bits Clock Enable Register (1Eh)** (See Section 14.31 on page 41), setting the desired bit to “1” enables BITS Clock mode for that channel. The following diagrams show how the BITS clock function operates.

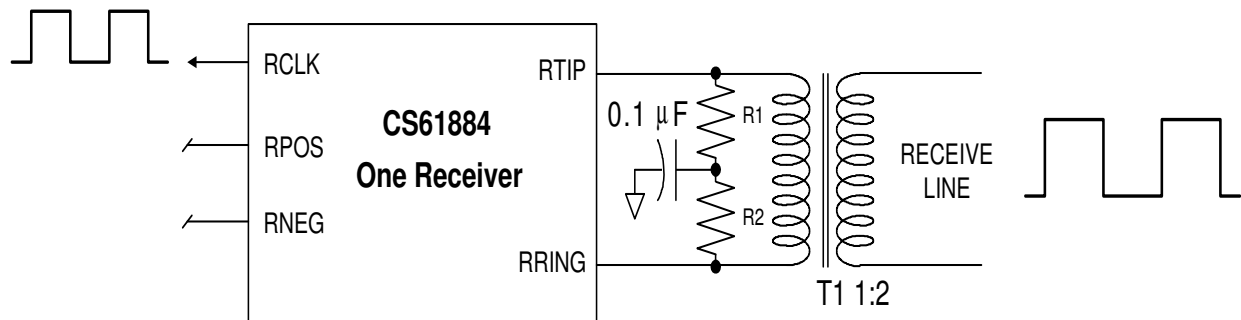


Figure 3. G.703 BITS Clock Mode in NRZ Mode

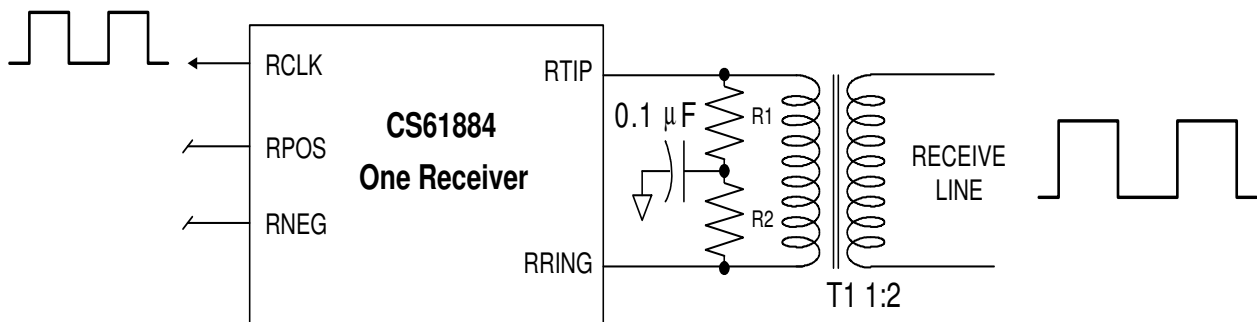


Figure 4. G.703 BITS Clock Mode in RZ Mode

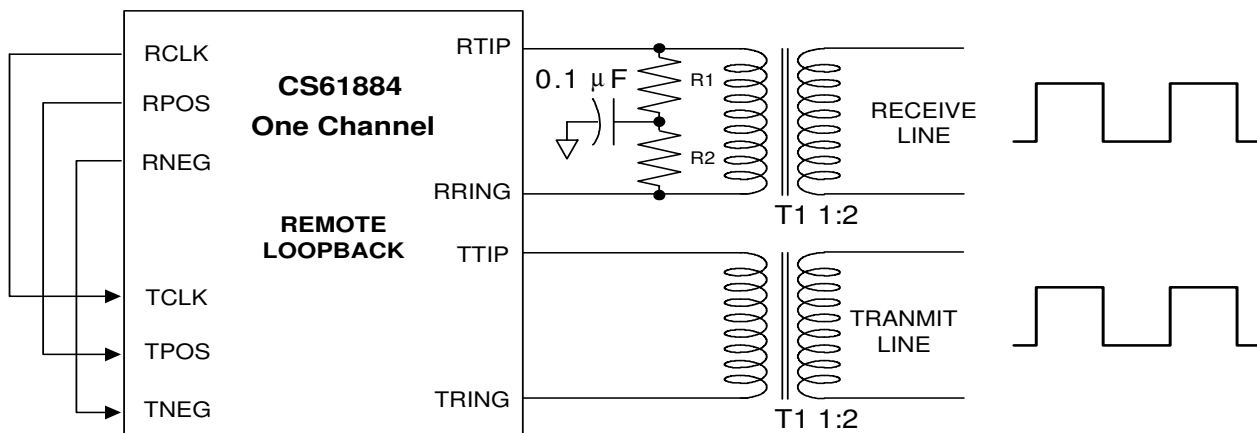


Figure 5. G.703 BITS Clock Mode in Remote Loopback

9. TRANSMITTER

The CS61884 contains eight identical transmitters that each use a low power matched impedance driver to eliminate the need for external load matching resistors, while providing superior return loss. As a result, the TTIP/TRING outputs can be connected directly to the transformer allowing one hardware circuit for 100 Ω (T1/J1), 120 Ω (E1), and 75 Ω (E1) applications.

Digital transmit data is input into the CS61884 through the TPOS/TNEG input pins. These pins accept data in one of three formats: unipolar, bipolar, or RZ. In either unipolar or bipolar mode, the CS61884 internally generates a pulse shape compliant to the ANSI T1.102 mask for T1/J1 or the G.703 mask for E1 (Refer to [Figure 6](#) and [Figure 7](#)). The pulse shaping applied to the transmit data can be selected in hardware mode or in host mode.

In hardware mode, the pulse shape is selected for all channels via the LEN[2:0] pins (Refer to [Table 5 on page 25](#)). This sets the pulse shape for all eight transmitters to one of the prestored line lengths. The CBLSEL pin in combination with the LEN[2:0] pins set the line impedance for all eight channels. The CBLSEL pin also selects between E1 120 Ω or E1 75 Ω modes, when the LEN pins are configured for E1 operation mode.

In host mode, the pulse shape for each channel can be set independently, during NRZ operation mode, for proper clock recovery and jitter attenuation. In RZ Mode each channel can be set to either T1/J1 or E1, when there is no Mclk present (Refer to [RZ Mode](#) (See Section 9.3 on page 25).

To select the standard pulse shapes, the channels are selected individually using the [Line Length Channel ID Register \(10h\)](#) (See Section 14.17 on page 38), then the LEN[3:0] bits in the [Line Length Data Register \(11h\)](#) (See Section 14.18 on page 39) are set for the desired line length for that channel. The LEN bits select the line type and im-

pedance for both the receiver and the transmitter of the addressed channel.

NOTE: In host mode the CBLSEL pin is not used.

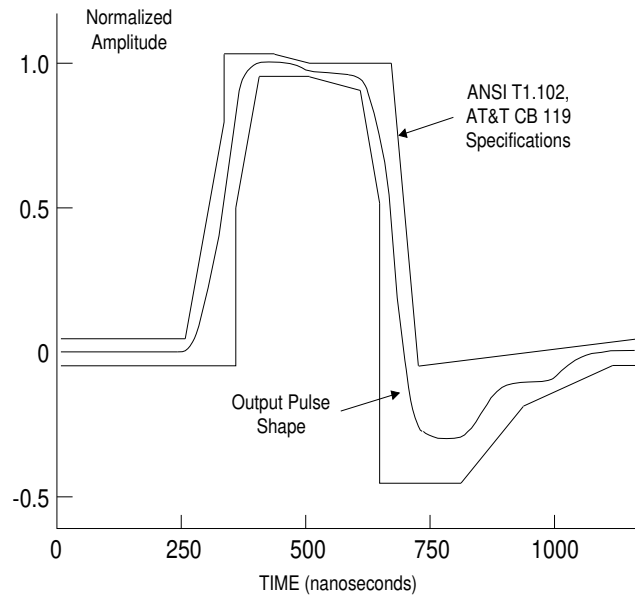


Figure 6. Pulse Mask at T1/J1 Interface

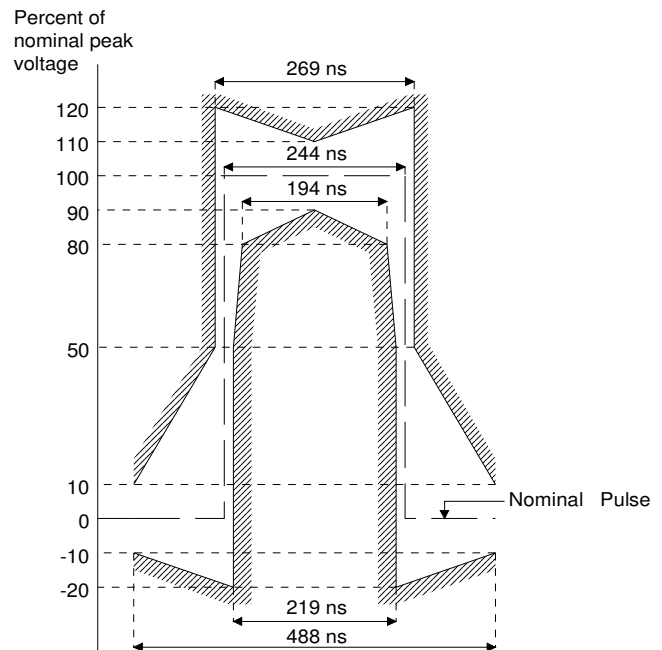


Figure 7. Pulse Mask at E1 Interface

The CS61884 also allows the user to customize the transmit pulse shapes to compensate for non-standard cables, transformers, or protection circuitry. For further information on the AWG Refer to [Arbitrary Waveform Generator](#) (See Section 15 on page 43).

For more information on the host mode registers, refer to [Register Descriptions](#) (See Section 14 on page 35).

9.1 Bipolar Mode

Bipolar mode provides transparent operation for applications in which the line coding function is performed by an external framing device. In this mode, the falling edge of TCLK samples NRZ data on TPOS/TNEG for transmission on TTIP/TRING.

9.2 Unipolar Mode

In unipolar mode, the CS61884 is configured such that transmit data is encoded using B8ZS, HDB3, or AMI line codes. This mode is activated by holding TNEG/UBS “High” for more than 16 TCLK cycles. Transmit data is input to the part via the TPOS/TDATA pin on the falling edge of TCLK. When operating the part in hardware mode, the CODEN pin is used to select between B8ZS/HDB3 or AMI encoding. During host mode operation, the line coding is selected via the [Global Control Register \(0Fh\)](#) (See Section 14.16 on page 38).

NOTE: The encoders/decoders are selected for all eight channels in both hardware and host mode.

9.3 RZ Mode

In RZ mode, the internal pulse shape circuitry is bypassed and RZ data driven into TPOS/TNEG is transmitted on TTIP/TRING. In this mode, the pulse width of the transmitter output is determined by the width of the RZ signal input to TPOS/TNEG. This mode is entered when MCLK does not exist and TCLK is held “High” for at least 12 μ sec.

9.4 Transmitter Powerdown / High-Z

The transmitters can be forced into a high impedance, low power state by holding TCLK of the appropriate channel low for at least 12 μ s or 140 MCLK cycles. In hardware and host mode, the TXOE pin forces all eight transmitters into a high impedance state within 1 μ s.

In host mode, each transmitter is individually controllable using the [Output Disable Register \(12h\)](#) (See Section 14.19 on page 39). The TXOE pin can be used in host mode, but does not effect the contents of the Output Enable Register. This feature is useful in applications that require redundancy.

9.5 Transmit All Ones (TAOS)

When TAOS is activated, continuous ones are transmitted on TTIP/TRING using MCLK as the transmit timing reference. In this mode, the TPOS and TNEG inputs are ignored.

In hardware mode, TAOS is activated by pulling TCLK “High” for more than 16 MCLK cycles.

Table 5. Hardware Mode Line Length Configuration Selection

LEN[2:0]	Transmit Pulse Configuration	Line Z	Operation
000	E1 3.0V / E1 2.37V	120 Ω / 75 Ω	E1
001	DS1, Option A (undershoot)	100 Ω	T1/J1
010	DS1, Option A (0 dB)	100 Ω	T1/J1
011	DSX-1: 0-133 ft. (0.6dB)	100 Ω	T1/J1
100	DSX-1: 133-266 ft. (1.2dB)	100 Ω	T1/J1
101	DSX-1: 266-399 ft. (1.8dB)	100 Ω	T1/J1
110	DSX-1: 399-533 ft. (2.4dB)	100 Ω	T1/J1
111	DSX-1: 533-655 ft. (3.0dB)	100 Ω	T1/J1