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CS6422

Enhanced Full-duplex Speakerphone IC

Features

- Single-chip, full-duplex, hands-free operation
- Optional Tx Noise Guard
- Programmable attenuation during double-talk
- Optional 34 dB microphone preamplifier
- Dual channel AGC'ed volume controls with mute
- Dual integrated 80 dB IDR codecs
- Speech-trained Network and Acoustic Echo Cancellers
- Rx and Tx supplementary echo suppression
- Configurable half-duplex training mode
- Powerdown mode
- Microcontroller Interface

General Description

Most modern speakerphones use half-duplex operation, which alternates transmission between the far-end talker and the speakerphone user. This is done to ensure stability because the acoustic coupling between the speaker and microphone is much higher in speakerphones than in handsets where the coupling is mechanically suppressed.

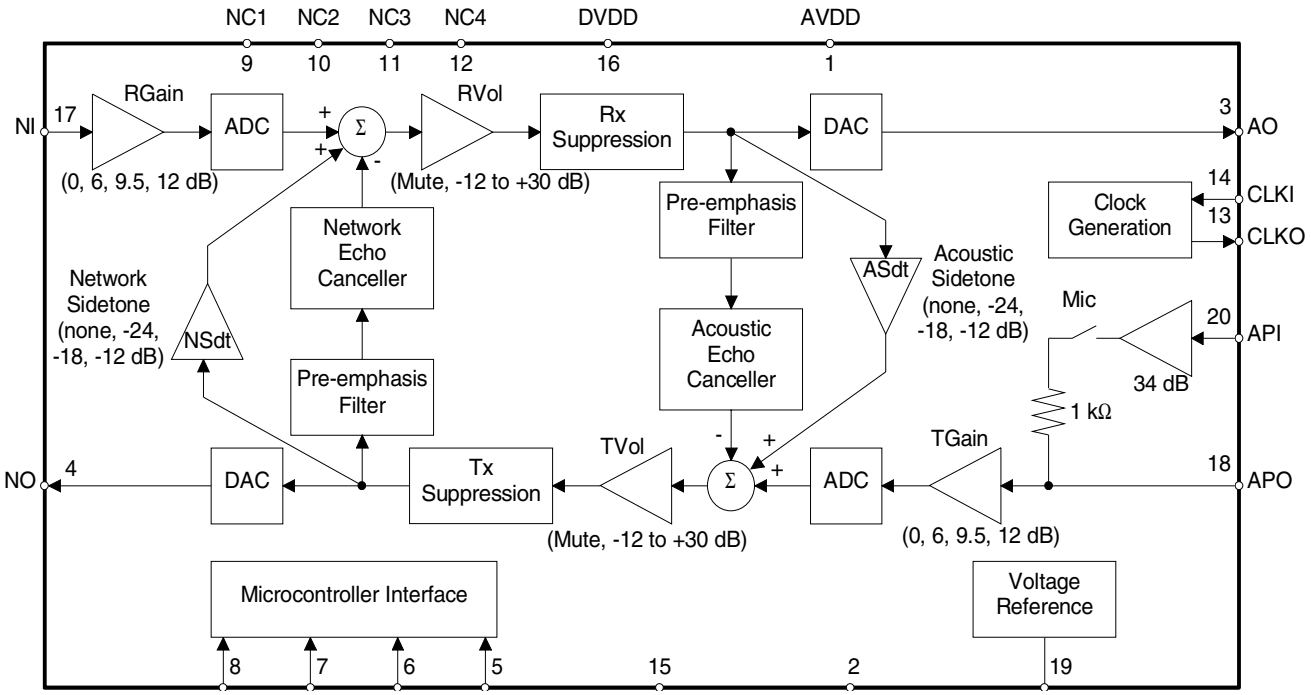
The CS6422 enables full-duplex conversation using echo cancellation and suppression in a single-chip solution. The CS6422 can easily replace existing half-duplex speakerphone ICs with a huge increase in conversation quality.

The CS6422 consists of telephone & audio interfaces, two codecs and an echo-cancelling DSP.

ORDERING INFORMATION

See page 48.

CDB6422 Evaluation Board



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1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Supply (AVDD, DVDD)			-0.3	6.0	V
Input Current (Except supply pins)		I_{in}	-10	+10	mA
Input Voltage	Analog Digital	V_{ina} V_{ind}	-0.3 -0.3	AVDD+0.3 DVDD+0.3	V
Ambient Operating Temperature		T_A	-40	85	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operation beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Units
DC Supply (AVDD, DVDD)			4.5	5.0	5.5	V
Ambient Operating Temperature	Commercial Industrial	T_{AOp}	0 -40	25 25	70 85	°C

POWER CONSUMPTION (T_A = 25°C, DVDD = AVDD = 5 V, f_{XTAL} = 20.480 MHz) (Note 1)

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Current, Analog ($\overline{RST}$=0)	P_{DA0}			1	mA
Power Supply Current, Analog ($\overline{RST}$=1)	P_{DA}		10	20	mA
Power Supply Current, Digital ($\overline{RST}$=0)	P_{DD0}			1	mA
Power Supply Current, Digital ($\overline{RST}$=1)	P_{DD}		50	80	mA

Notes: 1. AO and NO outputs are not loaded.

ANALOG CHARACTERISTICS (T_A = 25°C, DVDD = AVDD = 5 V, f_{XTAL} = 20.480 MHz)

Parameter		Symbol	Min	Typ	Max	Units
Input Offset Voltage (APO, NI)				2.12		V
Output Offset Voltage (AO, NO)				2.12		V
Transmit Group Delay	(Note 2)				6	ms
Receive Group Delay	(Note 2)				6	ms
Input Impedance (APO, NI)		Z_{in}		1.5		MΩ
Load Impedance (AO, NO)		Z_{load}	10			kΩ
Power Supply Rejection (1 kHz)				40		dB

Notes: 2. These parameters are guaranteed by design or by characterization.

ANALOG TRANSMISSION CHARACTERISTICS (T_A = 25°C, DVDD = AVDD = 5 V, f_{XTAL} = 20.480 MHz, RVol=TVol=RGain=TGain= 0 dB, HDD=TSD=RSD=1, analog inputs and outputs loaded with resistors and capacitors as shown in the typical connection diagram, Figure 4)

Parameter		Symbol	Min	Typ	Max	Units
Idle Channel Noise (Inputs grounded through a capacitor)	C-Message weighted (0-4 kHz) C-Message weighted (0-4 kHz) Psophometrically weighted (0-4 kHz)			-80 11 -78	-73	dBV dBrnC0 dBm0p
Signal-to-Noise Ratio (1.0 V_{rms}, 1 kHz sine wave input)	C-Message weighted (0-4 kHz)	SNR	73	80		dB
Total Harmonic Distortion (1.0 V_{rms}, 1 kHz sine wave input)	C-Message weighted (0-4 kHz)	THD		0.030	0.1	%
Programmable Analog Gain	RGain/TGain = 00 RGain/TGain = 01 RGain/TGain = 10 RGain/TGain = 11			0 6 9.5 12		dB
Volume Control Stepsize (TVol/RVol)				3		dB
ADC Full-scale Voltage Input			0.9	1.0		V_{rms}
DAC Full-scale Voltage Output				1.0	1.2	V_{rms}
ADC Noise Floor	C-Message weighted (0-4 kHz)			-83		dBV
DAC Noise Floor, DAC muted	C-Message weighted (0-4 kHz)			-83		dBV

MICROPHONE AMPLIFIER (T_A = 25°C, DVDD = AVDD = 5 V, f_{XTAL} = 20.480 MHz)

Parameter		Symbol	Min	Typ	Max	Units
Gain (Z_{source} = 50Ω)		A_{mic}		34		dB
Signal-to-Noise Ratio	C-Message weighted (0-4 kHz)	SNRm		70		dB
Input Impedance		Z_{inm}		8		kΩ
Input Offset Voltage		V_{offm}		2.12		V

DIGITAL CHARACTERISTICS (T_A = 25°C, DVDD = AVDD = 5 V,f_{XTAL} = 20.480 MHz)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	DVDD-1.0			V
Low-Level Input Voltage	V_{IL}			1.0	V
Input Leakage Current	I_{leak}			10	µA
Input Capacitance	C_{IN}		5		pF

ANALOG TRANSMISSION CHARACTERISTICS (T_A = -40°C to 85°C, DVDD = AVDD = 5 V, f_{XTAL} =20.480 MHz, RVol=TVol=RGain=TGain= 0 dB, HDD=TSD=RSD=1, analog inputs and outputs loaded with resistors and capacitors as shown in the typical connection diagram, Figure 4)

Parameter		Symbol	Min	Typ	Max	Units
Idle Channel Noise	C-Message weighted (0-4 kHz)			-80	-72	dBV
(Inputs grounded	C-Message weighted (0-4 kHz)			11		dBrnC0
through a capacitor)	Psophometrically weighted (0-4 kHz)			-78		dBm0p
Signal-to-Noise Ratio (1.0 V_{rms}, 1 kHz sine wave input)	C-Message weighted (0-4 kHz)	SNR	72	80		dB
Total Harmonic Distortion (1.0 V_{rms}, 1 kHz sine wave input)	C-Message weighted (0-4 kHz)	THD		0.030	0.1	%
Programmable Analog Gain	RGain/TGain = 00			0		dB
	RGain/TGain = 01			6		
	RGain/TGain = 10			9.5		
	RGain/TGain = 11			12		
Volume Control Stepsize (TVol/RVol)				3		dB
ADC Full-scale Voltage Input			0.9	1.0		V_{rms}
DAC Full-scale Voltage Output				1.0	1.2	V_{rms}
ADC Noise Floor	C-Message weighted (0-4 kHz)			-83		dBV
DAC Noise Floor, DAC muted	C-Message weighted (0-4 kHz)			-83		dBV

MICROPHONE AMPLIFIER (T_A = 25°C, DVDD = AVDD = 5 V, f_{XTAL} = 20.480 MHz)

Parameter		Symbol	Min	Typ	Max	Units
Gain (Z_{source} = 50Ω)		A_{mic}		34		dB
Signal-to-Noise Ratio	C-Message weighted (0-4 kHz)	SNRm		70		dB
Input Impedance		Z_{inm}		8		kΩ
Input Offset Voltage		V_{offm}		2.12		V

DIGITAL CHARACTERISTICS (T_A = 25°C, DVDD = AVDD = 5 V,f_{XTAL} = 20.480 MHz)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	DVDD-1.0			V
Low-Level Input Voltage	V_{IL}			1.0	V
Input Leakage Current	I_{leak}			10	µA
Input Capacitance	C_{IN}		5		pF

SWITCHING CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units
Digital input rise time	t_{rise}			1.0	µs
$\overline{RST}$ low time	t_{RSTL}	1.0			µs
CLKI frequency	f_{CLKI}		20.480		MHz
CLKI duty cycle	t_{LCLKI}	40	50	60	%
CLKI high or low time	t_{HLCLKI}	19.5			ns
Min $\overline{DRDY}$ falling to $\overline{DRDY}$ falling (CLKI = 20.480 MHz)	t_{DRDY}		125		µs
STROBE high or low time	$t_{HLSTROBE}$	55			ns
$\overline{DRDY}$ falling to STROBE rising setup time	t_{sDRDY}	30			ns
DATA valid to STROBE rising setup time	t_{sDATA}	30			ns
STROBE rising to DATA valid hold time	t_{hDATA}	30			ns
STROBE rising to $\overline{DRDY}$ rising hold time	t_{hDRDY}	30			ns
Min $\overline{RST}$ rising to 4th extra STROBE pulse (cold reset)	t_{cRST}		110		ms
Max $\overline{RST}$ rising to 4th extra STROBE pulse (warm reset)	t_{wRST}		100		ms

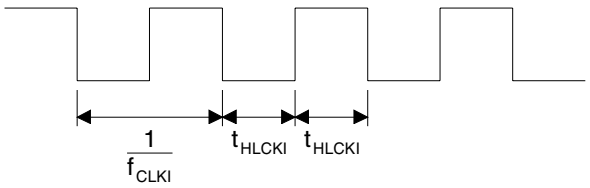

Figure 1. CLKI Timing

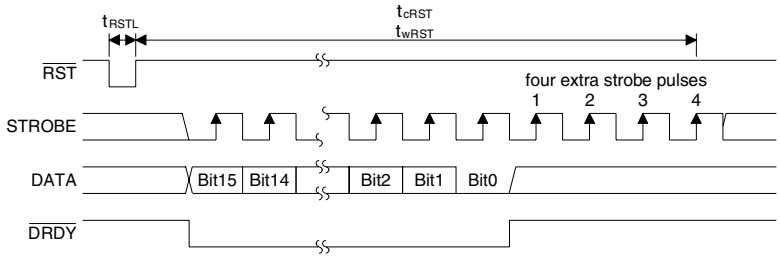

Figure 2. Reset Timing

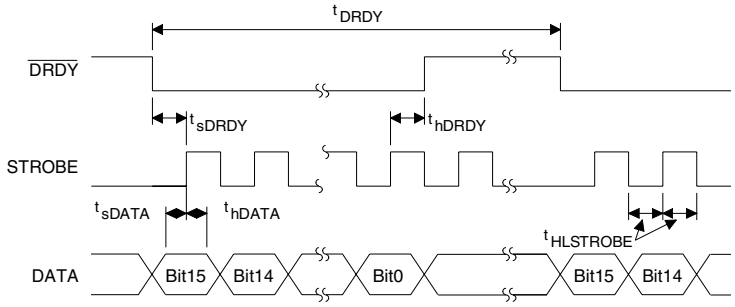

Figure 3. Microcontroller Interface Timing

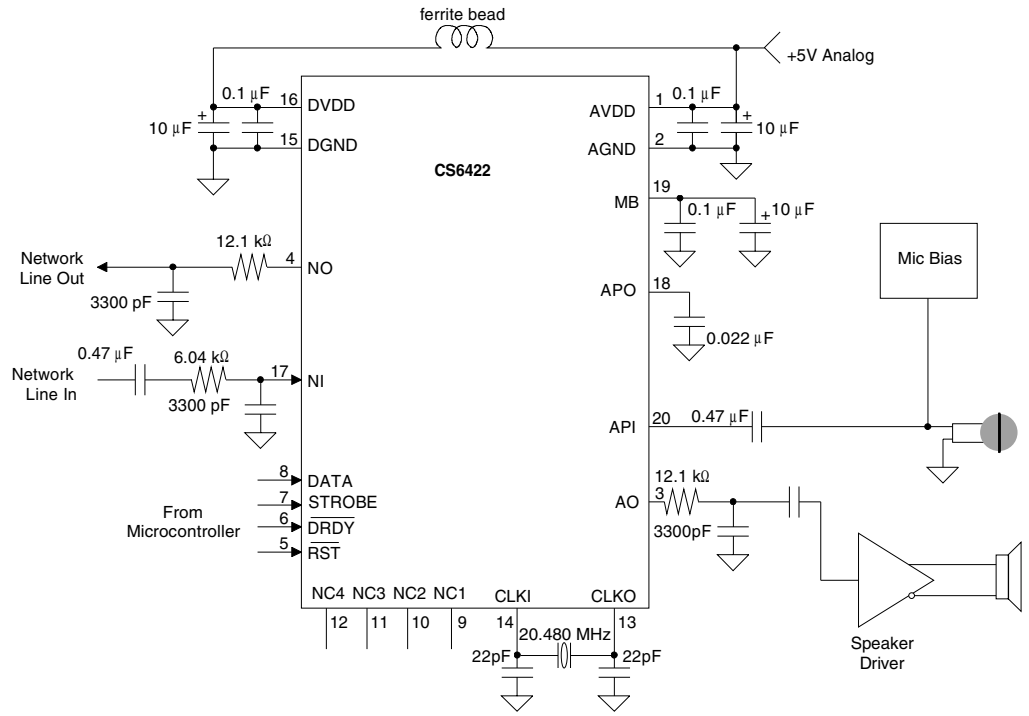

Figure 4. Typical Connection Diagram (Microphone Preamplifier Enabled)

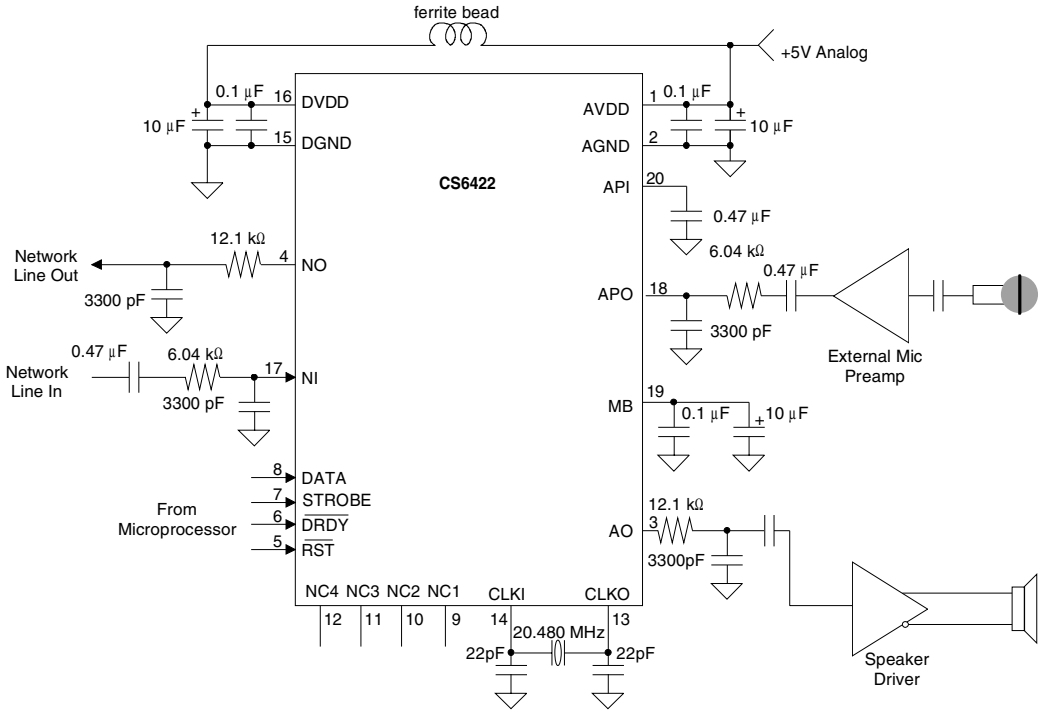

Figure 5. Typical Connection Diagram (Microphone Preamplifier Disabled)

2. OVERVIEW

The CS6422 is a full-duplex speakerphone chip for use in hands-free communications with telephony quality audio. Common applications include speakerphones, inexpensive video-conferencing, and hands-free cellular phone car kits. The CS6422 requires very few external components and allows system control through a microcontroller interface.

Hands-free communication through a microphone and speaker typically results in acoustic feedback or howling because the loop gain of the system exceeds unity by the time audio amplitudes are adjusted to a reasonable level. The solution to the howling problem has typically been half-duplex, where either the transmit or the receive channel is active, never both at the same time. This prevents instability, but diminishes the overall communication quality by clipping words and forcing each talker to speak in turn.

Full-duplex conversation, where both transmit and receive channels are active simultaneously, is the conversation quality we enjoy when using handsets. Full-duplex for hands-free communications is achieved in the CS6422 using a digital signal processing technique called "Echo Cancellation." The end result is a more natural conversation than half-duplex, with no awkward breaks and pauses, allowing both parties to speak simultaneously.

Echo Cancellation reduces overall loop gain and the acoustic coupling between speaker and microphone. This coupling reduction prevents the annoying effect of hearing one's own delayed speech, which is worsened when there is delay in the system, such as vocoder delay in digital cellular phones.

The CS6422 is a complete system implementation of a Digital Signal Processor with RAM and program ROM, running Echo Cancellation algorithms developed at Crystal Semiconductor using customer input, integrated with two delta-sigma codecs. The CS6422 is intended to provide a full-duplex speakerphone solution with a minimum of design effort while displacing existing half-duplex speakerphone chips.

3. FUNCTIONAL DESCRIPTION

The CS6422 is divided into four external interface blocks. The analog interfaces connect the device to the transmit and receive paths. Control functions are accessible through the microcontroller interface. Two pins accommodate either a crystal or an externally applied digital clock signal. Analog and digital power and ground are provided through four pins.

3.1 Analog Interface

In a speakerphone application, one input of the CS6422 connects to the signal from the microphone, called the near-end or transmit input, and one output connects to the speaker. The output that leads to the speaker is called the near-end or receive output. Together, the input and output that connect to the microphone and speaker form the Acoustic Interface.

The signal received at the near-end input is passed to the far-end or transmit output after acoustic echo cancellation. This signal is sent to the telephone line. The signal from the telephone line is received at the far-end input, also called the receive input, and this signal is passed to the receive output after network echo cancellation. The far-end input and output form the Network Interface.

The analog interfaces are physically implemented using delta sigma converters running at an output word rate of 8 kHz, resulting in a passband from DC to 4 kHz. Because the inputs are analog to digital converters (ADCs), anti-aliasing and full-scale input voltage must be kept in mind. The ADCs expect a single-pole RC filter with a corner at 8 kHz, and they are post-compensated internally to prevent any resulting passband droop. The ADCs also expect a maximum of 0.9 V_{rms} (2.5 V_{pp}) at their inputs (which are biased around 2.12 VDC). A signal

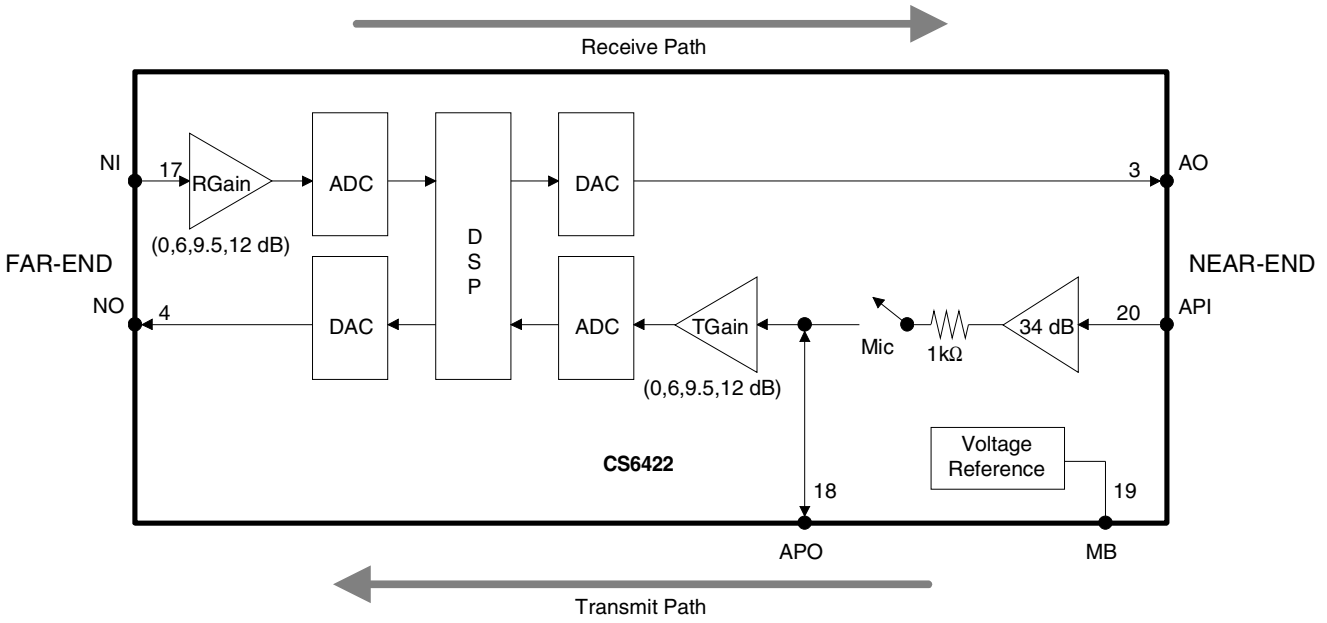

Figure 6. Analog Interface

of higher amplitude will clip the ADC input and will result in poor echo canceller performance. See Section 4., "Design Considerations" for more details.

The outputs are delta-sigma digital to analog converters (DACs) and have similar requirements to the ADCs. The DACs are pre-compensated to expect a single-pole RC filter with a corner frequency at 4 kHz. The full scale voltage output from a DAC is 1.1 V_{rms} (3.1 V_{pp}) maximum, 1 V_{rms} typical, biased around 2.12 VDC.

3.1.1 Acoustic Interface

The pins API (pin 20), APO (pin 18), AO (pin 3), and MB (pin 19) form the Acoustic Interface. A block diagram of the Acoustic Interface is shown in Figure 6.

API and APO are, respectively, the input and output of the built-in microphone pre-amplifier. The pre-amplifier is an inverting amplifier with a fixed gain of 34 dB biased around an input offset voltage of 2.12 V. APO is the output of the pre-amplifier after a 1 kΩ (typical) resistor. The circuitry connected to the amplifier input must present low source impedance (<100 Ω) to the API pin or the gain will be reduced. When using the internal mic preamp, a 0.022 µF capacitor should be placed between APO and ground to provide the anti-aliasing filter required by the ADC, as shown in Figure 4. The pre-amplifier may be bypassed by clearing the 'Mic' bit (Register 0, bit 15) using the Microcontroller Interface (see Section 3.2, "Microcontroller Interface"). If the internal mic preamp is not used, a 0.022 µF capacitor should be tied between API and ground, and APO should be driven directly. In this case, the signal into APO must be low-pass filtered by a single-pole RC filter with a corner frequency at 8 kHz (see Figure 5).

Following the pre-amplifier is a programmable analog gain stage, called TGain, which is controlled

through the Microcontroller Interface. This gain stage allows gains of 0 dB, 6 dB, 9.5 dB, and 12 dB to be added prior to the ADC input. The default gain stage setting is 0 dB.

The signal at APO should not exceed 2.5 V_{pp} at the 0 dB gain stage setting. If a different gain setting is used, then the full-scale signal at APO must also change. Table 1 shows full-scale voltages as measured at APO for the given programmable gain:

Gain Setting	Full-scale Voltage
0 dB	2.5 V_{pp}
6 dB	1.25 V_{pp}
9.5 dB	0.84 V_{pp}
12 dB	0.63 V_{pp}

Table 1. Full scale voltages for each gain stage

MB serves to provide decoupling for the internal voltage reference, and must have a 0.1 µF and a 10 µF capacitor to ground for bypass. *Noise on MB will strongly influence the overall analog performance of the CS6422.*

The acoustic output, AO, should connect to a single-pole low-pass RC network with a corner frequency of 4 kHz, which will filter out-of-band components. The full-scale voltage swing at AO is 3.1 V_{pp} maximum, 1 V_{rms} typical. AO is capable of driving a load of 10 kΩ or more.

3.1.2 Network Interface

The pins NI (pin 17) and NO (pin 4) form the Network Interface. The details of the Network Interface are shown in Figure 6.

NI is the input from the telephone network into the CS6422. The signal into NI must be low pass filtered by a single-pole RC filter with a corner frequency of 8 kHz.

RGain, a programmable analog gain stage accessible through the Microcontroller Interface, amplifies signals received at NI. This gain stage allows a gain of 0 dB, 6 dB, 9.5 dB, or 12 dB to be added prior to the ADC input. The default gain stage setting for the network side is 0 dB.

The signal at NI should not exceed 2.5 V_{pp} at the 0 dB gain stage setting. If another gain setting is selected, then the full-scale signal at NI will change. Table 1 shows full-scale voltages as measured at NI for the given programmable gain.

The output to the telephone network side, NO, should connect to a single pole RC network with a corner frequency at 4 kHz, which will filter out-of-band components. The maximum swing NO is capable of producing is 3.1 V_{pp} maximum, 1 V_{rms} typical. NO is capable of driving a load of 10 kΩ or more.

3.2 Microcontroller Interface

The registers and control functions of the CS6422 are accessible through the Microcontroller Interface, which consists of three pins: DATA (pin 8), STROBE (pin 7), and $\overline{\text{DRDY}}$ (pin 6). These inputs can connect to the outputs of a microcontroller to allow write-only access to the 16-bit Microcontroller Control Register (MCR).

3.2.1 Description

The Microcontroller Interface is implemented by a serial shift register that is clocked by STROBE and gated by $\overline{\text{DRDY}}$. The microcontroller begins the transaction by setting $\overline{\text{DRDY}}$ low while STROBE is low. The most significant bit (MSB), Bit 15, of the 16-bit data word should be presented to the DATA pin and then STROBE should be brought high to shift the data bit into the CS6422. STROBE should be brought low again so it is ready to shift the next bit into the shift register. The next data bit should then be presented to the DATA pin ready to be latched by the rising edge of STROBE. This procedure repeats for all sixteen bits as shown in Figure 7. After the last bit (Bit 0) has been shifted in, $\overline{\text{DRDY}}$ should be brought high to indicate the conclusion of the transfer, and *four or more extra*

STROBE pulses must be applied to latch the data into the CS6422.

Since the MCR is a shift register, the STROBE can be run arbitrarily slowly with a duty cycle limited only by the minimum high and low time specified in *"Switching Characteristics"*. *The Microcontroller Interface is polled at 125 µs intervals, so register writes must be spaced at least 125 µs apart or the register contents may be overwritten.*

3.2.2 Register Definitions

The six control registers accessible through the MCR are described in detail in the following tables. These registers are addressed by bits b3-0 of the MCR. *Bit 'b0' must always be '0'*. Table 2 shows the register map with the default settings. Tables 3 through 8 show the control registers in more detail.

The Register Map at the top of each register description shows the names of all the bits, with their reset values below the bitfield name. The reset value can also be found in the Word column of the bitfield summary as indicated by an '*'.

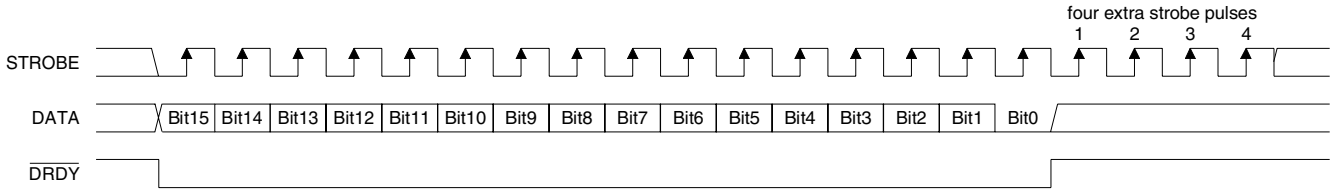

Figure 7. Microcontroller Interface

#	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3-0
0	Mic 1	HDD 0	GB 10		RVol 0100				TSD 0	ACC 00		TSMde 0	0000
1	THDet 00		Taps 10		TVol 1010				RSD 0	NCC 00		AuNECD 0	0010
2	RHDet 00		RSThd 00		NseRmp 00		HDly 00		HHold 0	TDSRmp 0	RDSRmp 0	IdlTx 0	0100
3	TSAtt 00		PCSen 0	TDbtS 000			RDbtS 00		TSThd 00		TSBias 00		0110
4	AErle 00		AFNse 00		NErle 00		NFNse 00		RGain 00		TGain 00		1000
5	HwID 0	TD 0	APCD 0	NPCD 0	APFD 0	NPFD 0	AECD 0	NECD 0	ASdt 00		NSdt 00		1010

Table 2. MCR Control Register Mapping

3.3 Register 0

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Mic	HDD	GB		RVol				TSD	ACC		TSMde	0	0	0	0
1	0	10		0100				0	00		0				
A				4				0				0			

Bits	Name	Function	Word	Operation
15	Mic	Microphone preamplifier enable	0 1*	disable mic preamp enable mic preamp
14	HDD	Half-Duplex Disable	0* 1	enable half-duplex disable half-duplex
13-12	GB	Graded Beta	00 01 10* 11	0.00 dB/ms 0.75 dB/ms 0.38 dB/ms 0.19 dB/ms
11-8	RVol	Rx Volume control	0000 0001 --- 0100* --- 1010 1011 --- 1101 1110 1111	+30 dB +27 dB --- +18 dB --- +0 dB -3 dB --- -9 dB -12 dB mute
7	TSD	Tx Suppression Disable	0* 1	enable Tx suppression disable Tx suppression
6-5	ACC	AEC Coefficient Control	00* 01 10 11	Normal Clear Freeze reserved
4	TSMde	Tx Suppression Mode	0* 1	enable noise guard disable noise guard

* Denotes reset value

Table 3. Register 0 Bit Definitions

3.3.1 MIC - MICROPHONE PREAMPLIFIER ENABLE

The microphone preamplifier described in Section 3.1.1, “Acoustic Interface” is enabled by default, but may be disabled by setting Mic to ‘0’. Refer to Section 3.1.1, “Acoustic Interface” for more details on using the Microphone Preamplifier.

3.3.2 HDD - HALF-DUPLEX DISABLE

In normal operation, the CS6422 will be in a half-duplex mode if the echo canceller is not providing enough loop gain reduction to prevent howling. This half-duplex mode is active at power-up while the adaptive filter begins to train. Half-duplex mode prevents howling and also masks the convergence process.

In some cases, such as when measuring convergence speed (see Section 4.3.2, “Testing Issues”), the half-duplex mode is undesirable. By default, the half-duplex mode is enabled.

3.3.3 GB - GRADED BETA

The room-size adjustment scheme called “graded beta,” provided for the acoustic echo canceller in the CS6422, is controlled by GB. The network echo canceller does not support graded beta.

Graded beta is an architectural enhancement to the CS6422 which takes advantage of the fact that acoustic echoes tend to decay exponentially with time. The CS6422 can increase the beta, or update gain, for the coefficients of the adaptive filter which occur earlier in time and decrease it for those that occur later in time, which increases convergence speed while maintaining stability. In order to make this improvement, there is an implicit assumption that the decay rate of the echo is known. The graded beta control allows the system designer to adjust this. For very acoustically live rooms, use either no decay (00) or slight decay (11). Cars and acoustically dead rooms can benefit from the most rapid decay (01).

3.3.4 RVOL - RECEIVE VOLUME CONTROL

Volume in the receive path is set by RVol. The volume control in the receive direction is implemented by a peak-limiting automatic gain control (AGC) and digital attenuation at the near-end output DAC.

The AGC is discussed in detail in Section 4., “Design Considerations”. See Section 4.1.3, “AGC”for a full explanation of how it functions.

When the reference level is set to +0 dB, the AGC is disabled. Volume control is implemented by digital attenuation in 3 dB steps from this point on down. The maximum gain is +30 dB and the minimum is -12 dB. The lowest gain setting (1111) mutes the receive path.

The default setting for RVol is +18 dB.

3.3.5 TSD - TRANSMIT SUPPRESSION DISABLE

The Transmit Supplementary Echo Suppression function is a non-linear echo control mechanism. Transmit Suppression introduces TSAtt (see Register 3) of attenuation into the transmit path when it is engaged. When TSMde = ‘1’, the transmit suppressor engages when there is speech detected in the receive path and no near-end speech is present. When TSMde = ‘0’, the default case, the transmit suppressor engages when there is no near-end speech present. When near-end speech is present, the suppression attenuation is removed. By default, the transmit suppression function is enabled.

3.3.6 ACC - ACOUSTIC COEFFICIENT CONTROL

The coefficients of the AEC adaptive filters in the CS6422 are controlled by ACC. The default position (00) yields normal operation, which means the coefficients are free to adjust themselves to the echo path in order to cancel echo. When set to the clear position (01), the adaptive filter coefficients are all held at zero, so the echo canceller is effectively disabled. Note that unless the half-duplex mode is disabled, this will force the CS6422 into half-duplex mode. The freeze position (10) causes the coefficients to retain their current values and not change.

3.3.7 TSMDE - TRANSMIT SUPPRESSION MODE

TSMde enables the Noise Guard feature of the CS6422. Noise Guard is a noise squelch feature that operates in the transmit path (from the near-end microphone to the far-end speaker). In traditional hands-free systems where the near-end talker is located in a noisy environment, the near-end system will remain in transmit mode and send that noise to the far-end listener. This creates a real problem if the listener is using a traditional half-duplex speakerphone because the far-end phone will stay in receive mode, thus preventing the far-end talker from being heard. Noise Guard eliminates this problem by squelching the transmit channel at the near-end unless near-end speech is detected, permitting the far-end speakerphone to switch normally during the conversation.

Noise Guard is also useful in cellular hands-free car applications because it prevents car noise from reaching the far-end while the near-end talker is silent.

Noise Guard is usually disabled when "half-duplex Idle return-to-Transmit" is enabled. See the Register 2 description for more information. Noise Guard is enabled by default.

3.4 Register 1

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
THDet		Taps		TVol				RSD	NCC		AuNECD	0	0	1	0
00		10		1010				0	00		0				
2				A				0				2			

Bits	Name	Function	Word	Operation
15-14	THDet	Tx Half-duplex Detection threshold	00* 01 10 11	6 dB 9 dB 12 dB reserved
13-12	Taps	AEC/NEC Tap allocation	00 01 10* 11	444/64 (55.5 ms/8 ms) 380/128 (47.5 ms/16 ms) 316/192 (39.5 ms/24 ms) 252/256 (31.5 ms/32 ms)
11-8	TVol	Tx Volume control	0000 0001 --- 0100 --- 1010* 1011 --- 1101 1110 1111	+30 dB +27 dB --- +18 dB --- +0 dB -3 dB --- -9 dB -12 dB mute
7	RSD	Rx Suppression Disable	0* 1	enable Rx suppression disable Rx suppression
6-5	NCC	NEC Coefficient Control	00* 01 10 11	Normal Clear Freeze reserved
4	AuNECD	Auto re-engage NEC Disable	0* 1	enable Auto NEC disable Auto NEC

* Denotes reset value

Table 4. Register 1 Bit Definitions

3.4.1 THDET - TRANSMIT HALF-DUPLEX DETECTION THRESHOLD

The sensitivity of the speech detector controls channel switching and ownership in half-duplex mode. The transmit speech detector registers speech if the transmit channel signal power is THDet above the noise floor of the transmit channel.

3.4.2 TAPS - AEC/NEC TAP ALLOCATION

The CS6422 has a total of 63.5 ms of echo canceller taps that it can partition for use by the network and acoustic echo cancellers. By default, the CS6422 allocates 39.5 ms for the AEC and 24 ms for the NEC. See NErle, NFNse, AErle, and AFNse in Register 4, and AECD and NECD in Register 5 for more options when an echo path is nonexistent.

3.4.3 TVOL - TRANSMIT VOLUME CONTROL

Volume in the transmit path is controlled by TVol. Like receive volume, the transmit volume is controlled by an AGC. See RVol in Register 0 for more details. The default setting for TVol is +0 dB.

3.4.4 RSD - RECEIVE SUPPRESSION DISABLE

The Receive Supplementary Echo Suppression function is a non-linear echo control mechanism. Supplementary Echo Suppression attenuates signals in the receive direction by 24 dB when far-end speech is absent in the receive path. The attenuation is released only when the receive channel is active. By default, the receive suppression function is enabled.

3.4.5 NCC - NETWORK COEFFICIENT CONTROL

The NEC adaptive filter's coefficients are controlled by NCC. See ACC in Register 0 for more details. The default setting for NCC is Normal mode.

3.4.6 AUNECD - AUTO RE-ENGAGE NEC DISABLE

AuNECD works in conjunction with NFNse in the determination of whether the Network Echo Canceller should be enabled or disabled. If the CS6422 determines that a network coupling path does not exist and disables the NEC (which can occur only if NFNse is set to a non-zero value), then AuNECD allows the DSP to re-enable the NEC if at some point during the call a network path appears.

An example occurs in a digital PBX environment. Initially, a 4-wire 'intercom' call is placed between two stations. The CS6422 at the near-end determines that a network path is not present and disables the NEC. During the call, one of the stations conferences in a call from an external analog line. A network coupling path is introduced by the addition of the analog line due to the impedance mismatch at the 2-to-4 wire converter. If AuNECD is enabled, the CS6422 at the near-end will detect the presence of the network coupling path and re-enable the NEC automatically, drop to half-duplex, and retrain.

3.5 Register 2

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RHDet		RSThd		NseRmp		HDly		HHold	TDSRmp	RDSRmp	IdlTx	0	1	0	0
00		00		00		00		0	0	0	0				
0				0				0				4			

Bits	Name	Function	Word	Operation
15-14	RHDet	Rx Half-duplex Detection threshold	00* 01 10 11	6 dB 9 dB 12 dB reserved
13-12	RSThd	Rx Suppression Threshold	00* 01 10 11	6 dB 9 dB 12 dB reserved
11-10	NseRmp	Noise estimator Ramp rate	00* 01 10 11	3 dB/s 6 dB/s 12 dB/s reserved
9-8	HDly	half-duplex Holdover Delay	00* 01 10 11	200 ms 100 ms 150 ms reserved
7	HHold	Hold in half-duplex on Howl	0* 1	disable HHold enable HHold
6	TDSRmp	Tx Double-talk Suppression Ramp rate	0* 1	slow normal
5	RDSRmp	Rx Double-talk Suppression Ramp rate	0* 1	slow normal
4	IdlTx	half-duplex Idle return-to-Transmit	0* 1	disable IdlTx enable IdlTx

* Denotes reset value

Table 5. Register 2 Bit Definitions

3.5.1 RHDET - RECEIVE HALF-DUPLEX DETECTION THRESHOLD

The sensitivity of the speech detector controls channel switching and ownership in half-duplex mode. The receive speech detector registers speech if the receive channel signal power is RHDet above the noise floor for the receive channel.

3.5.2 RSTHD - RECEIVE SUPPRESSION THRESHOLD

This parameter sets the threshold for far-end speech detection for disengaging receive suppression. The speech detector that disengages the receive suppression has its sensitivity controlled by RSThd. The suppression is inserted into the receive path unless signal from the far-end exceeds the receive channel noise power by RSThd, in which case speech is assumed to be detected and the suppression is defeated until speech is no longer detected. Decreasing RSThd to make the speech detector more sensitive could result in false detections due to spurious noise events which may cause an unpleasant noise modulation at the near-end. Increasing RSThd makes it robust to spurious noise, but may suppress weak far-end talkers. RSThd does not affect the ability of the receive suppressor to attenuate residual network echo.

3.5.3 NSERMP - NOISE ESTIMATOR RAMP RATE

The background noise power estimators increase at a programmable rate until the background noise power estimate equals the current input power estimate. The background noise power estimators quickly track drops in the current input power estimate. Choose large values of NseRmp if the environment is expected to have rapidly varying noise levels. Choose small values of NseRmp if the environment is expected to have relatively constant noise power.

3.5.4 HDLY - HALF-DUPLEX HOLDOVER DELAY

After a channel goes idle in the half-duplex mode of operation, a change of channel ownership is inhibited for HDly in order to prevent false switching due to echoes. The half-duplexor will be more immune to false switching if this delay is longer, but it will also prevent a fast response to legitimate channel changes. Short values of HDly mimic a more full-duplex like behavior, but may be susceptible to false switching due to echo.

3.5.5 HHOLD - HOLD IN HALF-DUPLEX ON HOWL

This is a control flag which, if enabled, holds the system in half-duplex when a howl event is detected. The system may transition to full-duplex if the flag is subsequently cleared. The default state of HHold is ‘disabled’, thus when a howl is detected, the CS6422 will temporarily drop into half-duplex, retrain, and transition back into full-duplex on its own.

3.5.6 TDSRMP - TX DOUBLE-TALK SUPPRESSION RAMP RATE

When “Tx Double-talk Suppression attenuation” (TDbtS, Register 3) is set to a non-zero value, the CS6422 will introduce a programmable amount of attenuation into the transmit path during a double-talk event, that is, when the near-end talker and far-end talker are speaking simultaneously. TDSRmp controls the decay rate of the transmit double-talk attenuation (the attack rate is ~40 ms).

The ‘slow’ setting of TDSRmp results in an attenuation decay rate of about 1 second. The ‘normal’ setting of TDSRmp results in an attenuation decay rate of about 100 ms.

3.5.7 RDSRMP - RX DOUBLE-TALK SUPPRESSION RAMP RATE

When “Rx Double-talk Suppression attenuation” (RDbtS, Register 3) is set to a non-zero value, the CS6422 will introduce a programmable amount of attenuation into the receive path during a double-talk event. RDSRmp controls the decay rate of the receive double-talk attenuation (the attack rate is ~40 ms).

The ‘slow’ setting of RDSRmp results in an attenuation decay rate of about 1 second. The ‘normal’ setting of RDSRmp results in an attenuation decay rate of about 100 ms.

3.5.8 IDLTX - HALF-DUPLEX IDLE RETURN-TO-TRANSMIT

When IdlTx is enabled, the CS6422’s half-duplex engine will automatically switch into <Transmit> mode from the <Idle> state. The <Idle> state is entered when the previously active channel has been silent for the time period set by HDly (half-duplex Holdover Delay) in Register 2.

The use of IdlTx permits a full-duplex-like behavior when operating in half-duplex at the beginning of a call. This benefit is most noticeable when the listener at the far end is using a handset.

When TSMde is set to ‘0’ (Noise Guard enabled), IdlTx is usually disabled. IdlTx is disabled by default.

3.6 Register 3

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
TSAtt		PCSen	TDbtS			RDbtS		TSThd		TSBias		0	1	1	0
00		0	000			00		00		00					
0			0					0				6			

Bits	Name	Function	Word	Operation
15-14	TSAtt	Tx Suppression Attenuation	00* 01 10 11	18 dB 12 dB 24 dB reserved
13	PCSen	Path Change Sensitivity	0* 1	high sensitivity low sensitivity
12-10	TDbtS	Tx Double-talk Suppression attenuation	000* 001 010 ... 110 111	0 dB 3 dB 6 dB ... 18 dB 21 dB
9-8	RDbtS	Rx Double-talk Suppression attenuation	00* 01 10 11	0 dB 3 dB 6 dB 9 dB
7-6	TSThd	Tx Suppression Threshold	00* 01 10 11	15 dB 12 dB 9 dB 18 dB
5-4	TSBias	Tx Suppression Bias	00* 01 10 11	18 dB 15 dB 21 dB reserved

* Denotes reset value

Table 6. Register 3 Bit Definitions

3.6.1 TSATT - TRANSMIT SUPPRESSION ATTENUATION

This parameter sets the amount of attenuation inserted into the transmit path when transmit suppression is engaged.

3.6.2 PCSEN- PATH CHANGE SENSITIVITY

The Acoustic Interface is likely to have many path changes as people move about in the room where the full-duplex speakerphone is being used. The sensitivity of the path change detector can be changed with the PCSen bit. Set PCSen to '0' for high sensitivity and '1' for low sensitivity.

In any adaptive echo cancelling system, there is a trade-off between hearing echo and remaining in full-duplex when the acoustic path changes. When PCSen is set to '0' for high sensitivity, the CS6422 will tend to drop to half-duplex in the event of a path change, preventing the far-end listener from hearing echo as the adaptive filter adjusts to the new path.

When PCSen is set to '1' for low sensitivity, the CS6422 will tend to remain in full-duplex during the path change, and the far-end listener may hear some residual echo as the adaptive filter adjusts to the new path.

3.6.3 TDBTS - TX DOUBLE-TALK SUPPRESSION ATTENUATION

This parameter controls the amount of attenuation that is added to the transmit channel during double-talk, that is, when parties at both ends of the link are speaking simultaneously.

3.6.4 RDBTS - RX DOUBLE-TALK SUPPRESSION ATTENUATION

This parameter controls the amount of attenuation that is added to the receive path during double-talk.

3.6.5 TSTHD - TRANSMIT SUPPRESSION THRESHOLD

This parameter sets the ERLE requirement for discrimination between echo and near-end speech by the transmit suppressor. See Section 4.1.4.1, "Transmit Suppression" for full details.

3.6.6 TSBIAS - TRANSMIT SUPPRESSION BIAS

This bias level affects the ease with which near-end speech may break-in or be attenuated by far-end echo which causes the transmit suppressor to engage. See Section 4.1.4.1, "Transmit Suppression" for full details.

3.7 *Register 4*

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AErle		AFNse		NErle		NFNse		RGain		TGain		1	0	0	0
00		00		00		00		00		00					
0				0				0				8			

Bits	Name	Function	Word	Operation
15-14	AErle	AEC Erle threshold	00* 01 10 11	24 dB 18 dB 30 dB reserved
13-12	AFNse	AEC Full-duplex Noise threshold	00* 01 10 11	zero -42 dB -54 dB reserved
11-10	NErle	NEC Erle threshold	00* 01 10 11	24 dB 18 dB 30 dB reserved
9-8	NFNse	NEC Full-duplex Noise threshold	00* 01 10 11	zero -42 dB -54 dB reserved
7-6	RGain	Rx analog Gain	00* 01 10 11	0 dB 6 dB 9.5 dB 12 dB
5-4	TGain	Tx analog Gain	00* 01 10 11	0 dB 6 dB 9.5 dB 12 dB

* Denotes reset value

Table 7. Register 4 Bit Definitions

3.7.1 AERLE - AEC ERLE THRESHOLD

The CS6422 will allow full-duplex operation when the ERLE provided by the AEC exceeds the value programmed at AErle. See also AFNse. See Section 6., “Glossary” for a definition of ERLE.

3.7.2 AFNSE - AEC FULL-DUPLEX NOISE THRESHOLD

AFNse works in conjunction with AErle to determine when the CS6422 should transition into full-duplex operation. AFNse specifies a noise level. If the current noise level at the near-end input is greater than AFNse, then AErle is used to determine if full-duplex is allowed, that is, the AEC must provide at least AErle of cancellation in order for the CS6422 to transition to full-duplex.

If the noise level is below AFNse, the CS6422 uses an internal estimate of asymptotic performance to determine whether or not to transition to full-duplex. If AFNse is zero, AErle is used as the exclusive full-duplex criterion.

3.7.3 NERLE - NEC ERLE THRESHOLD

The CS6422 will allow full-duplex operation only when the ERLE provided by the NEC exceeds the threshold set by NErle. See also NFNse. See Section 6., “Glossary” for a definition of ERLE.

3.7.4 NFNSE - NEC FULL-DUPLEX NOISE THRESHOLD

NFNse works in conjunction with NErle to determine when the CS6422 should transition into full-duplex operation. If the noise level at the far-end input is greater than NFNse, then NErle is used to determine if full-duplex is allowed. If the noise level is below the level of NFNse, the CS6422 uses an internal estimate of asymptotic performance to determine whether or not to transition to full-duplex. If NFNse is zero, NErle is always used as the exclusive full-duplex criterion.

If NFNse is non-zero, then the CS6422 will automatically disable the NEC if a network coupling path is not detected. Thus in systems in which the presence of a network path is not known, NFNse should be set to a non-zero value. See also AuNECD.

3.7.5 RGAIN - RECEIVE ANALOG GAIN

RGain selects the amount of additional on-chip analog gain to be supplied to the network input of the CS6422. The output of this amplifier stage feeds the receive path ADC, and can supply 0 dB, 6 dB, 9.5 dB, or 12 dB of gain to the signal path. The gain setting defaults to 0 dB.

Note: Changing the analog gain will change the full-scale voltage as applied to the input pin. Make sure that the ADC input does not clip with the gain stage on.3.

3.7.6 TGAIN - TRANSMIT ANALOG GAIN