Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

CS7250B

Digital MEMS Microphone with High Performance and Low Power Modes

Features

- High acoustic overload point (AOP, 131 dB SPL)
- High signal-to-noise ratio (SNR, 66 dB)
- Low variation in sensitivity (±1 dB)
- Low current consumption
  - 650 µA (High Performance Mode)
  - 160 µA (Low Power Mode)
  - 5 µA (Standby Mode)
- PDM digital audio output
- Bottom-port LGA package
- 1.8-V supply

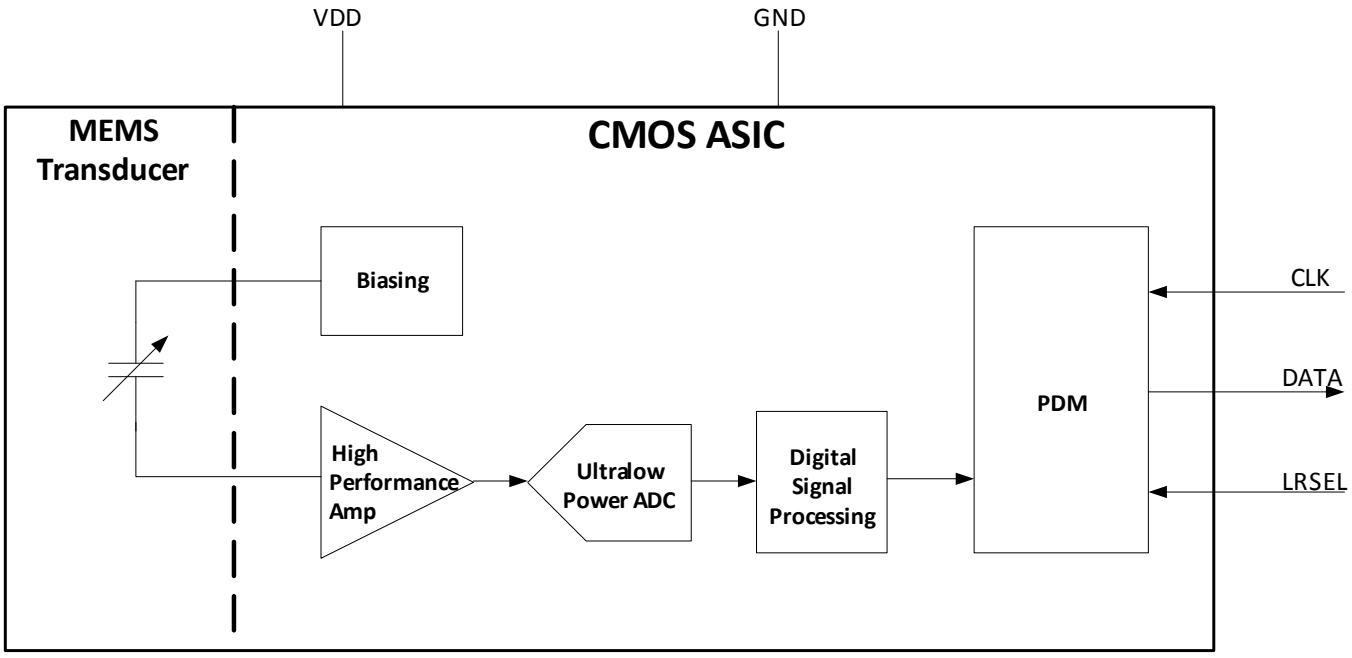
Description

The CS7250B is a high-performance digital MEMS microphone, offering class-leading total harmonic distortion (THD) performance, excellent SNR, and low power consumption.

The CS7250B supports two operational modes, selected according to the applied clock frequency. Low Power Mode is ideal for always-on voice activity detection; High Performance Mode is optimized for high fidelity recording.

The CS7250B incorporates a high-performance ADC, which outputs a single-bit data stream using pulse density modulation (PDM) encoding. The CS7250B supports selectable left/right channel assignment for a two-channel digital microphone interface, enabling efficient connection of multiple microphones in stereo/array configurations.

The CS7250B is available in a 3.50 x 2.65 x 0.98-mm bottom-port LGA package, with port diameter of 0.325 mm. It is ideal for portable applications such as smartphones, tablets, wearables and portable speech-recognition devices.



Preliminary Product Information

This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

Table of Contents

1 Pin Descriptions

1.1 LGA Pinout

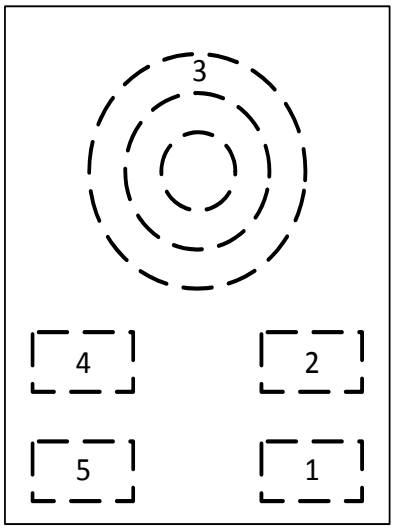


Figure 1-1. Top-Down (Through-Package) View

1.2 Pin Descriptions

A description of each pin on the CS7250B is provided in Table 1-1.

Table 1-1. Pin Descriptions

Name	Pin #	I/O	Description
DATA	1	O	PDM data output
LRSEL	2	I	Channel select 0 = Data output following falling CLK edge 1 = Data output following rising CLK edge This pin must be tied to VDD or GND—there is no internal pull-up/-down provided.
GND	3		Ground
CLK	4	I	Clock input
VDD	5		Power supply

2 Typical Connection Diagram

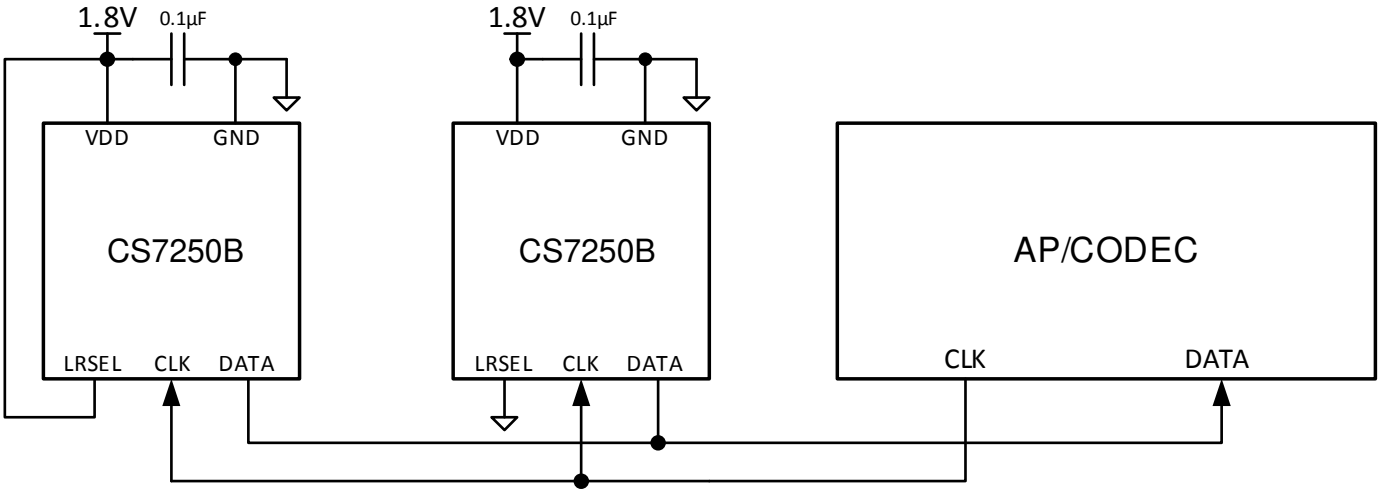


Figure 2-1. Typical Connection Diagram

Stereo connection of two CS7250B digital microphones is shown in Fig. 2-1.

It is recommended to connect a 0.1-µF decoupling capacitor between the VDD and GND pins of the CS7250B. A ceramic 0.1-µF capacitor with X7R dielectric or better is suitable. The capacitor should be placed as close to the CS7250B as possible.

3 Characteristics and Specifications

Table 3-1. Parameter Definitions

Parameter	Definition
Sensitivity	A measure of the microphone output response to the acoustic pressure of a 1-kHz, 94 dB SPL (1 Pa RMS) sine wave. This is referenced to the output Full Scale Range (FSR) of the microphone.
Full Scale Range (FSR)	Sensitivity, electrical noise floor and power supply rejection are measured with reference to the output full scale range (FSR) of the microphone. FSR is defined as the amplitude of a 1-kHz sine-wave output whose positive peak value reaches 100% density of logic 1s and whose negative peak value reaches 0% density of logic 1s. This is the largest 1-kHz sine wave that fits in the digital output range without clipping. Note that, because the definition of FSR is based on a sine wave, it is possible to support a square wave test signal output whose level is +3 dBFS.
Total harmonic distortion (THD)	The ratio of the RMS sum of the harmonic distortion products in the specified bandwidth (see note) relative to the RMS amplitude of the fundamental (i.e., test frequency) output.
Signal-to-noise ratio (SNR)	A measure of the difference in level between the output response of a 1-kHz, 94 dB SPL sine wave and the idle noise output.
Dynamic Range (DR)	The ratio of the 10% THD microphone output level (in response to a sine wave input) and the idle noise output.

Note: Unless otherwise specified, all performance measurements are specified with a low-pass brick-wall filter and, where noted, an A-weighted filter. The low-pass filter removes out-of-band noise.

Table 3-2. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage	VDD	1.62	1.8	1.98	V
Ground	GND	—	0	—	V
Clock frequency	F_{CLK}	0.3	—	3.2	MHz
Operating temperature range	T_A	–40	—	+85	ºC

Table 3-3. Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under electrical characteristics at the test conditions specified.

Parameter	Symbol	Min	Max	Units
Supply voltage [1]	VDD	–0.3	2.4	V
Input voltage [1]	V_{IN}	–0.3	2.3 [2]	V
Input current [3]	I_{IN}	–10	+10	mA
Operating temperature range	T_A	–40	+105	ºC
Storage temperature prior to soldering	T_{Stgp}	—	30	ºC
Storage relative humidity prior to soldering	RH_{Stgp}	—	60	%
Storage temperature after soldering	T_{Stg}	–40	+105	ºC

ESD-sensitive device. The CS7250B is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device. This device is qualified to current JEDEC ESD standards

1. All voltages are measured with respect to GND.
2. If VDD is above the minimum recommended operating level (see Table 3-2), the maximum input voltage is VDD + 0.3 V.
3. Input current is positive when flowing into the device.

Table 3-4. Acoustic and Electrical Characteristics

Test conditions (unless specified otherwise):
VDD = 1.8 V, GND = 0 V, CLK = 3.072 MHz, T_A = +25ºC, 55 ±15% RH, 1-kHz, 94 dB SPL test signal, no load on DATA pin.

Parameter [1]			Min	Typ	Max	Units
General characteristics	Directivity			Omnidirectional		—
	Polarity	Positive sound pressure		Increasing density of 1s		—
	Sensitivity [2]		–37	–36	–35	dBFS
High Performance Mode (CLK = 3.072 MHz)	Acoustic overload	THD < 10%	—	131	—	dB SPL
	THD	94 dB SPL 125 dB SPL	— —	0.2 1	— —	% %
	SNR	A-weighted	—	66	—	dB
	DR	A-weighted	—	103	—	dB
	Acoustic noise floor	A-weighted	—	28	—	dB SPL
	Electrical noise floor	A-weighted	—	–102	—	dBFS
	PSR (with respect to VDD)	100 mV p-p, swept sine wave, 20 Hz–20 kHz, A-weighted	—	–90	—	dBFS
Low Power Mode (CLK = 768 kHz)	Acoustic overload	THD < 10%	—	120	—	dB SPL
	THD	117 dB SPL	—	1	—	%
	SNR	20 Hz–8 kHz, A-weighted	—	62	—	dB
	DR	20 Hz–8 kHz, A-weighted	—	88	—	dB
	Acoustic noise floor	20 Hz–8 kHz, A-weighted	—	32	—	dB SPL
	Electrical noise floor	20 Hz–8 kHz, A-weighted	—	–98	—	dBFS
	PSR (with respect to VDD)	100 mV p-p, swept sine wave, 20 Hz–8 kHz, A-weighted	—	–90	—	dBFS
Frequency response	Frequency response	–3 dB low frequency +3 dB high frequency	— —	35 13	— —	Hz kHz
	Frequency response flatness	200 Hz–8 kHz	–1	—	+1	dB
Digital I/O [3]	Input HIGH Level		0.65 × VDD	—	—	V
	Input LOW Level		—	—	0.35 × VDD	V
	Output HIGH Level	I_{OH} = 1 mA	0.9 × VDD	—	—	V
	Output LOW Level	I_{OL} = –1 mA	—	—	0.1 × VDD	V
	Input capacitance		—	3	5	pF
	Input leakage		–1	—	1	µA
	Load capacitance (DATA)		—	—	200	pF
Miscellaneous characteristics	Current consumption [4]	High Performance Mode, CLK = 3.072 MHz Low Power Mode, CLK = 768 kHz Standby Mode, CLK = 0 Hz	— — —	650 160 5	— — 10	µA µA µA
	Startup time	From power applied to output within 0.5 dB of sensitivity specification	—	15	—	ms
	Mode-transition time	From Low Power Mode to High Performance Mode	—	10	—	ms
	CLK frequency range [5,6]	High Performance Mode Low Power Mode Standby Mode	1.4 300 —	— — 0	3.2 800 —	MHz kHz Hz

1. Performance measurements are specified with a low-pass brick-wall filter and, where noted, an A-weighted filter. The low-pass filter removes out-of-band noise. The Low Power Mode is measured with a cut-off frequency of 8 kHz; all other measurements are with a 20 kHz cut-off frequency.
2. Sensitivity is measured at production test 0.9 s after power up.
3. Note that digital input pins should not be left unconnected or floating.
4. Measured without a load on the DATA pin.
5. High Performance and Low Power Modes are selected according to the CLK frequency.
6. Standby Mode is selected when the CLK input is stopped; this is a power-saving mode. Normal operation resumes automatically when the CLK input frequency is within the specified operational limits. Note that the VDD supply is still required in Standby Mode.

Table 3-5. Audio Interface Timing

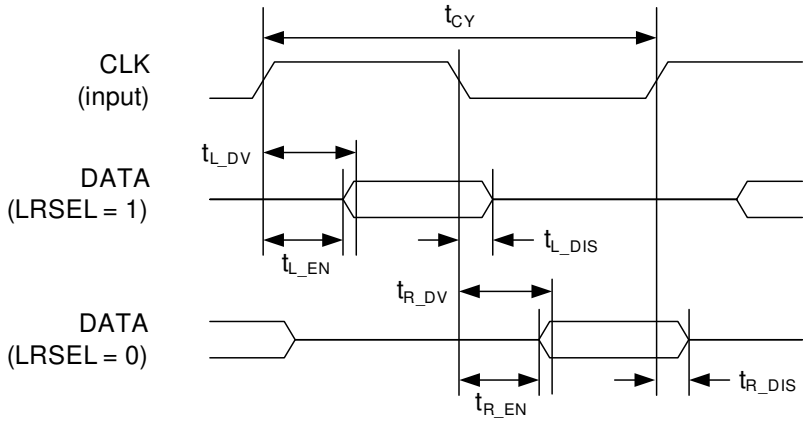
The following timing information is valid across the full range of recommended operating conditions.

Parameter [1]		Symbol	Min	Typ	Max	Units
CLK cycle time		t_{CY}	313	—	3333	ns
CLK duty cycle		—	60:40	—	40:60	—
CLK rise/fall time		—	—	—	6	ns
DATA enable time	From rising CLK edge, LRSEL = 0	t_{R_EN}	14	—	—	ns
	From falling CLK edge, LRSEL = 1	t_{L_EN}	14	—	—	ns
DATA valid time	From rising CLK edge, LRSEL = 0	t_{R_DV}	20	—	90	ns
	From falling CLK edge, LRSEL = 1	t_{L_DV}	20	—	90	ns
DATA disable time	From falling CLK edge, LRSEL = 0	t_{R_DIS}	—	—	10	ns
	From rising CLK edge, LRSEL = 1	t_{L_DIS}	—	—	10	ns

Notes:

- The DATA output is high-impedance when not outputting data; this enables the outputs of two microphones to be connected together with the data from one microphone interleaved with the data from the other. (The microphones must be configured to transmit on opposite channels in this case.)
- In a typical configuration, the left channel is transmitted following the rising CLK edge (LRSEL = 1). In this case, the left channel should be sampled by the receiving device on the falling CLK edge.
- Similarly, the right channel is typically transmitted following the falling CLK edge (LRSEL = 0). In this case, the right channel should be sampled by the receiving device on the rising CLK edge.
- The CS7250B operating mode is selected according to the CLK frequency; see Table 3-4 for further details.

1. Digital microphone interface timing.



DATA is high-impedance (Hi-Z) when not outputting data

4 Typical Performance

4.1 Audio Frequency Response

Test conditions: VDD = 1.8 V, GND = 0 V, CLK = 3.072 MHz, no load on DATA pin.

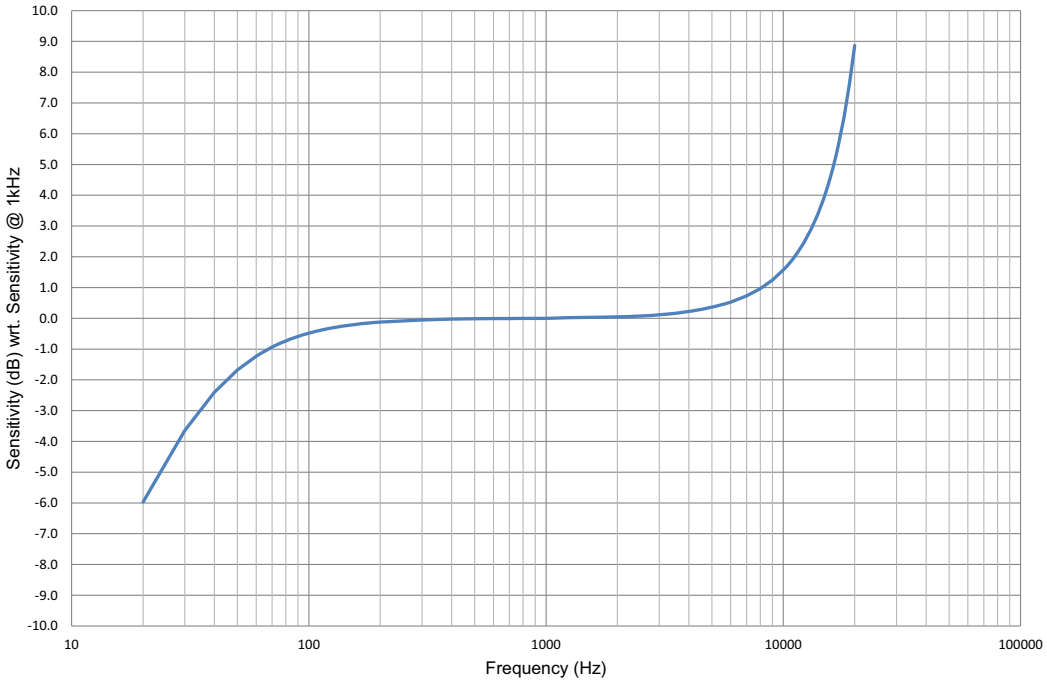


Figure 4-1. Sensitivity vs. Audio Frequency (20 Hz–20 kHz)

4.2 THD Performance

Test conditions: VDD = 1.8 V, GND = 0 V, CLK = 3.072 MHz, no load on DATA pin.

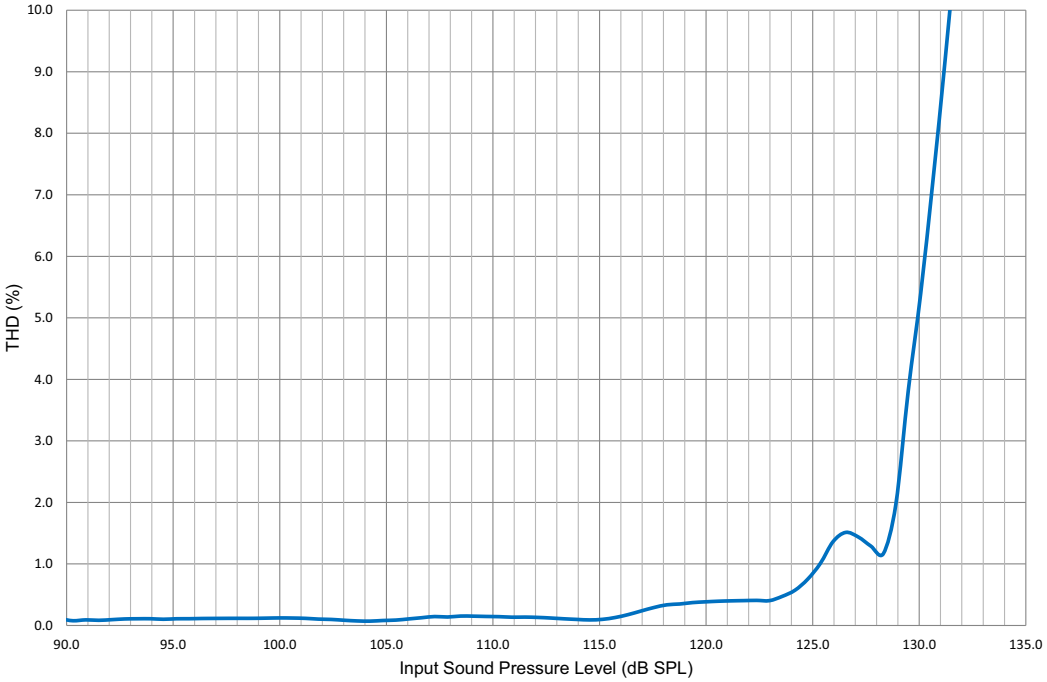


Figure 4-2. THD (%) vs. Input Sound Pressure Level (dB SPL)

5 Applications Information

Cirrus Logic provides a range of audio codecs incorporating a digital microphone input interface; these support direct connection to digital microphones such as the CS7250B.

Further information on Cirrus Logic audio codecs is provided in the respective product data sheet, which is available from the Cirrus Logic website

5.1 Important Assembly Guidelines

- Do not put a vacuum over the port hole of the microphone. Placing a vacuum over the port hole can damage the device.
- Do not board wash the microphone after a reflow process. Board washing and the associated cleaning agents can damage the device.
- Do not expose to ultrasonic cleaning methods.
- Do not use a vapor phase reflow process. The vapor can damage the device.
- Please refer to application note WAN0273 *MEMS Mic Assembly and Handling Guidelines* for further assembly and handling guidelines.

5.2 PCB Land Pattern and Paste Stencil

The recommended PCB land pattern and paste stencil pattern for the CS7250B microphone are shown in Fig. 5-1 and Fig. 5-2 respectively.

See also application note WAN0284 *General Design Considerations for MEMS Microphones* for further details of PCB footprint design. Full definition of the package dimensions is provided in Section 6.

The recommended PCB land pattern is shown in Fig. 5-1.

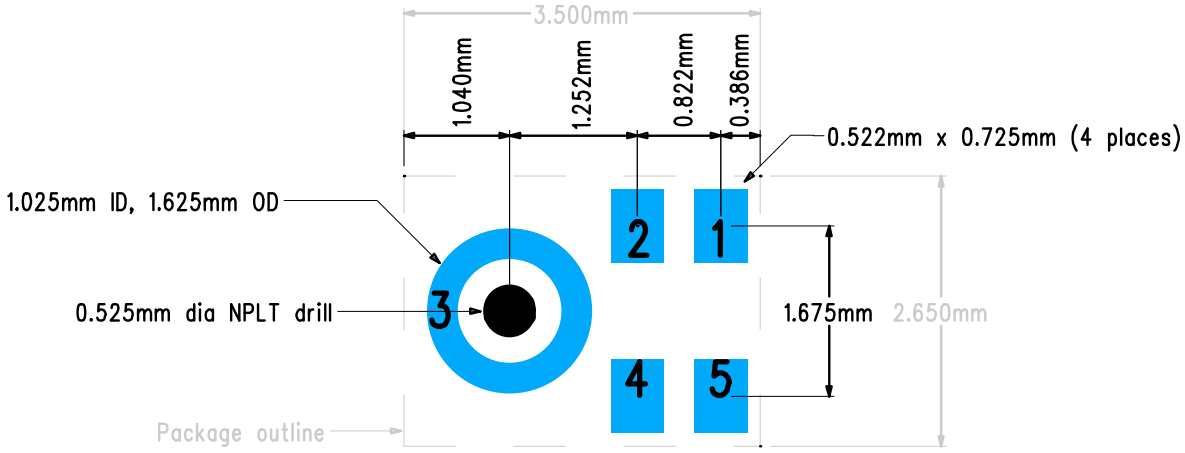


Figure 5-1. PCB Land Pattern, Top View

The recommended PCB paste stencil pattern is shown in Fig. 5-2.

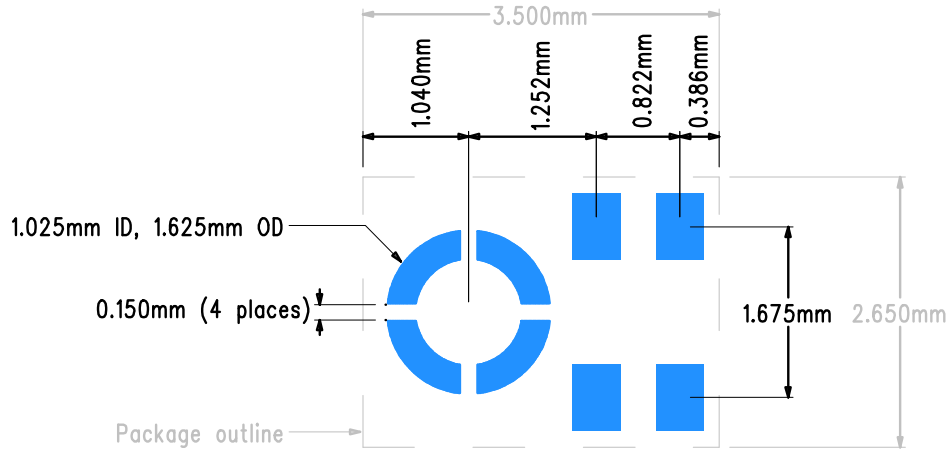
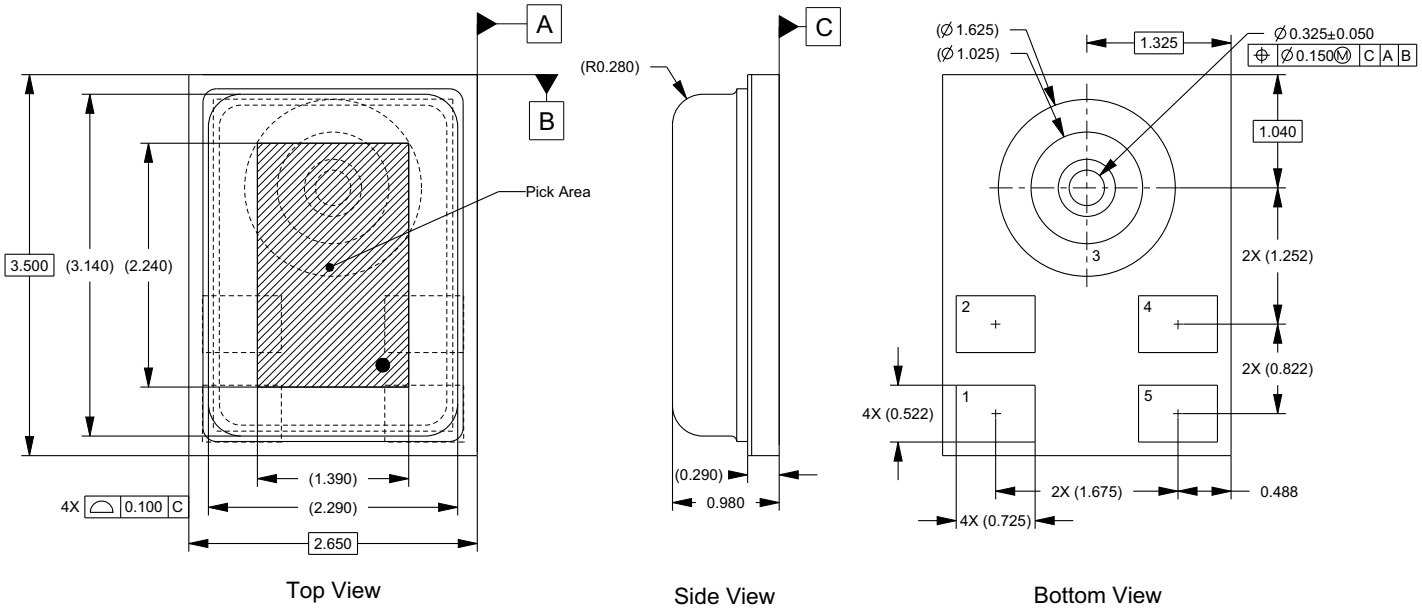


Figure 5-2. PCB Paste Stencil, Top View

6 Package Dimension



Top View Side View Bottom View

Unless otherwise specified, dimensions are in millimeters and tolerance is ±0.100

7 Ordering Information

Table 7-1. Ordering Information

Product	Description	Package	Halogen Free	Pb Free	Grade	Temperature Range	Container	Order #
CS7250B	Digital MEMS Microphone with High Performance and Low Power Modes	LGA	Yes	Yes	Commercial	–40 to +85°C	Tape and Reel [1]	CS7250B–CAZR

1. Reel quantity = 5000

8 References

- WAN0273 *MEMS Mic Assembly and Handling Guidelines*
- WAN0284 *General Design Considerations for MEMS Microphones*

9 Revision History

Table 9-1. Revision History

Revision	Changes
PP1 MAY '17	• Clarification of sensitivity specification added (Table 3-4). • THD and frequency-response specifications updated (Table 3-4). • Frequency response plot updated (Section 4.2). • Order quantity updated (Section 7).

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.