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CS8140, CS8141

5.0 V, 500 mA Linear Regulator with ENABLE, $\overline{\text{RESET}}$, and Watchdog

The CS8140 and CS8141 are linear regulators suited for microprocessor applications in automotive environments.

These ON Semiconductor parts provide the power for the microprocessors along with many of the control functions needed in today's computer based systems. Incorporating all of these features saves both cost, and board space.

Packages are available for surface mounting as well as through hole mounting.

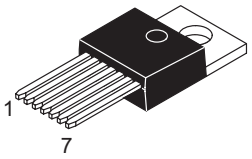
The CS8141 has the same feature set as the CS8140 with the exception of the response to the watchdog signals (WDI). The CS8141 only responds to input signals (WDI) which are below the preset watchdog frequency threshold.

Features

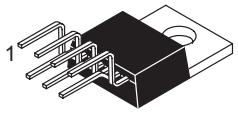
- 5.0 V ±4.0%, 500 mA Output Voltage
- μP Compatible Control Functions
  - Watchdog
  - $\overline{\text{RESET}}$
  - ENABLE
- Low Dropout Voltage (1.25 V @ 500 mA)
- Low Quiescent Current (7.0 mA @ 500 mA)
- Low Noise, Low Drift
- Low Current SLEEP Mode (I_Q = 250 μA)
- Fault Protection
  - Thermal Shutdown
  - Short Circuit
  - 60 V Peak Transient Voltage

ON Semiconductor®

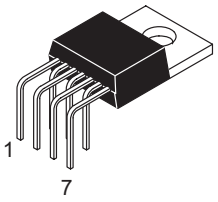
http://onsemi.com



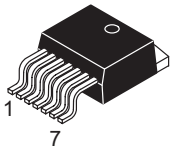
TO−220−7
T SUFFIX
CASE 821E



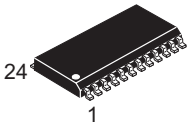
TO−220−7
TVA SUFFIX
CASE 821J



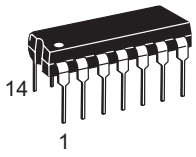
TO−220−7
THA SUFFIX
CASE 821H



D²PAK−7
DPS SUFFIX
CASE 936AB



SO−24L
DW SUFFIX
CASE 751E



DIP−14
N SUFFIX
CASE 646

ORDERING INFORMATION

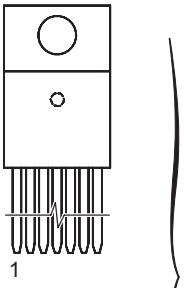
See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 14 of this data sheet.

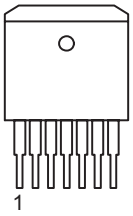
PIN CONNECTIONS

TO−220−7

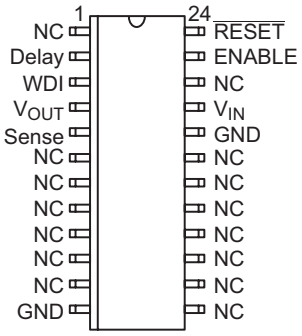


Tab = GND
Pin 1. V_{IN}
2. ENABLE
3. $\overline{RESET}$
4. GND
5. Delay
6. WDI
7. V_{OUT}

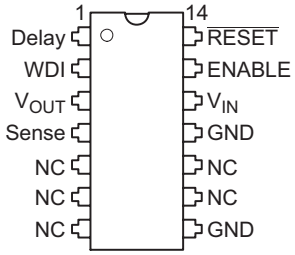
D^2PAK−7



SO−24L



DIP−14



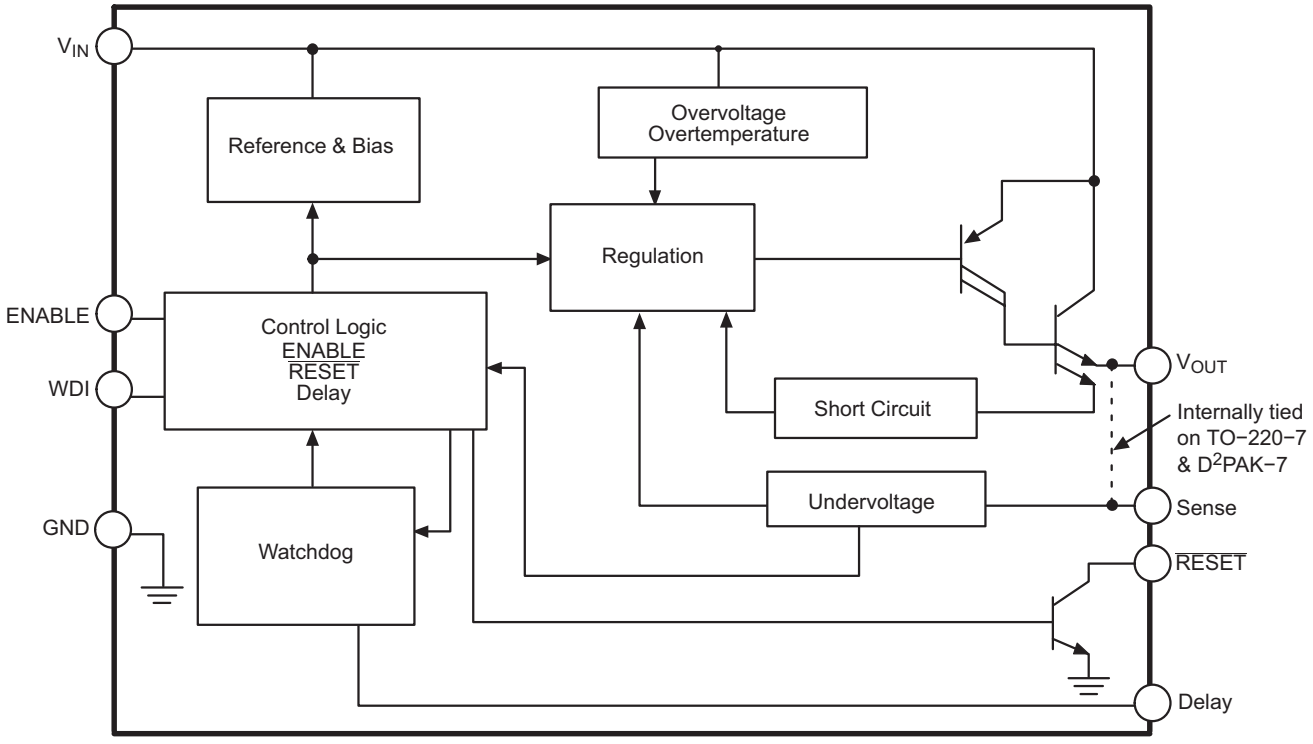


Figure 1. Block Diagram

MAXIMUM RATINGS*

Rating	Value	Unit
Input Operating Range	−0.5 to 26	V
Peak Transient Voltage (46 V Load Dump @ 14 V V_{BAT})	60	V
Electrostatic Discharge (Human Body Model)	4.0	kV
WDI Input Signal Range	−0.3 to 7.0	V
Internal Power Dissipation	Internally Limited	−
Junction Temperature Range (T_J)	−40 to +150	°C
Storage Temperature Range	−65 to +150	°C
ENABLE	−0.3 to V_{IN}	V
Package Thermal Resistance, TO−220−7 Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$	 1.6 50	 °C/W °C/W
Package Thermal Resistance, D^2PAK−7 Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$	 1.5 10−50†	 °C/W °C/W
Package Thermal Resistance, SO−24L Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$	 16 80	 °C/W °C/W
Package Thermal Resistance, DIP−14 Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$	 48 85	 °C/W °C/W
Lead Temperature Soldering: Wave Solder (through hole styles only) (Note 1) Reflow (SMD styles only) (Note 2)	260 peak 230 peak	°C

*The maximum package power dissipation must be observed.
†Depending on thermal properties of substrate $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$.
1. 10 second maximum.
2. 60 seconds max above 183°C.

ELECTRICAL CHARACTERISTICS ($7.0 \le V_{IN} \le 26$ V, $5.0\ mA \le I_{OUT} \le 500\ mA$, $-40°C \le T_J \le 150°C$, $-40°C \le T_A \le 125°C$, unless otherwise noted.) Note 3.

Characteristic	Test Conditions	Min	Typ	Max	Unit
Output Stage (V_{OUT})					
Output Voltage, V_{OUT}	$7.0\ V \le V_{IN} \le 26$ V, $5.0\ mA < I_{OUT} < 500\ mA$	4.8	5.0	5.2	V
Dropout Voltage ($V_{IN} - V_{OUT}$)	$I_{OUT} = 500\ mA$	−	1.25	1.50	V
Line Regulation	$I_{OUT} = 50\ mA$, $7.0\ V \le V_{IN} \le 26$ V,	−	5.0	25	mV
Load Regulation	$V_{IN} = 14$ V, $50\ mA \le I_{OUT} \le 500\ mA$	−	5.0	80	mV
Output Impedance, R_{OUT}	500 mA DC and 10 mA AC, 100 Hz ≤ f ≤ 10 kHz	−	200	−	mΩ
Quiescent Current, (I_Q) Active Mode Sleep Mode	 $0 \le I_{OUT} \le 500\ mA$, $7.0\ V \le V_{IN} \le 26$ V $I_{OUT} = 0\ mA$, $V_{IN} = 13$ V, ENABLE = 0 V	 − −	 7.0 0.25	 15 0.50	 mA mA
Ripple Rejection	$7.0\ V \le V_{IN} \le 17$ V, $I_{OUT} = 250\ mA$, f = 120 Hz	60	75	−	dB
Current Limit	−	700	1200	2000	mA
Thermal Shutdown	−	150	180	−	°C
Overvoltage Shutdown	$V_{OUT} < 1.0$ V	30	34	38	V

3. To observe safe operating junction temperatures, low duty cycle pulse testing is used in tests where applicable.

ELECTRICAL CHARACTERISTICS (continued) ($7.0 \le V_{IN} \le 26$ V, 5.0 mA $\le I_{OUT} \le$ 500 mA, −40°C $\le T_J \le$ 150°C, −40°C $\le T_A \le$ 125°C, unless otherwise noted.) Note 4.

Characteristic	Test Conditions	Min	Typ	Max	Unit
ENABLE					
Threshold HIGH LOW	 $V_{OUT} \ge 0.5$ V, ($V_{OUT(ON)}$) $V_{OUT} < 0.5$ V, ($V_{OUT(OFF)}$)	 − 3.5	 4.05 3.95	 4.50 −	 V V
Threshold Hysteresis	(HIGH − LOW)	−	100	−	mV
$\overline{\text{RESET}}$					
Threshold HIGH $V_{R(HI)}$	V_{OUT} Increasing	4.65	4.90	V_{OUT} − 0.05	V
Threshold LOW $V_{R(LOW)}$	V_{OUT} Decreasing	4.50	4.70	4.90	V
Threshold Hysteresis (V_{RH})	(HIGH − LOW)	150	200	250	mV
RESET Output Leakage $\overline{\text{RESET}}$ = HIGH	$V_{OUT} \ge V_{R(HI)}$	−	−	25	μA
Output Voltage Low ($V_{L(LOW)}$)	1.0 V $\le V_{OUT} \le V_{R(LOW)}$, R_P = 2.7 kΩ, Note 5.	−	0.1	0.4	V
Output Voltage Low (V_{Rpeak})	V_{OUT}, Power up, Power down	−	0.6	1.0	V
Delay Times t_{POR}	C_{DELAY} = 0.1 μF	30	47.5	65	ms
Delay Times $t_{WDI(\overline{RESET})}$	C_{DELAY} = 0.1 μF	0.5	1.0	1.5	ms
Watchdog					
Input Voltage High	−	2.0	−	−	V
Input Voltage Low	−	−	−	0.8	V
Input Current	WDI $\le V_{OUT}$	−	0	10	μA
Threshold Frequency $f_{WDI(LOWER)}$	C_{DELAY} = 0.1 μF	64	77	96	Hz
Threshold Frequency $f_{WDI(UPPER)}$ (Note 6.)	C_{DELAY} = 0.1 μF	218	262	326	Hz

4. To observe safe operating junction temperatures, low duty cycle pulse testing is used in tests where applicable.
5. R_P is connected to $\overline{\text{RESET}}$ and V_{OUT}.
6. CS8140 only.

PACKAGE LEAD DESCRIPTION

PACKAGE LEAD #				LEAD SYMBOL	
TO−220−7	D²PAK−7	SO−24L	DIP−14	LEAD SYMBOL	FUNCTION
1	1	21	12	V_{IN}	Supply voltage to IC, usually direct from the battery.
2	2	23	13	ENABLE	CMOS compatible logical input. V_{OUT} is disabled when ENABLE is LOW and WDI is beyond its preset limits.
3	3	24	14	$\overline{\text{RESET}}$	CMOS compatible output lead. $\overline{\text{RESET}}$ goes low whenever V_{OUT} drops below 4.5% of it's typical value for more than 2.0 μs or WDI signal falls outside it's window limits.
4	4	12, 20	8, 11	GND	Ground Connection.
5	5	2	1	Delay	Timing capacitor for Watchdog and $\overline{\text{RESET}}$ functions.
6	6	3	2	WDI	CMOS compatible input lead. The Watchdog function monitors the falling edge of the incoming digital pulse train. The signal is usually generated by the system microprocessor.
7	7	4	3	V_{OUT}	Regulated output voltage, 5.0 V (Typ).
−	−	1, 6−11, 13−19, 22	5−7, 9, 10	NC	No connection.
−	−	5	4	Sense	Kelvin connection which allows remote sensing of output voltage for improved regulation.

TYPICAL PERFORMANCE CHARACTERISTICS

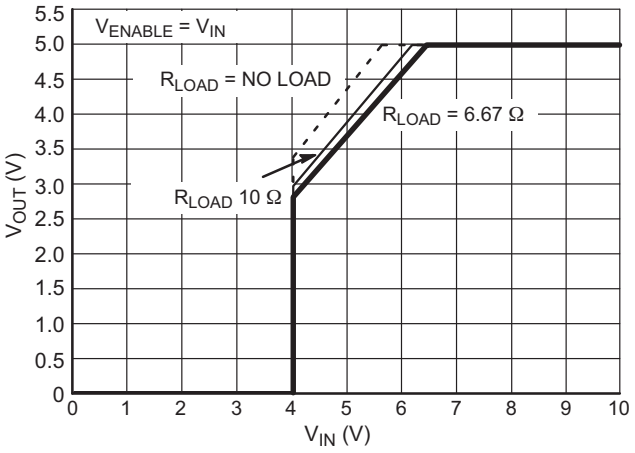


Figure 2. V_{OUT} vs. V_{IN} over R_{LOAD}; T = 25°C

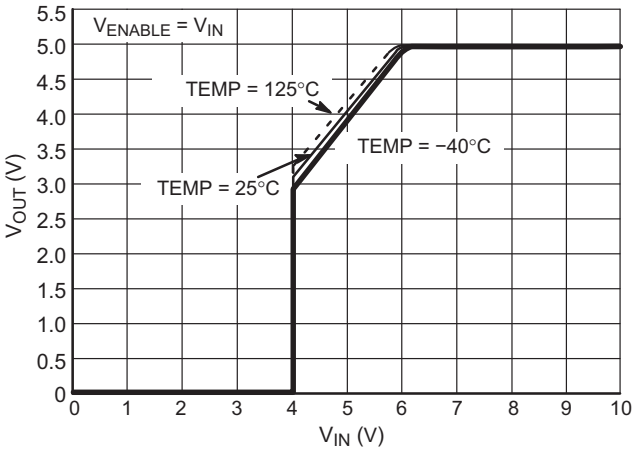


Figure 3. V_{OUT} vs. V_{IN} Over Temperature; R_{LOAD} = 25 Ω

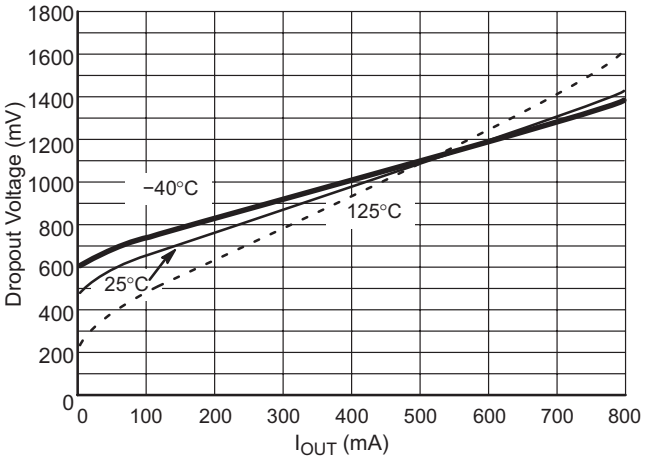


Figure 4. Dropout Voltage vs. Output Current Over Temperature

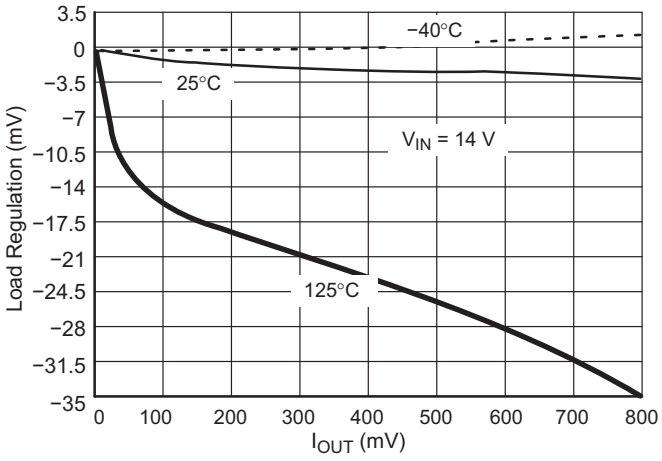


Figure 5. Load Regulation vs. Output Current Over Temperature

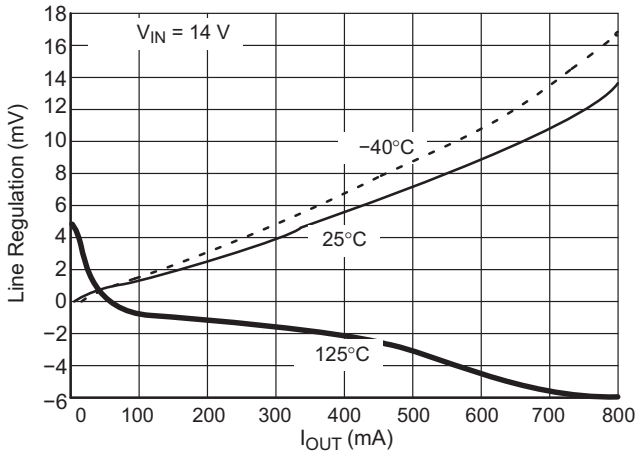


Figure 6. Line Regulation vs. Output Current Over Temperature

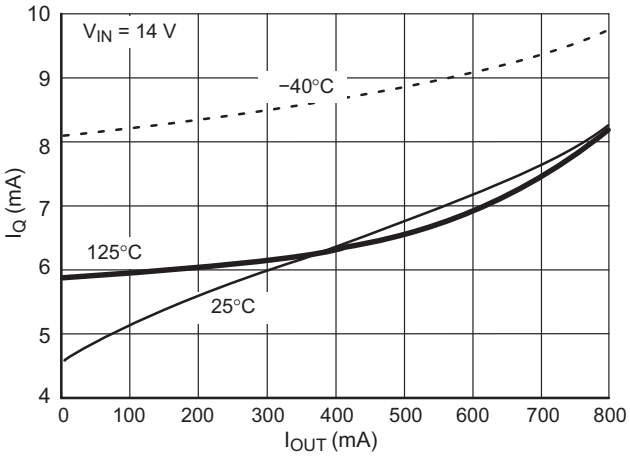


Figure 7. Quiescent Current vs. Output Current Over Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

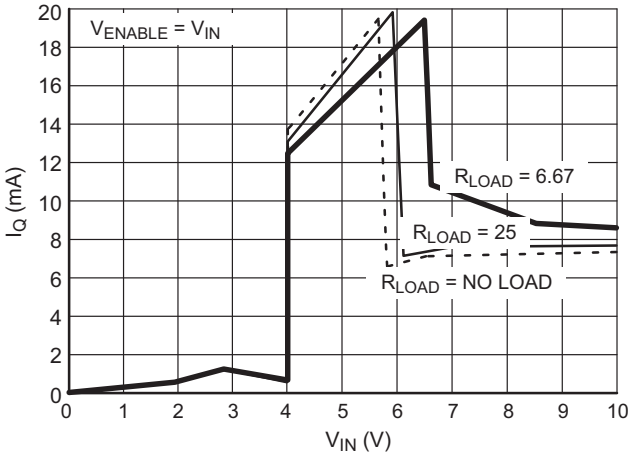


Figure 8. Quiescent Current vs. V_{IN} Over R_{LOAD}; T = 25°C

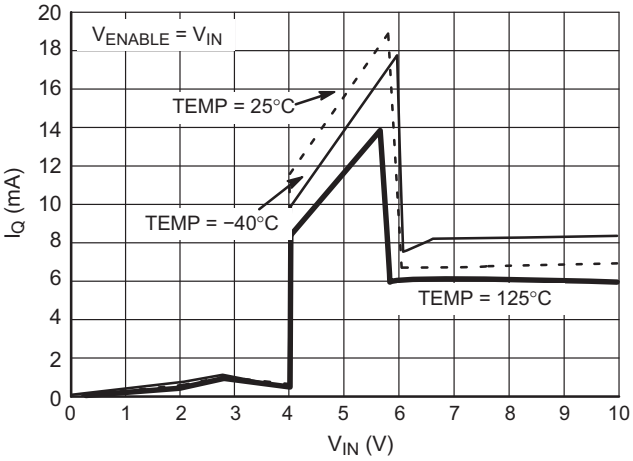


Figure 9. Quiescent Current vs. V_{IN} Over Temperature; R_{LOAD} = 25 Ω

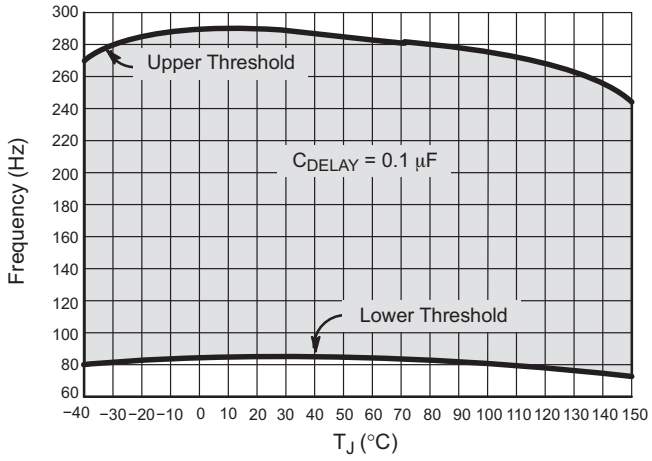


Figure 10. Watchdog Frequency Thresholds vs. Temperature

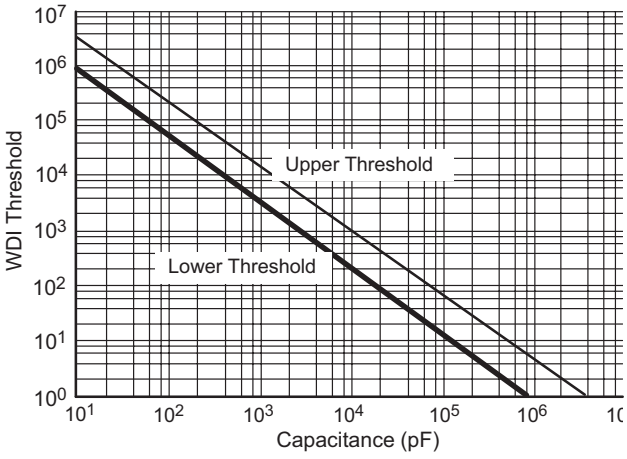


Figure 11. Watchdog Frequency Threshold vs. C_{DELAY}

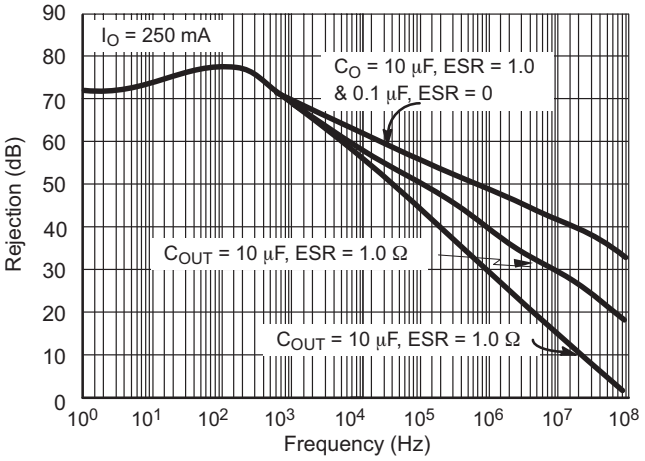


Figure 12. Ripple Rejection vs. Frequency

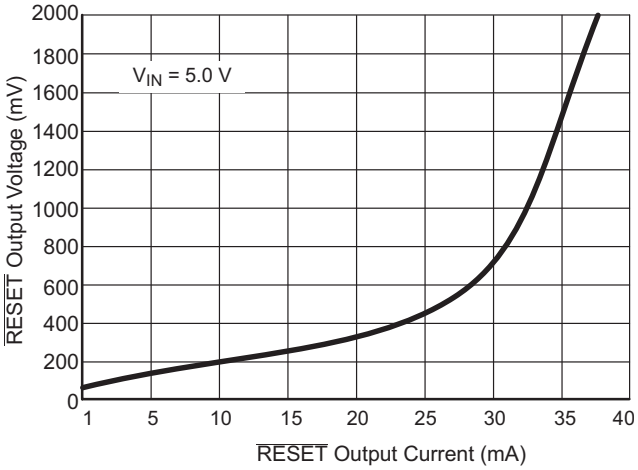


Figure 13. $\overline{RESET}$ Output Voltage vs. Output Current

DEFINITION OF TERMS

Dropout Voltage: The input−output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14 V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak−to−peak input ripple voltage to the peak−to−peak output ripple voltage.

Current Limit: Peak current that can be delivered to the output.

CIRCUIT DESCRIPTION

The CS8140 is a 5.0 V Watchdog Regulator with protection circuitry and three logic control functions that allow a microprocessor to control its own power supply. The CS8140 is designed for use in automotive, switch mode power supply post regulator, and battery powered systems.

Basic regulator performance characteristics include a low noise, low drift, 5.0 V ±4.0% precision output voltage with low dropout voltage (1.25 V @ I_{OUT} = 500 mA) and low quiescent current (7.0 mA @ I_{OUT} = 500 mA). On board short circuit, thermal, and overvoltage protection make it possible to use this regulator in particularly harsh operating environments.

The Watchdog logic function monitors an input signal (WDI) from the microprocessor or other signal source. When the signal frequency moves outside externally programmable window limits, a $\overline{\text{RESET}}$ signal is generated ($\overline{\text{RESET}}$). An external capacitor (C_{DELAY}) programs the watchdog window frequency limits as well as the power on reset (POR) and $\overline{\text{RESET}}$ delay.

The $\overline{\text{RESET}}$ function is activated by any of three conditions: the watchdog signal moves outside of its preset limits; the output voltage drops out of regulation by more than 4.5%; or the IC is in its power up sequence. The $\overline{\text{RESET}}$ signal is independent of V_{IN} and reliable down to V_{OUT} = 1.0 V.

In conjunction with the Watchdog, the ENABLE function controls the regulator's power consumption. The CS8140's output stage and its attendant circuitry are enabled by setting the ENABLE lead high. The regulator goes into sleep mode when the ENABLE lead goes low and the watchdog signal moves outside its preset window limits. This unique combination of control functions in the CS8140 gives the microprocessor control over its own power down sequence: i.e. it gives the microprocessor the flexibility to perform housekeeping functions before it powers down.

The CS8141 has the same features as the CS8140, except that the CS8141 only responds to input signals (WDI) which are below the preset watchdog frequency threshold.

VOLTAGE REFERENCE AND OUTPUT CIRCUITRY

Precision Voltage Reference

The regulated output voltage depends on the precision band gap voltage reference in the IC. By adding an error amplifier into the feedback loop, the output voltage is maintained within ±4.0% over temperature and supply variation.

Output Stage

The composite PNP−NPN output structure (Figure 14) provides 500 mA (min) of output current while maintaining a low drop out voltage (1.25 V) and drawing little quiescent current (7.0 mA).

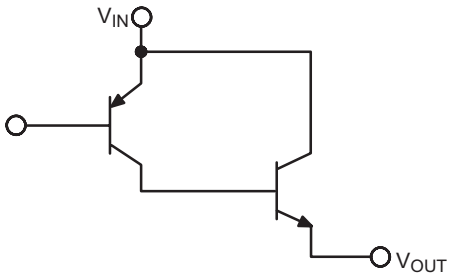


Figure 14. Composite Output Stage of the CS8140/1

The NPN pass device prevents deep saturation of the output stage which in turn improves the IC's efficiency by preventing excess current from being used and dissipated by the IC.

Output Stage Protection

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (Figure 15).

If the input voltage rises above 30 V (e.g. load dump), the output shuts down. This response protects the internal circuitry and enables the IC to survive unexpected voltage transients.

Using an emitter sense scheme, the amount of current through the NPN pass transistor is monitored. Feedback

circuitry insures that the output current never exceeds a preset limit.

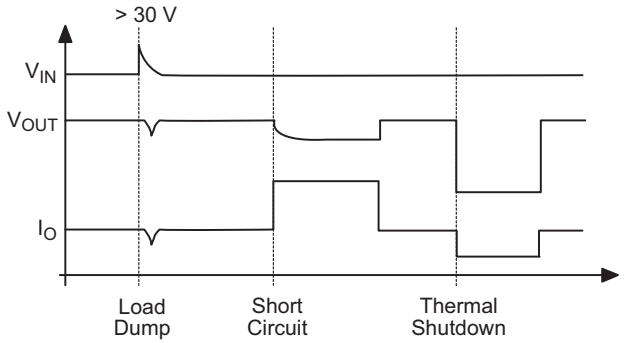


Figure 15. Typical Circuit Waveforms for Output Stage Protection

Should the junction temperature of the power device exceed 180°C (Typ), the power transistor is turned off. Thermal shutdown is an effective means to prevent die overheating since the power transistor is the principle heat source in the IC.

REGULATOR CONTROL FUNCTIONS

The CS8140 differs from all other linear regulators in its unique combination of control features.

Watchdog and ENABLE Function

V_{OUT} is controlled by the logic functions ENABLE and Watchdog (Table 1).

Table 1. V_{OUT} as a Function of ENABLE and Watchdog

V_{OUT} (V)					
	WDI				
ENABLE	Slow	Normal	Fast	High	Low
H	5	5	5	5	5
L	0	5	0	0	0

As long as ENABLE is high or ENABLE is low and the Watchdog signal is normal, V_{OUT} will be at 5.0 V (Typ). If ENABLE is low and the Watchdog signal moves outside programmable limits, the output transistor turns off and the IC goes into SLEEP mode. Only the ENABLE circuitry in the IC remains powered up, drawing a quiescent current of 250 μA.

The Watchdog monitors the frequency of an incoming WDI signal. If the signal falls outside of the WDI window, a frequency programmable pulse train is generated at the $\overline{\text{RESET}}$ lead (Figure 16) until the correct Watchdog input signal reappears at the lead (ENABLE = HIGH).

The lower and upper window threshold limits of the watchdog function are set by the value of C_{DELAY}. The limits are determined according to the following equations for the CS8140:

(a) $t_{WDI(LOWER)} = (1.3 \times 10^{5})C_{DELAY}$ or

$f_{WDI(LOWER)} = (7.69 \times 10^{-6})C_{DELAY}^{-1}$

(b) $t_{WDI(UPPER)} = (3.82 \times 10^{-4})C_{DELAY}$ or

$f_{WDI(UPPER)} = (2.62 \times 10^{-5})C_{DELAY}^{-1}$

For the CS8141 the lower limit is determined by the equations in (a) above.

The capacitor C_{DELAY} also determines the frequency of the $\overline{\text{RESET}}$ signal and the POWER−ON−$\overline{\text{RESET}}$ (POR) delay period.

$\overline{\text{RESET}}$ Function

The $\overline{\text{RESET}}$ function is activated when the Watchdog signal is outside of its preset window (Figure 16), when the regulator is in its power up state (Figure 17) or when V_{OUT} drops below V_{OUT} −4.5% for more than 2.0 μs (Figure 18)

If the Watchdog signal falls outside of the preset voltage and frequency window, a frequency programmable pulse train is generated at the $\overline{\text{RESET}}$ lead (Figure 16) until the correct Watchdog input signal reappears at the lead. The duration of the $\overline{\text{RESET}}$ pulse is determined by C_{DELAY} according to the following equation:

$$t_{WDI(\overline{RESET})} = (1.0 \times 10^{4})C_{DELAY}$$

$\overline{\text{RESET}}$ CIRCUIT WAVEFORMS WITH DELAYS INDICATED

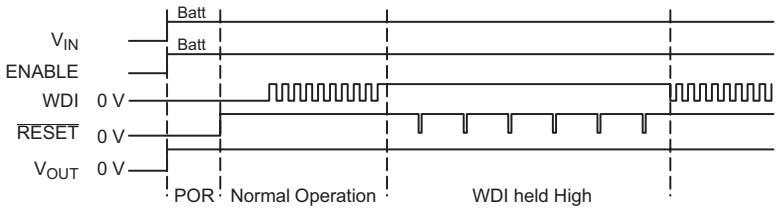
If an undervoltage condition exists, the voltage on the $\overline{\text{RESET}}$ lead goes low and the delay capacitor, C_{DELAY}, is discharged. $\overline{\text{RESET}}$ remains low until output is in regulation, the voltage on C_{DELAY} exceeds the upper switching threshold and the Watchdog input signal is within its set window limits (Figures 17 and 18). The delay after the output is in regulation is:

$$t_{POR(typ)} = (4.75 \times 10^{5})C_{DELAY}$$

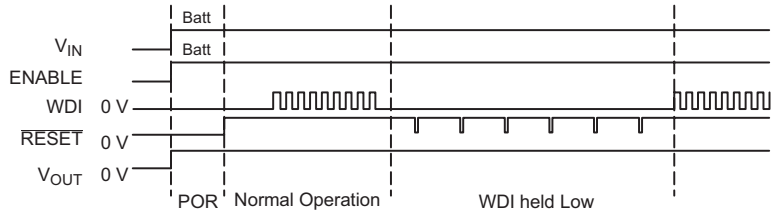
The $\overline{\text{RESET}}$ delay circuit is also programmed with the external cap C_{DELAY}.

The output of the reset circuit is an open collector NPN. $\overline{\text{RESET}}$ is operational down to V_{OUT} = 1.0 V. Both $\overline{\text{RESET}}$ and its delay are governed by comparators with hysteresis to avoid undesirable oscillations.

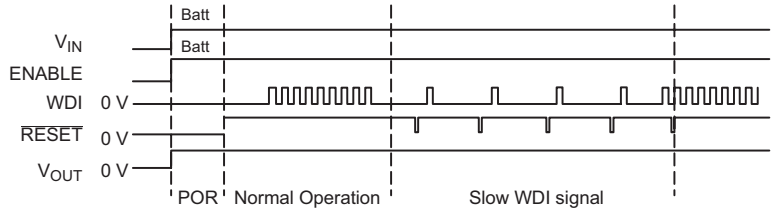
V_{OUT} When Watchdog is Held High and ENABLE = HIGH



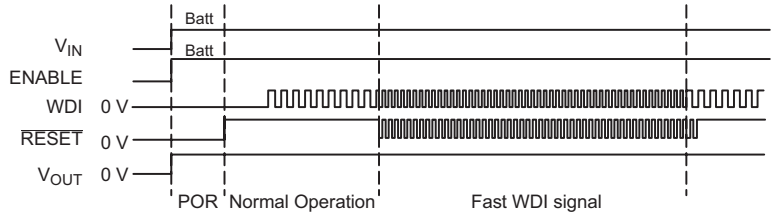
V_{OUT} When Watchdog is Held Low and ENABLE = HIGH



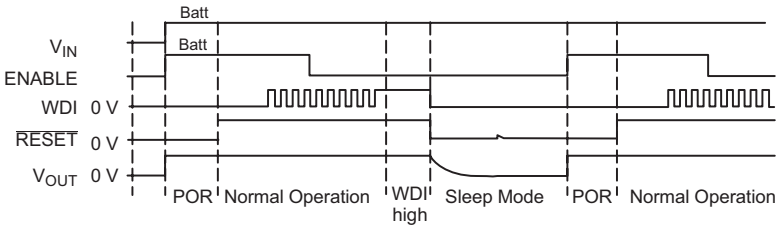
V_{OUT} When Watchdog is too Slow and ENABLE = HIGH



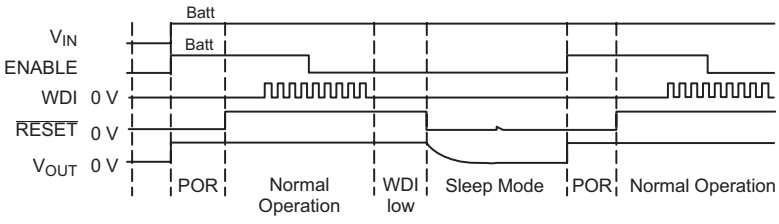
V_{OUT} When Watchdog is too Fast and ENABLE = HIGH



WDI Held High After a Normal Period of Operation; ENABLE = LOW



WDI Held Low or is too Slow after a Normal Period of Operation; ENABLE = LOW



WDI Frequency Rises Above the Upper Frequency Threshold After a Normal Period of Operation; ENABLE = LOW (for CS8140 only)

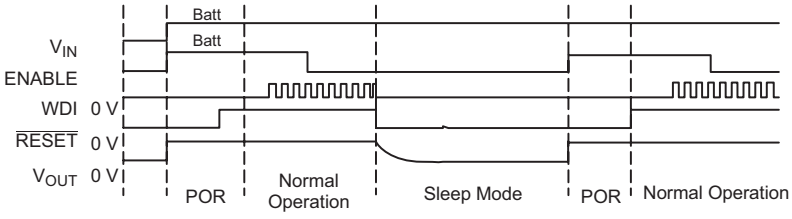


Figure 16. Timing Diagrams for Watchdog and ENABLE Functions

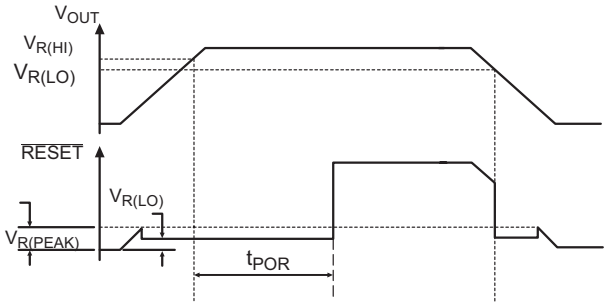


Figure 17. Power $\overline{\text{RESET}}$ and Power Down

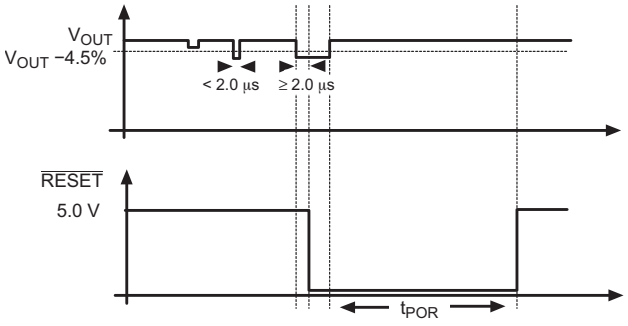


Figure 18. Undervoltage Triggered $\overline{\text{RESET}}$

APPLICATION NOTES

CS8140 DESIGN EXAMPLE

The CS8140 with its unique integration of linear regulator and control features: $\overline{\text{RESET}}$, ENABLE and WATCHDOG, provides a single IC solution for a microprocessor power supply. The reset delay, reset duration and watchdog frequency limits are all determined by a single capacitor. For a particular microprocessor the overriding requirement is usually the reset delay (also known as power on reset). The capacitor is chosen to meet this requirement and the reset duration and watchdog frequency follow.

The reset delay is given by:

$$t_{POR(typ)} = (4.75 \times 10^5)C_{DELAY}$$

Assume that the reset delay must be 200 ms minimum.

From the CS8140 data sheet the reset delay has a ±37% tolerance due to the regulator.

Assume the capacitor tolerance is ±10%.

$$t_{POR(min)} = (4.75 \times 10^5 \times 0.63) \times C_{DELAY} \times 0.9$$

$$C_{DELAY(min)} = \frac{t_{POR(min)}}{2.69 \times 10^5}$$

$$C_{DELAY(min)} = 0.743\ \mu F$$

Closest standard value is 0.82 μF.

Minimum and maximum delays using 0.82 μF are 220 ms and 586 ms.

The duration of the reset pulse is given by:

$$T_{WDI(\overline{RESET})(typ)} = (1.0 \times 10^4) \times C_{DELAY}$$

This has a tolerance of ±50% due to the IC, and ±10% due to the capacitor.

The duration of the reset pulse ranges from 3.69 ms to 13.5 ms.

The watchdog signal can be expressed as a frequency or time. From a programmers point of view, time is more useful since they must ensure that a watchdog signal is issued consistently several times per second.

The maximum and minimum watchdog times are given by:

$$t_{WDI(LOWER)} = (1.3 \times 10^5)C_{DELAY}$$

$$t_{WDI(UPPER)} = (3.82 \times 10^4)C_{DELAY}$$

There is a tolerance of ±20% due to the CS8140.

With a capacitor tolerance of ±10%:

$$t_{WDI(LOWER)} = (1.3 \times 10^5) \times 1.2 \times 1.1 \times C_{Delay}$$

$$t_{WDI(UPPER)} = (3.82 \times 10^4) \times 0.8 \times 0.9 \times C_{Delay}$$

$$t_{WDI(LOWER)} = 141\ \text{ms (max)}$$

$$t_{WDI(UPPER)} = 22.5\ \text{ms (max)}$$

$$t_{WDI(LOWER)} = (1.3 \times 10^5) \times 0.8 \times 0.9 \times C_{DELAY}$$

$$t_{WDI(UPPER)} = (3.82 \times 10^4) \times 1.2 \times 1.1 \times C_{DELAY}$$

$$t_{WDI(LOWER)} = 76\ \text{ms (min)}$$

$$t_{WDI(UPPER)} = 41\ \text{ms (min)}$$

The software must be written so that a watchdog signal arrives at least every 76 ms but not faster than every 41 ms (Figure 19).

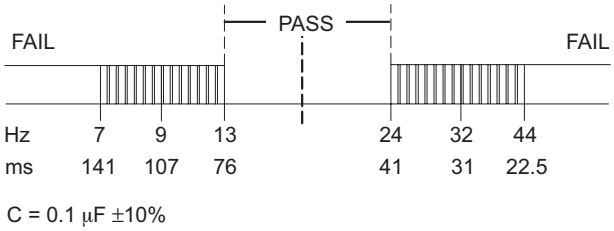


Figure 19. WDI Signal for C_{Delay} = 0.82 μF using CS8140

The CS8141 is identical to the CS8140 except that the CS8141 only has a lower watchdog frequency threshold.

The designer using this part need only be concerned with $t_{WDI(LOWER)}$ as shown in Figure 20.

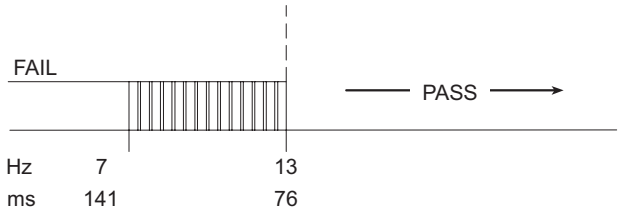


Figure 20. WDI Signal for C_{Delay} = 0.82 μF using CS8141

ENERGY CONSERVATION AND SMART FEATURES

Energy conservation is another benefit of using a regulator with integrated microprocessor control features. Using the CS8140 or CS8141 as indicated in Figure 21, the microprocessor can control its own power down sequence. The momentary contact switch quickly charges C1 through R1.

When the voltage across C1 reaches 3.95 V (the enable threshold), the output switches on and V_{OUT} rises to 5.0 V. After a delay period determined by C_{Delay}, a frequency programmable reset pulse train is generated at the reset output. The pulse train continues until the correct watchdog signal appears at the WDI lead. C1 is now left to discharge through the input impedance of the enable lead (approximately 150 kΩ) and the enable signal disappears. The output voltage remains at 5.0 V as long as the CS8140 continues to receive the correct watchdog signal.

The microprocessor can power itself down by terminating its watchdog signal. When the microprocessor finishes its housekeeping or power down software routine, it stops sending a watchdog signal. In response, the regulator generates a reset signal and goes into a sleep mode where V_{OUT} drops to 0 V, shutting down the microprocessor.

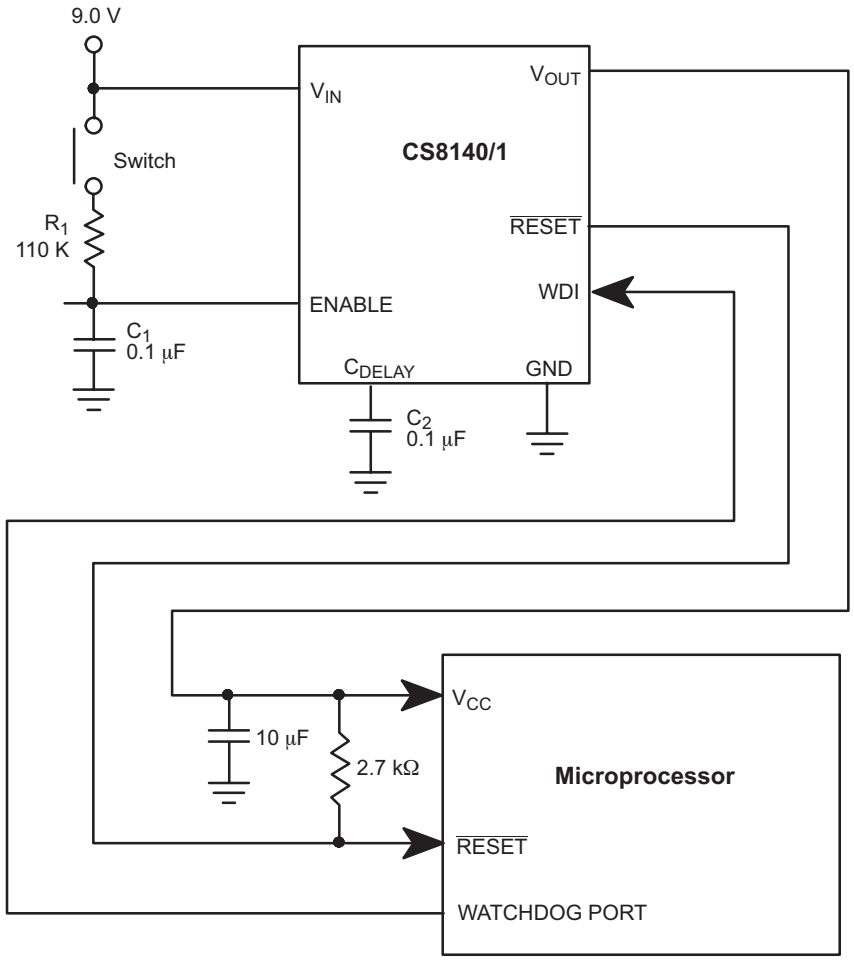
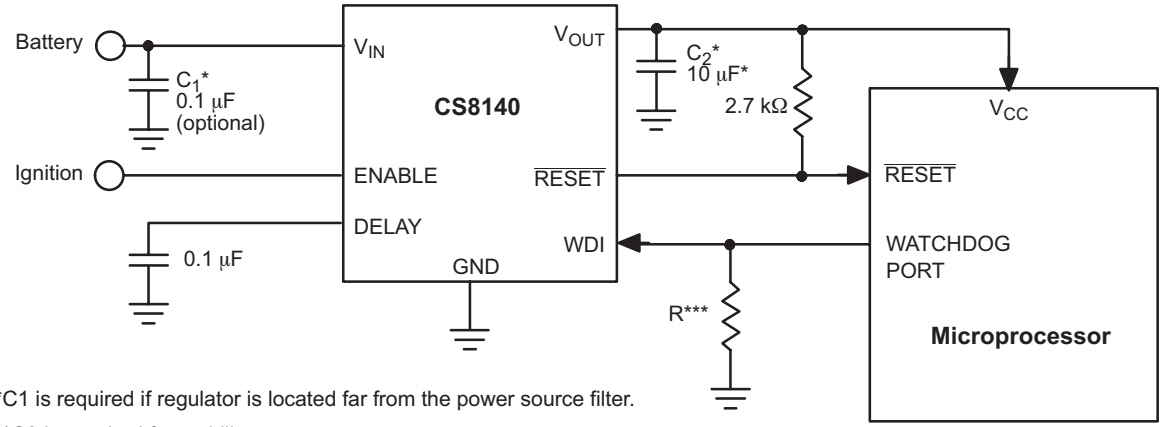


Figure 21. Application Diagram for CS8140. The CS8140 Provides a 5.0 V Tightly Regulated Supply and Control Function to the Microprocessor. In this Application, the Microprocessor Controls its own Power Down Sequence (see text).



*C1 is required if regulator is located far from the power source filter.

**C2 is required for stability.

***R ≤ 80 kΩ.

Figure 22. Application Diagram

STABILITY CONSIDERATIONS

The output or compensation capacitor C_2 in Figure 22 helps determine three main characteristics of a linear regulator: start−up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor C_2 shown in Figure 22 should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for C_2 for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Increase the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of ± 20% so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in step 3 above.

CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 23) is:

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}]I_{OUT(max)} + V_{IN(max)}I_Q \quad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,
$V_{OUT(min)}$ is the minimum output voltage,
$I_{OUT(max)}$ is the maximum output current for the application, and
I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

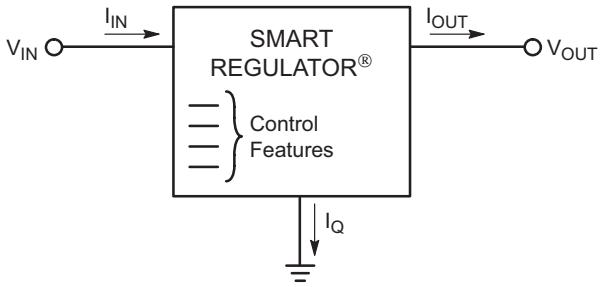


Figure 23. Single Output Regulator With Key Performance Parameters Labeled

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150^{\circ}C - T_A}{P_D} \quad (2)$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

HEAT SINKS

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$.

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA} \quad (3)$$

where:

$R_{\Theta JC}$ = the junction−to−case thermal resistance,

$R_{\theta CS}$ = the case−to−heatsink thermal resistance, and

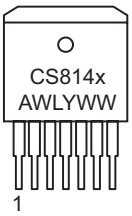
$R_{\theta SA}$ = the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

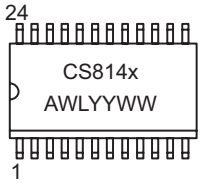
MARKING DIAGRAMS

TO−220−7

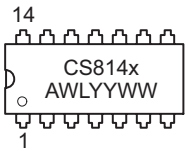
D²PAK−7
936AB



SO−24L



DIP−14



x = 0 or 1
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

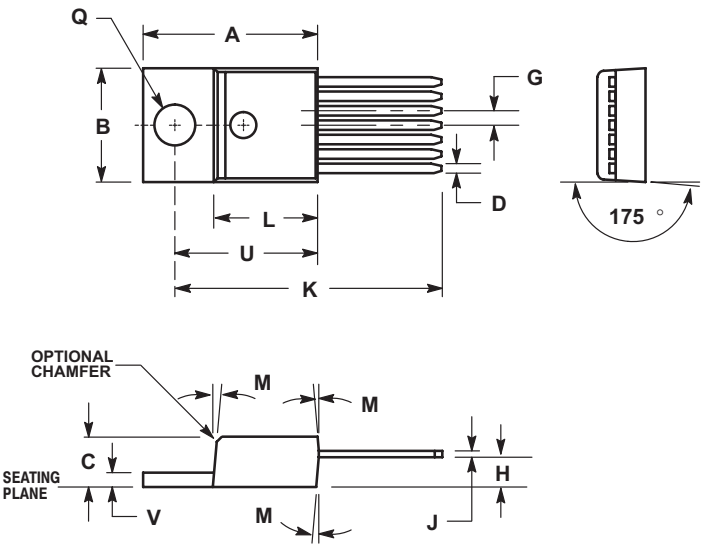
DEVICE ORDERING INFORMATION

Device	Package	Shipping†
CS8140YT7	TO−220−7, Straight	50 Units/Rail
CS8140YTVA7	TO−220−7, Vertical	50 Units/Rail
CS8140YTHA7	TO−220−7, Horizontal	50 Units/Rail
CS8140YDW24	SO−24L	31 Units/Rail
CS8140YDWR24	SO−24L	1000 Tape & Reel
CS8140YN14	DIP−14	25 Units/Rail
CS8141YT7	TO−220−7, Straight	50 Units/Rail
CS8141YTVA7	TO−220−7, Vertical	50 Units/Rail
CS8141YTHA7	TO−220−7, Horizontal	50 Units/Rail
CS8141YDPS7	D²PAK−7	50 Units/Rail
CS8141YDPSR7	D²PAK−7	750 Tape & Reel
CS8141YDW24	SO−24L	31 Units/Rail
CS8141YDWR24	SO−24L	1000 Tape & Reel
CS8141YN14	DIP−14	25 Units/Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

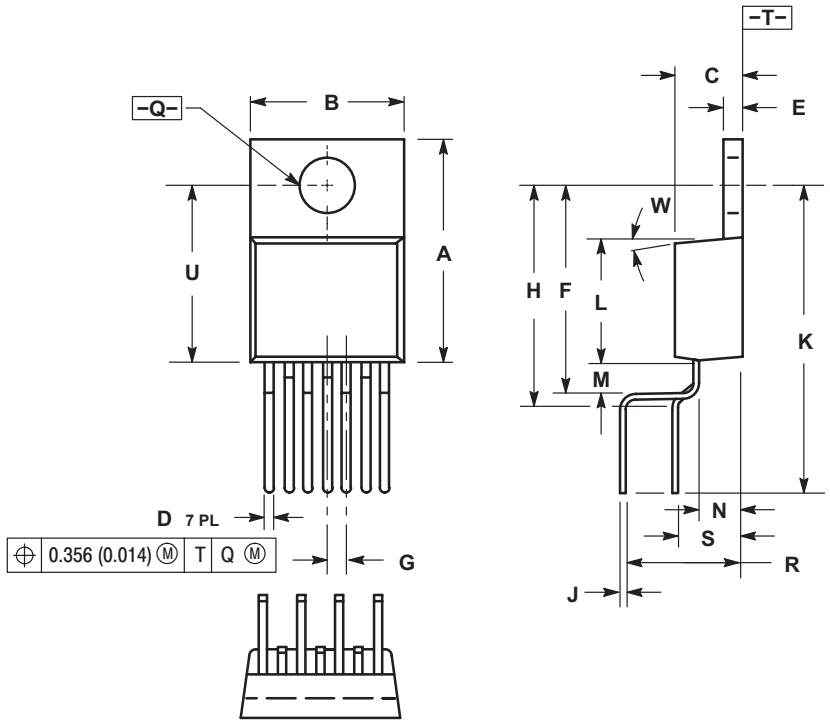
TO−220−7
T SUFFIX
CASE 821E−04
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.003 (0.076) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. 821E−01 THRU 821−03 OBSOLETE, NEW STANDARD 821E−04.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.600	0.610	15.24	15.49
B	0.386	0.403	9.80	10.23
C	0.170	0.180	4.32	4.56
D	0.028	0.037	0.71	0.94
G	0.045	0.055	1.15	1.39
H	0.088	0.102	2.24	2.59
J	0.018	0.026	0.46	0.66
K	1.028	1.042	26.11	26.47
L	0.355	0.365	9.02	9.27
M	5 ° NOM		5 ° NOM	
Q	0.142	0.148	3.61	3.75
U	0.490	0.501	12.45	12.72
V	0.045	0.055	1.15	1.39

TO−220−7
TVA SUFFIX
CASE 821J−02
ISSUE A

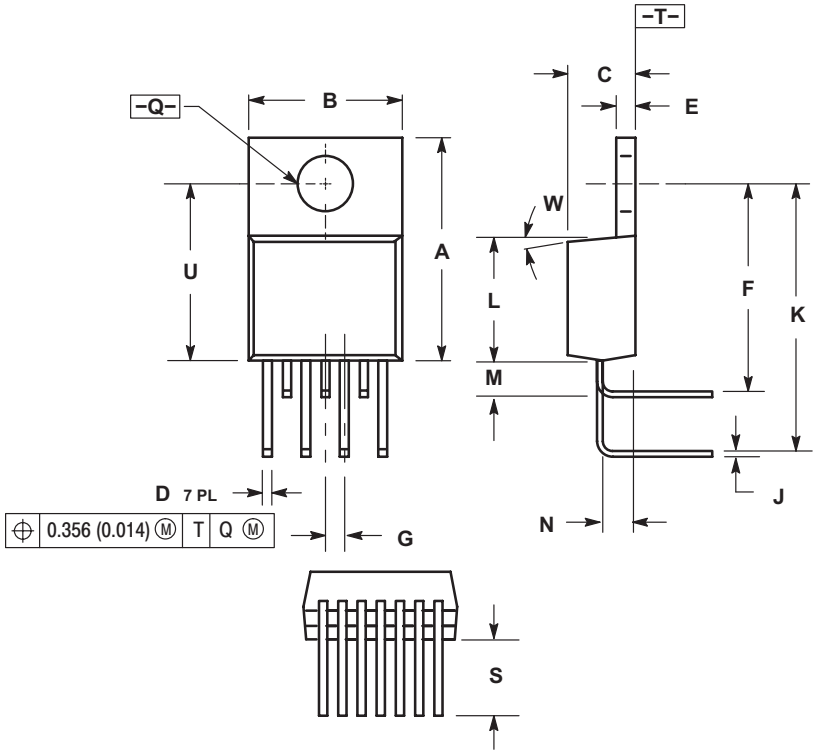


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.560	0.590	14.22	14.99
B	0.385	0.415	9.77	10.54
C	0.160	0.190	4.06	4.82
D	0.023	0.037	0.58	0.94
E	0.045	0.055	1.14	1.40
F	0.540	0.555	13.72	14.10
G	0.050 BSC		1.27 BSC	
H	0.570	0.595	14.48	15.11
J	0.014	0.022	0.36	0.56
K	0.785	0.800	19.94	20.32
L	0.322	0.337	8.18	8.56
M	0.073	0.088	1.85	2.24
N	0.090	0.115	2.28	2.91
Q	0.146	0.156	3.70	3.95
R	0.289	0.304	7.34	7.72
S	0.164	0.179	4.17	4.55
U	0.460	0.475	11.68	12.07
W	3 °		3 °	

PACKAGE DIMENSIONS

TO−220−7
THA SUFFIX
CASE 821H−02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.
1. LEADS MAINTAIN A RIGHT ANGLE WITH RESPECT TO THE PACKAGE BODY TO WITH ± 0.020".

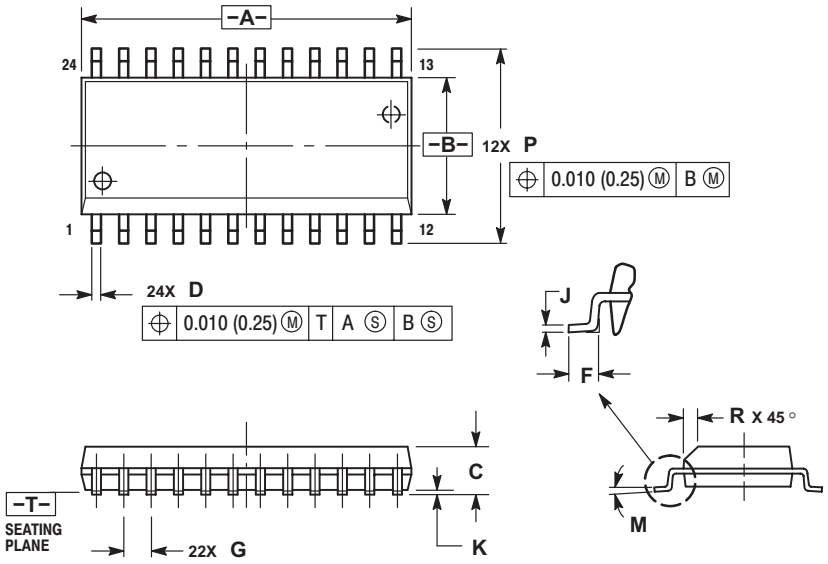
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.560	0.590	14.22	14.99
B	0.385	0.415	9.77	10.54
C	0.160	0.190	4.06	4.82
D	0.023	0.037	0.58	0.94
E	0.045	0.055	1.14	1.40
F	0.568	0.583	14.43	14.81
G	0.050 BSC		1.27 BSC	
J	0.015	0.022	0.38	0.56
K	0.728	0.743	18.49	18.87
L	0.322	0.337	8.18	8.56
M	0.101	0.116	2.57	2.95
N	0.090	0.115	2.28	2.91
Q	0.146	0.156	3.70	3.95
S	0.150	0.200	3.81	5.08
U	0.460	0.475	11.68	12.07
W	3 °		3 °	

D²PAK−7
DPS SUFFIX
CASE 936AB−01
ISSUE O

For D²PAK Outline and Dimensions − Contact Factory

PACKAGE DIMENSIONS

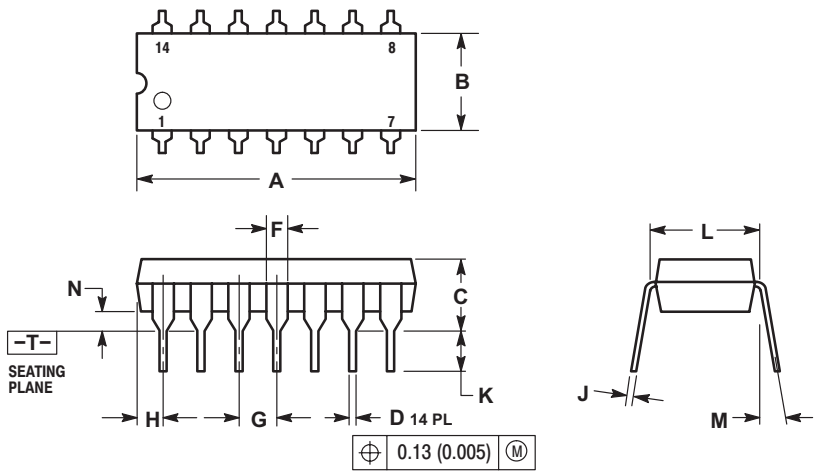
SO−24L
DW SUFFIX
CASE 751E−04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0 °	8 °	0 °	8 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

DIP−14
N SUFFIX
CASE 646−04
ISSUE M



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.740	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.160	0.180	4.06	4.57
D	0.015	0.020	0.38	0.51
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
H	0.052	0.072	1.32	1.83
J	0.008	0.012	0.20	0.30
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10 °	---	10 °
N	0.020	0.040	0.51	1.02

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