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CS8371

8.0 V/1.0 A, 5.0 V/250 mA Dual Regulator with Independent Output Enables and NOCAP™

The CS8371 is an 8.0 V/5.0 V dual output linear regulator. The 8.0 V ±5.0% output sources 1.0 A, while the 5.0 V ±5.0% output sources 250 mA. Each output is controlled by its own ENABLE lead. Setting the ENABLE input high turns on the associated regulator output. Holding both ENABLE inputs low puts the IC into sleep mode where current consumption is less than 10 μA.

The regulator is protected against overvoltage, short−circuit and thermal runaway conditions. The device can withstand 45 V load dump transients making suitable for use in automotive environments. ON's proprietary NOCAP solution is the first technology which allows the output to be stable without the use of an external capacitor.

The CS8371 is available in a 7 lead TO−220 package with copper tab. The tab can be connected to a heatsink if necessary.

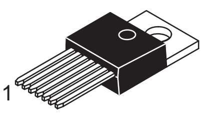
Features

- Two Regulated Outputs
  - 8.0 V ±5.0%; 1.0 A
  - 5.0 V ±5.0%; 250 mA
- Independent ENABLE for Each Output
- Seperate Sense Feedback Lead for 8.0 V Output
- < 10 μA Sleep Mode Current
- Fault Protection
  - Overvoltage Shutdown
  - +45 V Peak Transient Voltage
  - Short Circuit
  - Thermal Shutdown
- CMOS Compatible, Low Current ENABLE Inputs
- Pb−Free Packages are Available*

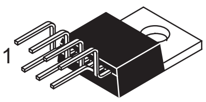
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

http://onsemi.com

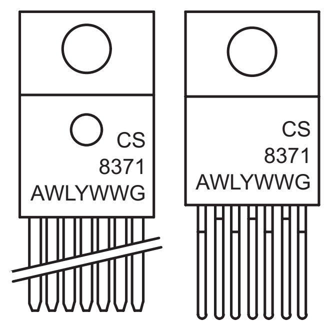


TO−220
SEVEN LEAD
T SUFFIX
CASE 821E



TO−220
SEVEN LEAD
TVA SUFFIX
CASE 821J

PIN CONNECTIONS AND MARKING DIAGRAM



Tab = GND
Pin 1. ENABLE$_1$
2. ENABLE$_2$
3. V_{OUT2}
4. GND
5. Sense
6. V_{CC}
7. V_{OUT1}

A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
CS8371ET7	TO−220 STRAIGHT	50 Units/Rail
CS8371ET7G	TO−220 STRAIGHT (Pb−Free)	50 Units/Rail
CS8371ETVA7	TO−220 VERTICAL	50 Units/Rail
CS8371ETVA7G	TO−220 VERTICAL (Pb−Free)	50 Units/Rail

June, 2006 − Rev. 12

Publication Order Number:
CS8371/D

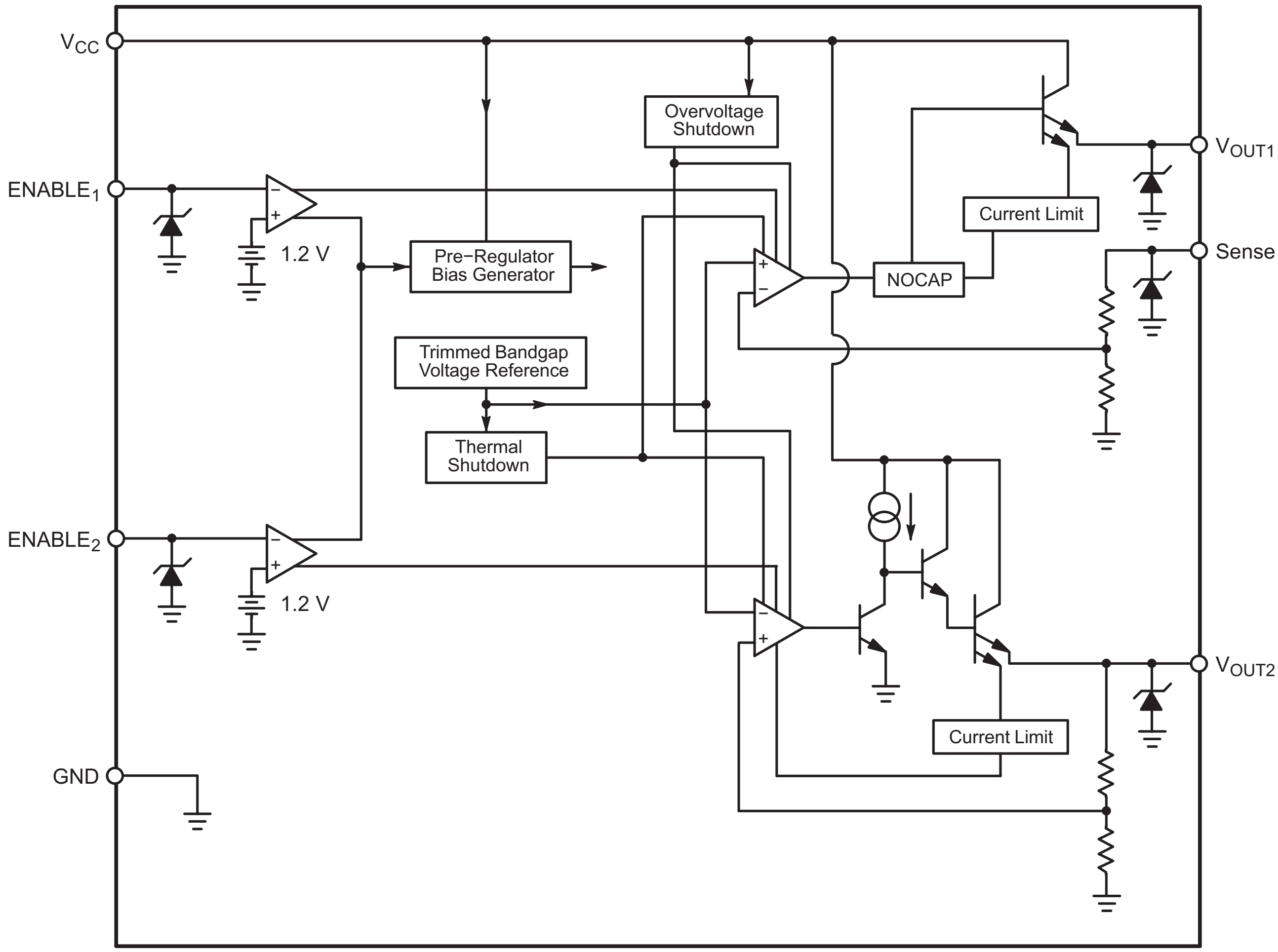


Figure 1. Block Diagram

MAXIMUM RATINGS

Rating	Value	Unit
Power Dissipation	Internally Limited	−
ENABLE Input Voltage Range	−0.6 to +10	V
Load Current (8.0 V Regulator)	Internally Limited	−
Load Current (5.0 V Regulator)	Internally Limited	−
Transient Peak Voltage (31 V Load Dump @ 14 V V_{CC})	45	V
Storage Temperature Range	−65 to +150	°C
Junction Temperature Range	−40 to +150	°C
Lead Temperature Soldering: Wave Solder (through hole styles only) (Note 1)	260 peak	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. 10 second maximum.

ELECTRICAL CHARACTERISTICS: ($-40°C \le T_A \le +85°C$, $10.5\ V \le V_{CC} \le 16\ V$, $ENABLE_1 = ENABLE_2 = 5.0\ V$, $I_{OUT1} = I_{OUT2} = 5.0\ mA$, unless otherwise stated.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
PRIMARY OUTPUT (V_{OUT1})					
Output Voltage	$I_{OUT1} = 1.0\ A$	7.60	8.00	8.40	V
Line Regulation	$10.5\ V \le V_{CC} \le 26\ V$	–	–	50	mV
Load Regulation	$5.0\ mA \le I_{OUT1} \le 1.0\ A$	–	–	150	mV
Sleep Mode Quiescent Current	$V_{CC} = 14\ V$, $ENABLE_1 = ENABLE_2 = 0\ V$	0	0.2	10.0	μA
Quiescent Current	$V_{CC} = 14\ V$, $I_{OUT1} = 1.0\ A$, $I_{OUT2} = 250\ mA$	–	–	30	mA
Dropout Voltage	$I_{OUT1} = 250\ mA$ $I_{OUT1} = 1.0\ A$	–	– –	1.2 1.5	V V
Quiescent Bias Current	$I_{OUT1} = 5.0\ mA$, $ENABLE_2 = 0\ V$, $V_{CC} = 14\ V$, $I_Q = I_{CC} - I_{OUT1}$ $I_{OUT1} = 1.0\ A$, $ENABLE_2 = 0\ V$, $V_{CC} = 14\ V$, $I_Q = I_{CC} - I_{OUT1}$	– –	– –	10 22	mA mA
Ripple Rejection	f = 120 Hz, $V_{CC} = 14\ V$ with 1.0 V_{PP} AC, $C_{OUT} = 0\ \mu F$ f = 10 kHz, $V_{CC} = 14\ V$ with 1.0 V_{PP} AC, $C_{OUT} = 0\ \mu F$ f = 20 kHz, $V_{CC} = 14\ V$ with 1.0 V_{PP} AC, $C_{OUT} = 0\ \mu F$	– – –	90 74 68	– – –	dB dB dB
Current Limit	$V_{CC} = 16\ V$	1.1	–	2.5	A
Overshoot Voltage	$5.0\ mA \le I_{REG1} \le 1.0\ A$	–	–	6.0	V
Output Noise	10 Hz − 100 kHz	–	300	–	μV_{rms}
SECONDARY OUTPUT (V_{OUT2})					
Output Voltage	$I_{OUT2} = 250\ mA$	4.75	5.00	5.25	V
Line Regulation	$7.0\ V \le V_{CC} \le 26\ V$	–	–	40	mV
Load Regulation	$5.0\ mA \le I_{OUT2} \le 250\ mA$	–	–	100	mV
Dropout Voltage	$I_{OUT2} = 5.0\ mA$ $I_{OUT2} = 250\ mA$	–	– –	2.2 2.5	V V
Quiescent Bias Current	$I_{OUT2} = 5.0\ mA$, ENABLE1 = 0 V, $V_{CC} = 14\ V$, $I_Q = I_{CC} - I_{OUT2}$ $I_{OUT2} = 250\ mA$, ENABLE1 = 0 V, $V_{CC} = 14\ V$, $I_Q = I_{CC} - I_{OUT2}$	– –	– –	7.0 8.0	mA mA
Ripple Rejection	f = 120 Hz, $V_{CC} = 14\ V$ with 1.0 V_{PP} AC, $C_{OUT} = 0\ \mu F$ f = 10 kHz, $V_{CC} = 14\ V$ with 1.0 V_{PP} AC, $C_{OUT} = 0\ \mu F$ f = 20 kHz, $V_{CC} = 14\ V$ with 1.0 V_{PP} AC, $C_{OUT} = 0\ \mu F$	– – –	90 75 67	– – –	dB dB dB
Current Limit	$V_{CC} = 16\ V$	270	–	600	mA
Overshoot Voltage	$5.0\ mA \le I_{REG2} \le 250\ mA$	–	–	4.3	V
Output Noise	10 Hz − 100 kHz	–	170	–	μV_{rms}
ENABLE FUNCTION (ENABLE)					
Input Current	$V_{CC} = 14\ V$, $0\ V \le ENABLE \le 5.5\ V$	−150	–	150	μA
Input Voltage	Low High	0 2.0	– –	0.8 5.0	V V
PROTECTION CIRCUITRY					
ESD Threshold	Human Body Model	±2.0	±4.0	–	kV
Overvoltage Shutdown	–	24	–	30	V
Thermal Shutdown	Guaranteed by Design	150	180	–	°C
Thermal Hysteresis	–	–	30	–	°C

PACKAGE PIN DESCRIPTION

PACKAGE LEAD #		
7 Lead TO−220	LEAD SYMBOL	FUNCTION
1	$ENABLE_1$	ENABLE control for the 8.0 V, 1.0 A output.
2	$ENABLE_2$	ENABLE control for the 5.0 V, 250 mA output.
3	V_{OUT2}	5.0 V ±5.0%, 250 mA regulated output.
4	GND	Ground.
5	Sense	Sense feedback for the primary 8.0 V output.
6	V_{CC}	Supply voltage, usually from battery.
7	V_{OUT1}	8.0 V ±5.0%, 1.0 A regulated output.

TYPICAL PERFORMANCE CHARACTERISTICS

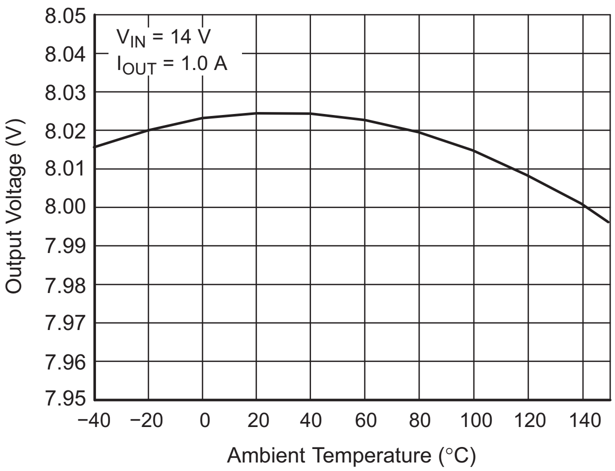


Figure 2. Regulator 1 Output Voltage

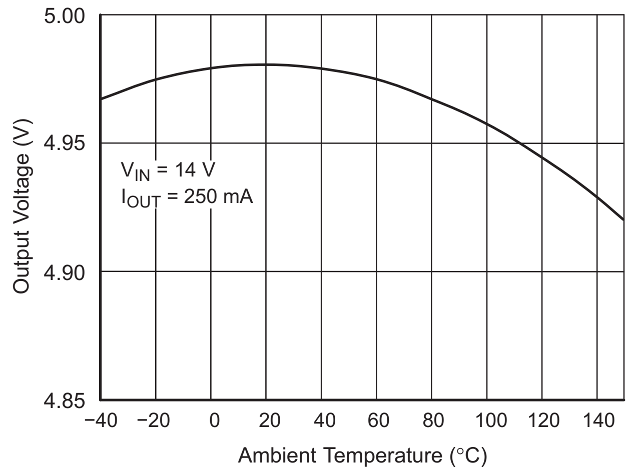


Figure 3. Regulator 2 Output Voltage

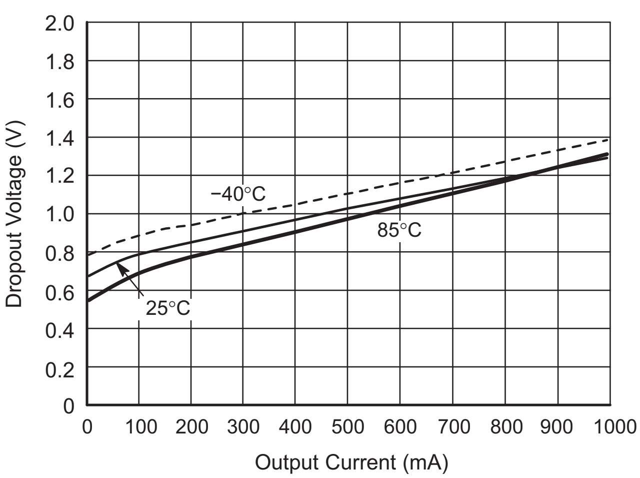


Figure 4. Regulator 1 Dropout Voltage

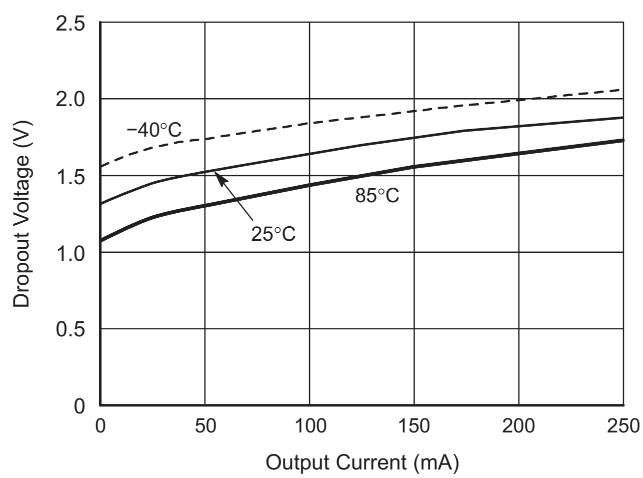


Figure 5. Regulator 2 Dropout Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

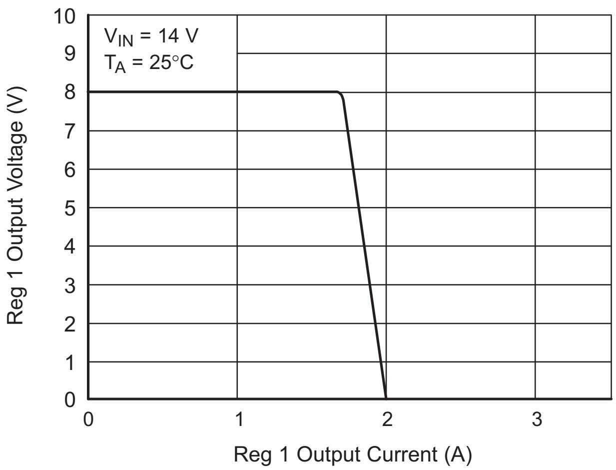


Figure 6. Regulator 1 Current Limit

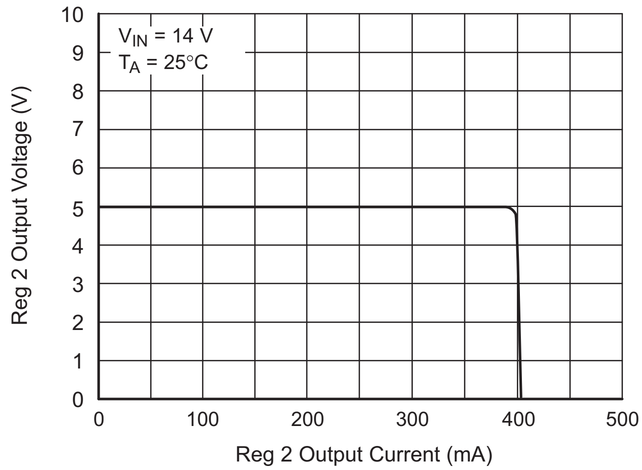


Figure 7. Regulator 2 Current Limit

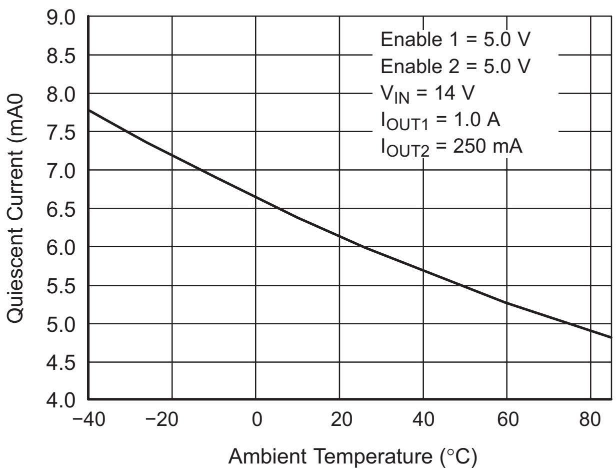


Figure 8. Quiescent Current

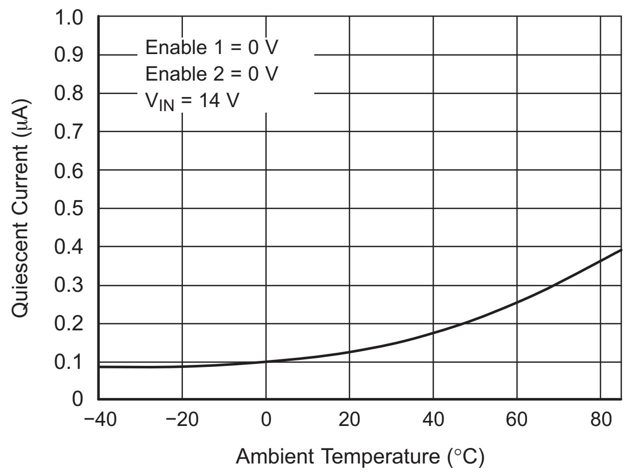


Figure 9. Quiescent Current

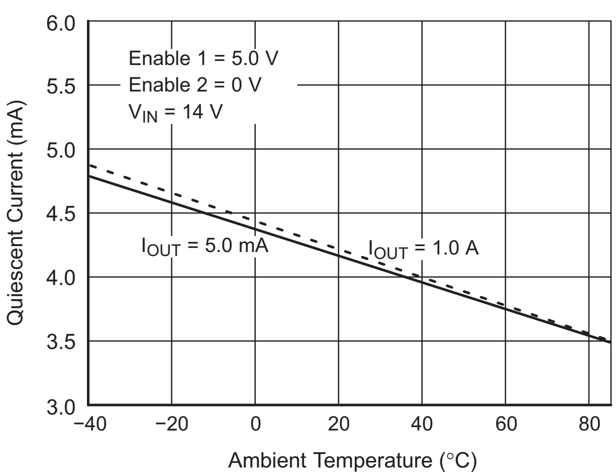


Figure 10. Regulator 1 Quiescent Current

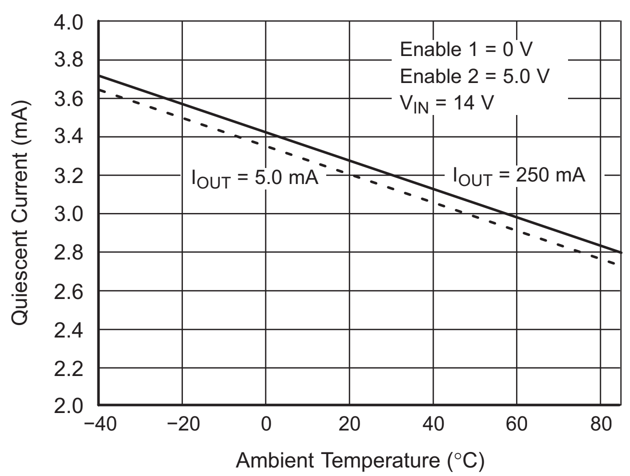


Figure 11. Regulator 2 Quiescent Current

TYPICAL PERFORMANCE CHARACTERISTICS

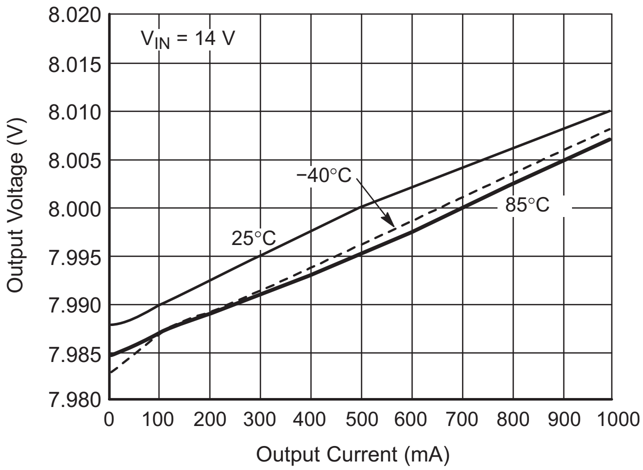


Figure 12. Regulator 1 Load Regulation

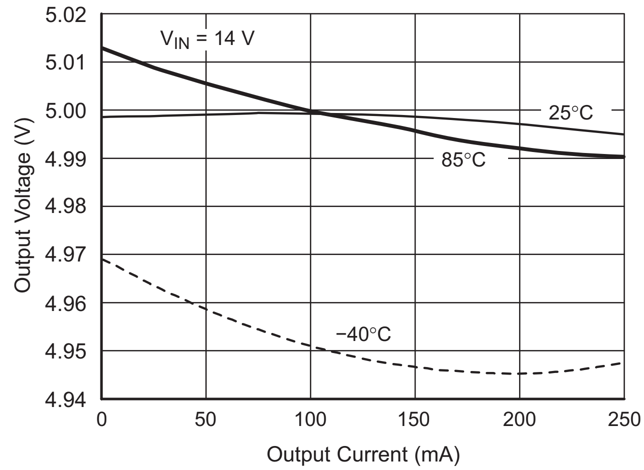


Figure 13. Regulator 2 Load Regulation

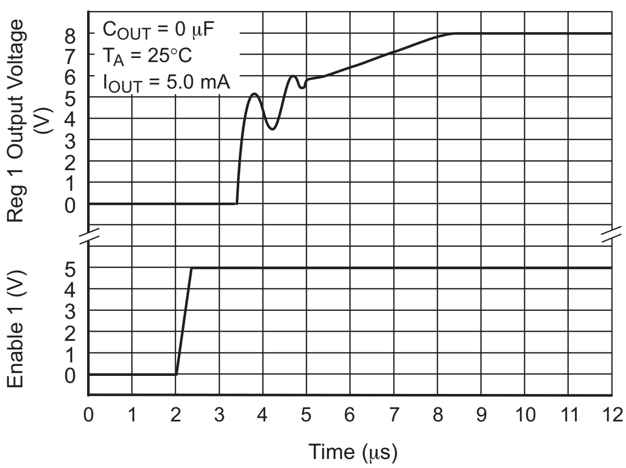


Figure 14. Regulator 1 Startup

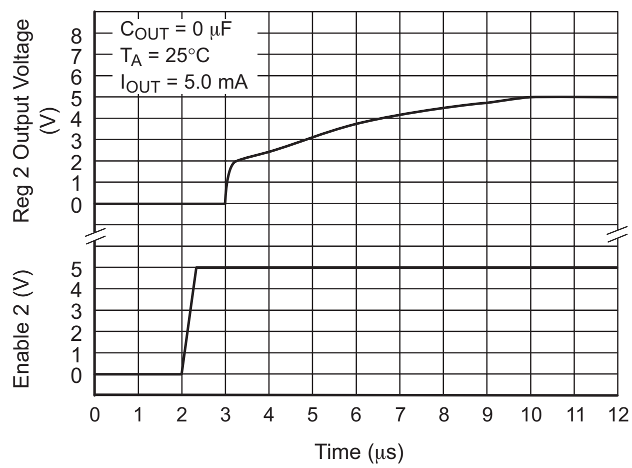


Figure 15. Regulator 2 Startup

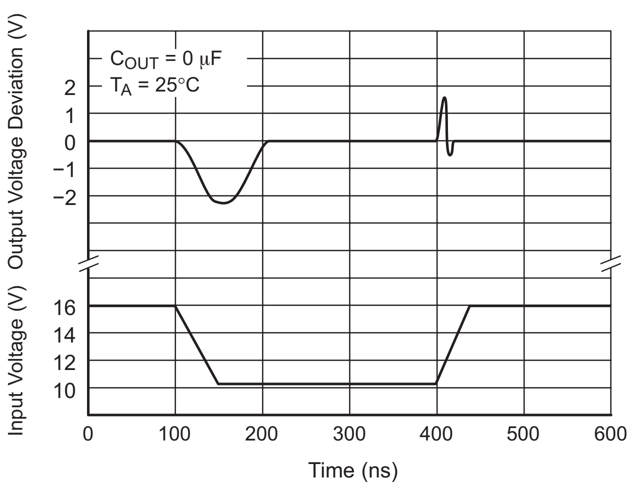


Figure 16. Regulator 1 Line Transient Response

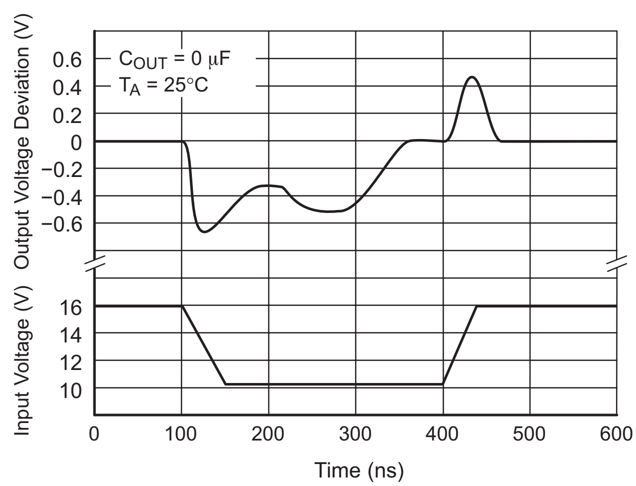


Figure 17. Regulator 2 Line Transient Response

TYPICAL PERFORMANCE CHARACTERISTICS

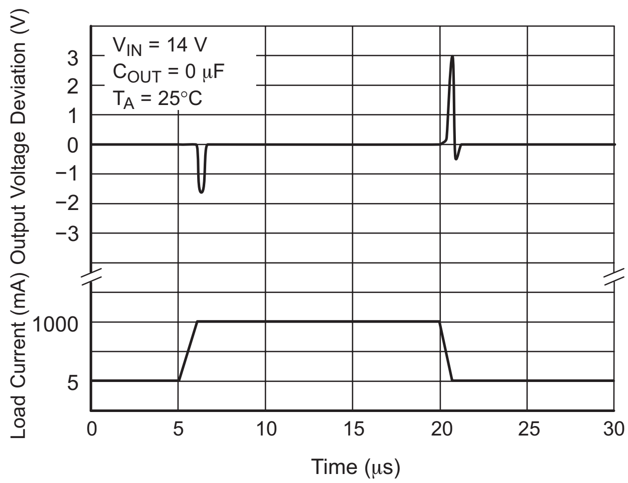


Figure 18. Regulator 1 Load Transient Response

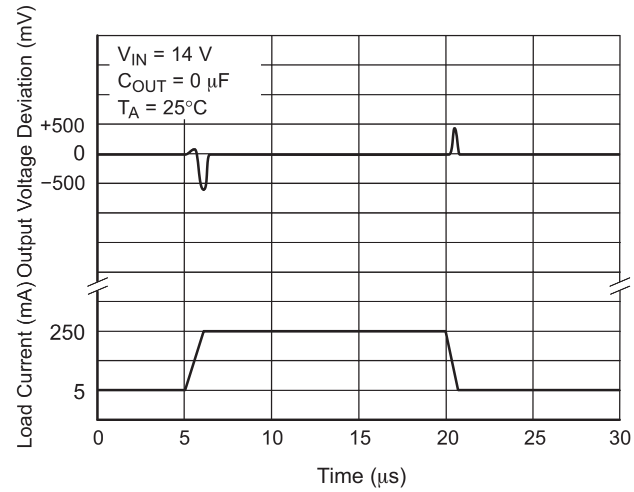


Figure 19. Regulator 2 Load Transient Response

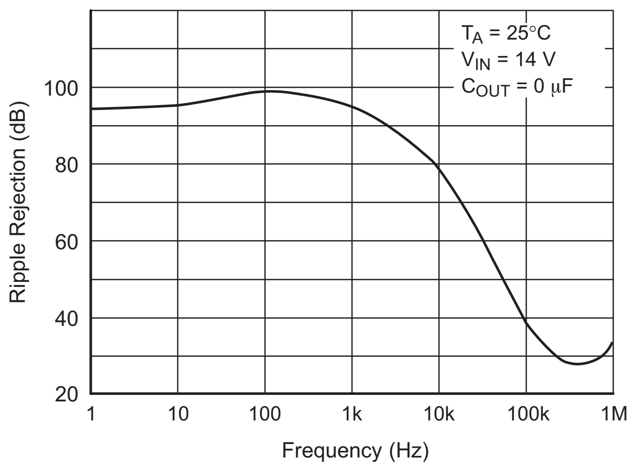


Figure 20. Regulator 1 Ripple Rejection

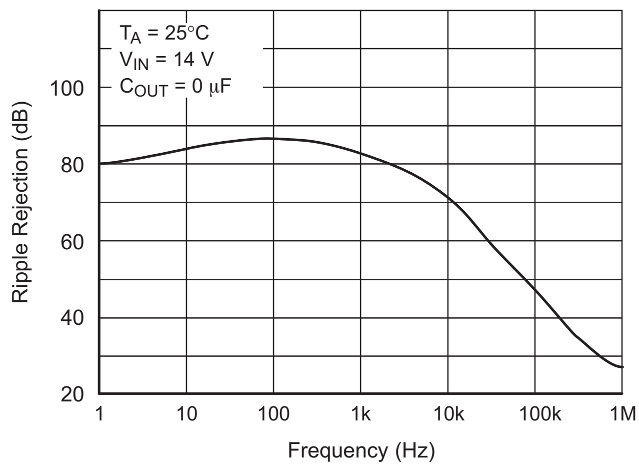


Figure 21. Regulator 2 Ripple Rejection

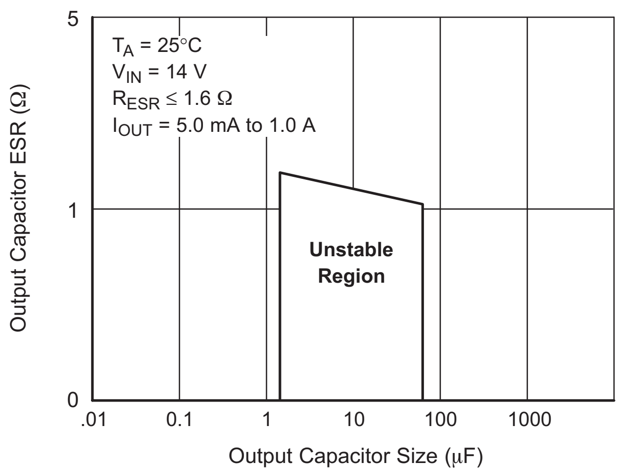


Figure 22. Regulator 1 Stability

DEFINITION OF TERMS

Dropout Voltage − The input−output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14 V input, dropout voltage is dependent upon load current and junction temperature.

Current Limit − Peak current that can be delivered to the output.

Input Voltage − The DC voltage applied to the input terminals with respect to ground.

Input Output Differential − The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation − The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation − The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability − Output voltage stability under accelerated life−test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage − The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current − The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection − The ratio of the peak−to−peak input ripple voltage to the peak−to−peak output ripple voltage.

Temperature Stability of V_{OUT} − The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

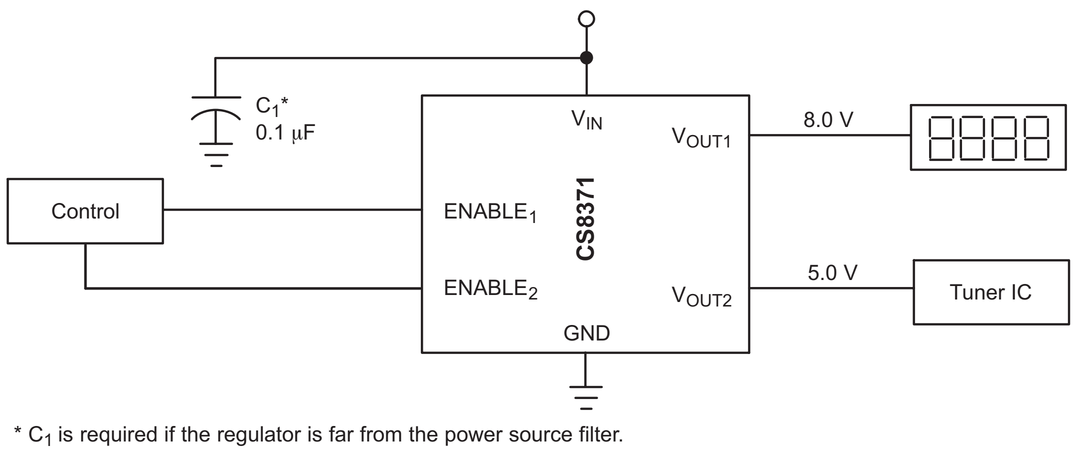


Figure 23. Applications Circuit

APPLICATION NOTES

With seperate control of each output channel, the CS8371 is ideal for applications where each load must be switched independently. In an automotive radio, the 8.0 V output drives the displays and tape drive motors while the 5.0 V output supplies the Tuner IC and memory.

Stability Considerations/NOCAP

Normally a low dropout or quasi−low dropout regulator (or any type requiring a slow lateral PNP in the control loop) necessitates a large external compensation capacitor at the output of the IC. The external capacitor is also used to curtail overshoot, determine startup delay time and load transient response.

Traditional LDO regulators typically have low unity gain bandwidth, display overshoot and poor ripple rejection. Compensation is also an issue because the high frequency load capacitor value, ESR (Equivalent Series Resistance) and board layout parasitics all can create oscillations if not properly accounted for.

NOCAP is an ON Semiconductor exclusive output stage which internally compensates the LDO regulator over temperature, load and line variations without the need for an expensive external capacitor. It incorporates high gain (>80 dB) and large unity gain bandwidth (>100 kHz) while maintaining many of the characteristics of a single−pole amplifier (large phase margin and no overshoot).

NOCAP is ideally suited for slow switching or steady loads. If the load displays large transient current requirements, such as with high frequency microprocessors, an output storage capacitor may be needed. Some large capacitor and small capacitor ESR values at the output may cause small signal oscillations at the output. This will depend on the load conditions. With these types of loads, a traditional output stage may be better suited for proper operation.

Output 1 employs NOCAP. Refer to the plots in the Typical Performance Characteristics section for appropriate output capacitor selections for stability if an external capacitor is required by the switching characteristics of the load. Output 2 has a Darlington NPN−type output structure and is inherently stable with any type of capacitive load or no capacitor at all.

Calculating Power Dissipation in a Dual Output Linear Regulator

The maximum power dissipation for a dual output regulator (Figure 24) is

$$P_{D(max)} = \{V_{IN(max)} - V_{OUT1(min)}\}I_{OUT1(max)} + \{V_{IN(max)} - V_{OUT2(min)}\}I_{OUT2(max)} + V_{IN(max)}I_Q \quad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT1(min)}$ is the minimum output voltage from V_{OUT1},

$V_{OUT2(min)}$ is the minimum output voltage from V_{OUT2},

$I_{OUT1(max)}$ is the maximum output current, for the application,

$I_{OUT2(max)}$ is the maximum output current, for the application, and

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^{\circ}C - T_A}{P_D} \quad (2)$$

The value of $R_{\theta JA}$ can be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

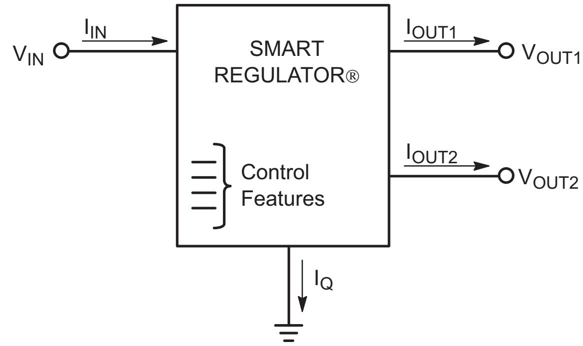


Figure 24. Dual Output Regulator With Key Performance Parameters Labeled.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,

$R_{\theta CS}$ = the case−to−heatsink thermal resistance, and

$R_{\theta SA}$ = the heatsink−to−ambient thermal resistance.

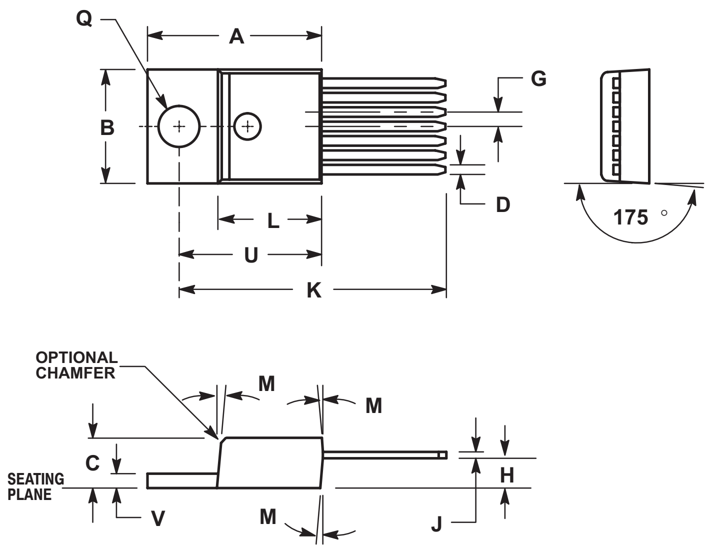
$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

PACKAGE THERMAL DATA

Parameter		TO−220 SEVEN LEAD	Unit
$R_{\theta JC}$	Typical	2.4	°C/W
$R_{\theta JA}$	Typical	50	°C/W

PACKAGE DIMENSIONS

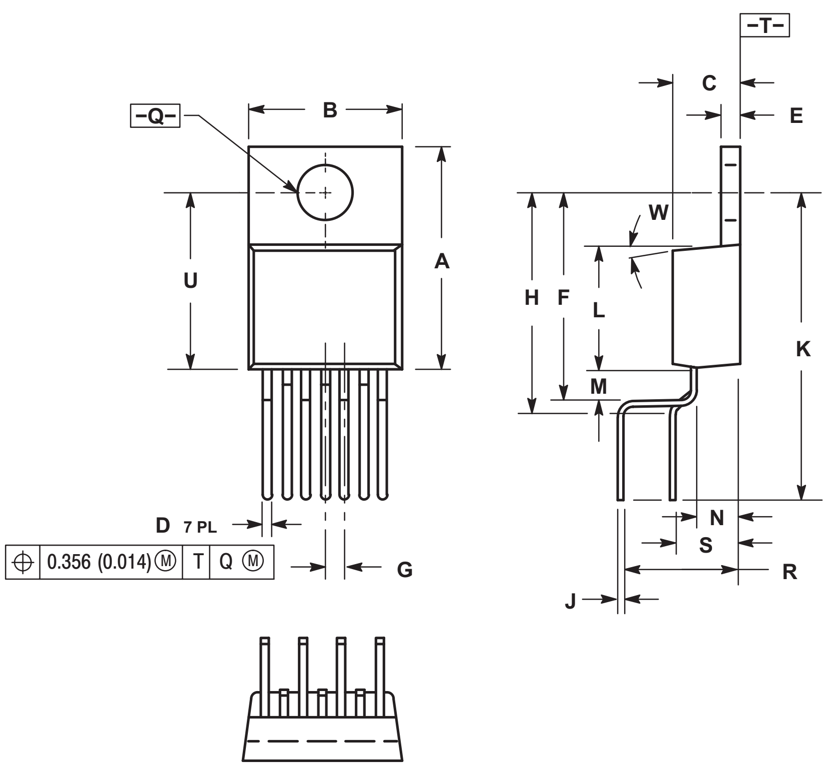
7 LEAD, TO−220
T SUFFIX
CASE 821E−04
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.003 (0.076) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. 821E−01 THRU 821−03 OBSOLETE, NEW STANDARD 821E−04.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.600	0.610	15.24	15.49
B	0.386	0.403	9.80	10.23
C	0.170	0.180	4.32	4.56
D	0.028	0.037	0.71	0.94
G	0.045	0.055	1.15	1.39
H	0.088	0.102	2.24	2.59
J	0.018	0.026	0.46	0.66
K	1.028	1.042	26.11	26.47
L	0.355	0.365	9.02	9.27
M	5 ° NOM		5 ° NOM	
Q	0.142	0.148	3.61	3.75
U	0.490	0.501	12.45	12.72
V	0.045	0.055	1.15	1.39

7 LEAD, TO−220
TVA SUFFIX
CASE 821J−02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.560	0.590	14.22	14.99
B	0.385	0.415	9.77	10.54
C	0.160	0.190	4.06	4.82
D	0.023	0.037	0.58	0.94
E	0.045	0.055	1.14	1.40
F	0.540	0.555	13.72	14.10
G	0.050 BSC		1.27 BSC	
H	0.570	0.595	14.48	15.11
J	0.014	0.022	0.36	0.56
K	0.785	0.800	19.94	20.32
L	0.322	0.337	8.18	8.56
M	0.073	0.088	1.85	2.24
N	0.090	0.115	2.28	2.91
Q	0.146	0.156	3.70	3.95
R	0.289	0.304	7.34	7.72
S	0.164	0.179	4.17	4.55
U	0.460	0.475	11.68	12.07
W	3 °		3 °	

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