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CS8406

192 kHz Digital Audio Interface Transmitter

Features

- Complete EIAJ CP1201, IEC-60958, AES3, S/PDIF-compatible Transmitter
- +3.3 V or 5.0 V Digital Supply (VD)
- +3.3 V or 5.0 V Digital Interface (VL)
- On-Chip Channel Status and User Bit Buffer Memories Allow Block-Sized Updates
- Flexible 3-Wire Serial Digital Audio Input Port
- Up to 192-kHz Frame Rate
- Microcontroller Write Access to Channel Status and User Bit Data
- On-Chip Differential Line Driver
- Generates CRC Codes and Parity Bits
- Stand-Alone Mode Allows Use without a Microcontroller

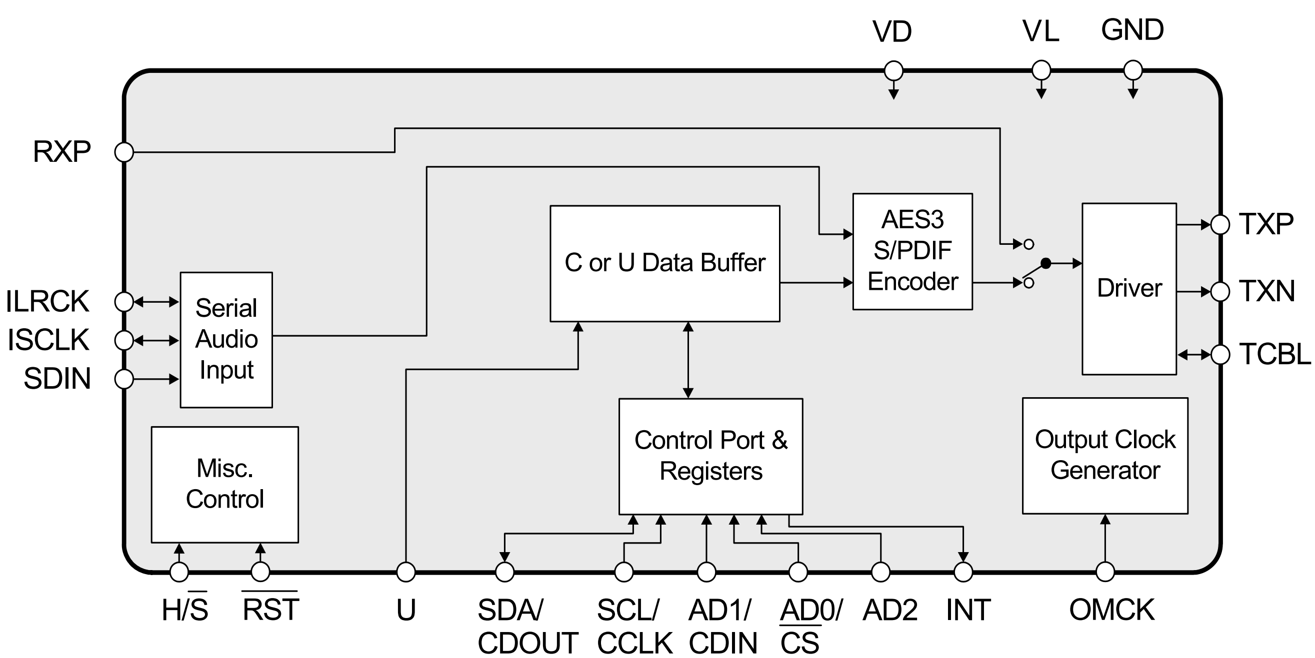
General Description

The CS8406 is a monolithic CMOS device which encodes and transmits audio data according to the AES3, IEC60958, S/PDIF, or EIAJ CP1201 standards. The CS8406 accepts audio and digital data, which is then multiplexed, encoded, and driven onto a cable.

The audio data is input through a configurable, 3-wire input port. The channel status and user bit data are input through an SPI™ or I²C® microcontroller port, and may be assembled in block-sized buffers. For systems with no microcontroller, a Stand-Alone Mode allows direct access to channel status and user bit data pins.

The CS8406 is available in a 28-pin TSSOP and SOIC package for both Commercial (-10º to +70ºC) and Automotive grade (-40º to +85ºC). The CDB8416 Demonstration board is also available for device evaluation and implementation suggestions. Please refer to "Ordering Information" on page 34 for complete details.

Target applications include A/V Receivers, CD-R, DVD receivers, digital mixing consoles, effects processors, set-top boxes, and computer and automotive audio systems.



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1. CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.)

SPECIFIED OPERATING CONDITIONS

(GND = 0 V, all voltages with respect to 0 V)

Parameter		Symbol	Min	Typ	Max	Units
Power Supply Voltage		VD VL	3.14 3.14	3.3 or 5.0 3.3 or 5.0	5.25 5.25	V V
Ambient Operating Temperature:	Commercial Grade Automotive Grade	T_A T_A	-10 -40	- -	+70 +85	°C °C

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V; all voltages with respect to 0 V. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.)

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	VD, VL	-	6.0	V
Input Current, Any Pin Except Supplies (Note 1)	I_{in}	-	±10	mA
Input Voltage	V_{in}	-0.3	VL + 0.3	V
Ambient Operating Temperature (power applied)	T_A	-55	125	°C
Storage Temperature	T_{stg}	-65	150	°C

Notes:

1. Transient currents of up to 100 mA will not cause SCR latch-up.

DC ELECTRICAL CHARACTERISTICS

(GND = 0 V; all voltages with respect to 0 V.)

Parameters		Symbol	Min	Typ	Max	Units
Power-Down Mode (Note 2)						
Supply Current in power down	VD = 3.3 V VD = 5.0 V VL = 3.3 V VL = 5.0 V	ID ID IL IL	- - - -	20 40 0 0	- - - -	µA µA µA µA
Normal Operation (Note 3)						
Supply Current at 48 kHz frame rate (Note 4)	VD = 3.3 V VD = 5.0 V VL = 3.3 V VL = 5.0 V	ID ID IL IL	- - - -	1.9 3.5 6.5 10.6	- - - -	mA mA mA mA
Supply Current at 192 kHz frame rate (Note 4)	VD = 3.3 V VD = 5.0 V VL = 3.3 V VL = 5.0 V	ID ID IL IL	- - - -	7.6 12.7 7.2 12	- - - -	mA mA mA mA

2. Power Down Mode is defined as $\overline{\text{RST}}$ = LO with all clocks and data lines held static.
3. Normal operation is defined as $\overline{\text{RST}}$ = HI.
4. Assumes that no inputs are left floating. It is recommended that all digital inputs be driven high or low at all times.

DIGITAL INPUT CHARACTERISTICS

Parameters	Symbol	Min	Typ	Max	Units
Input Leakage Current	I_{in}	-	-	±0.5	µA
Input Hysteresis (all inputs except OMCK)		-	0.25	-	V

DIGITAL INTERFACE SPECIFICATIONS

(GND = 0 V; all voltages with respect to 0 V.)

Parameters		Symbol	Min	Max	Units
High-Level Output Voltage (I_{OH} = -3.2 mA), except TXP/TXN		V_{OH}	VL - 1.0	-	V
Low-Level Output Voltage (I_{OH} = 3.2 mA), except TXP/TXN		V_{OL}	-	0.4	V
High-Level Output Voltage, TXP, TXN	(21 mA at VL = 5.0 V) (15 mA at VL = 3.3 V)		VL - 0.7 VL - 0.7	VL VL	V V
Low-Level Output Voltage, TXP, TXN	(21 mA at VL = 5.0 V) (16 mA at VL = 3.3 V)		- -	0.7 0.7	V V
High-Level Input Voltage	VD = 5.0 V VD = 3.3 V	V_{IH}	2.75 2.0	VL + 0.3 VL + 0.3	V V
Low-Level Input Voltage	VD = 5.0 V VD = 3.3 V	V_{IL}	-0.3 -0.3	0.8 0.8	V V

TRANSMITTER CHARACTERISTICS

Parameters		Symbol	Typ	Units
TXP Output Resistance	VL = 5.0 V VL = 3.3 V	R_{TXP}	26.5 33.5	Ω Ω
TXN Output Resistance	VL = 5.0 V VL = 3.3 V	R_{TXN}	26.5 33.5	Ω Ω

SWITCHING CHARACTERISTICS

(Inputs: Logic 0 = 0 V, Logic 1 = VL; C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Units
$\overline{\text{RST}}$ pin Low Pulse Width		200	-	-	µs
OMCK Frequency for OMCK = 512*Fs		4.1	-	98.4	MHz
OMCK Low and High Width for OMCK = 512*Fs		4.1	-	-	ns
OMCK Frequency for OMCK = 384*Fs		3.1	-	73.8	MHz
OMCK Low and High Width for OMCK = 384*Fs		6.1	-	-	ns
OMCK Frequency for OMCK = 256*Fs		2.0	-	49.2	MHz
OMCK Low and High Width for OMCK = 256*Fs		8.1	-	-	ns
OMCK Frequency for OMCK = 128*Fs		1.0	-	24.6	MHz
OMCK Low and High Width for OMCK = 128*Fs		18.3	-	-	ns
Frame Rate		8	-	192	kHz
AES3 Transmitter Output Jitter		-	200	-	ps RMS

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORTS

(Inputs: Logic 0 = 0 V, Logic 1 = VL; C_L = 20 pF)

Parameter		Symbol	Min	Typ	Max	Units
SDIN Setup Time Before ISCLK Active Edge	(Note 5)	t_{ds}	10	-	-	ns
SDIN Hold Time After ISCLK Active Edge	(Note 5)	t_{dh}	8	-	-	ns
Master Mode						
OMCK to ISCLK active edge delay	(Note 5)	t_{smd}	0	-	17	ns
OMCK to ILRCK delay	(Note 6)	t_{lmd}	0	-	16	ns
ISCLK and ILRCK Duty Cycle			-	50	-	%
Slave Mode						
ISCLK Period		t_{sckw}	36	-	-	ns
ISCLK Input Low Width		t_{sckl}	14.4	-	-	ns
ISCLK Input High Width		t_{sckh}	14.4	-	-	ns
ISCLK Active Edge to ILRCK Edge	(Note 7)	t_{lrckd}	10	-	-	ns
ILRCK Edge Setup Before ISCLK Active Edge	(Note 8)	t_{lrcks}	10	-	-	ns

Notes:

5. The active edge of ISCLK is programmable in Software Mode.
6. The polarity of ILRCK is programmable in Software Mode.
7. Prevents the previous ISCLK edge from being interpreted as the first one after ILRCK has changed.
8. This setup time ensures that this ISCLK edge is interpreted as the first one after ILRCK has changed.

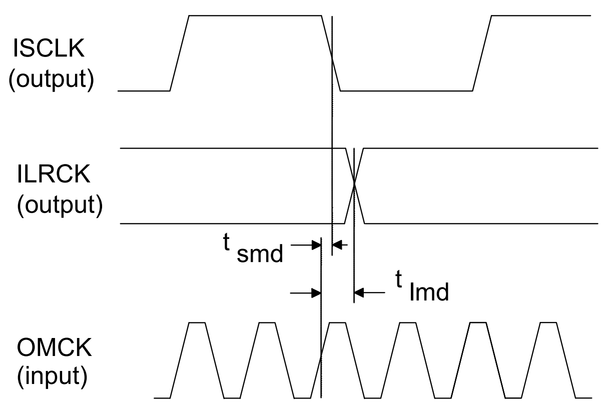


Figure 1. Audio Port Master Mode Timing

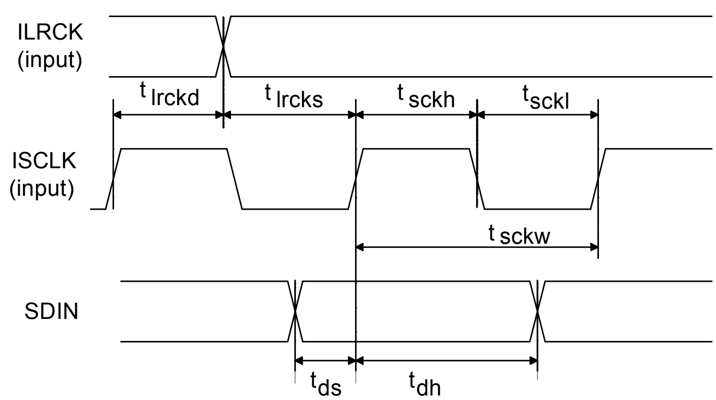


Figure 2. Audio Port Slave Mode and Data Input Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI MODE

(Inputs: Logic 0 = 0 V, Logic 1 = VL; C_L = 20 pF)

Parameter		Symbol	Min	Typ	Max	Units
CCLK Clock Frequency	(Note 9)	f_{sck}	0	-	6.0	MHz
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	-	ns
CCLK Low Time		t_{scl}	66	-	-	ns
CCLK High Time	(Note 10)	t_{sch}	MAX ((1/256 F_S + 8), 66)			ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	-	ns
CCLK Rising to DATA Hold Time	(Note 11)	t_{dh}	15	-	-	ns
CCLK Falling to CDOUT Stable		t_{pd}	-	-	50	ns
Rise Time of CDOUT		t_{r1}	-	-	25	ns
Fall Time of CDOUT		t_{f1}	-	-	25	ns
Rise Time of CCLK and CDIN	(Note 12)	t_{r2}	-	-	100	ns
Fall Time of CCLK and CDIN	(Note 12)	t_{f2}	-	-	100	ns

Notes:

9. If Fs is lower than 51.850 kHz, the maximum CCLK frequency should be less than 115 Fs. This is dictated by the timing requirements necessary to access the Channel Status and User Bit buffer memory. Access to the control register file can be carried out at the full 6 MHz rate.
10. T_{sch} must be greater than the larger of the two values, either 1/256FS + 8 ns, or 66 ns.
11. Data must be held for sufficient time to bridge the transition time of CCLK.
12. For f_{sck} < 1 MHz.

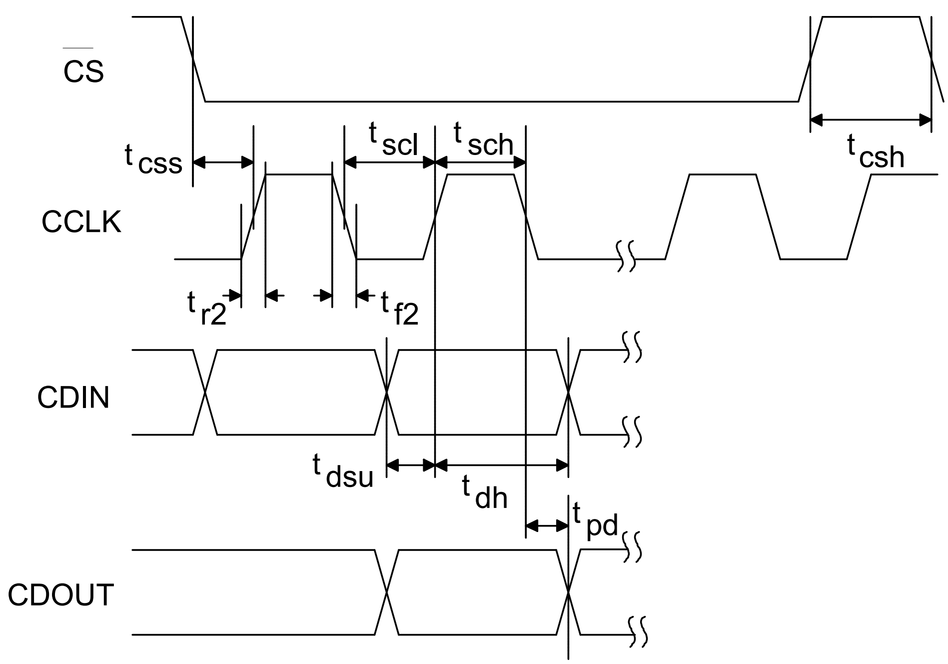


Figure 3. SPI Mode Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - I²C MODE

(Inputs: Logic 0 = 0 V, Logic 1 = VL; C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Units
SCL Clock Frequency	fscl	-	-	100	kHz
Bus Free Time Between Transmissions	t_{buf}	4.7	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	-	µs
Clock Low Time	t_{low}	4.7	-	-	µs
Clock High Time	t_{high}	4.0	-	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	-	µs
SDA Hold Time from SCL Falling (Note 13)	t_{hdd}	0	-	-	µs
SDA Setup Time to SCL Rising	t_{sud}	250	-	-	ns
Rise Time of Both SDA and SCL Lines	t_r	-	-	1000	ns
Fall Time of Both SDA and SCL Lines	t_f	-	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	-	µs

13. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

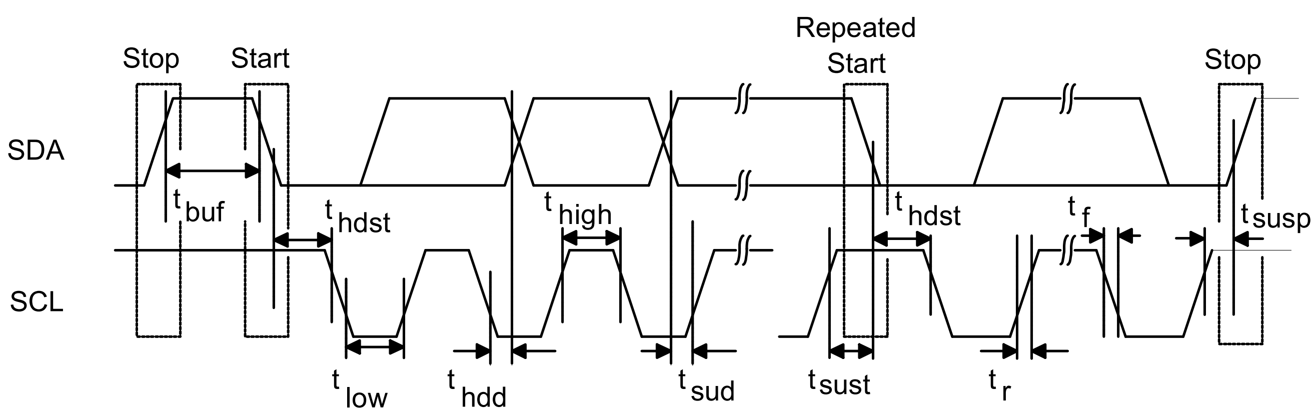


Figure 4. I²C Mode Timing

2. TYPICAL CONNECTION DIAGRAMS

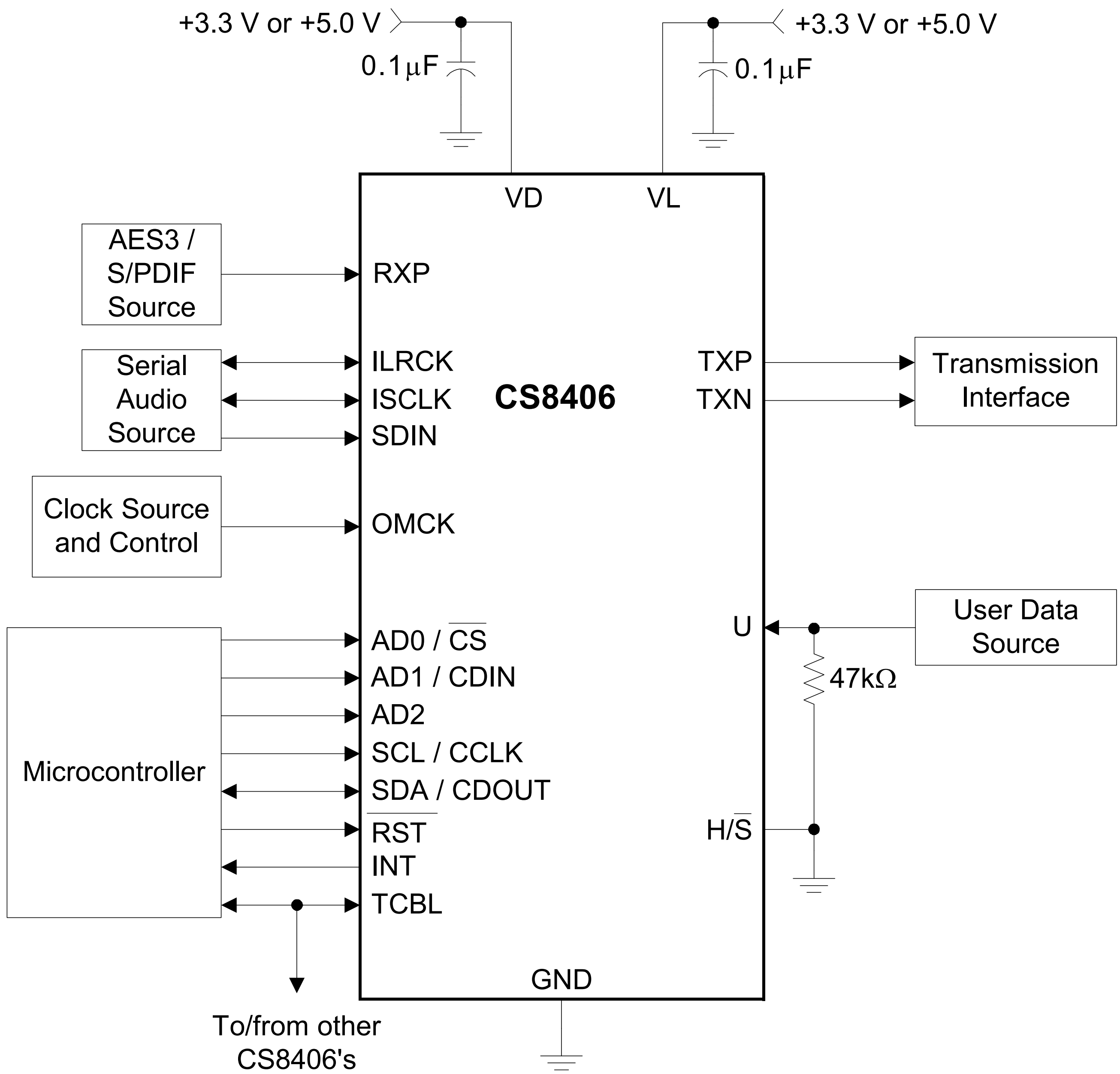


Figure 5. Recommended Connection Diagram for Software Mode

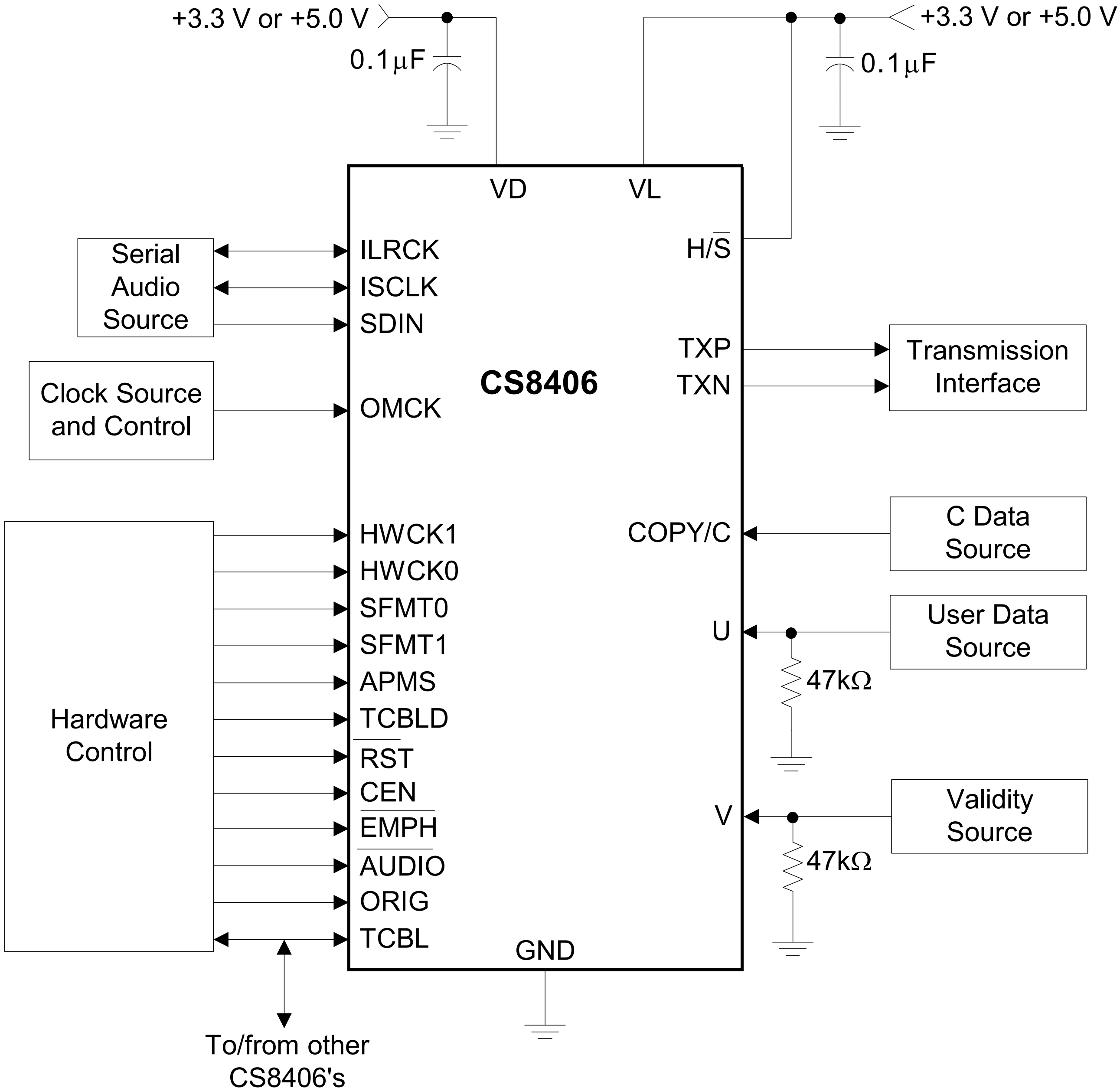


Figure 6. Recommended Connection Diagram for Hardware Mode

3. GENERAL DESCRIPTION

The CS8406 is a monolithic CMOS device which encodes and transmits audio data according to the AES3, IEC60958, S/PDIF, and EIAJ CP1201 interface standards. The CS8406 accepts audio, channel status and user data, which is then multiplexed, encoded, and driven onto a cable.

The audio data is input through a configurable, 3-wire input port. The channel status bits and user bit data are input through an SPI or I²C Mode microcontroller port and may be assembled in separate block sized buffers.

For systems with no microcontroller, a Stand-Alone Mode allows direct access to channel status and user data input pins.

Target applications include CD-R, DAT, DVD, MD and VTR equipment, mixing consoles, digital audio transmission equipment, high quality A/D converters, effects processors, set-top TV boxes, and computer audio systems.

Figure 5 shows the supply and external connections to the CS8406 when configured for operation with a microcontroller. Figure 6 shows the supply and external connections to the CS8406 when configured for operation without a microcontroller.

3.1 AES3 and S/PDIF Standards Documents

This data sheet assumes that the user is familiar with the AES3 and S/PDIF data formats. It is advisable to have current copies of the AES3 and IEC60958 specifications on hand for easy reference.

The latest AES3 standard is available from the Audio Engineering Society or ANSI at www.aes.org or www.ansi.org. Obtain the latest IEC60958 standard from ANSI or from the International Electrotechnical Commission at www.iec.ch. The latest EIAJ CP-1201 standard is available from the Japanese Electronics Bureau.

Application Note 22: *Overview of Digital Audio Interface Data Structures* contains a useful tutorial on digital audio specifications, but it should not be considered a substitute for the standards.

The paper *An Understanding and Implementation of the SCMS Serial Copy Management System for Digital Audio Transmission*, by Clifton Sanchez, is an excellent tutorial on SCMS. It is available from the AES as reprint 3518.

4. THREE-WIRE SERIAL INPUT AUDIO PORT

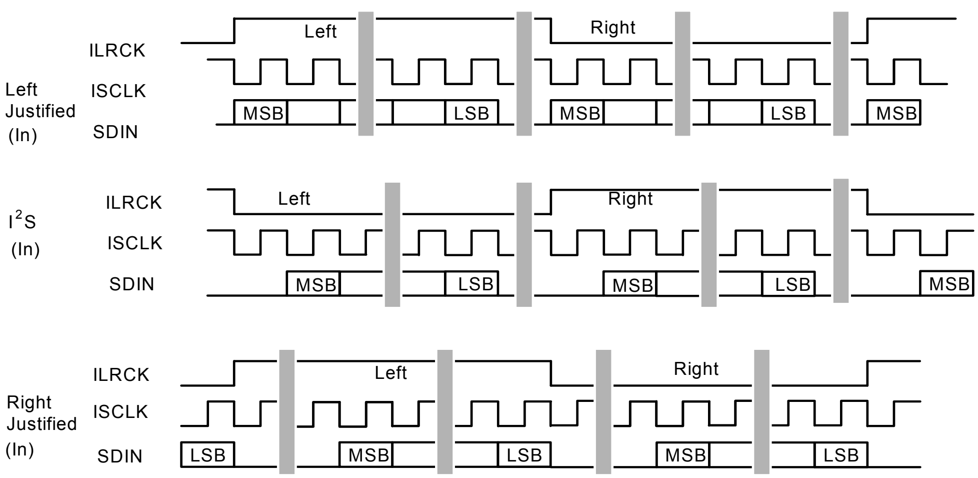
A 3-wire serial audio input port is provided. The interface format can be adjusted to suit the attached device through the control registers. The following parameters are adjustable:

- Master or slave
- Serial clock frequency
- Audio data resolution
- Left or right justification of the data relative to left/right clock
- Optional one-bit cell delay of the first data bit
- Polarity of the bit clock
- Polarity of the left/right clock (by setting the appropriate control bits, many formats are possible.)

Figure 7 shows a selection of common input formats with the corresponding control bit settings.

In Master Mode, the left/right clock and the serial bit clock are outputs, derived from the OMCK input pin master clock.

In Slave Mode, the left/right clock and the serial bit clock are inputs. The left/right clock must be synchronous to the OMCK master clock, but the serial bit clock can be asynchronous and discontinuous if required. The left/right clock should be continuous, but the duty cycle can be less than the specified typical value of 50% if enough serial clocks are present in each phase to clock all the data bits.



	SIMS*	SISF*	SIRES[1:0]*	SIJUST*	SIDEL*	SISPOL*	SILRPOL*
Left Justified	X	X	00+	0	0	0	0
I²S	X	X	00+	0	1	0	1
Right Justified	X	X	XX	1	0	0	0

X = don't care to match format, but does need to be set to the desired setting

+ I²S can accept an arbitrary number of bits, determined by the number of ISCLK cycles

* See Serial Input Port Data Format Register Bit Descriptions for an explanation of the meaning of each bit

Figure 7. Serial Audio Input Example Formats

5. AES3 TRANSMITTER

The CS8406 includes an AES3 digital audio transmitter. A comprehensive buffering scheme provides write access to the channel status and user data. This buffering scheme is described in "Appendix B: Channel Status and User Data Buffer Management" on page 36.

The AES3 transmitter encodes and transmits audio and digital data according to the AES3, IEC60958 (S/PDIF), and EIAJ CP-1201 interface standards. Audio and control data are multiplexed together and bi-phase mark encoded. The resulting bit stream is driven to an output connector either directly or through a transformer. The transmitter is clocked from the clock input pin, OMCK. If OMCK is asynchronous to the data source, an interrupt bit (TSLIP) is provided that will go high every time a data sample is dropped or repeated.

The channel status (C) and user (U) bits in the transmitted data stream are taken from storage areas within the CS8406. The user can access the internal storage or configure the CS8406 to run in one of several automatic modes. "Appendix B: Channel Status and User Data Buffer Management" on page 36 provides detailed descriptions of each automatic mode and describes methods of accessing the storage areas. The transmitted user bit data can optionally be input through the U pin, under the control of a control port register bit.

Figures 8 and 9 show the C/U/V timing requirements.

5.1 TXN and TXP Drivers

The AES3 transmitter line drivers are low skew, low impedance, differential outputs capable of driving cables directly. Both drivers are set to ground during reset ($\overline{\text{RST}}$ = LOW), when no AES3 transmit clock is provided, and optionally under the control of a register bit. The CS8406 also allows immediate muting of the AES3 transmitter audio data through a control register bit.

External components are used to terminate and isolate the external cable from the CS8406. These components are detailed in "Appendix A: External AES3/SPDIF/IEC60958 Transmitter Components" on page 35.

5.2 Mono Mode Operation

An alternate method for transmitting an AES3 192 kHz sample rate stream is Mono Mode. Mono Mode is implemented by using the two sub-frames in a 96 kHz biphase encoded stream to carry consecutive samples of a single channel of a 192 kHz PCM stream (i.e. a mono signal). This allows older equipment, whose AES3 transmitters and receivers are not rated for 192 kHz frame rate operation, to handle 192 kHz sample rate information. In this Mono Mode, two AES3 cables and two CS8406's are needed for stereo data transfer. The CS8406 is set to Mono Mode by the MMT control bit.

In Mono Mode, the input port will run at the audio sample rate (Fs), while the AES3 transmitter frame rate will be at Fs/2. Consecutive left or right channel serial audio data samples may be selected for transmission on the A and B sub-frames, and the channel status block transmitted is also selectable.

Using Mono Mode is only necessary if the incoming audio sample rate is already at 192 kHz and contains both left and right audio data words. The "Mono Mode" AES3 output stream may also be achieved by keeping the CS8406 in normal stereo mode, and placing consecutive audio samples in the left and right positions in an incoming 96 kHz word rate data stream. Figure 9 shows the C/U/V timing requirements.

5.3 Transmitted Frame and Channel Status Boundary Timing

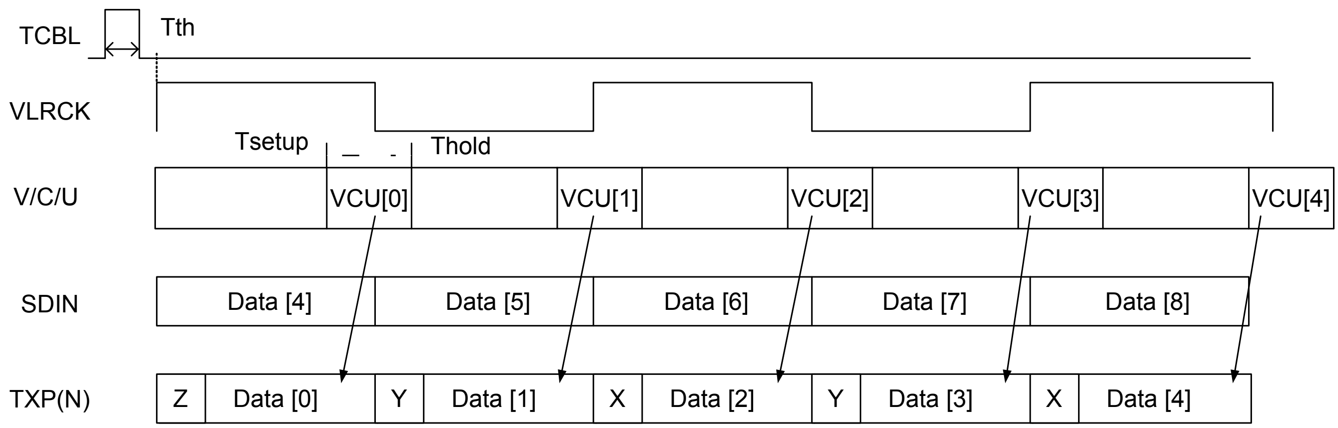
The TCBL pin is used to indicate the start of transmitted channel status block boundaries and may be an input or an output.

In some applications, it may be necessary to control the precise timing of the transmitted AES3 frame boundaries. This may be achieved in two ways:

a) With TCBL set to input, driving TCBL high for >3 OMCK clocks will cause a frame start, as well as a new channel status block start.

b) If the serial audio input port is in Slave Mode and TCBL is set to output, the start of the A channel sub-frame will be aligned with the leading edge of ILRCK.

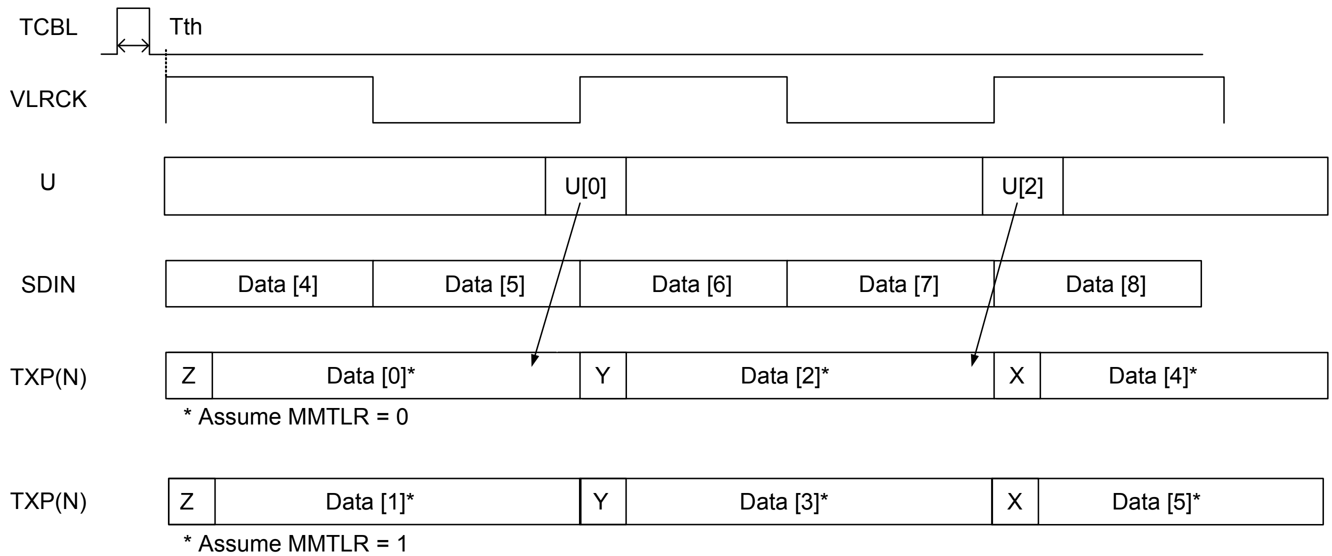
The timing of TCBL, VLRCK, C, U, and V are illustrated in Figure 8 and Figure 9. VLRCK is the internal virtual word clock signal, and is used here only to illustrate the timing of the C, U, and V bits. In Stereo Mode VLRCK = AES3 frame rate and in Mono Mode VLRCK = 2 x AES3 frame rate. If the serial audio input port is set to Slave Mode and TCBL is an output, VLRCK = ILRCK when SILRPOL = 0 and VLRCK = $\overline{\text{ILRCK}}$ when SILRPOL = 1. If the serial audio input port is set to master mode and TCBL is an input, VLRCK = ILRCK when SILRPOL = 0 and VLRCK = $\overline{\text{ILRCK}}$ when SILRPOL = 1.



Note:

1. $T_{setup} \geq$ 15% AES3 frame rate
2. $T_{hold} = 0$
3. T_{th} > 3 OMCKS if TCBL is an input

Figure 8. AES3 Transmitter Timing for C, U, and V Pin Input Data, Stereo Mode



Note:

1. $T_{setup} \geq$ 15% AES3 frame rate
2. $T_{hold} = 0$
3. $T_{th} >$ 3 OMCKS if TCBL is an input

Figure 9. AES3 Transmitter Timing for C, U, and V Pin Input Data, Mono Mode

6. CONTROL PORT DESCRIPTION

The control port is used to access the registers, allowing the CS8406 to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

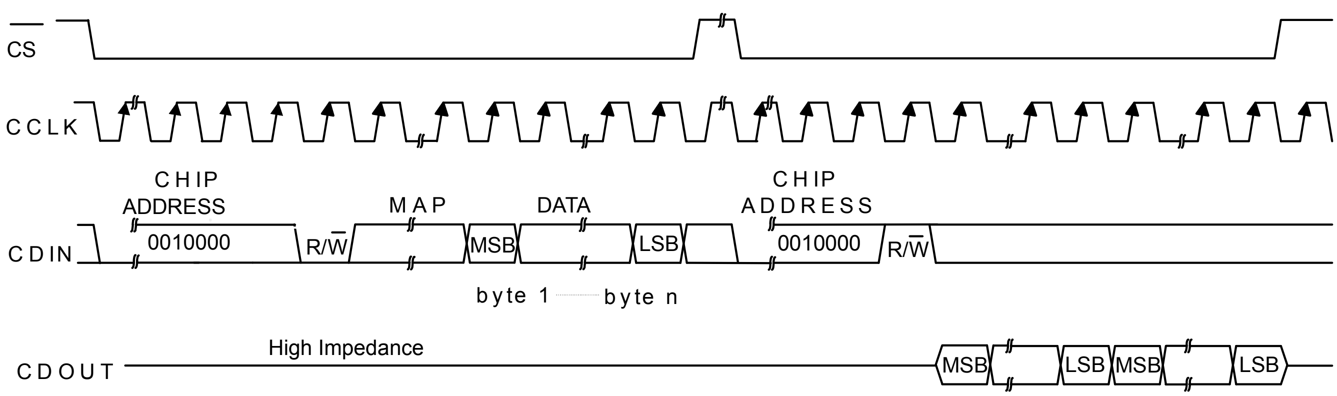
The control port has two modes: SPI and I²C, with the CS8406 acting as a slave device. SPI Mode is selected if there is a high to low transition on the AD0/$\overline{CS}$ pin, after the $\overline{RST}$ pin has been brought high. I²C Mode is selected by connecting the AD0/$\overline{CS}$ pin through a resistor to VL or GND, thereby permanently selecting the desired AD0 bit address state.

6.1 SPI Mode

In SPI Mode, $\overline{CS}$ is the CS8406 chip select signal, CCLK is the control port bit clock (input into the CS8406 from the microcontroller), CDIN is the input data line from the microcontroller, and CDOUT is the output data line to the microcontroller. Data is clocked in on the rising edge of CCLK and out on the falling edge.

Figure 10 shows the operation of the control port in SPI Mode. To write to a register, bring $\overline{CS}$ low. The first seven bits on CDIN form the chip address and must be 0010000. The eighth bit is a read/write indicator (R/$\overline{W}$), which should be low to write. The next eight bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data which will be placed into the register designated by the MAP. During writes, the CDOUT output stays in the Hi-Z state. It may be externally pulled high or low with a 47 kΩ resistor, if desired.

To read a register, the MAP has to be set to the correct address by executing a partial write cycle which finishes ($\overline{CS}$ high) immediately after the MAP byte. To begin a read, bring $\overline{CS}$ low, send out the chip address and set the read/write bit (R/$\overline{W}$) high. The next falling edge of CCLK will clock out the MSB of the addressed register (CDOUT will leave the high impedance state). The MAP automatically increments so data for successive registers will appear consecutively.



MAP = Memory Address Pointer, 7 bits, MSB first

Figure 10. Control Port Timing in SPI Mode

6.2 I²C Mode

In I²C Mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL. There is no $\overline{CS}$ pin. Pins AD0, AD1, and AD2 form the three least significant bits of the chip address and should be connected to VL or GND as desired.

The signal timing for both a read and write cycle are shown in Figure 11 and Figure 12. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS8406 after a Start condition consists of a 7 bit chip address field and a R/$\overline{W}$ bit (high for a read, low for a write). The upper 4 bits of the 7-bit address field are fixed at 0010. To communicate with a CS8406, the chip address field, which is the first byte sent to the CS8406, should match 0010 followed by the settings of the AD2, AD1, and AD0 pins. The eighth bit of the address is the R/$\overline{W}$ bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. The MAP automatically increments, so consecutive registers can read from or written to easily. Each byte is separated by an acknowledge bit (ACK). The ACK bit is output from the CS8406 after each input byte is read, and is input to the CS8406 from the microcontroller after each transmitted byte.

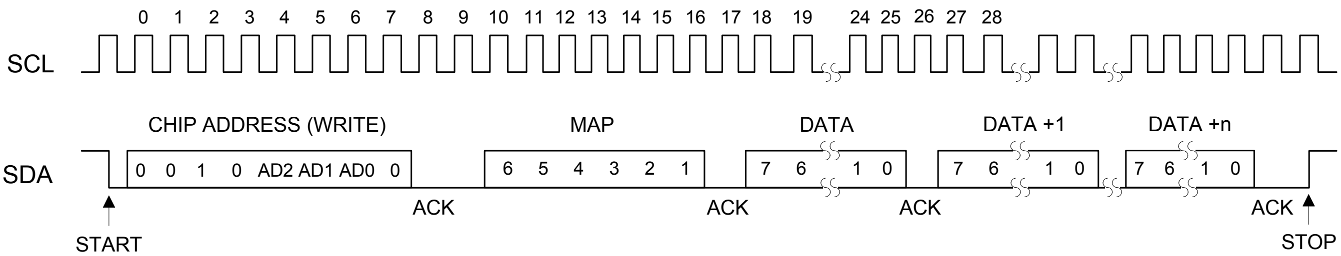


Figure 11. Control Port Timing, I²C Slave Mode Write

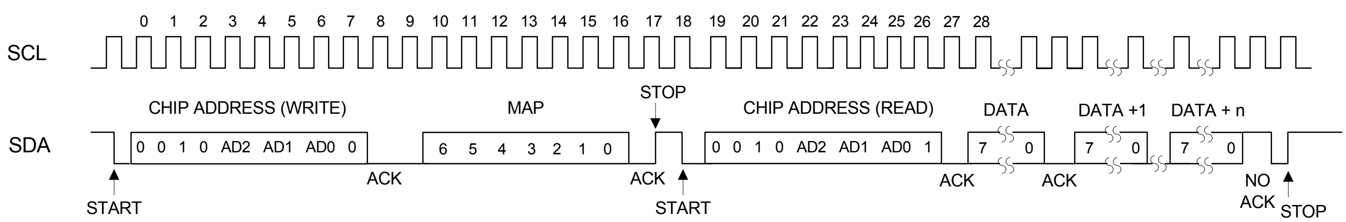


Figure 12. Control Port Timing, I²C Slave Mode Read

Since the read operation cannot set the MAP, an aborted write operation is used as a preamble. As shown in Figure 12, the write operation is aborted after the acknowledge for the MAP by sending a stop condition.

7. CONTROL PORT REGISTER SUMMARY

Addr (HEX)	Function	7	6	5	4	3	2	1	0
00	Reserved	0	0	0	0	0	0	0	0
01	Control 1	0	VSET	0	MUTEAES	0	INT1	INT0	TCBLD
02	Control 2	0	0	0	0	0	MMT	MMCST	MMTLR
03	Data Flow Control	0	TXOFF	AESBP	0	0	0	0	0
04	Clock Source Control	0	RUN	CLK1	CLK0	0	0	0	0
05	Serial Input Format	SIMS	SISF	SIRES1	SIRES0	SIJUST	SIDEL	SISPOL	SILRPOL
06	Reserved	0	0	0	0	0	0	0	0
07	Interrupt 1 Status	TSLIP	0	0	0	0	0	EFTC	0
08	Interrupt 2 Status	0	0	0	0	0	EFTU	0	0
09	Interrupt 1 Mask	TSLIPM	0	0	0	0	0	EFTCM	0
0A	Interrupt 1 Mode (MSB)	TSLIP1	0	0	0	0	0	EFTC1	0
0B	Interrupt 1 Mode (LSB)	TSLIP0	0	0	0	0	0	EFTC0	0
0C	Interrupt 2 Mask	0	0	0	0	0	EFTUM	0	0
0D	Interrupt 2 Mode (MSB)	0	0	0	0	0	EFTU1	0	0
0E	Interrupt 2 Mode (LSB)	0	0	0	0	0	EFTU0	0	0
0F-11	Reserved	0	0	0	0	0	0	0	0
12	CS Data Buffer Control	0	0	BSEL	0	0	EFTCI	CAM	0
13	U Data Buffer Control	0	0	0	UD	UBM1	UBM0	0	EFTUI
1D-1F	Reserved	0	0	0	0	0	0	0	0
20-37	C or U Data Buffer								
7F	ID and Version	ID3	ID2	ID1	ID0	VER3	VER2	VER1	VER0

Table 1. Control Register Map Summary

Note: Reserved registers must not be written to during normal operation. Some reserved registers are used for test modes, which can completely alter the normal operation of the CS8406.

8. CONTROL PORT REGISTER BIT DEFINITIONS

8.1 Memory Address Pointer (MAP)

Not a register

7	6	5	4	3	2	1	0
0	MAP6	MAP5	MAP4	MAP3	MAP2	MAP1	MAP0

MAP[6:0] - Memory Address Pointer. Will automatically increment after each read or write.

8.2 Default = ‘000000’Control 1 (01h)

7	6	5	4	3	2	1	0
0	VSET	0	MUTEAES	0	INT1	INT0	TCBLD

VSET - Transmitted Validity bit level

Default = ‘0’

0 - Indicates data is valid, linear PCM audio data
1 - Indicates data is invalid or not linear PCM audio data

MUTEAES - Mute control for the AES transmitter output

Default = ‘0’

0 - Not Muted
1 - Muted

INT1:0 - Interrupt output pin (INT) control

Default = ‘00’

00 - Active high; high output indicates interrupt condition has occurred
01 - Active low, low output indicates an interrupt condition has occurred
10 - Open drain, active low. Requires an external pull-up resistor on the INT pin.
11 - Reserved

TCBLD - Transmit Channel Status Block pin (TCBL) direction specifier

Default = ‘0’

0 - TCBL is an input
1 - TCBL is an output

8.3 Control 2 (02h)

7	6	5	4	3	2	1	0
0	0	0	0	0	MMT	MMTCS	MMTLR

MMT - Select AES3 transmitter mono or stereo operation

Default = ‘0’

0 - Normal stereo operation
1 - Output either left or right channel inputs into consecutive subframe outputs (Mono Mode, left or right is determined by MMTLR bit)

MMTCS - Select A or B channel status data to transmit in Mono Mode

Default = ‘0’

0 - Use channel A CS data for the A subframe and use channel B CS data for the B subframe
1 - Use the same CS data for both the A and B subframe outputs. If MMTLR = 0, use the left channel CS data. If MMTLR = 1, use the right channel CS data.

MMTLR - Channel Selection for AES Transmitter Mono Mode

Default = ‘0’

0 - Use left channel input data for consecutive subframe outputs
1- Use right channel input data for consecutive subframe outputs

8.4 Data Flow Control (03h)

7	6	5	4	3	2	1	0
0	TXOFF	AESBP	0	0	0	0	0

The Data Flow Control register configures the flow of audio data. The output data should be muted prior to changing bits in this register to avoid transients.

TXOFF - AES3 Transmitter Output Driver Control

Default = ‘0

0 - AES3 transmitter output pin drivers normal operation
1 - AES3 transmitter output pin drivers drive to 0 V.

AESBP - AES3 bypass mode selection

Default = ‘0’

0 - Normal operation
1 - Connect the AES3 transmitter driver input di rectly to the RXP pin, which becomes a normal TTL threshold digital input.

8.5 Clock Source Control (04h)

7	6	5	4	3	2	1	0
0	RUN	CLK1	CLK0	0	0	0	0

This register configures the clock sources of various blocks. In conjunction with the Data Flow Control register, various Receiver/Transmitter/Transceiver modes may be selected.

RUN - Controls the internal clocks, allowing the CS8406 to be placed in a “powered down” low current consumption, state.

Default = ‘0’

0 - Internal clocks are stopped. Internal state machines are reset. The fully static control port registers are operational, allowing registers to be read or changed. Reading and writing the U and C data buffers is not possible. Power consumption is low.
1 - Normal part operation. This bit must be set to 1 to allow the CS8406 to begin operation. All input clocks should be stable in frequency and phase when RUN is set to 1.

CLK1:0 - Output master clock (OMCK) input frequency to output sample rate (Fs) ratio selector. If these bits are changed during normal operation, always stop the CS8406 first (RUN = 0), write the new value, then start the CS8406 (RUN = 1).

Default = ‘00’

00 - OMCK frequency is 256*Fs
01 - OMCK frequency is 384*Fs
10 - OMCK frequency is 512*Fs
11 - OMCK frequency is 128*Fs

8.6 Serial Audio Input Port Data Format (05h)

7	6	5	4	3	2	1	0
SIMS	SISF	SIRES1	SIRES0	SIJUST	SIDEL	SISPOL	SILRPOL

SIMS - Master/Slave Mode Selector

Default = ‘0’

0 - Serial audio input port is in Slave Mode
1 - Serial audio input port is in Master Mode

SISF - ISCLK frequency (for Master Mode)

Default = ‘0’

0 - 64*Fs
1 - 128*Fs

SIRES1:0 - Resolution of the input data, for right-justified formats

Default = ‘00’

00 - 24-bit resolution
01 - 20-bit resolution
10 - 16-bit resolution
11 - Reserved

SIJUST - Justification of SDIN data relative to ILRCK

Default = ‘0’

0 - Left-justified
1 - Right-justified

SIDEL - Delay of SDIN data relative to ILRCK, for left-justified data formats

Default = ‘0’

0 - MSB of SDIN data occurs in the first ISCLK period after the ILRCK edge (Left-Justified Mode)
1 - MSB of SDIN data occurs in the second ISCLK period after the ILRCK edge (I^2S Mode)

SISPOL - ISCLK clock polarity

Default = ‘0’

0 - SDIN sampled on rising edges of ISCLK
1 - SDIN sampled on falling edges of ISCLK

SILRPOL - ILRCK clock polarity

Default = ‘0’

0 - SDIN data is for the left channel when ILRCK is high
1 - SDIN data is for the right channel when ILRCK is high

8.7 Interrupt 1 Status (07h) (Read Only)

7	6	5	4	3	2	1	0
TSLIP	0	0	0	0	0	EFTC	0

For all bits in this register, a ‘1’ means the associated interrupt condition has occurred at least once since the register was last read. A ‘0’ means the associated interrupt condition has NOT occurred since the last reading of the register. Reading the register resets all bits to ‘0’, unless the Interrupt Mode is set to level and the interrupt source is still true. Status bits that are masked off in the associated mask register will always be ‘0’ in this register. This register defaults to 00h.

TSLIP - AES3 transmitter source data slip interrupt

In data flows where OMCK, which clocks the AES3 transmitter, is asynchronous to the data source, this bit will go high every time a data sample is dropped or repeated. When TCBL is an input, this bit will go high on receipt of a new TCBL signal.

EFTC - E to F C-buffer transfer interrupt. The source for this bit is true during the E to F buffer transfer in the C bit buffer management process.

8.8 Interrupt 2 Status (08h) (Read Only)

7	6	5	4	3	2	1	0
0	0	0	0	0	EFTU	0	0

For all bits in this register, a ‘1’ means the associated interrupt condition has occurred at least once since the register was last read. A ‘0’ means the associated interrupt condition has NOT occurred since the last reading of the register. Reading the register resets all bits to ‘0’, unless the Interrupt Mode is set to level and the interrupt source is still true. Status bits that are masked off in the associated mask register will always be ‘0’ in this register. This register defaults to 00h.

EFTU - E to F U-buffer transfer interrupt. (Block Mode only) The source of this bit is true during the E to F buffer transfer in the U bit buffer management process.

8.9 Interrupt 1 Mask (09h)

7	6	5	4	3	2	1	0
TSLIPM	0	0	0	0	0	EFTCM	0

The bits of this register serve as a mask for the Interrupt 1 register. If a mask bit is set to 1, the error is unmasked, meaning that its occurrence will affect the INT pin and the status register. If a mask bit is set to 0, the error is masked, meaning that its occurrence will not affect the INT pin or the status register. The bit positions align with the corresponding bits in Interrupt 1 register. This register defaults to 00h.

8.10 Interrupt 1 Mode MSB (0Ah) and Interrupt 1 Mode LSB (0Bh)

7	6	5	4	3	2	1	0
TSLIP1	0	0	0	0	0	EFTC1	0
TSLIP0	0	0	0	0	0	EFTC0	0

The two Interrupt Mode registers form a 2-bit code for each Interrupt Register 1 function. There are three ways to set the INT pin active in accordance with the interrupt condition. In the Rising edge active mode, the INT pin becomes active on the arrival of the interrupt condition. In the Falling edge active mode, the INT pin becomes active on the removal of the interrupt condition. In Level active mode, the INT interrupt pin becomes active during the interrupt condition. Be aware that the active level (Active High or Low) only depends on the INT[1:0] bits. These registers default to 00.

00 - Rising edge active
01 - Falling edge active
10 - Level active
11 - Reserved

8.11 Interrupt 2 Mask (0Ch)

7	6	5	4	3	2	1	0
0	0	0	0	0	EFTUM	0	0

The bits of this register serve as a mask for the Interrupt 2 register. If a mask bit is set to 1, the error is unmasked, meaning that its occurrence will affect the INT pin and the status register. If a mask bit is set to 0, the error is masked, meaning that its occurrence will not affect the INT pin or the status register. The bit positions align with the corresponding bits in Interrupt 2 register. This register defaults to 00h.

8.12 Interrupt 2 Mode MSB (0Dh) and Interrupt Mode 2 LSB (0Eh)

7	6	5	4	3	2	1	0
0	0	0	0	0	EFTU1	0	0
0	0	0	0	0	EFTU0	0	0

The two Interrupt Mode registers form a 2-bit code for each Interrupt Register 1 function. There are three ways to set the INT pin active in accordance with the interrupt condition. In the Rising edge active mode, the INT pin becomes active on the arrival of the interrupt condition. In the Falling edge active mode, the INT pin becomes active on the removal of the interrupt condition. In Level active mode, the INT interrupt pin becomes active during the interrupt condition. Be aware that the active level (Active High or Low) only depends on the INT[1:0] bits. These registers default to 00.

00 - Rising edge active
01 - Falling edge active
10 - Level active
11 - Reserved

8.13 Channel Status Data Buffer Control (12h)

7	6	5	4	3	2	1	0
0	0	BSEL	0	0	EFTCI	CAM	0

BSEL - Selects the data buffer register addresses to contain User data or Channel Status data

Default = ‘0’

0 - Data buffer address space contains Channel Status data
1 - Data buffer address space contains User data

Note: There are separate complete buffers for the Channel Status and User bits. This control bit determines which buffer appears in the address space.

EFTCI - E to F C-data buffer transfer inhibit bit.

Default = ‘0’

0 - Allow C-data E to F buffer transfers
1 - Inhibit C-data E to F buffer transfers

CAM - C-data buffer control port access mode bit

Default = ‘0’

0 - One-Byte Mode
1 - Two-Byte Mode

8.14 User Data Buffer Control (13h)

7	6	5	4	3	2	1	0
0	0	0	UD	UBM1	UBM0	0	EFTUI

UD - User bit data source specifier

Default = ‘0’

0 - U Pin is the source of transmitted U data
1 - U data buffer is the source of transmitted U data

UBM1:0 - Sets the operating mode of the AES3 User bit manager

Default = ‘00’

00 - Transmit all zeros mode
01 - Block Mode
10 - Reserved
11 - Reserved

EFTUI - E to F U-data buffer transfer inhibit bit (valid in Block Mode only).

Default = ‘0’

0 - Allow U-data E to F buffer transfers
1 - Inhibit U-data E to F buffer transfers

8.15 Channel Status Bit or User Bit Data Buffer (20h - 37h)

Either the channel status data buffer E or the separate user bit data buffer E (provided UBM bits are set to Block Mode) is accessible through these register addresses.

8.16 CS8406 I.D. and Version Register (7Fh) (Read Only)

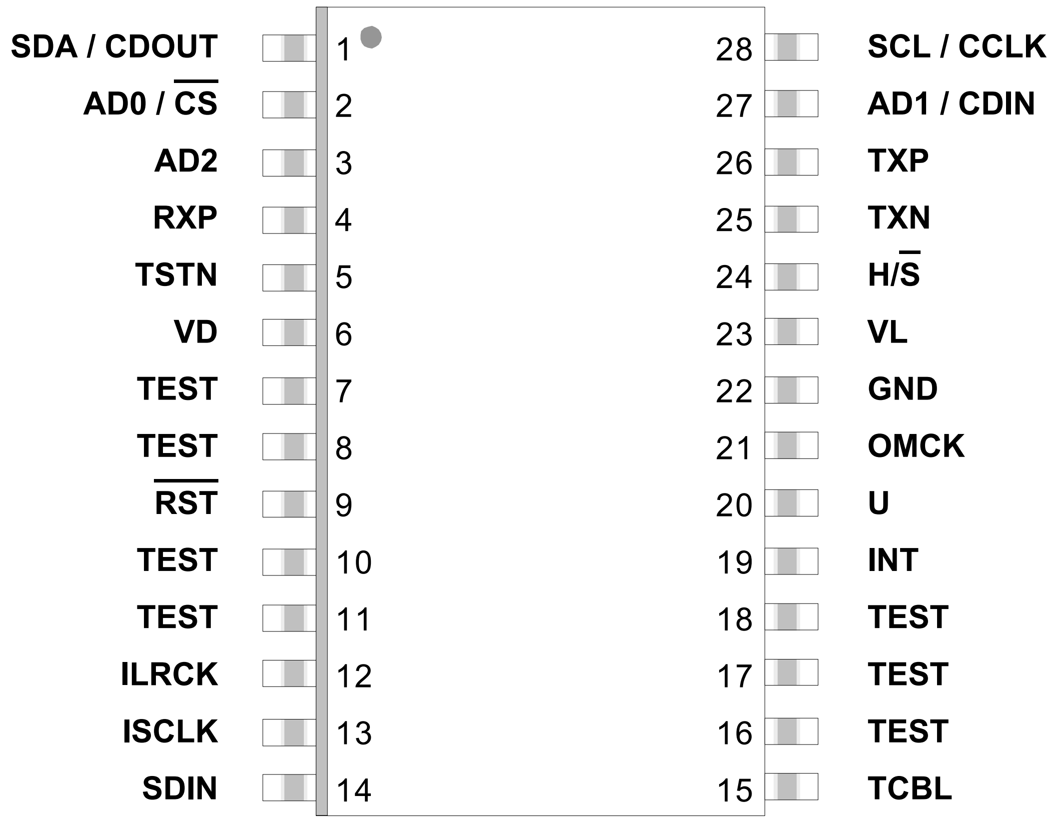
7	6	5	4	3	2	1	0
ID3	ID2	ID1	ID0	VER3	VER2	VER1	VER0

ID[3:0] - ID code for the CS8406. Permanently set to 1110

VER[3:0] = 0001 (revision A)

VER[3:0] = 0010 (revision B)

9. PIN DESCRIPTION - SOFTWARE MODE



VD	6	**Digital Power** (*Input*) - Digital core power supply. Typically +3.3 V or +5.0 V.
VL	23	**Logic Power** (*Input*) - Input/Output power supply. Typically +3.3 V or +5.0 V.
GND	22	**Ground** (*Input*) - Ground for I/O and core logic.
$\overline{RST}$	9	**Reset** (*Input*) - When $\overline{RST}$ is low, the CS8406 enters a low power mode and all internal states are reset. On initial power up, $\overline{RST}$ must be held low until the power supply is stable, and all input clocks are stable in frequency and phase. This is particularly true in Hardware Mode with multiple CS8406 devices, where synchronization between devices is important.
H/$\overline{S}$	24	**Hardware/Software Control Mode Select** (*Input*) -Determines the method of controlling the operation of the CS8406, and the method of accessing CS and U data. In Software Mode, device control and CS and U data access is primarily through the control port, using a microcontroller. To select Software Mode, this pin should be permanently tied to GND.
TXN **TXP**	25 26	**Differential Line Drivers** (*Output*) - These pins transmit biphase encoded data. The drivers are pulled low while the CS8406 is in the reset state.
OMCK	21	**Master Clock** (*Input*) - The frequency can be set through the control port registers.
ISCLK	13	**Serial Audio Bit Clock** (*Input/Output*) - Serial bit clock for audio data on the SDIN pin.
ILRCK	12	**Serial Audio Input Left/Right Clock** (*Input/Output*) - Word rate clock for the audio data on the SDIN pin.
SDIN	14	**Serial Audio Data Port** (*Input*) - Audio data serial input pin.