Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

CS8415A

96 kHz Digital Audio Interface Receiver

Features

- Complete EIAJ CP1201, IEC-60958, AES3, S/PDIF-compatible Receiver
- +5.0 V Analog Supply (VA+)
- +3.3 V or +5.0 V Digital Interface (VL+)
- 7:1 S/PDIF Input MUX
- Flexible 3-wire Serial Digital Output Port
- 8-kHz to 96-kHz Sample Frequency Range
- Low-jitter Clock Recovery
- Pin and Microcontroller Read Access to Channel Status and User Data
- Microcontroller and Standalone Modes
- Differential Cable Receiver
- On-chip Channel Status and User Data Buffer Memories
- Auto-detection of Compressed Audio Input Streams
- Decodes CD Q Sub-Code
- OMCK System Clock Mode

General Description

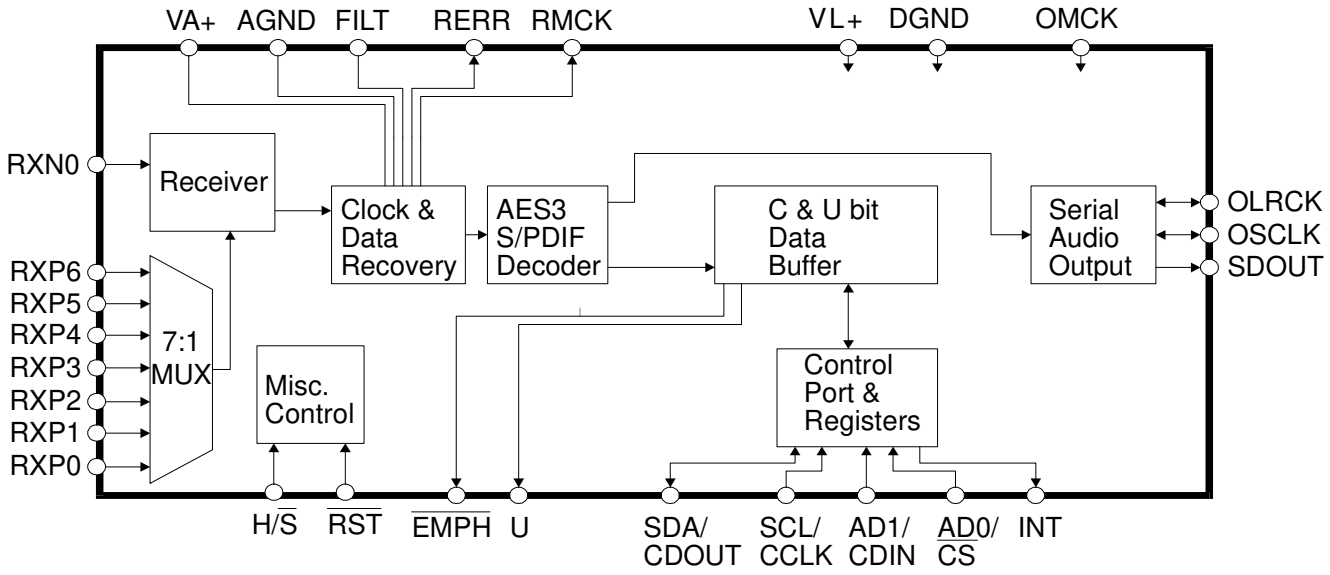
The CS8415A is a monolithic CMOS device which receives and decodes one of 7 channels of audio data according to the IEC60958, S/PDIF, EIAJ CP1201, or AES3. The CS8415A has a serial digital audio output port and comprehensive control ability through a 4-wire microcontroller port. Channel status and user data are assembled in block-sized buffers, making read access easy.

A low-jitter clock recovery mechanism yields a very clean recovered clock from the incoming AES3 stream.

Stand-alone operation allows systems with no microcontroller to operate the CS8415A with dedicated output pins for channel status data.

The CS8415A is available in a 28-pin TSSOP and SOIC package in both Commerical (-10 to +70°C) and Industrial grades (-40 to +85° C). The CDB8415A Customer Demonstration board is also available for device evaluation and implementation suggestions. Please refer to page 2 for ordering information.

Target applications include A/V receivers, CD-R, DVD receivers, multimedia speakers, digital mixing consoles, effects processors, set-top boxes, and computer and automotive audio systems.



ORDERING INFORMATION

Product	Description	Package	Grade	Temp Range	Pb-Free	Container	Order Number
CS8415A	96 kHz Digital Audio Interface Receiver	28-TSSOP	Commercial	-10 to +70°C	YES	Rail	CS8415A-CZZ
						Tape and Reel	CS8415A-CZZR
					NO	Rail	CS8415A-CZ
						Tape and Reel	CS8415A-CZR
			Industrial	-40 to +85°C	YES	Rail	CS8415A-IZZ
						Tape and Reel	CS8415A-IZZR
		28-SOIC	Commercial	-10 to +70°C	YES	Rail	CS8415A-CSZ
						Tape and Reel	CS8415A-CSZR
					NO	Rail	CS8415A-CS
						Tape and Reel	CS8415A-CSR
CDB8415A	CS8415A Evaluation Board		-	-	-	-	CDB8415A

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. CHARACTERISTICS AND SPECIFICATIONS

All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.

SPECIFIED OPERATING CONDITIONS

AGND, DGND = 0 V, all voltages with respect to 0 V.

Parameter		Symbol	Min	Typ	Max	Units
Power Supply Voltage (Note 1)		VA+ VL+	4.5 2.85	5.0 3.3 or 5.0	5.5 5.5	V V
Ambient Operating Temperature:	Commercial Grade Industrial Grade	T_A	-10 -40	- -	+70 +85	°C

Notes:

1. I²C protocol is supported only in VL+ = 5.0 V mode.

ABSOLUTE MAXIMUM RATINGS

AGND, DGND = 0 V; all voltages with respect to 0 V. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	VL+,VA+	-	6.0	V
Input Current, Any Pin Except Supplies (Note 2)	I_{in}	-	±10	mA
Input Voltage	V_{in}	-0.3	(VL+) + 0.3	V
Ambient Operating Temperature (power applied)	T_A	-55	125	°C
Storage Temperature	T_{stg}	-65	150	°C

2. Transient currents of up to 100 mA will not cause SCR latch-up.

DC ELECTRICAL CHARACTERISTICS

AGND = DGND = 0 V; all voltages with respect to 0 V.

Parameters		Symbol	Min	Typ	Max	Units
Power-down Mode (Note 3)						
Supply Current in power down	VA+ VL+ = 3.3 V VL+ = 5.0 V		- - -	20 60 60	- - -	µA µA µA
Normal Operation (Note 4)						
Supply Current at 48 kHz frame rate	VA+ VL+ = 3.3 V VL+ = 5.0 V		- - -	6.3 30.1 46.5	- - -	mA mA mA
Supply Current at 96 kHz frame rate	VA+ VL+ = 3.3 V VL+ = 5.0 V		- - -	6.6 44.8 76.6	- - -	mA mA mA

3. Power Down Mode is defined as $\overline{RST}$ = LO with all clocks and data lines held static.
4. Normal operation is defined as $\overline{RST}$ = HI.

DIGITAL INPUT CHARACTERISTICS

Parameters	Symbol	Min	Typ	Max	Units
Input Leakage Current	I_{in}	-	±1	±10	µA
Differential Input Voltage, RXP0 to RXN0	V_{TH}	-	200	-	mV

DIGITAL INTERFACE SPECIFICATIONS

AGND = DGND = 0 V; all voltages with respect to 0 V.

Parameters	Symbol	Min	Max	Units
High-Level Output Voltage (I_{OH} = -3.2 mA)	V_{OH}	(VL+) - 1.0	-	V
Low-Level Output Voltage (I_{OH} = 3.2 mA)	V_{OL}	-	0.4	V
High-Level Input Voltage, except RX_n	V_{IH}	2.0	(VL+) + 0.3	V
Low-Level Input Voltage, except RX_n (Note 5)	V_{IL}	-0.3	0.4/0.8	V

5. At 5.0 V mode, V_{IL} = 0.8 V (Max), at 3.3 V mode, V_{IL} =0.4 V (Max).

SWITCHING CHARACTERISTICS

Inputs: Logic 0 = 0 V, Logic 1 = VL+; C_L = 20 pF.

Parameter	Symbol	Min	Typ	Max	Units
$\overline{RST}$ pin Low Pulse Width		200	-	-	µs
PLL Clock Recovery Sample Rate Range		8.0	-	108.0	kHz
RMCK output jitter (Note 6)		-	200	-	ps RMS
RMCK output duty cycle		40	50	60	%

6. Cycle-to-cycle using 32 to 96 kHz external PLL filter components.

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORTS

Inputs: Logic 0 = 0 V, Logic 1 = VL+; C_L = 20 pF.

Parameter		Symbol	Min	Typ	Max	Units
OSCLK Active Edge to SDOUT Output Valid	(Note 7)	t_{dpd}	-	-	20	ns
Master Mode						
RMCK to OSCLK active edge delay	(Note 7)	t_{smd}	0	-	10	ns
RMCK to OLRCK delay	(Note 8)	t_{lmd}	0	-	10	ns
OSCLK and OLRCK Duty Cycle			-	50	-	%
Slave Mode						
OSCLK Period	(Note 9)	t_{sckw}	36	-	-	ns
OSCLK Input Low Width		t_{sckl}	14	-	-	ns
OSCLK Input High Width		t_{sckh}	14	-	-	ns
OSCLK Active Edge to OLRCK Edge	(Note 7, 8, 10)	t_{lrckd}	20	-	-	ns
OLRCK Edge Setup Before OSCLK Active Edge	Notes 7, 8, 11	t_{lrcks}	20	-	-	ns

7. The active edges of OSCLK are programmable.
8. The polarity OLRCK is programmable.
9. No more than 128 SCLK per frame.
10. This delay is to prevent the previous OSCLK edge from being interpreted as the first one after OLRCK has changed.
11. This setup time ensures that this OSCLK edge is interpreted as the first one after OLRCK has changed.

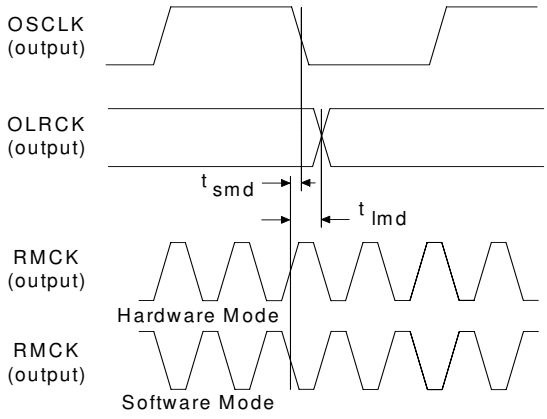


Figure 1. Audio Port Master Mode Timing

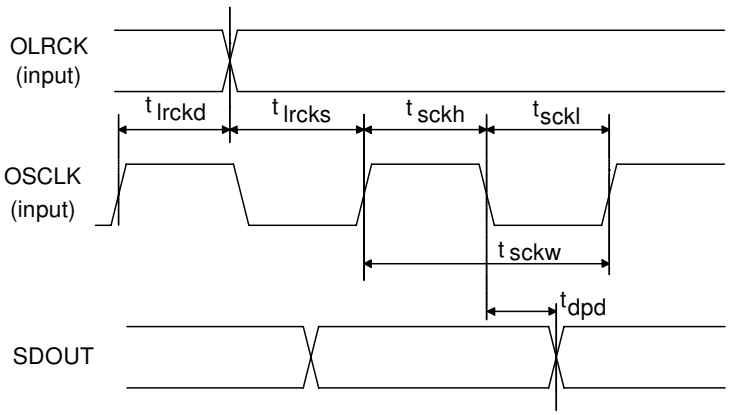


Figure 2. Audio Port Slave Mode and Data Input Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI MODE

Inputs: Logic 0 = 0 V, Logic 1 = VL+; C_L = 20 pF.

Parameter		Symbol	Min	Typ	Max	Units
CCLK Clock Frequency	(Note 12)	f_{sck}	0	-	6.0	MHz
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	-	ns
CCLK Low Time		t_{scl}	66	-	-	ns
CCLK High Time		t_{sch}	66	-	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	-	ns
CCLK Rising to DATA Hold Time	(Note 13)	t_{dh}	15	-	-	ns
CCLK Falling to CDOUT Stable		t_{pd}	-	-	50	ns
Rise Time of CDOUT		t_{r1}	-	-	25	ns
Fall Time of CDOUT		t_{f1}	-	-	25	ns
Rise Time of CCLK and CDIN	(Note 14)	t_{r2}	-	-	100	ns
Fall Time of CCLK and CDIN	(Note 14)	t_{f2}	-	-	100	ns

12. If Fs is lower than 46.875 kHz, the maximum CCLK frequency should be less than 128 Fs. This is dictated by the timing requirements necessary to access the Channel Status and User Bit buffer memory. Access to the control register file can be carried out at the full 6 MHz rate. The minimum allowable input sample rate is 8 kHz, so choosing CCLK to be less than or equal to 1.024 MHz should be safe for all possible conditions.
13. Data must be held for sufficient time to bridge the transition time of CCLK.
14. For f_{sck} <1 MHz.

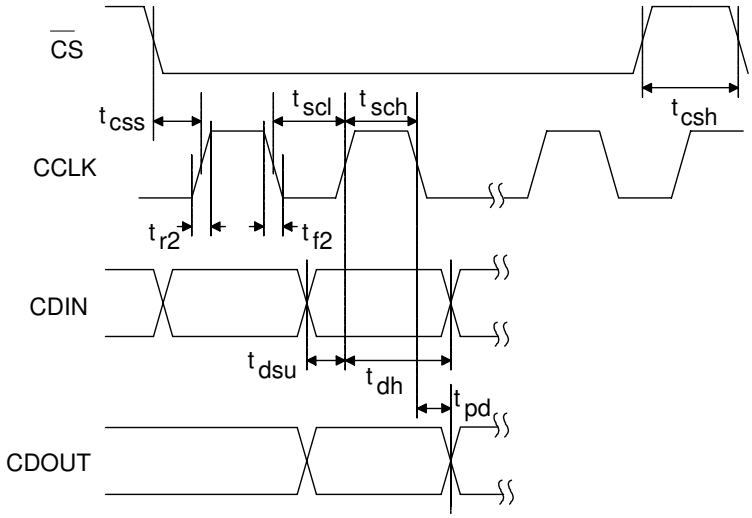


Figure 3. SPI Mode Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - I²C MODE

(Note 15), Inputs: Logic 0 = 0 V, Logic 1 = VL+; C_L = 20 pF.

Parameter	Symbol	Min	Typ	Max	Units
SCL Clock Frequency	fscl	-	-	100	kHz
Bus Free Time Between Transmissions	t_{buf}	4.7	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	-	µs
Clock Low Time	t_{low}	4.7	-	-	µs
Clock High Time	t_{high}	4.0	-	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	-	µs
SDA Hold Time from SCL Falling (Note 16)	t_{hdd}	0	-	-	µs
SDA Setup Time to SCL Rising	t_{sud}	250	-	-	ns
Rise Time of Both SDA and SCL Lines	t_r	-	-	25	ns
Fall Time of Both SDA and SCL Lines	t_f	-	-	25	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	-	µs

15. I²C protocol is supported only in VL+ = 5.0 V mode.

16. Data must be held for sufficient time to bridge the 25 ns transition time of SCL.

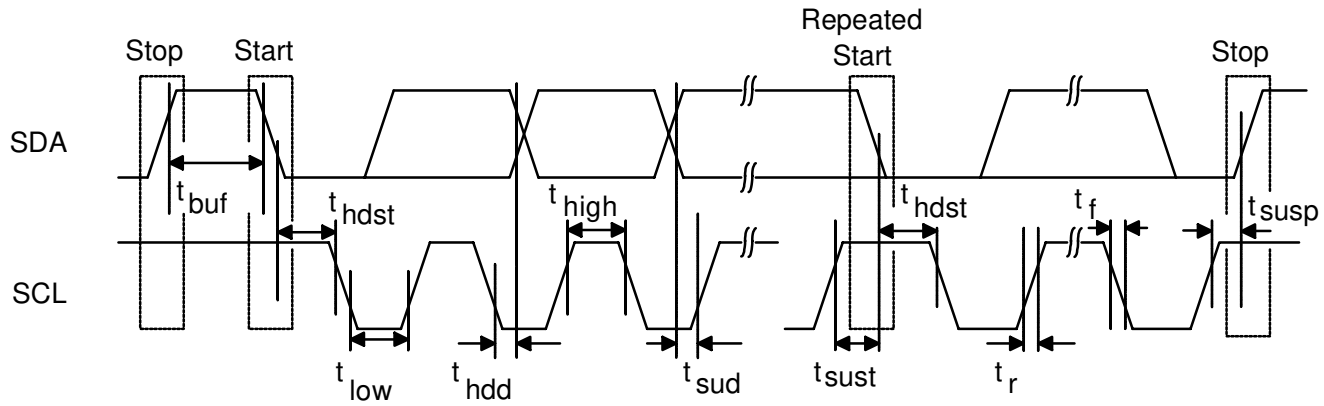
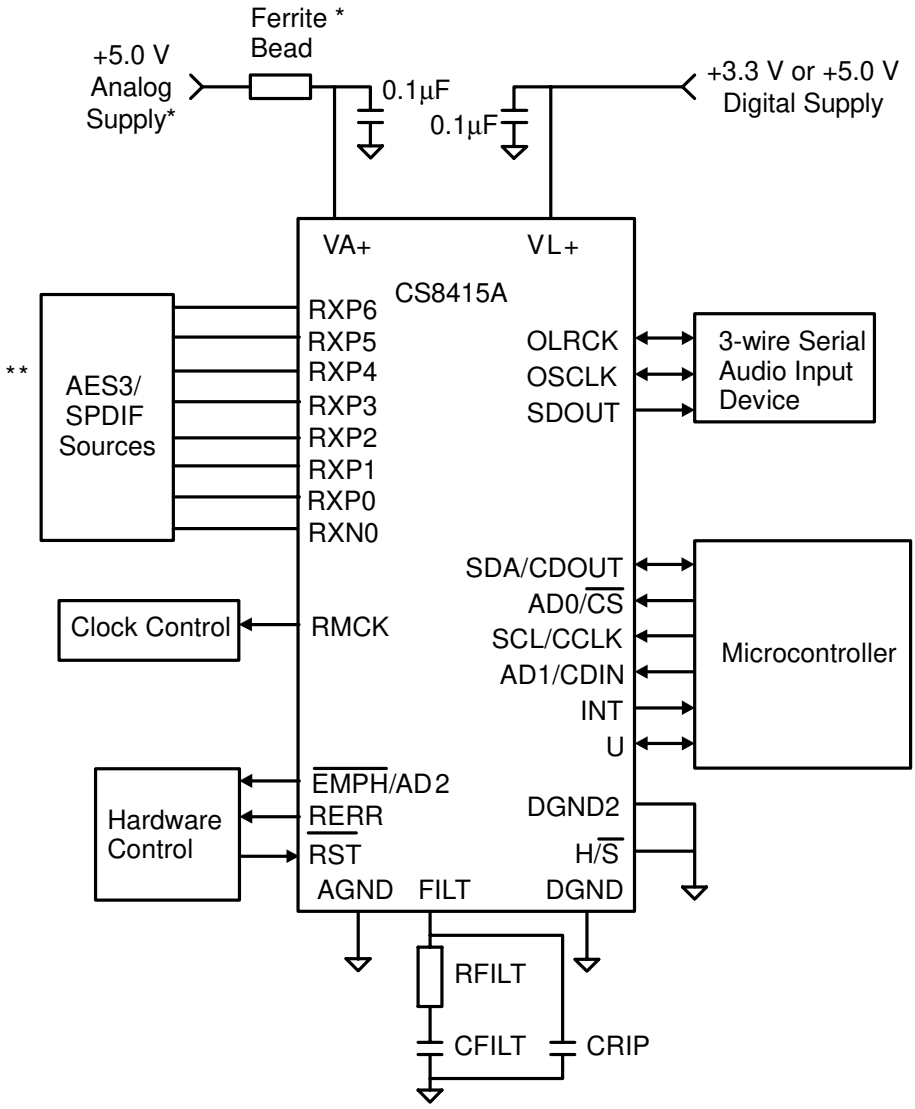


Figure 4. I²C Mode Timing

2. TYPICAL CONNECTION DIAGRAM



* A separate analog supply is only necessary in applications where RMCK is used for a jitter sensitive task. For applications where RMCK is not used for a jitter sensitive task, connect VA+ to VD+ via a ferrite bead. Keep the decoupling capacitor between VA+ and AGND.

** Please see section 5.1 "7:1 S/PDIF Input Multiplexer" and Appendix A for typical input configurations and recommended input circuits.

Figure 5. Recommended Connection Diagram for Software Mode

3. GENERAL DESCRIPTION

The CS8415A is a monolithic CMOS device which receives and decodes audio data according to the AES3, IEC60958, S/PDIF, and EIAJ CP1201 interface standards.

Input data is either differential or single-ended. A low-jitter clock is recovered from the incoming data using a PLL. The decoded audio data is output through a configurable, 3-wire output port. The channel status and user data are assembled in block-sized buffers and may be accessed through an SPI or I²C microcontroller port. For systems with no microcontroller, a stand-alone mode allows direct access to channel status and user data output pins.

Target applications include AVR, CD-R, DAT, DVD, multimedia speakers, MD and VTR equipment, mixing consoles, digital audio transmission and receiving equipment, high-quality D/A and A/D converters, effects processors, set-top boxes, and computer audio systems.

Figure 5 shows the supply and external connections to the CS8415A, when configured for operation with a microcontroller.

3.1 AES3 and S/PDIF Standards Documents

This data sheet assumes that the user is familiar with the AES3 and S/PDIF data formats. It is advisable to have current copies of the AES3 and IEC60958 specifications on hand for easy reference.

The latest AES3 standard is available from the Audio Engineering Society or ANSI at www.aes.org or www.ansi.org. Obtain the latest IEC60958 standard from ANSI or from the International Electrotechnical Commission at www.iec.ch. The latest EIAJ CP-1201 standard is available from the Japanese Electronics Bureau.

Cirrus Logic Application Note 22: *Overview of Digital Audio Interface Data Structures* contains a useful tutorial on digital audio specifications, but it should not be considered a substitute for the standards.

The paper *An Understanding and Implementation of the SCMS Serial Copy Management System for Digital Audio Transmission*, by Clifton Sanchez, is an excellent tutorial on SCMS. It is available from the AES as preprint 3518.

4. SERIAL AUDIO OUTPUT PORT

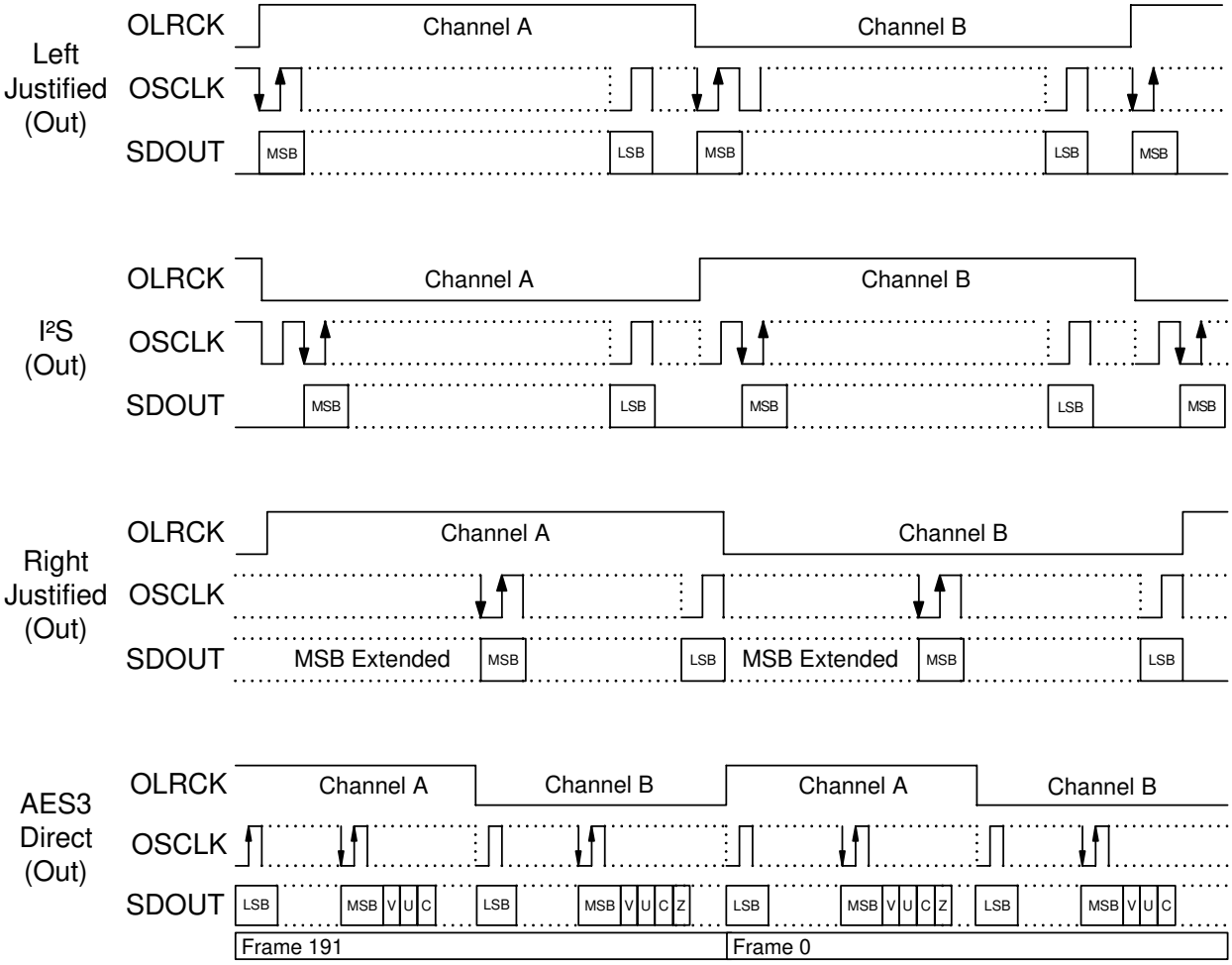
A 3-wire serial audio output port is provided. The port can be adjusted to suit the attached device setting the control registers. The following parameters are adjustable: master or slave, serial clock frequency, audio data resolution, left or right justification of the data relative to left/right clock, optional one-bit cell delay of the first data bit, the polarity of the bit clock, and the polarity of the left/right clock. By setting the appropriate control bits, many formats are possible.

Figure 6 shows the selection of common output formats including the control bit settings. It should be noted that in right-justified mode, the serial audio output data is "MSB extended". This means that in a sub-frame where the MSB of the data is '1', all bits preceding the MSB in the sub-frame will also be '1'. Conversely, in a sub-frame where the MSB of the data is '0', all bits preceding the MSB in the sub-frame will also be '0'.

A special AES3 direct output format is included, which allows the serial output port access to the V, U, and C bits embedded in the serial audio data stream. The P bit is replaced by a Z bit that marks the subframe just prior to the start of each block. The received channel status block start signal is only available in hardware mode, as the RCBL pin.

In master mode, the left/right clock and the serial bit clock are outputs, derived from the recovered RMCK clock. In slave mode, the left/right clock and the serial bit clock are inputs. The left/right clock must be synchronous to the appropriate master clock, but the serial bit clock can be asynchronous and discontinuous if required. By appropriate phasing of the left/right clock and control of the serial clocks, multiple CS8415As can share one serial port. The left/right clock should be continuous, but the duty cycle can be less than the specified typical value of 50% if enough serial clocks are present in each phase to clock all the data bits. When in slave mode, the serial audio output port must not be set for right-justified data. When using the serial audio output port in slave mode with an OLRCK input which is asynchronous to the incoming AES3 data, an interrupt bit (OSLIP) is provided to indicate

when repeated or dropped samples occur. The CS8415A allows immediate mute of the serial audio output port audio data by the MUTESAO bit of Control Register 1.



	SOMS*	SOSF*	SORES[1:0]*	SOJUST*	SODEL*	SOSPOL*	SOLRPOL*
Left Justified	X	X	XX	0	0	0	0
I²S	X	X	XX	0	1	0	1
Right Justified	1	X	XX	1	0	0	0
AES3 Direct	X	X	11	0	0	0	0

X = don't care to match format, but does need to be set to the desired setting

* See Serial Output Data Format Register Bit Descriptions for an explanation of the meaning of each bit

Figure 6. Serial Audio Output Example Formats

5. AES3 RECEIVER

The CS8415A includes an AES3 digital audio receiver. A comprehensive buffering scheme provides read access to the channel status and user data. This buffering scheme is described in Appendix B.

The AES3 receiver accepts and decodes audio and digital data according to the AES3, IEC60958 (S/PDIF), and EIAJ CP-1201 interface standards. The receiver consists of a differential input stage, driven through pins RXP0 and RXN0, a PLL-based clock recovery circuit, and a decoder which separates the audio data from the channel status and user data.

External components are used to terminate and isolate the incoming data cables from the CS8415A. These components are detailed in Appendix A.

5.1 7:1 S/PDIF Input Multiplexer

The CS8415A employs a 7:1 S/PDIF Input Multiplexer to accommodate up to seven channels of input digital audio data. Digital audio data is single-ended and input through the RXP[0:6] pins. When any portion of the multiplexer is implemented, unused RXP pins should be tied to ground, and RXN0 must be AC-coupled to ground. The multiplexer select line control is accessed through bits MUX[2:0] in the Control 2 register. The multiplexer defaults to RXP0. Therefore, the default configuration is for a differential signal to be input through RXP0 & RXN0. Please see Appendix A for recommended input circuits.

5.2 OMCK System Clock Mode

A special clock switching mode is available that allows the clock that is input through the OMCK pin to be output through the RMCK pin. This feature is controlled by the SWCLK bit in register 1 of the control registers. When the PLL loses lock, the frequency of the VCO drops to 300 kHz. The clock switching mode allows the clock input through OMCK to be used as a clock in the system without any disruption when the PLL loses lock. For example, when the input is removed from the receiver. When SWCLK is enabled and this mode is implemented, RMCK is an output and is not bi-directional. This clock switching is performed glitch-free. Please note that internal circuitry associated with RMCK is not driven by OMCK. This means that OSCLK and OLRCK continue to be derived from the PLL and are not usable in this mode. This function is available only in software mode.

5.3 PLL, Jitter Attenuation, and Varispeed

Please see Appendix C for general description of the PLL, selection of recommended PLL filter components, and layout considerations. Figure 5 shows the recommended configuration of the two capacitors and one resistor that comprise the PLL filter.

5.4 Error Reporting and Hold Function

While decoding the incoming AES3 data stream, the CS8415A can identify several kinds of error, indicated in the Receiver Error register. The UNLOCK bit indicates whether the PLL is locked to the incoming AES3 data. The V bit reflects the current validity bit status. The CONF (confidence) bit is the logical OR of BIP and UNLOCK. The BIP (bi-phase) error bit indicates an error in incoming bi-phase coding. The PAR (parity) bit indicates a received parity error.

The error bits are "sticky" - they are set on the first occurrence of the associated error and will remain set until the user reads the register through the control port. This enables the register to log all unmasked errors that occurred since the last time the register was read.

The Receiver Error Mask register allows masking of individual errors. The bits in this register serve as masks for the corresponding bits of the Receiver Error Register. If a mask bit is set to 1, the error is unmasked, which implies the following: its occurrence will be reported in the receiver error register, induce a

pulse on RERR, invoke the occurrence of a RERR interrupt, and affect the current audio sample according to the status of the HOLD bits. The HOLD bits allow a choice of holding the previous sample, replacing the current sample with zero (mute), or not changing the current audio sample. If a mask bit is set to 0, the error is masked, which implies the following: its occurrence will not be reported in the receiver error register, will not induce a pulse on RERR or generate a RERR interrupt, and will not affect the current audio sample. The QCRC and CCRC errors do not affect the current audio sample, even if unmasked.

5.5 Channel Status Data Handling

The first 2 bytes of the Channel Status block are decoded into the Receiver Channel Status register. The setting of the CHS bit in the Channel Status Data Buffer Control register determines whether the channel status decodes are from the A channel (CHS = 0) or B channel (CHS = 1).

The PRO (professional) bit is extracted directly. For consumer data, the COPY (copyright) bit is extracted, and the category code and L bits are decoded to determine SCMS status, indicated by the ORIG (original) bit. If the category code is set to General on the incoming AES3 stream, copyright will always be indicated even when the stream indicates no copyright. Finally, the $\overline{\text{AUDIO}}$ bit is extracted and used to set an $\overline{\text{AUDIO}}$ indicator, as described in the Non-audio Auto-detection section below.

If 50/15 µs pre-emphasis is detected, the state of the $\overline{\text{EMPH}}$ pin is adjusted accordingly.

The encoded channel status bits which indicate sample word length are decoded according to AES3-1992 or IEC 60958. Audio data routed to the serial audio output port is unaffected by the word length settings and all 24 bits are passed on as received.

Appendix A describes the overall handling of Channel Status and User data.

5.6 User Data Handling

The incoming user data is buffered in a user accessible buffer. Received user data may also be output to the U pin under the control of a control register bit. Depending on the clocking options selected, there may not be a clock available to qualify the U data output. Figure 7 illustrates the timing. If the incoming user data bits have been encoded as Q-channel subcode, the data is decoded and presented in 10 consecutive register locations. An interrupt may be enabled to indicate the decoding of a new Q-channel block, which may be read through the control port.

5.7 Non-Audio Auto-Detection

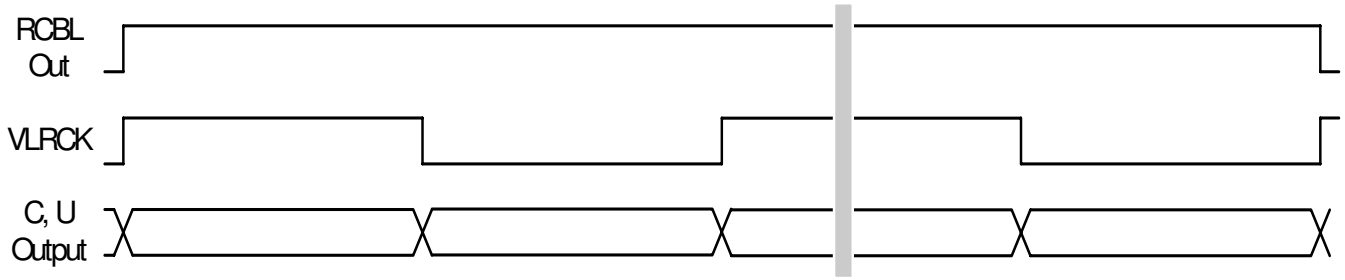
An AES3 data stream may be used to convey non-audio data, thus it is important to know whether the incoming AES3 data stream is digital audio or not. This information is typically conveyed in channel status bit 1 ($\overline{\text{AUDIO}}$), which is extracted automatically by the CS8415A. However, certain non-audio sources, such as AC-3® or MPEG encoders, may not adhere to this convention, and the bit may not be properly set. The CS8415A AES3 receiver can detect such non-audio data. This is accomplished by looking for a 96-bit sync code, consisting of 0x0000, 0x0000, 0x0000, 0x0000, 0xF872, and 0x4E1F. When the sync code is detected, an internal AUTODETECT signal will be asserted. If no additional sync codes are detected within the next 4096 frames, AUTODETECT will be de-asserted until another sync code is detected. The $\overline{\text{AUDIO}}$ bit in the Receiver Channel Status register is the logical OR of AUTODETECT and the received channel status bit 1. If non-audio data is detected, the data is still processed exactly as if it were normal audio. It is up to the user to mute the outputs as required.

5.8 Mono Mode Operation

An AES3 stream may be used in more than one way to transmit 96 kHz sample rate data. One method is to double the frame rate of the current format. This results in a stereo signal with a sample rate of 96 kHz, carried over a single twisted pair cable. An alternate method is implemented using the 2 sub-frames in a 48-kHz frame rate AES3 signal to carry consecutive samples of a mono signal, resulting in a 96-kHz sample rate stream. This allows older equipment, whose AES3 transmitters and receivers are not rated for 96-kHz frame rate operation, to handle 96-kHz sample rate information. In this “mono mode”, 2 AES3 cables are needed for stereo data transfer. The CS8415A offers mono mode operation, controlled through the MMR control register bit.

The receiver mono mode effectively doubles Fs compared to the input frame rate. The clock output on the RMCK pin tracks Fs, and so is doubled in frequency compared to stereo mode. The receiver will run at a frame rate of Fs/2, and the serial audio output port will run at Fs. Sub-frame A data will be routed to both the left and right data fields on SDOUT. Similarly, sub-frame B data will be routed to both the left and right data fields of the next word clock cycle of SDOUT.

Using mono mode is only necessary if the serial audio output port must run at 96 kHz. If the CS8415A is kept in normal stereo mode, and receives AES3 data arranged in mono mode, then the serial audio output port will run at 48 kHz, with left and right data fields representing consecutive audio samples.



- RCBL and C output are only available in hardware mode.
- RCBL goes high 2 frames after receipt of a Z preamble, and is high for 16 frames.
- VLRCK is a virtual word clock, which may not exist, but is used to illustrate the C/U timing.
- VLRCK duty cycle is 50%. VLRCK frequency is always equal to the incoming frame rate.
- If the serial audio output port is in master mode, VLRCK = OLRCK
- If the serial audio output port is in slave mode, then VLRCK needs to be externally created, if required.
- C and U transitions are aligned within ± 1% of VLRCK period to VLRCK edges.

Figure 7. AES3 ReceiverTiming for C & U Pin Output Data

6. CONTROL PORT DESCRIPTION AND TIMING

The control port is used to access the registers, allowing the CS8415A to be configured for the desired operational modes and formats. In addition, Channel Status and User data may be read through the control port. The operation of the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has 2 modes: SPI and I²C, with the CS8415A acting as a slave device. SPI mode is selected if there is a high-to-low transition on the AD0/$\overline{CS}$ pin, after the $\overline{RST}$ pin has been brought high. I²C mode is selected by connecting the AD0/$\overline{CS}$ pin to VL+ or DGND, thereby permanently selecting the desired AD0 bit address state.

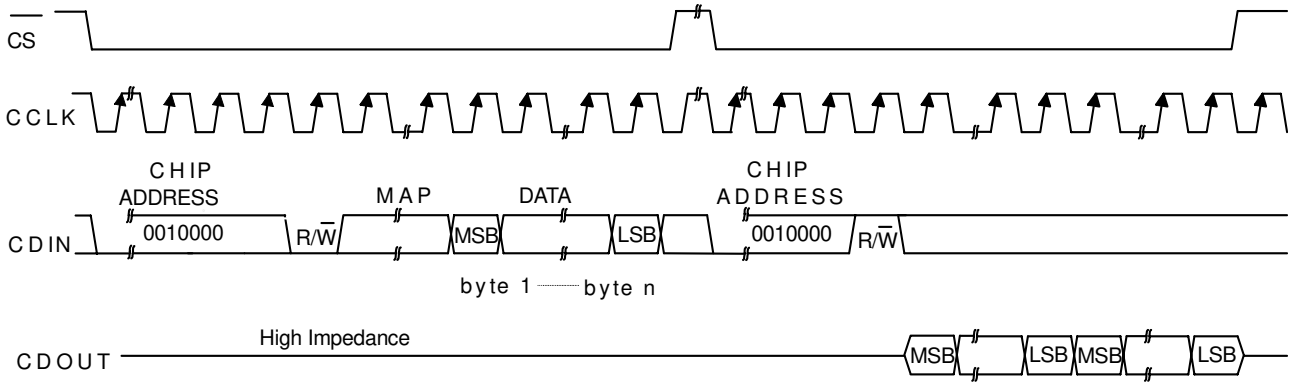
6.1 SPI™ Mode

In SPI mode, $\overline{CS}$ is the CS8415A chip select signal, CCLK is the control port bit clock (input into the CS8415A from the microcontroller), CDIN is the input data line from the microcontroller, CDOUT is the output data line to the microcontroller. Data is clocked in on the rising edge of CCLK and out on the falling edge.

Figure 8 shows the operation of the control port in SPI mode. To write to a register, bring $\overline{CS}$ low. The first seven bits on CDIN form the chip address and must be 0010000b. The eighth bit is a read/write indicator (R/$\overline{W}$), which should be low to write. The next eight bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data which will be placed into the register designated by the MAP. During writes, the CDOUT output stays in the Hi-Z state. It may be externally pulled high or low with a 47 kΩ resistor, if desired.

There is a MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, the MAP will stay constant for successive read or writes. If INCR is set to a 1, the MAP will autoincrement after each byte is read or written, allowing block reads or writes of successive registers.

To read a register, the MAP has to be set to the correct address by executing a partial write cycle which finishes ($\overline{CS}$ high) immediately after the MAP byte. The MAP auto increment bit (INCR) may be set or not, as desired. To begin a read, bring $\overline{CS}$ low, send out the chip address and set the read/write bit (R/$\overline{W}$) high. The next falling edge of CCLK will clock out the MSB of the addressed register (CDOUT will leave the high impedance state). If the MAP auto increment bit is set to 1, the data for successive registers will appear consecutively.



MAP = Memory Address Pointer, 8 bits, MSB first

Figure 8. Control Port Timing in SPI Mode

6.2 I²C Mode

In I²C mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL, with the clock to data relationship as shown in Figure 9. There is no $\overline{CS}$ pin. Each individual CS8415A is given a unique address. Pins AD0 and AD1 form the two least significant bits of the chip address and should be connected to VL+ or DGND as desired. The $\overline{EMPH}$ pin is used to set the AD2 bit by connecting a resistor from the $\overline{EMPH}$ pin to VL+ or to DGND. The state of the pin is sensed while the CS8415A is being reset. The upper 4 bits of the 7-bit address field are fixed at 0010b. To communicate with a CS8415A, the chip address field, which is the first byte sent to the CS8415A, should match 0010b followed by the settings of the $\overline{EMPH}$, AD1, and AD0. The eighth bit of the address is the R/$\overline{W}$ bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS8415A after each input byte is read, and is input to the CS8415A from the microcontroller after each transmitted byte. I²C mode is supported only with VL+ in 5V mode.

6.3 Interrupts

The CS8415A has a comprehensive interrupt capability. The INT output pin is intended to drive the interrupt input pin on the host microcontroller. The INT pin may be set to be active-low, active-high or active-low with no active pull-up transistor. This last mode is used for active-low, wired-OR hook-ups, with multiple peripherals connected to the microcontroller interrupt input pin.

Many conditions can cause an interrupt, as listed in the interrupt status register descriptions. Each source may be masked off through mask register bits. In addition, each source may be set to rising edge, falling edge, or level-sensitive. Combined with the option of level-sensitive or edge-sensitive modes within the microcontroller, many different configurations are possible, depending on the needs of the equipment designer.

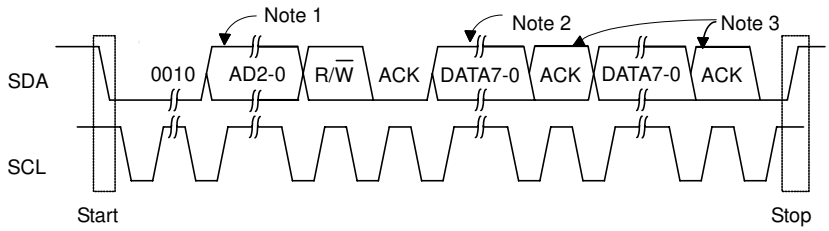


Figure 9. Control Port Timing in I²C Mode

Notes:

1. AD2 is derived from a resistor attached to the $\overline{EMPH}$ pin.
   AD1 and AD0 are determined by the state of the corresponding pins.
2. If operation is a write, this byte contains the Memory Address Pointer, MAP.
3. If operation is a read, the last bit of the read should be NACK (high).

7. CONTROL PORT REGISTER SUMMARY

Addr (HEX)	Function	7	6	5	4	3	2	1	0
01	Control 1	SWCLK	0	MUTESAO	0	0	INT1	INT0	0
02	Control 2	0	HOLD1	HOLD0	RMCKF	MMR	MUX2	MUX1	MUX0
04	Clock Source Control	0	RUN	0	0	0	0	0	0
06	Serial Output Format	SOMS	SOSF	SORES1	SORES0	SOJUST	SODEL	SOSPOL	SOLRPOL
07	Interrupt 1 Status	0	OSLIP	0	0	0	DETC	0	RERR
08	Interrupt 2 Status	0	0	0	0	DETU	0	QCH	0
09	Interrupt 1 Mask	0	OSLIPM	0	0	0	DETCM	0	RERRM
0A	Interrupt 1 Mode (MSB)	0	OSLIP1	0	0	0	DETC1	0	RERR1
0B	Interrupt 1 Mode (LSB)	0	OSLIP0	0	0	0	DETC0	0	RERR0
0C	Interrupt 2 Mask	0	0	0	0	DETUM	0	QCHM	0
0D	Interrupt 2 Mode (MSB)	0	0	0	0	DETU1	0	QCH1	0
0E	Interrupt 2 Mode (LSB)	0	0	0	0	DETU0	0	QCH0	0
0F	Receiver CS Data	AUX3	AUX2	AUX1	AUX0	PRO	$\overline{\text{AUDIO}}$	COPY	ORIG
10	Receiver Errors	0	QCRC	CCRC	UNLOCK	V	CONF	BIP	PAR
11	Receiver Error Mask	0	QCRCM	CCRCM	UNLOCKM	VM	CONFM	BIPM	PARM
12	CS Data Buffer Control	0	0	BSEL	CBMR	DETCI	0	CAM	CHS
13	U Data Buffer Control	0	0	0	0	0	0	DETUI	0
14-1D	Q sub-code Data								
1E	OMCK/RMCK Ratio	ORR7	ORR6	ORR5	ORR4	ORR3	ORR2	ORR1	ORR0
20-37	C or U Data Buffer								
7F	ID and Version	ID3	ID2	ID1	ID0	VER3	VER2	VER1	VER0

Table 1. Control Register Map Summary

7.1 Memory Address Pointer (MAP)

7	6	5	4	3	2	1	0
INCR	MAP6	MAP5	MAP4	MAP3	MAP2	MAP1	MAP0

INCR - Auto Increment Address Control Bit

Default = ‘0’

0 - Disabled
1 - Enabled

MAP6:MAP0 - Register address

Note: Reserved registers must not be written to during normal operation. Some reserved registers are used for test modes, which can completely alter the normal operation of the CS8415A.

8. CONTROL PORT REGISTER BIT DEFINITIONS

8.1 Control 1 (01h)

7	6	5	4	3	2	1	0
SWCLK	0	MUTESAO	0	0	INT1	INT0	0

SWCLK - Controls output of OMCK on RMCK when PLL loses lock

Default = '0'

0 - RMCK default function
1 - OMCK output on RMCK pin

MUTESAO - Mute control for the serial audio output port

Default = '0'

0 - Disabled
1 - Enabled

INT1:0 - Interrupt output pin (INT) control

Default = '00'

00 - Active high; high output indicates interrupt condition has occurred
01 - Active low, low output indicates an interrupt condition has occurred
10 - Open drain, active low. Requires an external pull-up resistor on the INT pin.
11 - Reserved

8.2 Control 2 (02h)

7	6	5	4	3	2	1	0
0	HOLD1	HOLD0	RMCKF	MMR	MUX2	MUX1	MUX0

HOLD1:0 - Determine how received audio sample is affected when a receiver error occurs

Default = '00'

00 - Hold the last valid audio sample
01 - Replace the current audio sample with 00 (mute)
10 - Do not change the received audio sample
11 - Reserved

RMCKF - Select recovered master clock output pin frequency.

Default = '0'

0 - RMCK is equal to 256 * Fs
1 - RMCK is equal to 128 * Fs

MMR - Select AES3 receiver mono or stereo operation

Default = '0'

0 - Normal stereo operation
1 - A and B subframes treated as consecutive samples of one channel of data.
Data is duplicated to both left and right parallel outputs of the AES receiver block.
The sample rate (Fs) is doubled compared to MMR=0

MUX2:0 - 7:1 S/PDIF Input Multiplexer Select Line Control

Default = '000'

000 - RXP0
001 - RXP1
010 - RXP2
011 - RXP3
100 - RXP4
101 - RXP5
110 - RXP6
111 - Reserved

8.3 Clock Source Control (04h)

7	6	5	4	3	2	1	0
0	RUN	0	0	0	0	0	0

This register configures the clock sources of various blocks. In conjunction with the Data Flow Control register, various Receiver/Transmitter/Transceiver modes may be selected.

RUN - Controls the internal clocks, allowing the CS8415A to be placed in a "powered down", low current consumption, state.

Default = '0'

0 - Internal clocks are stopped. Internal state machines are reset. The fully static control port is operational, allowing registers to be read or changed. Reading and writing the U and C data buffers is not possible. Power consumption is low.

1 - Normal part operation. This bit must be written to the 1 state to allow the CS8415A to begin operation. All input clocks should be stable in frequency and phase when RUN is set to 1.

8.4 Serial Audio Output Port Data Format (06h)

7	6	5	4	3	2	1	0
SOMS	SOSF	SORES1	SORES0	SOJUST	SODEL	SOSPOL	SOLRPOL

SOMS - Master/Slave Mode Selector

Default = '0'

0 - Serial audio output port is in slave mode
1 - Serial audio output port is in master mode

SOSF - OSCLK frequency (for master mode)

Default = '0'

0 - 64*Fs
1 - 128*Fs

SORES1:0 - Resolution of the output data on SDOUT

Default = '00'

00 - 24-bit resolution
01 - 20-bit resolution
10 - 16-bit resolution
11 - Direct copy of the received NRZ data from the AES3 receiver (including C, U, and V bits, the time slot

normally occupied by the P bit is used to indicate the location of the block start, SDOUT pin only, serial audio output port clock must be derived from the AES3 receiver recovered clock)

SOJUST - Justification of SDOUT data relative to OLRCK

Default = '0'

0 - Left-justified
1 - Right-justified (master mode only)

SODEL - Delay of SDOUT data relative to OLRCK, for left-justified data formats

Default = '0'

0 - MSB of SDOUT data occurs in the first OSCLK period after the OLRCK edge
1 - MSB of SDOUT data occurs in the second OSCLK period after the OLRCK edge

SOSPOL - OSCLK clock polarity

Default = '0'

0 - SDOUT sampled on rising edges of OSCLK
1 - SDOUT sampled on falling edges of OSCLK

SOLRPOL - OLRCK clock polarity

Default = '0'

0 - SDOUT data is for the left channel when OLRCK is high
1 - SDOUT data is for the right channel when OLRCK is high

8.5 Interrupt 1 Status (07h) (Read Only)

7	6	5	4	3	2	1	0
0	OSLIP	0	0	0	DETC	0	RERR

For all bits in this register, a "1" means the associated interrupt condition has occurred at least once since the register was last read. A "0" means the associated interrupt condition has NOT occurred since the last reading of the register. Reading the register resets all bits to 0, unless the interrupt mode is set to level and the interrupt source is still true. Status bits that are masked off in the associated mask register will always be "0" in this register. This register defaults to 00h.

OSLIP - Serial audio output port data slip interrupt

When the serial audio output port is in slave mode, and OLRCK is asynchronous to the port data source, This bit will go high every time a data sample is dropped or repeated.

DETC - D to E C-buffer transfer interrupt.

Indicates the completion of a D to E C-buffer transfer. See "Channel Status and User Data Buffer Management" on page 38 for more information.

RERR - A receiver error has occurred.

The Receiver Error register may be read to determine the nature of the error which caused the interrupt.

8.6 Interrupt 2 Status (08h) (Read Only)

7	6	5	4	3	2	1	0
0	0	0	0	DETU	0	QCH	0

For all bits in this register, a “1” means the associated interrupt condition has occurred at least once since the register was last read. A ”0” means the associated interrupt condition has NOT occurred since the last reading of the register. Reading the register resets all bits to 0, unless the interrupt mode is set to level and the interrupt source is still true. Status bits that are masked off in the associated mask register will always be “0” in this register. This register defaults to 00h.

DETU - D to E U-buffer transfer interrupt.

Indicates the completion of a D to E U-buffer transfer. See “Channel Status and User Data Buffer Management” on page 38 for more information.

QCH - A new block of Q-subcode data is available for reading.

The data must be completely read within 588 AES3 frames after the interrupt occurs to avoid corruption of the data by the next block.

8.7 Interrupt 1 Mask (09h)

7	6	5	4	3	2	1	0
0	OSLIPM	0	0	0	DETCM	0	RERRM

The bits of this register serve as a mask for the Interrupt 1 register. If a mask bit is set to 1, the error is unmasked, meaning that its occurrence will affect the INT pin and the status register. If a mask bit is set to 0, the error is masked, meaning that its occurrence will not affect the INT pin or the status register. The bit positions align with the corresponding bits in Interrupt 1 register. This register defaults to 00h.

8.8 Interrupt 1 Mode MSB (0Ah) and Interrupt 1 Mode LSB (0Bh)

7	6	5	4	3	2	1	0
0	OSLIP1	0	0	0	DETC1	0	RERR1
0	OSLIP0	0	0	0	DETC0	0	RERR0

The two Interrupt Mode registers form a 2-bit code for each Interrupt Register 1 function. There are three ways to set the INT pin active in accordance with the interrupt condition. In the Rising edge active mode, the INT pin becomes active on the arrival of the interrupt condition. In the Falling edge active mode, the INT pin becomes active on the removal of the interrupt condition. In Level active mode, the INT interrupt pin becomes active during the interrupt condition. Be aware that the active level (Actice High or Low) only depends on the INT[1:0] bits. These registers default to 00.

00 - Rising edge active
01 - Falling edge active
10 - Level active
11 - Reserved

8.9 Interrupt 2 Mask (0Ch)

7	6	5	4	3	2	1	0
0	0	0	0	DETUM	0	QCHM	0

The bits of this register serve as a mask for the Interrupt 2 register. If a mask bit is set to 1, the error is unmasked, meaning that its occurrence will affect the INT pin and the status register. If a mask bit is set to 0, the error is masked, meaning that its occurrence will not affect the INT pin or the status register. The bit positions align with the corresponding bits in Interrupt 2 register. This register defaults to 00h.

8.10 Interrupt 2 Mode MSB (0Dh) and Interrupt 2 Mode LSB (0Eh)

7	6	5	4	3	2	1	0
0	0	0	0	DETU1	0	QCH1	0
0	0	0	0	DETU0	0	QCH0	0

The two Interrupt Mode registers form a 2-bit code for each Interrupt Register 1 function. There are three ways to set the INT pin active in accordance with the interrupt condition. In the Rising edge active mode, the INT pin becomes active on the arrival of the interrupt condition. In the Falling edge active mode, the INT pin becomes active on the removal of the interrupt condition. In Level active mode, the INT interrupt pin becomes active during the interrupt condition. Be aware that the active level (Actice High or Low) only depends on the INT[1:0] bits. These registers default to 00.

00 - Rising edge active
01 - Falling edge active
10 - Level active
11 - Reserved

8.11 Receiver Channel Status (0Fh) (Read Only)

7	6	5	4	3	2	1	0
AUX3	AUX2	AUX1	AUX0	PRO	$\overline{\text{AUDIO}}$	COPY	ORIG

The bits in this register can be associated with either channel A or B of the received data. The desired channel is selected with the CHS bit of the Channel Status Data Buffer Control Register.

AUX3:0 - Incoming auxiliary data field width, as indicated by the incoming channel status bits, decoded according to IEC60958 and AES3.

0000 - Auxiliary data is not present
0001 - Auxiliary data is 1 bit long
0010 - Auxiliary data is 2 bits long
0011 - Auxiliary data is 3 bits long
0100 - Auxiliary data is 4 bits long
0101 - Auxiliary data is 5 bits long
0110 - Auxiliary data is 6 bits long
0111 - Auxiliary data is 7 bits long
1000 - Auxiliary data is 8 bits long
1001 - 1111 Reserved

PRO - Channel status block format indicator

0 - Received channel status block is in consumer format
1 - Received channel status block is in professional format

$\overline{\text{AUDIO}}$ - Audio indicator

0 - Received data is linearly coded PCM audio
1 - Received data is not linearly coded PCM audio

COPY - SCMS copyright indicator

0 - Copyright asserted
1 - Copyright not asserted

If the category code is set to General in the incoming AES3 stream, copyright will always be indicated by COPY, even when the stream indicates no copyright.