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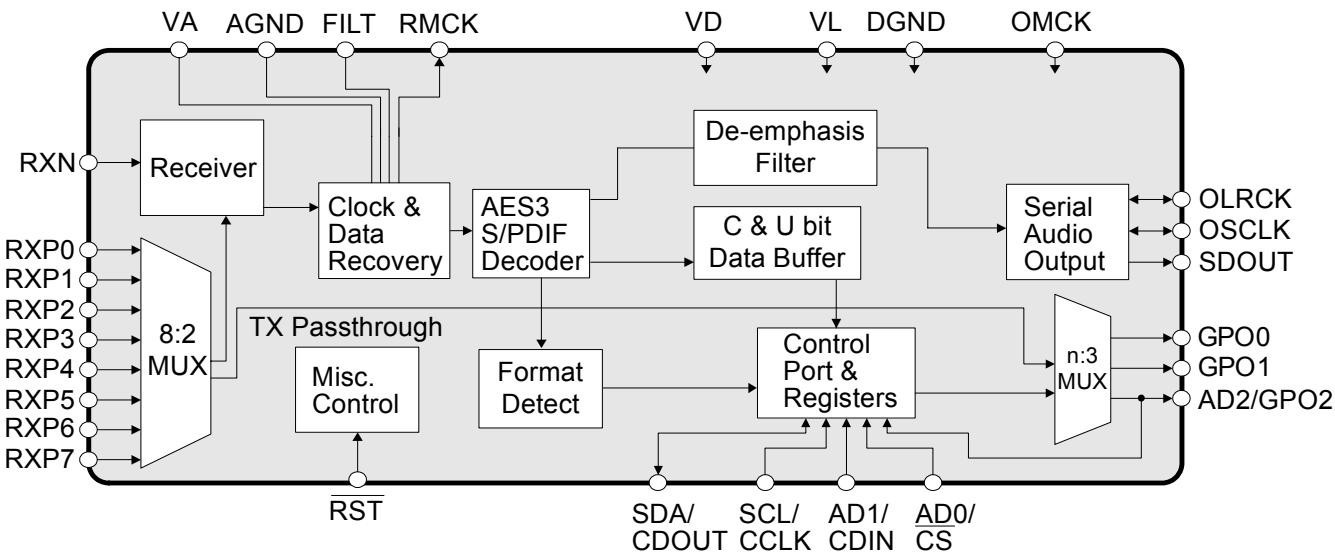
CS8416

192 kHz Digital Audio Interface Receiver

Features

- Complete EIAJ CP1201, IEC-60958, AES3, S/PDIF-Compatible Receiver
- +3.3 V Analog Supply (VA)
- +3.3 V Digital Supply (VD)
- +3.3 V or +5.0 V Digital Interface Supply (VL)
- 8:2 S/PDIF Input MUX
- AES/SPDIF Input Pins Selectable in Hardware Mode
- Three General Purpose Outputs (GPO) Allow Signal Routing
- Selectable Signal Routing to GPO Pins
- S/PDIF-to-TX Inputs Selectable in Hardware Mode
- Flexible 3-wire Serial Digital Output Port
- 32 kHz to 192 kHz Sample Frequency Range
- Low-Jitter Clock Recovery
- Pin and Microcontroller Read Access to Channel Status and User Data
- SPI™ or I²C® Control Port Software Mode and Stand-Alone Hardware Mode
- Differential Cable Receiver
- On-Chip Channel Status Data Buffer Memories
- Auto-Detection of Compressed Audio Input Streams
- Decodes CD Q Sub-Code
- OMCK System Clock Mode

See the General Description and Ordering Information on page 2.



General Description

The CS8416 is a monolithic CMOS device that receives and decodes one of eight stereo pairs of digital audio data according to the IEC60958, S/PDIF, EIAJ CP1201, or AES3 interface standards. The CS8416 has a serial digital audio output port and comprehensive control ability through a selectable control port in Software Mode or through selectable pins in Hardware Mode. Channel status data are assembled in buffers, making read access easy. GPO pins may be assigned to route a variety of signals to output pins.

A low-jitter clock recovery mechanism yields a very clean recovered clock from the incoming AES3 stream.

Stand-alone operation allows systems with no microcontroller to operate the CS8416 with dedicated output pins for channel status data.

The CS8416 is available in 28-pin TSSOP, SOIC, and QFN packages in Commercial grade (-10° to +70° C) and Automotive grade (-40° to +85° C). The CDB8416 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please refer to “Ordering Information” on page 59 for complete ordering information.

Target applications include A/V receivers, CD-R, DVD receivers, multimedia speakers, digital mixing consoles, effects processors, set-top boxes, and computer and automotive audio systems.

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1. CHARACTERISTICS AND SPECIFICATIONS

All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.

SPECIFIED OPERATING CONDITIONS

(AGND, DGND = 0 V, all voltages with respect to 0 V)

Parameter		Symbol	Min	Typ	Max	Units
Power Supply Voltage		VA VD VL	3.13 3.13 3.13	3.3 3.3 3.3 or 5.0	3.46 3.46 5.25	V V V
Ambient Operating Temperature:	Commercial Grade Automotive Grade	T_A	-10 -40	- -	+70 +85	°C

ABSOLUTE MAXIMUM RATINGS

(AGND, DGND = 0 V; all voltages with respect to 0 V. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.)

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	VA, VD,VL	-	6.0	V
Input Current, Any Pin Except Supplies (Note 1)	I_{in}	-	±10	mA
Input Voltage	V_{in}	-0.3	(VL) + 0.3	V
Ambient Operating Temperature (power applied)	T_A	-55	125	°C
Storage Temperature	T_{stg}	-65	150	°C

Notes:

1. Transient currents of up to 100 mA will not cause SCR latch-up.

DC ELECTRICAL CHARACTERISTICS

(AGND = DGND = 0 V; all voltages with respect to 0 V.)

Parameters		Symbol	Min	Typ	Max	Units
Power-Down Mode (Notes 2, 4)						
Supply Current in power-down	VA	IA	-	10	-	µA
	VD	ID	-	70	-	µA
	VL = 3.3 V	IL	-	10	-	µA
	VL = 5.0 V	IL	-	12	-	µA
Normal Operation (Notes 3, 4)						
Supply Current at 48 kHz frame rate	VA	IA	-	5.7	-	mA
	VD	ID	-	5.9	-	mA
	VL = 3.3 V	IL	-	2.8	-	mA
	VL = 5.0 V	IL	-	4.2	-	mA
Supply Current at 192 kHz frame rate	VA	IA	-	9.4	-	mA
	VD	ID	-	23	-	mA
	VL = 3.3 V	IL	-	7.8	-	mA
	VL = 5.0 V	IL	-	11.8	-	mA

Notes:

2. Power-Down Mode is defined as $\overline{RST}$ = LO with all clocks and data lines held static.
3. Normal operation is defined as $\overline{RST}$ = HI.
4. Assumes that no inputs are floating. It is recommended that all inputs be driven high or low at all times.

DIGITAL INPUT CHARACTERISTICS

(AGND = DGND = 0 V; all voltages with respect to 0 V.)

Parameters	Symbol	Min	Typ	Max	Units
Input Leakage Current	I_{IN}	-	-	±0.5	µA
Differential Input Sensitivity, RXP[7:0] to RXN	V_{TH}	-	150	200	mVpp
Input Hysteresis	V_H	0.15	-	1.0	V

DIGITAL INTERFACE SPECIFICATIONS

(AGND = DGND = 0 V; all voltages with respect to 0 V.)

Parameters	Symbol	Min	Max	Units
High-Level Output Voltage (I_{OH} = -3.2 mA)	V_{OH}	(VL) - 1.0	-	V
Low-Level Output Voltage (I_{OL} = 3.2 mA)	V_{OL}	-	0.5	V
High-Level Input Voltage, except RXP[7:0], RXN	V_{IH}	2.0	(VL) + 0.3	V
Low-Level Input Voltage, except RXP[7:0], RXN	V_{IL}	-0.3	0.8	V

SWITCHING CHARACTERISTICS

(Inputs: Logic 0 = 0 V, Logic 1 = VL; C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Units
$\overline{\text{RST}}$ Pin Low Pulse Width		200	-	-	µS
PLL Clock Recovery Sample Rate Range		30	-	200	kHz
RMCK Output Jitter (Note 5)		-	200	-	ps RMS
RMCK Output Duty-Cycle (Note 6) (Note 7)		45 50	50 55	55 65	% %
RMCK/OMCK Maximum Frequency		-	-	50	MHz

Notes:

5. Typical RMS cycle-to-cycle jitter.
6. Duty cycle when clock is recovered from biphase encoded input.
7. Duty cycle when OMCK is switched over for output on RMCK.

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORTS

(Inputs: Logic 0 = 0 V, Logic 1 = VL; C_L = 20 pF)

Parameter		Symbol	Min	Typ	Max	Units
OSCLK/OLRCK Active Edge to SDOUT Output Valid	(Note 8)	t_{dpd}	-	-	23	ns
Master Mode						
RMCK to OSCLK active edge delay	(Note 8)	t_{smd}	0	-	12	ns
RMCK to OLRCK delay	(Note 9)	t_{lmd}	0	-	12	ns
OSCLK and OLRCK Duty Cycle			-	50	-	%
Slave Mode						
OSCLK Period		t_{sckw}	36	-	-	ns
OSCLK Input Low Width		t_{sckl}	14	-	-	ns
OSCLK Input High Width		t_{sckh}	14	-	-	ns
OSCLK Active Edge to OLRCK Edge	(Notes 8,9,10)	t_{lrckd}	10	-	-	ns
OSCLK Edge Setup Before OSCLK Active-Edge	(Notes 8,9,11)	t_{lrcks}	10	-	-	ns

Notes:

8. In Software Mode the active edges of OSCLK are programmable.
9. In Software Mode the polarity of OLRCK is programmable.
10. This delay is to prevent the previous OSCLK edge from being interpreted as the first one after OLRCK has changed.
11. This setup time ensures that this OSCLK edge is interpreted as the first one after OLRCK has changed.

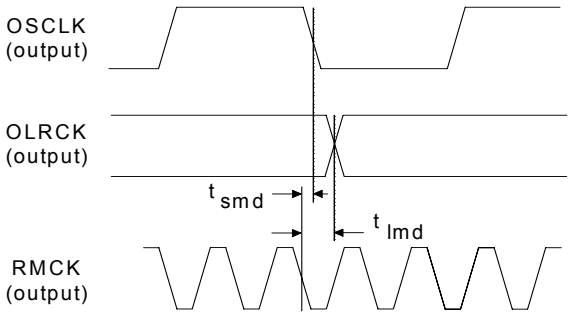


Figure 1. Audio Port Master Mode Timing

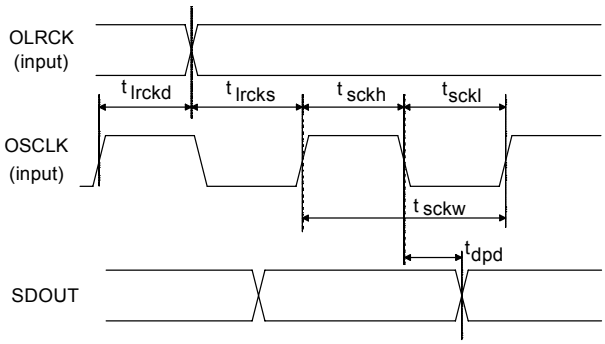


Figure 2. Audio Port Slave Mode and Data Input

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI MODE

(Inputs: Logic 0 = 0 V, Logic 1 = VL; C_L = 20 pF)

Parameter		Symbol	Min	Max	Unit
CCLK Clock Frequency	(Note 12)	f_{sck}	0	6.0	MHz
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 13)	t_{dh}	15	-	ns
CCLK Falling to CDOUT Stable		t_{pd}	-	50	ns
Rise Time of CDOUT		t_{r1}	-	25	ns
Fall Time of CDOUT		t_{f1}	-	25	ns
Rise Time of CCLK and CDIN	(Note 14)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 14)	t_{r2}	-	100	ns

Notes:

12. If Fs is lower than 46.875 kHz, the maximum CCLK frequency should be less than 128 Fs. This is dictated by the timing requirements necessary to access the Channel Status memory. Access to the control register file can be carried out at the full 6 MHz rate. The minimum allowable input sample rate is 32 kHz, so choosing CCLK to be less than or equal to 4.1 MHz should be safe for all possible conditions.
13. Data must be held for sufficient time to bridge the transition time of CCLK.
14. For f_{sck} <1 MHz.

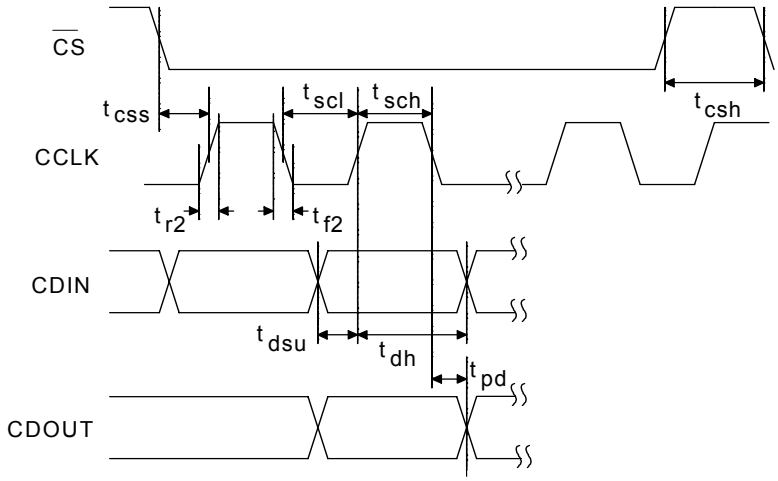


Figure 3. SPI Mode Timing

SWITCHING CHARACTERISTICS - CONTROL PORT- I²C FORMAT

(Inputs: Logic 0 = 0 V, Logic 1 = VL; C_L = 20 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 15)	t_{hdd}	10	-	ns
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_r	-	1000	ns
Fall Time SCL and SDA	t_f	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs

Notes:

15. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

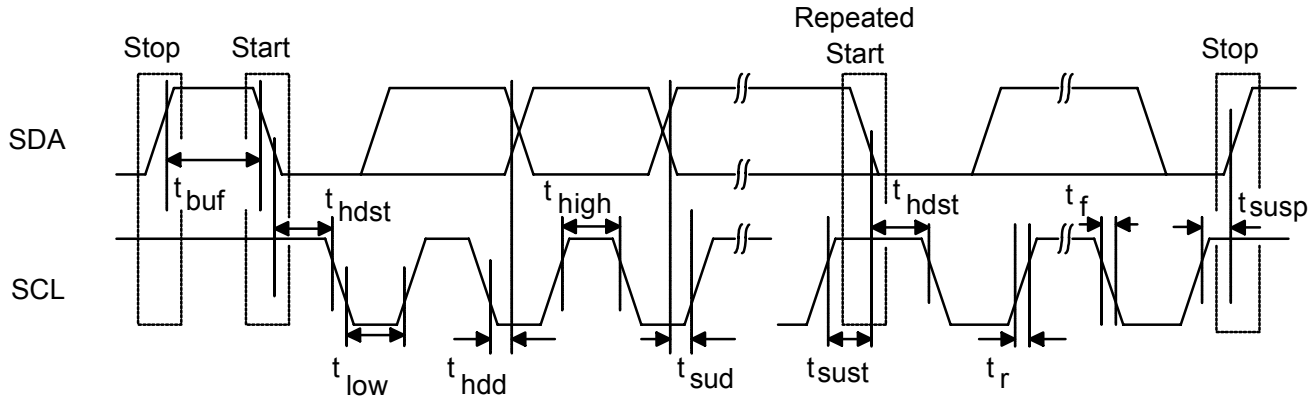
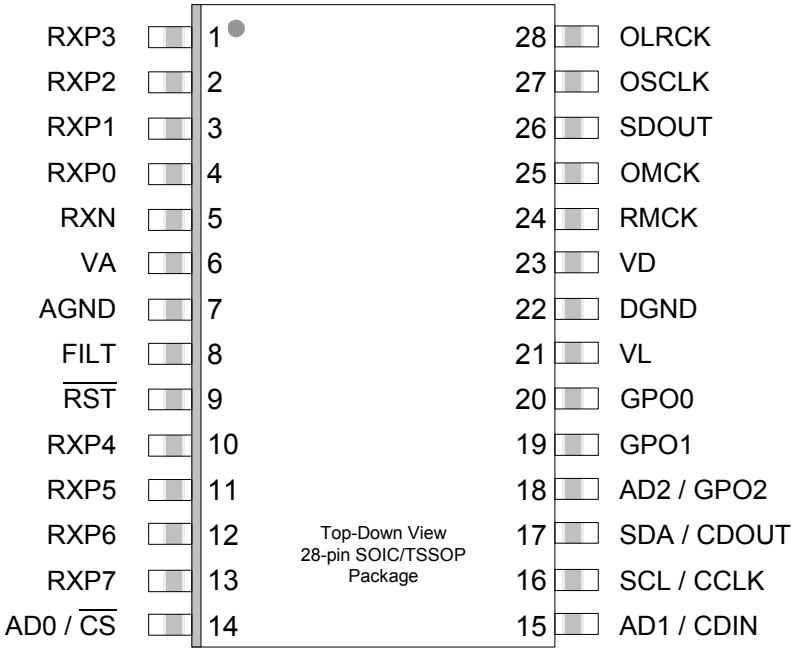


Figure 4. I²C Mode Timing

2. PIN DESCRIPTION - SOFTWARE MODE

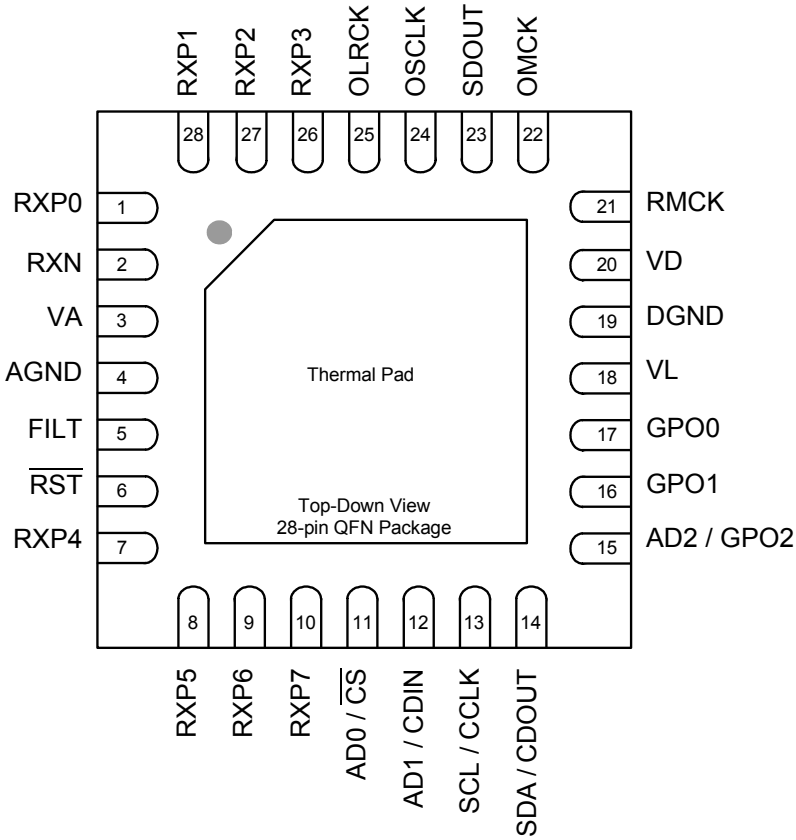
2.1 TSSOP Pin Description



Pin Name	Pin #	Pin Description
VA	6	**Analog Power** (*Input*) - Analog power supply. Nominally +3.3 V. This supply should have as little noise as possible since noise on this pin will directly affect the jitter performance of the recovered clock
VD	23	**Digital Power** (*Input*) – Digital core power supply. Nominally +3.3 V
VL	21	**Logic Power** (*Input*) – Input/Output power supply. Nominally +3.3 V or +5.0 V
AGND	7	**Analog Ground** (*Input*) - Ground for the analog circuitry in the chip. AGND and DGND should be connected to a common ground area under the chip.
DGND	22	**Digital & I/O Ground** (*Input*) - Ground for the I/O and core logic. AGND and DGND should be connected to a common ground area under the chip.
$\overline{\text{RST}}$	9	**Reset** (*Input*) - When $\overline{\text{RST}}$ is low, the CS8416 enters a low power mode and all internal states are reset. On initial power up, $\overline{\text{RST}}$ must be held low until the power supply is stable, and all input clocks are stable in frequency and phase.
FILT	8	**PLL Loop Filter** (*Output*) - An RC network should be connected between this pin and analog ground. For minimum PLL jitter, return the ground end of the filter network directly to AGND. See "PLL Filter" on page 53 for more information on the PLL and the external components.
RXP0 RXP1 RXP2 RXP3 RXP4 RXP5 RXP6 RXP7	4 3 2 1 10 11 12 13	**Positive AES3/SPDIF Input** (*Input*) - Single-ended or differential receiver inputs carrying AES3 or S/PDIF encoded digital data. The RXP[7:0] inputs comprise the 8:2 S/PDIF Input Multiplexer. The select line control is accessed using the Control 4 register (04h). Unused multiplexer inputs should be left floating or tied to AGND. See "External AES3/SPDIF/IEC60958 Receiver Components" on page 49 for recommended input circuits.

Pin Name	Pin #	Pin Description
RXN	5	**Negative AES3/SPDIF Input** (*Input*) - Single-ended or differential receiver input carrying AES3 or S/PDIF encoded digital data. Used along with RXP[7:0] to form an AES3 differential input. In single-ended operation this should be AC coupled to ground through a capacitor. See "External AES3/SPDIF/IEC60958 Receiver Components" on page 49 for recommended input circuits.
OMCK	25	**System Clock** (*Input*) - When the OMCK System Clock Mode is enabled using the SWCLK bit in the Control 1 register, the clock signal input on this pin is automatically output through RMCK on PLL unlock. OMCK serves as the reference signal for OMCK/RMCK ratio expressed in register 18h. "OMCK System Clock Mode" section on page 28
RMCK	24	**Input Section Recovered Master Clock** (*Output*) - Input section recovered master clock output from the PLL. Frequency defaults to 256x the sample rate (F_s) and may be set to 128x through the RMCKF bit in the Control 1 register (01h). RMCK may also be set to high impedance by the RXD bit in the Control 4 register (04h).
OSCLK	27	**Serial Audio Output Bit Clock** (*Input*/*Output*) - Serial bit clock for audio data on the SDOUT pin
OLRCK	28	**Serial Audio Output Left/Right Clock** (*Input*/*Output*) - Word rate clock for the audio data on the SDOUT pin. Frequency will be the output sample rate (Fs)
SDOUT	26	**Serial Audio Output Data** (*Output*) - Audio data serial output pin. This pin must be pulled high to VL through a 47 kΩ resistor to place the part in Software Mode.
SDA / CDOUT	17	**Serial Control Data I/O (I²C) / Data Out (SPI)** (*Input/Output*) - In I²C Mode, SDA is the control I/O data line. SDA is open drain and requires an external pull-up resistor to VL. In SPI Mode, CDOUT is the output data from the control port interface on the CS8416. See the "Control Port Description" section on page 33.
SCL / CCLK	16	**Control Port Clock** (*Input*) - Serial control interface clock and is used to clock control data bits into and out of the CS8416. CCLK is an open drain output and requires an external pull-up resistor to VL. See the "Control Port Description" section on page 33.
AD0 / $\overline{CS}$	14	**Address Bit 0 (I²C) / Control Port Chip Select (SPI)** (*Input)* - A falling edge on this pin puts the CS8416 into SPI Control Port Mode. With no falling edge, the CS8416 defaults to I²C Mode. In I²C Mode, AD0 is a chip address pin. In SPI Mode, $\overline{CS}$ is used to enable the control port interface on the CS8416. See the "Control Port Description" section on page 33.
AD1 / CDIN	15	**Address Bit 1 (I²C) / Serial Control Data in (SPI)** (*Input*) - In I²C Mode, AD1 is a chip address pin. In SPI Mode, CDIN is the input data line for the control port interface. See the "Control Port Description" section on page 33.
AD2 / GPO2	18	**General Purpose Output 2** *(Output)* - If using the I²C control port, this pin must be pulled high or low through a 47 kΩ resistor. See the "Control Port Description" section on page 33 and "General Purpose Outputs" on page 29 for GPO functions.
GPO1	19	**General Purpose Output 1** *(Output)* - See "General Purpose Outputs" on page 29 for GPO functions.
GPO0	20	**General Purpose Output 0** *(Output)* - See "General Purpose Outputs" on page 29 for GPO functions.

2.2 QFN Pin Description

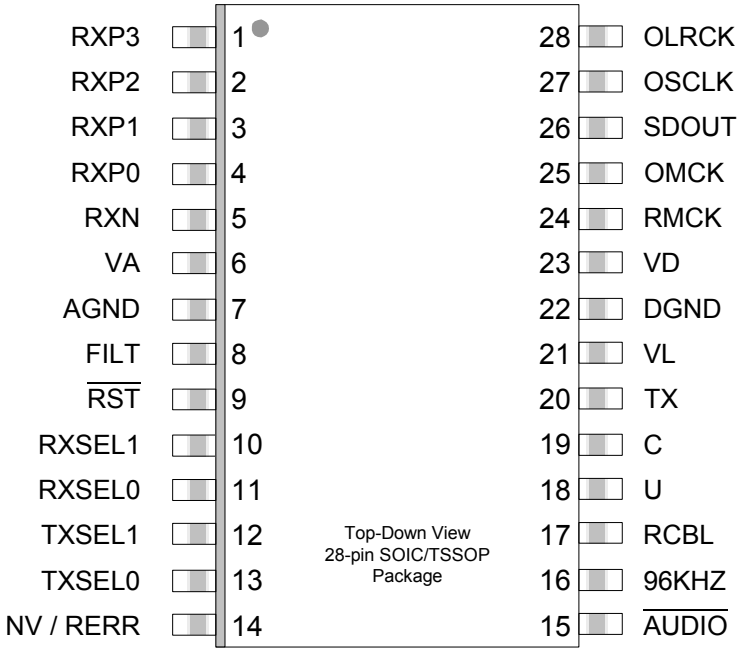


Pin Name	Pin #	Pin Description
VA	3	**Analog Power** (*Input*) - Analog power supply. Nominally +3.3 V. This supply should have as little noise as possible since noise on this pin will directly affect the jitter performance of the recovered clock
VD	20	**Digital Power** (*Input*) – Digital core power supply. Nominally +3.3 V
VL	18	**Logic Power** (*Input*) – Input/Output power supply. Nominally +3.3 V or +5.0 V
AGND	4	**Analog Ground** (*Input*) - Ground for the analog circuitry in the chip. AGND and DGND should be connected to a common ground area under the chip.
DGND	19	**Digital & I/O Ground** (*Input*) - Ground for the I/O and core logic. AGND and DGND should be connected to a common ground area under the chip.
$\overline{\text{RST}}$	6	**Reset** (*Input*) - When $\overline{\text{RST}}$ is low, the CS8416 enters a low power mode and all internal states are reset. On initial power up, $\overline{\text{RST}}$ must be held low until the power supply is stable, and all input clocks are stable in frequency and phase.
FILT	5	**PLL Loop Filter** (*Output*) - An RC network should be connected between this pin and analog ground. For minimum PLL jitter, return the ground end of the filter network directly to AGND. See "PLL Filter" on page 53 for more information on the PLL and the external components.

Pin Name	Pin #	Pin Description
RXP0 RXP1 RXP2 RXP3 RXP4 RXP5 RXP6 RXP7	1 28 27 26 7 8 9 10	**Positive AES3/SPDIF Input** (*Input*) - Single-ended or differential receiver inputs carrying AES3 or S/PDIF encoded digital data. The RXP[7:0] inputs comprise the 8:2 S/PDIF Input Multiplexer. The select line control is accessed using the Control 4 register (04h). Unused multiplexer inputs should be left floating or tied to AGND. See "External AES3/SPDIF/IEC60958 Receiver Components" on page 49 for recommended input circuits.
RXN	2	**Negative AES3/SPDIF Input** (*Input*) - Single-ended or differential receiver input carrying AES3 or S/PDIF encoded digital data. Used along with RXP[7:0] to form an AES3 differential input. In single-ended operation this should be AC coupled to ground through a capacitor. See "External AES3/SPDIF/IEC60958 Receiver Components" on page 49 for recommended input circuits.
OMCK	22	**System Clock** (*Input*) - When the OMCK System Clock Mode is enabled using the SWCLK bit in the Control 1 register, the clock signal input on this pin is automatically output through RMCK on PLL unlock. OMCK serves as the reference signal for OMCK/RMCK ratio expressed in register 18h. "OMCK System Clock Mode" section on page 28
RMCK	21	**Input Section Recovered Master Clock** (*Output*) - Input section recovered master clock output from the PLL. Frequency defaults to 256x the sample rate (F_s) and may be set to 128x through the RMCKF bit in the Control 1 register (01h). RMCK may also be set to high impedance by the RXD bit in the Control 4 register (04h).
OSCLK	24	**Serial Audio Output Bit Clock** (*Input*/*Output*) - Serial bit clock for audio data on the SDOUT pin
OLRCK	25	**Serial Audio Output Left/Right Clock** (*Input*/*Output*) - Word rate clock for the audio data on the SDOUT pin. Frequency will be the output sample rate (Fs)
SDOUT	23	**Serial Audio Output Data** (*Output*) - Audio data serial output pin. This pin must be pulled high to VL through a 47 kΩ resistor to place the part in Software Mode.
SDA / CDOUT	14	**Serial Control Data I/O (I²C) / Data Out (SPI)** (*Input/Output*) - In I²C Mode, SDA is the control I/O data line. SDA is open drain and requires an external pull-up resistor to VL. In SPI Mode, CDOUT is the output data from the control port interface on the CS8416. See the "Control Port Description" section on page 33.
SCL / CCLK	13	**Control Port Clock** (*Input*) - Serial control interface clock and is used to clock control data bits into and out of the CS8416. CCLK is an open drain output and requires an external pull-up resistor to VL. See the "Control Port Description" section on page 33.
AD0 / $\overline{CS}$	11	**Address Bit 0 (I²C) / Control Port Chip Select (SPI)** (*Input*) - A falling edge on this pin puts the CS8416 into SPI Control Port Mode. With no falling edge, the CS8416 defaults to I²C Mode. In I²C Mode, AD0 is a chip address pin. In SPI Mode, $\overline{CS}$ is used to enable the control port interface on the CS8416. See the "Control Port Description" section on page 33.
AD1 / CDIN	12	**Address Bit 1 (I²C) / Serial Control Data in (SPI)** (*Input*) - In I²C Mode, AD1 is a chip address pin. In SPI Mode, CDIN is the input data line for the control port interface. See the "Control Port Description" section on page 33.
AD2 / GPO2	15	**General Purpose Output 2** *(Output)* - If using the I²C control port, this pin must be pulled high or low through a 47 kΩ resistor. See the "Control Port Description" section on page 33 and "General Purpose Outputs" on page 29 for GPO functions.
GPO1	16	**General Purpose Output 1** *(Output)* - See "General Purpose Outputs" on page 29 for GPO functions.
GPO0	17	**General Purpose Output 0** *(Output)* - See "General Purpose Outputs" on page 29 for GPO functions.
THERMAL PAD	-	**Thermal Pad** - Thermal relief pad for optimized heat dissipation.

3. PIN DESCRIPTION - HARDWARE MODE

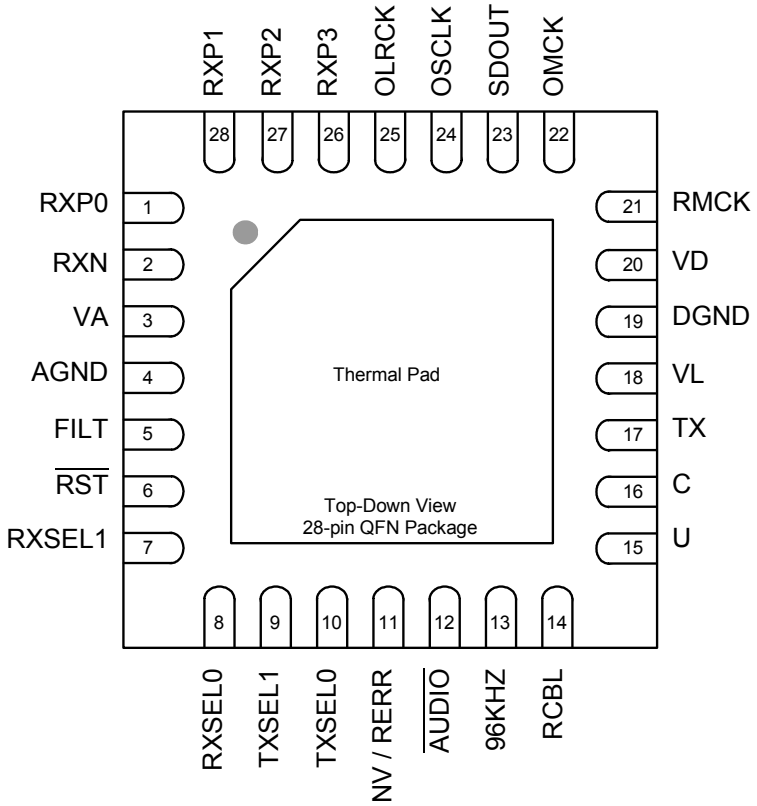
3.1 TSSOP Pin Description



Pin Name	Pin #	Pin Description
VA	6	**Analog Power** (*Input*) - Analog power supply. Nominally +3.3 V. This supply should have as little noise as possible since noise on this pin will directly affect the jitter performance of the recovered clock
VD	23	**Digital Power** (*Input*) – Digital core power supply. Nominally +3.3 V
VL	21	**Logic Power** (*Input*) – Input/Output power supply. Nominally +3.3 V or +5.0 V
AGND	7	**Analog Ground** (*Input*) - Ground for the analog circuitry in the chip. AGND and DGND should be connected to a common ground area under the chip.
DGND	22	**Digital & I/O Ground** (*Input*) - Ground for the I/O and core logic. AGND and DGND should be connected to a common ground area under the chip.
$\overline{\text{RST}}$	9	**Reset** (*Input*) - When $\overline{\text{RST}}$ is low, the CS8416 enters a low power mode and all internal states are reset. On initial power up, $\overline{\text{RST}}$ must be held low until the power supply is stable, and all input clocks are stable in frequency and phase.
FILT	8	**PLL Loop Filter** (*Output*) - An RC network should be connected between this pin and analog ground. For minimum PLL jitter, return the ground end of the filter network directly to AGND. See "PLL Filter" on page 53 for more information on the PLL and the external components.
RXP0 RXP1 RXP2 RXP3	4 3 2 1	**Positive AES3/SPDIF Input** (*Input*) - Single-ended or differential receiver inputs carrying AES3 or S/PDIF encoded digital data. The RXP[3:0] inputs comprise the 4:2 S/PDIF Input Multiplexer. The select line control is accessed using the RXPSEL[1:0] pins. Unused multiplexer inputs should be left floating or tied to AGND. See "External AES3/SPDIF/IEC60958 Receiver Components" on page 49 for recommended input circuits.
RXN	5	**Negative AES3/SPDIF Input** (*Input*) - Single-ended or differential receiver input carrying AES3 or S/PDIF encoded digital data. Used along with RXP[3:0] to form an AES3 differential input. In single-ended operation this should be AC coupled to ground through a capacitor. See "External AES3/SPDIF/IEC60958 Receiver Components" on page 49 for recommended input circuits.

Pin Name	Pin #	Pin Description
OMCK	25	**System Clock** (*Input*) - OMCK System Clock Mode is enabled by a transition (rising edge active) on OMCK after reset. When enabled, the clock signal input on this pin is automatically output through RMCK on PLL unlock. See "OMCK System Clock Mode" on page 28.
RMCK	24	**Input Section Recovered Master Clock** (*Output*) - Input section recovered master clock output from the PLL. Frequency is 256x the sample rate (F_s) when the U pin is pulled down by a 47 kΩ resistor to DGND. Frequency is 128x the sample rate (F_s) when the U pin is pulled up by a 47 kΩ resistor to VL.
OSCLK	27	**Serial Audio Output Bit Clock** (*Input*/*Output*) - Serial bit clock for audio data on the SDOUT pin
OLRCK	28	**Serial Audio Output Left/Right Clock** (*Input*/*Output*) - Word rate clock for the audio data on the SDOUT pin. Frequency will be the output sample rate (Fs)
SDOUT	26	**Serial Audio Output Data** (*Output*) - Audio data serial output pin. This pin must be pulled low to DGND through a 47 kΩ resistor to place the part in Hardware Mode.
RXSEL1 RXSEL0	10 11	**Receiver MUX Selector** *(Input)* - Used to select which pin, RXP[3:0], is used for the receiver input.
TXSEL1 TXSEL0	12 13	**TX Pin MUX SELECTION** *(Input)* - Used to select which pin, RXP[3:0], is passed to the TX pin output. If TX passthrough is not used, the user should set it to output one of the unused receiver inputs.
TX	20	**S/PDIF MUX Passthrough** (*Output)* - Single-ended signal is resolved to full-rail, but is not de-jittered before it is output. Output is set by TXSEL[1:0]. This pin is also used to select the type of phase detector (PDUR) at reset. If TX passthrough is not used, the user should set it to output one of the unused receiver inputs.
NV/RERR	14	**Non-Validity Receiver Error/Receiver Error** *(Output)* - Receiver error indicator. NVERR is selected by a 47 kΩ resistor to DGND. RERR is selected by a 47 kΩ resistor to VL.
AUDIO	15	**Audio Channel Status Bit** *(Output)* **–** When low, a valid linear PCM audio stream is indicated. See "Non-Audio Detection" on page 31. This pin is also used to select the serial port format (SFSEL1) at reset.
96KHZ	16	**96 kHz Sample Rate Detect** *(Output)* - If the input sample rate is ≤ 48 kHz, outputs a "0". Outputs a "1" if the sample rate is ≥ 88.1 kHz. Otherwise the output is indeterminate. Also used to set the Emphasis Audio Match feature at reset.
RCBL	17	Receiver Channel Status Block *(Output)* -Indicates the beginning of a received channel status block. RCBL goes high two frames after the reception of a Z preamble, remains high for 16 frames and then returns low for the remainder of the block. RCBL changes on rising edges of RMCK. Also used to set the serial audio port to master or slave at reset.
C	19	**Channel Status Data** (*Output*) - Outputs channel status data from the AES3 receiver, clocked by the rising and falling edges of OLRCK. Also used to select the serial port format (SFSEL0) at reset.
U	18	**User Data** (*Output*) - Outputs user data from the AES3 receiver, clocked by the rising and falling edges of OLRCK. Also used to select the frequency of RMCK to either 256*F_s or 128*F_s at reset.

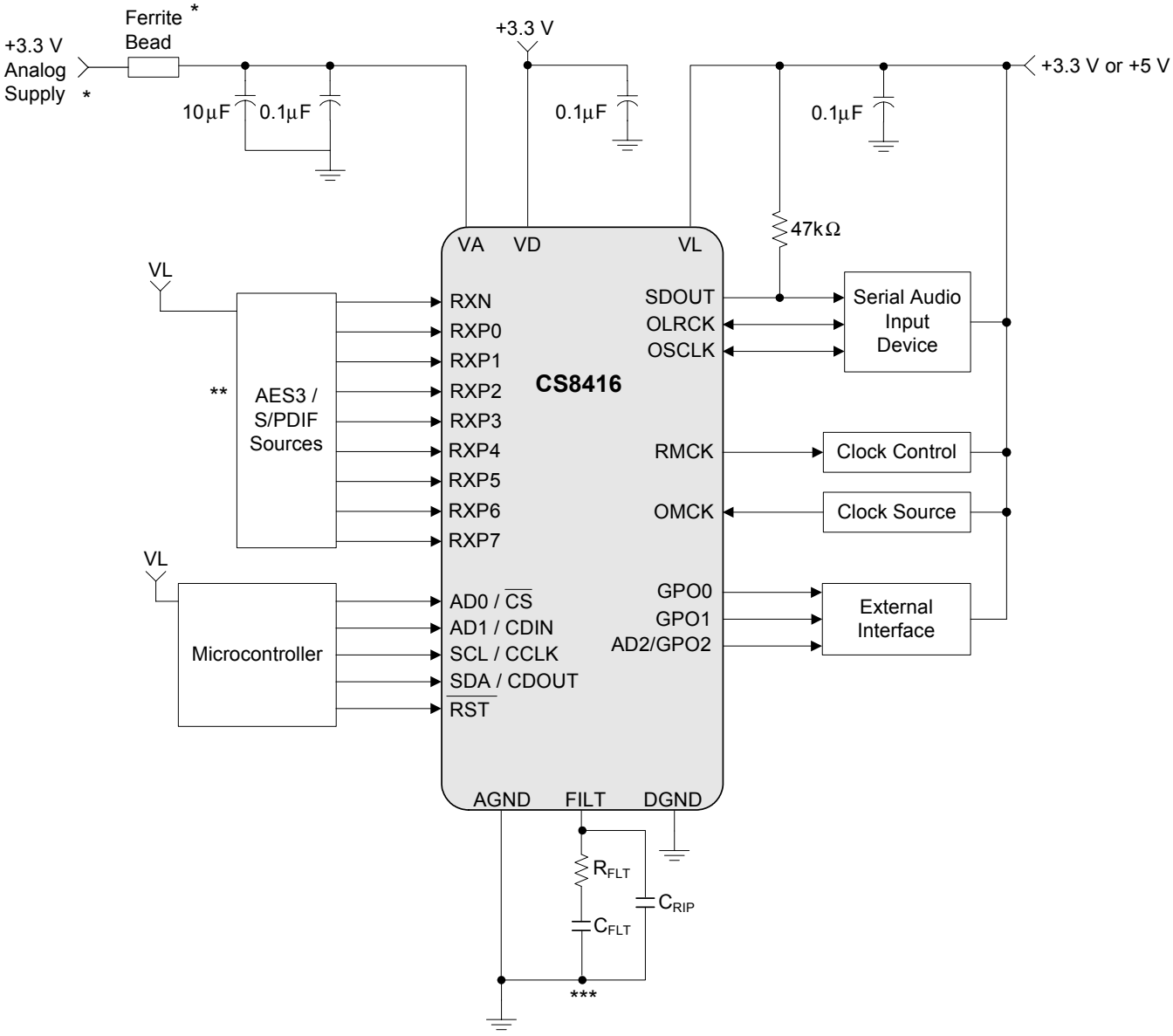
3.2 QFN Pin Description



Pin Name	Pin #	Pin Description
VA	3	**Analog Power** (*Input*) - Analog power supply. Nominally +3.3 V. This supply should have as little noise as possible since noise on this pin will directly affect the jitter performance of the recovered clock
VD	20	**Digital Power** (*Input*) – Digital core power supply. Nominally +3.3 V
VL	18	**Logic Power** (*Input*) – Input/Output power supply. Nominally +3.3 V or +5.0 V
AGND	4	**Analog Ground** (*Input*) - Ground for the analog circuitry in the chip. AGND and DGND should be connected to a common ground area under the chip.
DGND	19	**Digital & I/O Ground** (*Input*) - Ground for the I/O and core logic. AGND and DGND should be connected to a common ground area under the chip.
$\overline{\text{RST}}$	6	**Reset** (*Input*) - When $\overline{\text{RST}}$ is low, the CS8416 enters a low power mode and all internal states are reset. On initial power up, $\overline{\text{RST}}$ must be held low until the power supply is stable, and all input clocks are stable in frequency and phase.
FILT	5	**PLL Loop Filter** (*Output*) - An RC network should be connected between this pin and analog ground. For minimum PLL jitter, return the ground end of the filter network directly to AGND. See "PLL Filter" on page 53 for more information on the PLL and the external components.
RXP0 RXP1 RXP2 RXP3	1 28 27 26	**Positive AES3/SPDIF Input** (*Input*) - Single-ended or differential receiver inputs carrying AES3 or S/PDIF encoded digital data. The RXP[3:0] inputs comprise the 4:2 S/PDIF Input Multiplexer. The select line control is accessed using the RXPSEL[1:0] pins. Unused multiplexer inputs should be left floating or tied to AGND. See "External AES3/SPDIF/IEC60958 Receiver Components" on page 49 for recommended input circuits.

Pin Name	Pin #	Pin Description
RXN	2	**Negative AES3/SPDIF Input** (*Input*) - Single-ended or differential receiver input carrying AES3 or S/PDIF encoded digital data. Used along with RXP[3:0] to form an AES3 differential input. In single-ended operation this should be AC coupled to ground through a capacitor. See "External AES3/SPDIF/IEC60958 Receiver Components" on page 49 for recommended input circuits.
OMCK	22	**System Clock** (*Input*) - OMCK System Clock Mode is enabled by a transition (rising edge active) on OMCK after reset. When enabled, the clock signal input on this pin is automatically output through RMCK on PLL unlock. See "OMCK System Clock Mode" on page 28.
RMCK	21	**Input Section Recovered Master Clock** (*Output*) - Input section recovered master clock output from the PLL. Frequency is 256x the sample rate (F_S) when the U pin is pulled down by a 47 kΩ resistor to DGND. Frequency is 128x the sample rate (F_S) when the U pin is pulled up by a 47 kΩ resistor to VL.
OSCLK	24	**Serial Audio Output Bit Clock** (*Input*/*Output*) - Serial bit clock for audio data on the SDOUT pin
OLRCK	25	**Serial Audio Output Left/Right Clock** (*Input*/*Output*) - Word rate clock for the audio data on the SDOUT pin. Frequency will be the output sample rate (Fs)
SDOUT	23	**Serial Audio Output Data** (*Output*) - Audio data serial output pin. This pin must be pulled low to DGND through a 47 kΩ resistor to place the part in Hardware Mode.
RXSEL1 RXSEL0	7 8	**Receiver MUX Selector** *(Input)* - Used to select which pin, RXP[3:0], is used for the receiver input.
TXSEL1 TXSEL0	9 10	**TX Pin MUX SELECTION** *(Input)* - Used to select which pin, RXP[3:0], is passed to the TX pin output. If TX passthrough is not used, the user should set it to output one of the unused receiver inputs.
TX	17	**S/PDIF MUX Passthrough** (*Output)* - Single-ended signal is resolved to full-rail, but is not de-jittered before it is output. Output is set by TXSEL[1:0]. This pin is also used to select the type of phase detector (PDUR) at reset. If TX passthrough is not used, the user should set it to output one of the unused receiver inputs.
NV/RERR	11	**Non-Validity Receiver Error/Receiver Error** *(Output)* - Receiver error indicator. NVERR is selected by a 47 kΩ resistor to DGND. RERR is selected by a 47 kΩ resistor to VL.
AUDIO	12	**Audio Channel Status Bit** *(Output)* **–** When low, a valid linear PCM audio stream is indicated. See "Non-Audio Detection" on page 31. This pin is also used to select the serial port format (SFSEL1) at reset.
96KHZ	13	**96 kHz Sample Rate Detect** *(Output)* - If the input sample rate is ≤ 48 kHz, outputs a "0". Outputs a "1" if the sample rate is ≥ 88.1 kHz. Otherwise the output is indeterminate. Also used to set the Emphasis Audio Match feature at reset.
RCBL	14	Receiver Channel Status Block *(Output)* -Indicates the beginning of a received channel status block. RCBL goes high two frames after the reception of a Z preamble, remains high for 16 frames and then returns low for the remainder of the block. RCBL changes on rising edges of RMCK. Also used to set the serial audio port to master or slave at reset.
C	16	**Channel Status Data** (*Output*) - Outputs channel status data from the AES3 receiver, clocked by the rising and falling edges of OLRCK. Also used to select the serial port format (SFSEL0) at reset.
U	15	**User Data** (*Output*) - Outputs user data from the AES3 receiver, clocked by the rising and falling edges of OLRCK. Also used to select the frequency of RMCK to either 256*F_S or 128*F_S at reset.
THERMAL PAD	-	**Thermal Pad** - Thermal relief pad for optimized heat dissipation.

4. TYPICAL CONNECTION DIAGRAMS

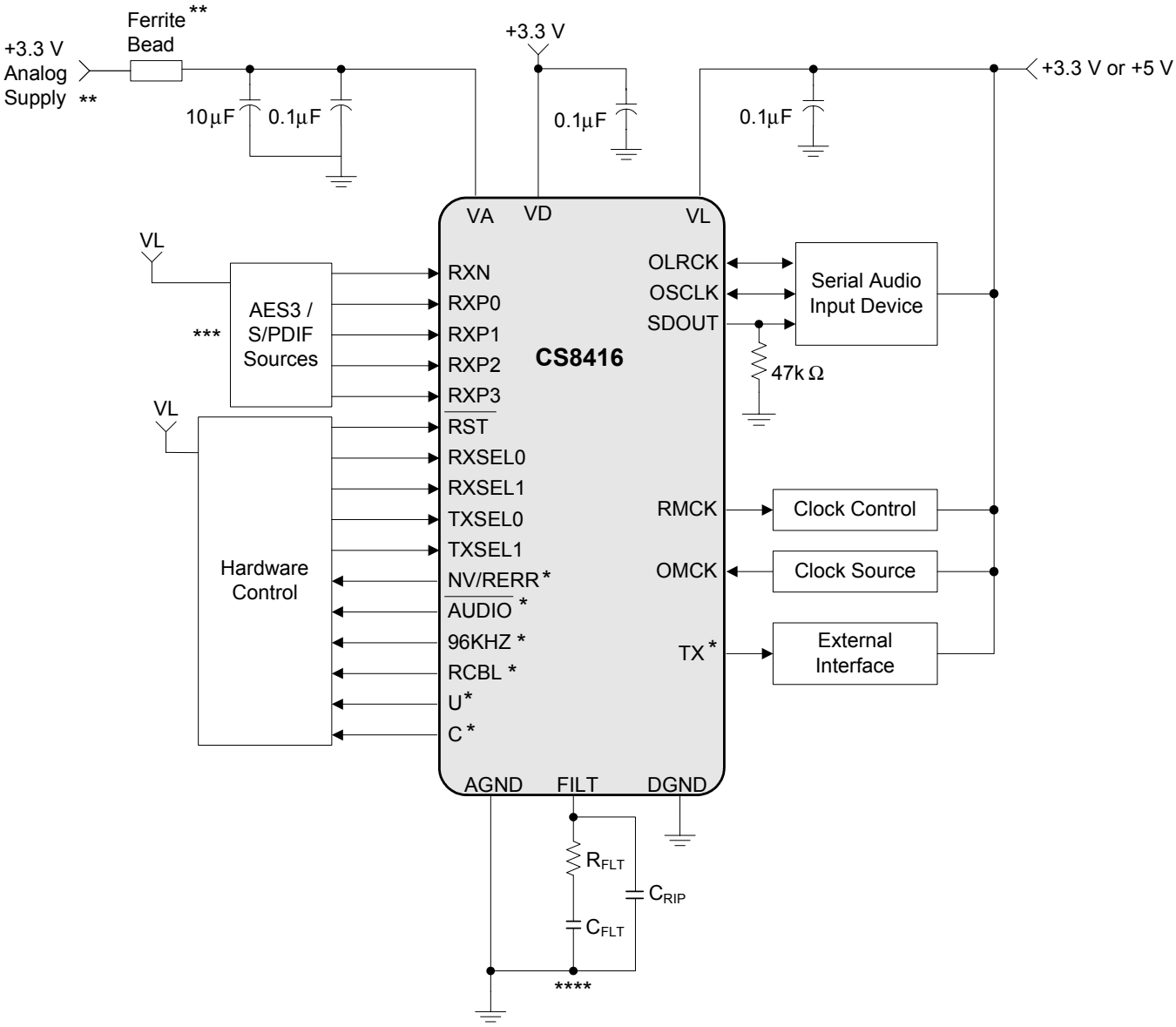


* A separate analog supply is only necessary in applications where RMCK is used for a jitter sensitive task. For applications where RMCK is not used for a jitter sensitive task, connect VA to VD via a ferrite bead. Keep decoupling capacitors between VA and AGND.

** See "S/PDIF Receiver" on page 27 and "External AES3/SPDIF/IEC60958 Receiver Components" on page 49 for typical input configurations and recommended input circuits.

*** For best jitter performance, connect the filter ground directly to the AGND pin. See Table 6 on page 54 for PLL filter values.

Figure 5. Typical Connection Diagram - Software Mode



* These pins must be pulled high to VL or low to DGND through a 47 kΩ resistor.

** A separate analog supply is only necessary in applications where RMCK is used for a jitter sensitive task. For applications where RMCK is not used for a jitter sensitive task, connect VA to VD via a ferrite bead. Keep decoupling capacitors between VA and AGND.

*** See "S/PDIF Receiver" on page 27 and "External AES3/SPDIF/IEC60958 Receiver Components" on page 49 for typical input configurations and recommended input circuits.

**** For best jitter performance connect the filter ground directly to the AGND pin. See Table 6 on page 54 for PLL filter values.

Figure 6. Typical Connection Diagram - Hardware Mode

5. APPLICATIONS

5.1 Reset, Power-Down and Start-Up

When $\overline{\text{RST}}$ is low, the CS8416 enters a low power mode and all internal states are reset, including the control port and registers, and the outputs are muted. In Software Mode, when $\overline{\text{RST}}$ is high, the control port becomes operational, and the desired settings should be loaded into the control registers. Writing a 1 to the RUN bit will then cause the part to leave the low power state and begin operation. After the PLL has settled, the serial audio outputs will be enabled.

Some options within the CS8416 are controlled by a start-up mechanism. During the reset state, some of the pins are reconfigured internally to be inputs. Immediately upon exiting the reset state, the level of these pins is sensed. The pins are then switched to be outputs. This mechanism allows output pins to be used to set alternative modes in the CS8416 by connecting a 47 kΩ resistor to between the pin and either VL (HI) or DGND (LO). For each mode, every start-up option select pin MUST have an external pull-up or pull-down resistor as there are no internal pull-up or pull-down resistors for these startup conditions (except for TX, which has an internal pull-down). In Software Mode, the only start-up option pins are GPO2, which are used to set a chip address bit for the control port in I²C Mode, and SDOUT, which selects between Hardware and Software Modes. The Hardware Mode uses many start-up options, which are detailed in Section 15.2 “Hardware Mode Function Selection” on page 46.

5.2 ID Code and Revision Code

The CS8416 has a register that contains a 4-bit code to indicate that the addressed device is a CS8416. This is useful when other CS84XX family members are resident in the same system, allowing common software modules.

The CS8416 4-bit revision code is also available. This allows the software driver for the CS8416 to identify which revision of the device is in a particular system, and modify its behavior accordingly. To allow for future revisions, it is strongly recommend that the revision code is read into a variable area within the microcontroller, and used wherever appropriate as revision details become known.

5.3 Power Supply, Grounding, and PCB Layout

For most applications, the CS8416 can be operated from a single +3.3 V supply, following normal supply decoupling practices (See Figures 5 and 6). For applications where the recovered input clock, output on the RMCK pin, is required to be low jitter, then use a separate, quiet, analog +3.3 V supply for VA, decoupled to AGND. Make certain that no digital traces are routed near VA, AGND, or FILT as noise may couple and degrade performance. These pins should be well isolated from switching signals and other noise sources.

VL sets the level for the digital inputs and outputs, as well as the AES/SPDIF receiver inputs.

Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. Decoupling capacitors should be mounted on the same side of the board as the CS8416 to minimize inductance effects, and all decoupling capacitors should be as close to the CS8416 as possible. See “PLL Filter” on page 53 for layout recommendations for the PLL.

6. GENERAL DESCRIPTION

The CS8416 is a monolithic CMOS device that receives and decodes audio data according to the AES3, IEC60958, S/PDIF, and EIAJ CP1201 interface standards.

The CS8416 provides an 8:2 multiplexer to select between eight inputs for decoding and to allow an input signal to be routed to an output of the CS8416. Input data can be either differential or single-ended. A low jitter clock is recovered from the incoming data using a PLL. The decoded audio data is output through a configurable, 3-wire serial audio output port. The channel status and Q-channel subcode portion of the user data are assembled in registers and may be accessed through an SPI or I²C port.

Three General Purpose Output (GPO) pins are provided to allow a variety of signals to be accessed under software control. In Hardware Mode, dedicated pins are used to select audio stream inputs for decoding and transmission to a dedicated TX pin. Hardware Mode also provides channel status and user data output pins.

Figures 5 and 6 show the power supply and external connections to the CS8416 when configured for Software Mode and Hardware Mode. Please note that all I/O pins, including RXN and RXP[7:0], operate at the VL voltage.

6.1 AES3 and S/PDIF Standards Documents

This document assumes that the user is familiar with the AES3 and S/PDIF data formats. It is advisable to have current copies of the AES3, IEC60958, and IEC61937 specifications on hand for easy reference.

The latest AES3 standard is available from the Audio Engineering Society or ANSI at www.aes.org or at www.ansi.org. Obtain a copy of the latest IEC60958/61937 standard from ANSI or from the International Electrotechnical Commission at www.iec.ch. The latest EIAJ CP-1201 standard is available from the Japanese Electronics Bureau.

Application Note 22: *Overview of Digital Audio Interface Data Structures* contains a useful tutorial on digital audio specifications, but it should not be considered a substitute for the standards.

The paper *An Understanding and Implementation of the SCMS Serial Copy Management System for Digital Audio Transmission*, by Clifton Sanchez, is an excellent tutorial on SCMS. It is available from the AES as reprint 3518.

7. SERIAL AUDIO OUTPUT PORT

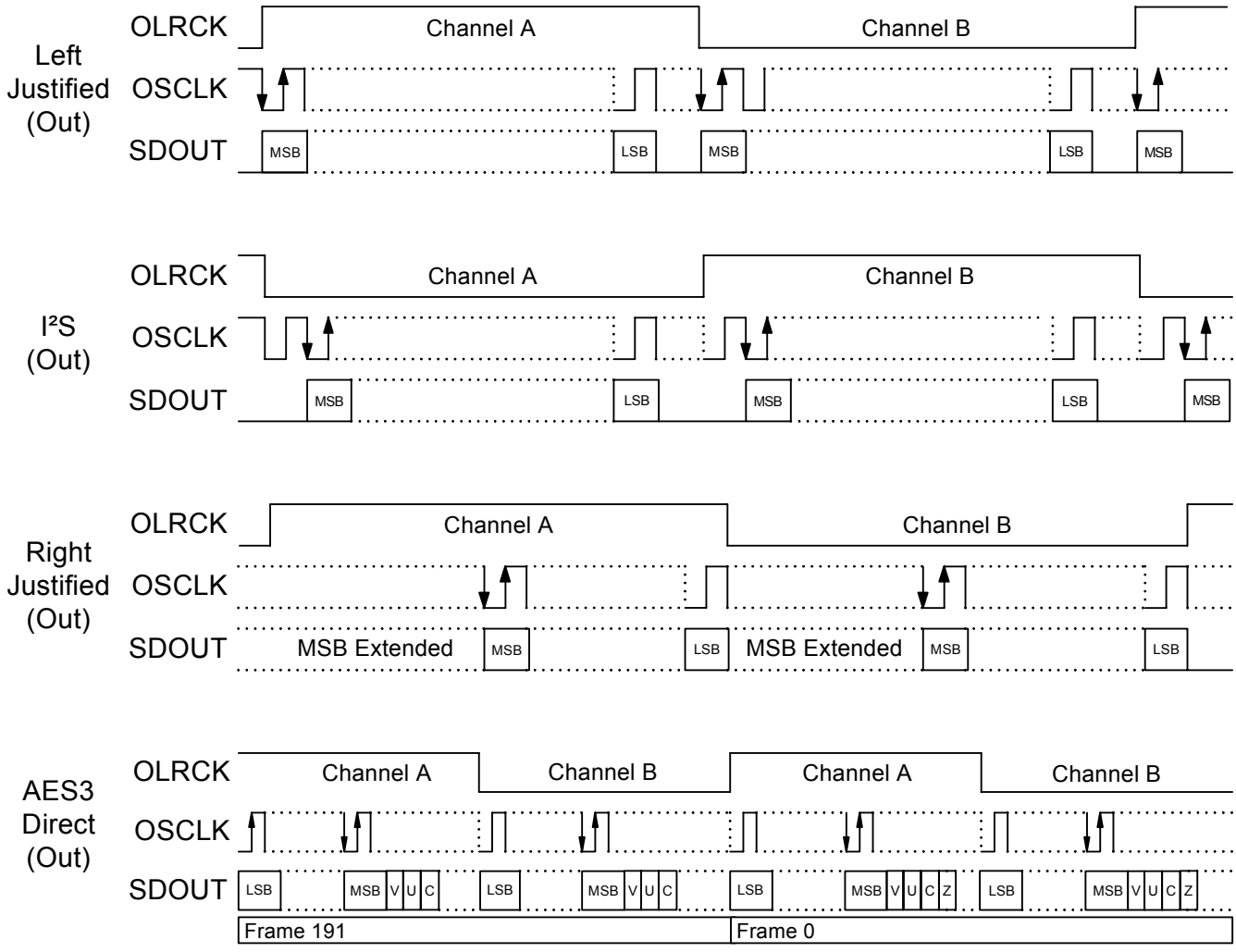
A 3-wire serial audio output port is provided. The port can be adjusted to suit the attached device by setting the control registers. The following parameters are adjustable: master or slave, serial clock frequency, audio data resolution, left- or right-justification of the data relative to left/right clock, optional one-bit cell delay of the first data bit, the polarity of the bit clock, and the polarity of the left/right clock. By setting the appropriate control bits, many formats are possible.

Figure 7 shows a selection of common output formats, along with the control bit settings. A special AES3 direct output format is included, which allows the serial output port access to the V, U, and C bits embedded in the serial audio data stream. When using the part in AES3 direct-output format, the de-emphasis filter must be off (see Section 14.4 on page 38). The P bit, which would normally be a parity bit, is replaced by a Z bit, which is used to indicate the start of each block. The received channel status block start signal is also available as the RCBL pin in Hardware Mode and through a GPO pin in Software Mode.

In master mode, the left/right clock (OLRCK) and the serial bit clock (OSCLK) are outputs, derived from the recovered RMCK clock. In slave mode, OLRCK and OSCLK are inputs. OLRCK is normally synchronous to the appropriate master clock, but OSCLK can be asynchronous and discontinuous if required. By appropriate phasing of OLRCK and control of the serial clocks, multiple CS8416's can share one serial port. OLRCK should be continuous, but the duty cycle can be less than the specified typical value of 50% if enough serial clocks are present in each phase to

clock all the data bits. When in slave mode, the serial audio output port cannot be set for right-justified data. The CS8416 allows immediate mute of the serial audio output port audio data by the MUTESAO bit of Control Register 1.

For more information about serial audio formats, refer to the Cirrus Logic applications note AN282, “The 2-Channel Serial Audio Interface: A Tutorial”, available at www.cirrus.com.



	SOMS*	SOSF*	SORES[1:0]*	SOJUST*	SODEL*	SOSPOL*	SOLRPOL*
Left-Justified	X	X	XX	0	0	0	0
I²S	X	X	XX	0	1	0	1
Right-Justified	1	X	XX	1	0	0	0
AES3 Direct	X	X	11	0	0	0	0

X = don’t care to match format, but does need to be set to the desired setting
* See Serial Output Data Format Register Bit Descriptions for an explanation of the meaning of each bit

Figure 7. Serial Audio Output Example Formats

7.1 Slip/Repeat Behavior

When using the serial audio output port in slave mode with an OLRCK input that is asynchronous to the incoming AES3 data, the interrupt bit OSLIP (bit 5 in the Interrupt 1 Status register, 0Dh) is provided to indicate when repeated or dropped samples occur. Refer to Figure 8 for the AES3 data format diagram.

When the serial output port is configured as slave, depending on the relative frequency of OLRCK to the input AES3 data (Z/X) preamble frequency, the data will be slipped or repeated at the output of the CS8416.

After a fixed delay from the Z/X preamble (a few periods of the internal clock, which is running at 256Fs), the circuit will look back in time until the previous Z/X preamble and check which of the following conditions occurred:

1. If during that time, the internal data buffer was not updated, a slip has occurred. Data from the previous frame will be output and OSLIP will be set to 1. Due to the OSLIP bit being “sticky,” it will remain 1 until the register is read. It will then be reset until another slip/repeat condition occurs.
2. If during that time the internal data buffer did not update between two positive or negative edges (depending on OLRPOL) of OLRCK, a repeat has occurred. In this case, the buffer data was updated twice, so the part has lost one frame of data. This event will also trigger OSLIP to be set to 1. Due to the OSLIP bit being “sticky,” it will remain 1 until the register is read. It will then be reset until another slip/repeat condition occurs.
3. If during that time, it did see a positive edge on OLRCK (or negative edge if the SOLRPOL is set to 1) no slip or repeat has happened. Due to the OSLIP bit being “sticky,” it will remain in its previous state until either the register is read or a slip/repeat condition occurs.

If the user reads OSLIP as soon as the event triggers, over a long period of time the rate of occurring INT will be equal to the difference in frequency between the input AES data and the slave serial output LRCK. The CS8416 uses a hysteresis window when a slip/repeat event occurs. The slip/repeat is triggered when an edge of OLRCK passes a window size from the beginning of the Z/X preamble. Without the hysteresis window, jitter on OLRCK with a frequency very close to Fs could slip back and forth, causing multiple slip/repeat events. The CS8416 uses a hysteresis window to ensure that only one slip/repeat happens even with jitter on OLRCK

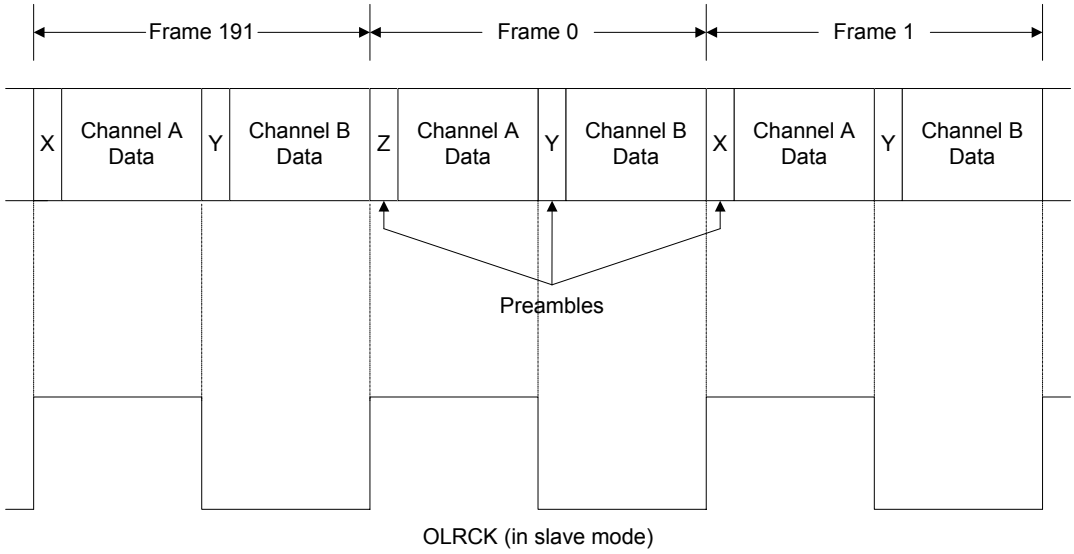


Figure 8. AES3 Data Format