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CIRRUS LOGIC®
Leading the Digital Entertainment Revolution™

CS8427

96 kHz Digital Audio Interface Transceiver

Features

- Complete EIAJ CP1201, IEC-60958, AES3, S/PDIF-compatible Transceiver
- +5.0 V Analog Supply (VA+)
- +3.3 V or +5.0 V Digital Interface (VL+)
- Flexible 3-wire Serial Digital I/O Ports
- Adjustable Sample Rate up to 96 kHz
- Low-jitter Clock Recovery
- Pin and Microcontroller Read/Write Access to Channel Status and User Data
- Microcontroller and Standalone Modes
- Differential Cable Driver and Receiver
- On-chip Channel Status and User Data Buffer Memories Permit Block Reads & Writes
- OMCK System Clock Mode
- Decodes Audio CD Q Sub-code

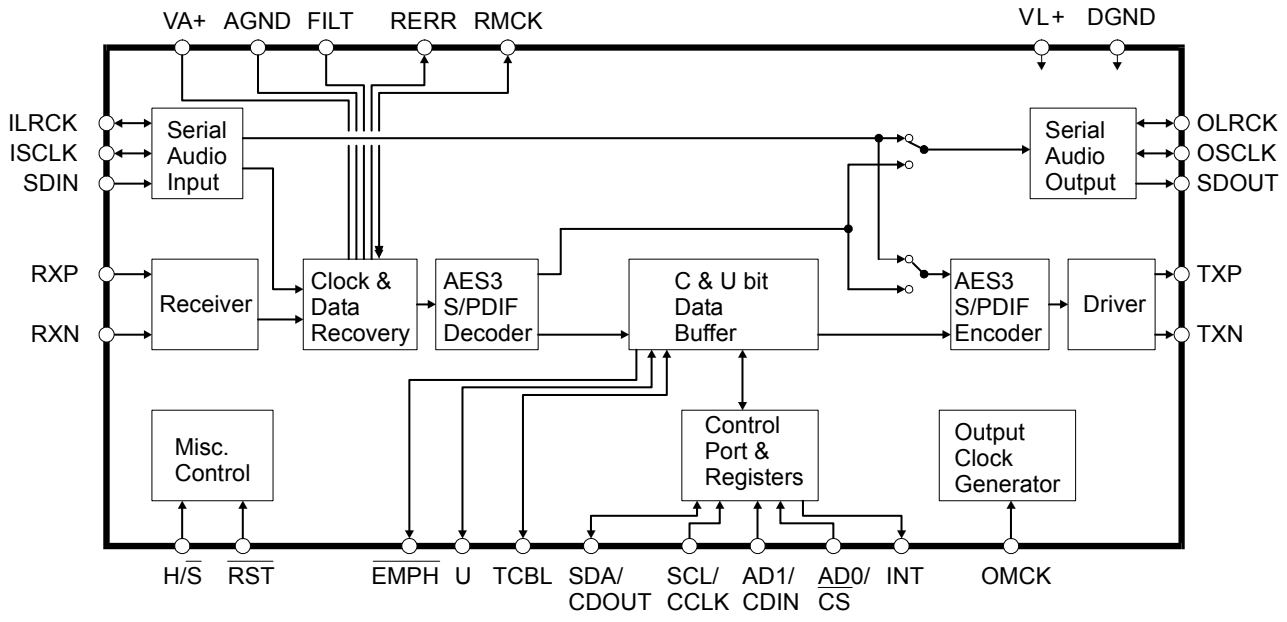
General Description

The CS8427 is a stereo digital audio transceiver with AES3 and serial digital audio inputs, AES3 and serial digital audio outputs, and includes comprehensive control ability through a 4-wire microcontroller port. Channel status and user data are assembled in block-sized buffers, making read/modify/write cycles easy.

A low-jitter clock recovery mechanism yields a very clean recovered clock from the incoming AES3 stream.

Target applications include A/V receivers, CD-R, DVD receivers, multimedia speakers, digital mixing consoles, effects processors, set-top boxes, and computer and automotive audio systems.

The CS8427 is available in 28-pin SOIC and TSSOP packages in Commercial (-10°C to +70°C) and Automotive (-40°C to +85°C) grades. The CDB8427 Customer Demonstration Board is also available for device evaluation and implementation suggestions. Please see "Ordering Information" on page 49 for complete details.



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1. CHARACTERISTICS AND SPECIFICATIONS

All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.

SPECIFIED OPERATING CONDITIONS

AGND, DGND = 0 V, all voltages with respect to 0 V.

Parameter		Symbol	Min	Typ	Max	Units
Power Supply Voltage	(Note 1)	VA+ VL+	4.5 2.85	5.0 3.3 or 5.0	5.5 5.5	V V
Ambient Operating Temperature:	'-CS', 'CSZ' & '-CZ' '-DS' & '-DZ'	T_A	-10 -40	- -	+70 +85	°C

Notes: 1. I²C protocol is supported only in VL+ = 5.0 V mode.

ABSOLUTE MAXIMUM RATINGS

AGND, DGND = 0 V; all voltages with respect to 0 V. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Parameter		Symbol	Min	Max	Units
Power Supply Voltage		VL+,VA+	-	6.0	V
Input Current, Any Pin Except Supplies	(Note 2)	I_{in}	-	±10	mA
Input Voltage		V_{in}	-0.3	(VL+) + 0.3	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Notes: 2. Transient currents of up to 100 mA will not cause SCR latch-up.

DC ELECTRICAL CHARACTERISTICS

AGND = DGND = 0 V; all voltages with respect to 0 V.

Parameters		Symbol	Min	Typ	Max	Units
Power-down Mode (Note 3)						
Supply Current in power down	VA+		-	20	-	µA
	VL+ = 3.3 V		-	60	-	µA
	VL+ = 5.0 V		-	60	-	µA
Normal Operation (Note 4)						
Supply Current at 48 kHz frame rate	VA+		-	6.3	-	mA
	VL+ = 3.3 V		-	30.1	-	mA
	VL+ = 5.0 V		-	46.5	-	mA
Supply Current at 96 kHz frame rate	VA+		-	6.6	-	mA
	VL+ = 3.3 V		-	44.8	-	mA
	VL+ = 5.0 V		-	76.6	-	mA

Notes: 3. Power Down Mode is defined as $\overline{RST}$ = LO with all clocks and data lines held static.

4. Normal operation is defined as $\overline{RST}$ = HI.

DIGITAL INPUT CHARACTERISTICS

Parameters	Symbol	Min	Typ	Max	Units
Input Leakage Current	I_{in}	-	±1	±10	µA
Differential Input Voltage, RXP0 to RXN	V_{TH}	-	200	-	mV

DIGITAL INTERFACE SPECIFICATIONS

AGND = DGND = 0 V; all voltages with respect to 0 V.

Parameters		Symbol	Min	Max	Units
High-Level Output Voltage (I_{OH} = -3.2 mA), except TXP/TXN		V_{OH}	(VL+) - 1.0	-	V
Low-Level Output Voltage (I_{OH} = 3.2 mA), except TXP/TXN		V_{OL}	-	0.4	V
High-Level Output Voltage, TXP, TXN	(23 mA at VL+ = 5.0 V)		(VL+) - 0.7	-	V
	(15.2 mA at VL+ = 3.3 V)		(VL+) - 0.7	-	V
Low-Level Output Voltage, TXP, TXN	(23 mA at VL+ = 5.0 V)		-	0.7	V
	(15.2 mA at VL+ = 3.3 V)		-	0.7	V
High-Level Input Voltage, except RXP, RXN		V_{IH}	2.0	(VL+) + 0.3	V
Low-Level Input Voltage, except RXP, RXN	(Note 5)	V_{IL}	-0.3	0.4/0.8	V

Notes: 5. At 5.0 V mode, V_{IL} = 0.8 V (Max), at 3.3 V mode, V_{IL} =0.4 V (Max).

TRANSMITTER CHARACTERISTICS

Parameters		Symbol	Min	Typ	Max	Units
TXP Output Resistance	VL+ = 5.0 V	R_{TXP}	-	26	-	Ω
	VL+ = 3.3 V		-	40	-	Ω
TXN Output Resistance	VL+ = 5.0 V	R_{TXN}	-	26	-	Ω
	VL+ = 3.3 V		-	40	-	Ω

SWITCHING CHARACTERISTICS

Inputs: Logic 0 = 0 V, Logic 1 = VL+; C_L = 20 pF.

Parameter	Symbol	Min	Typ	Max	Units
RST pin Low Pulse Width		200	-	-	µs
OMCK Frequency for OMCK = 512 * Fso		4.1	-	55.3	MHz
OMCK Low and High Width for OMCK = 512 * Fso		7.2	-	-	ns
OMCK Frequency for OMCK = 384 * Fso		3.1	-	41.5	MHz
OMCK Low and High Width for OMCK = 384 * Fso		10.8	-	-	ns
OMCK Frequency for OMCK = 256 * Fso		2.0	-	27.7	MHz
OMCK Low and High Width for OMCK = 256 * Fso		14.4	-	-	ns
PLL Clock Recovery Sample Rate Range		8.0	-	108.0	kHz
RMCK output jitter (Note 6)		-	200	-	ps RMS
RMCK output duty cycle		40	50	60	%
RMCK Input Frequency (Note 7)		1.8	-	27.7	MHz
RMCK Input Low and High Width (Note 7)		14.4	-	-	ns
AES3 Transmitter Output Jitter		-	-	1	ns

Notes: 6. Cycle-to-cycle locking to RXP/RXN using 32 to 96 kHz external PLL filter components.

7. PLL is bypassed (RXD1:0 bits in the Clock Source Control register set to 10b), clock is input to the RMCK pin.

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORTS

Inputs: Logic 0 = 0 V, Logic 1 = VL+; C_L = 20 pF.

Parameter		Symbol	Min	Typ	Max	Units
OSCLK Active Edge to SDOUT Output Valid	(Note 8)	t_{dpd}	-	-	20	ns
SDIN Setup Time Before ISCLK Active Edge	(Note 8)	t_{ds}	20	-	-	ns
SDIN Hold Time After ISCLK Active Edge	(Note 8)	t_{dh}	20	-	-	ns
Master Mode						
O/RMCK to I/OSCLK active edge delay	(Note 8, 9)	t_{smd}	0	-	10	ns
O/RMCK to I/OLRCK delay	(Note 10)	t_{lmd}	0	-	10	ns
I/OSCLK and I/OLRCK Duty Cycle			-	50	-	%
Slave Mode						
I/OSCLK Period	(Note 11)	t_{sckw}	36	-	-	ns
I/OSCLK Input Low Width		t_{sckl}	14	-	-	ns
I/OSCLK Input High Width		t_{sckh}	14	-	-	ns
I/OSCLK Active Edge to I/OLRCK Edge	(Note 8, 10, 12)	t_{lrckd}	20	-	-	ns
I/OLRCK Edge Setup Before I/OSCLK Active Edge	(Note 8, 10, 13)	t_{lrcks}	20	-	-	ns

Notes:
8. The active edges of ISCLK and OSCLK are programmable.
9. When OSCLK, OLRCK, ISCLK, and ILRCK are derived from OMCK they are clocked from its rising edge. When these signals are derived from RMCK, they are clocked from its falling edge.
10. The polarity of ILRCK and OLRCK is programmable.
11. No more than 128 SCLK per frame.
12. This delay is to prevent the previous I/OSCLK edge from being interpreted as the first one after I/OLRCK has changed.
13. This setup time ensures that this I/OSCLK edge is interpreted as the first one after I/OLRCK has changed.

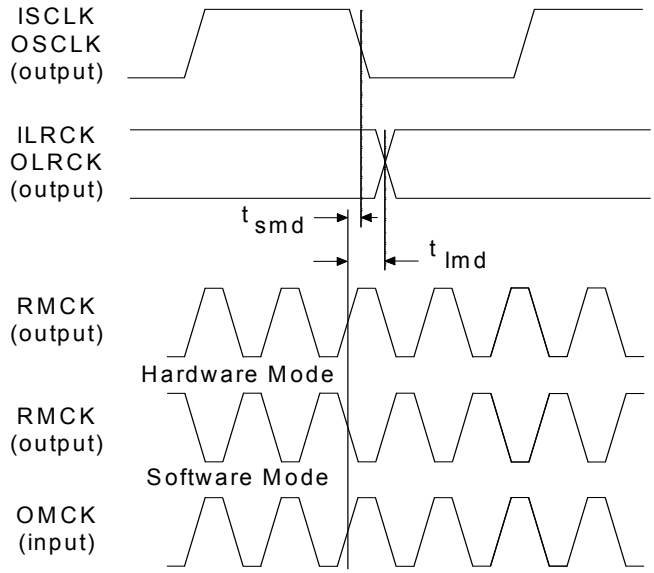


Figure 1. Audio Port Master Mode Timing

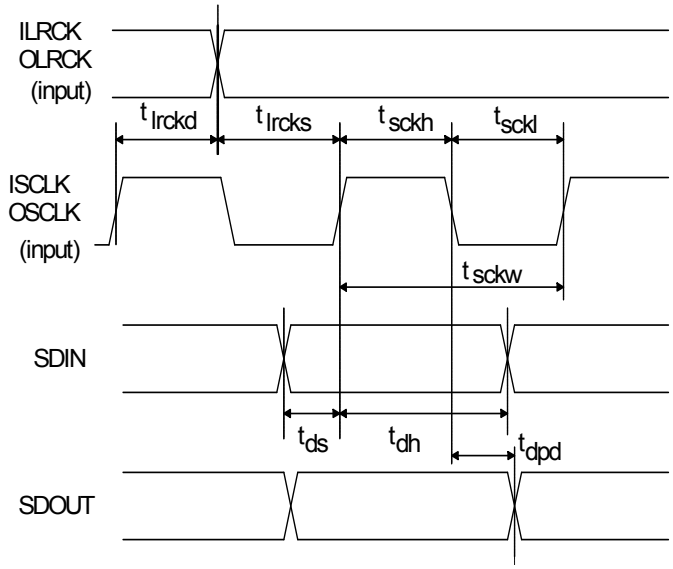


Figure 2. Audio Port Slave Mode and Data Input Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI MODE

Inputs: Logic 0 = 0 V, Logic 1 = VL+; C_L = 20 pF.

Parameter		Symbol	Min	Typ	Max	Units
CCLK Clock Frequency	(Note 14)	f_{sck}	0	-	6.0	MHz
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	-	ns
CCLK Low Time		t_{scl}	66	-	-	ns
CCLK High Time		t_{sch}	66	-	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	-	ns
CCLK Rising to DATA Hold Time	(Note 15)	t_{dh}	15	-	-	ns
CCLK Falling to CDOUT Stable		t_{pd}	-	-	50	ns
Rise Time of CDOUT		t_{r1}	-	-	25	ns
Fall Time of CDOUT		t_{f1}	-	-	25	ns
Rise Time of CCLK and CDIN	(Note 16)	t_{r2}	-	-	100	ns
Fall Time of CCLK and CDIN	(Note 16)	t_{f2}	-	-	100	ns

Notes: 14. If Fso or Fsi is lower than 46.875 kHz, the maximum CCLK frequency should be less than 128 Fso and less than 128 Fsi. This is dictated by the timing requirements necessary to access the Channel Status and User Bit buffer memory. Access to the control register file can be carried out at the full 6 MHz rate. The minimum allowable input sample rate is 8 kHz, so choosing CCLK to be less than or equal to 1.024 MHz should be safe for all possible conditions.

15. Data must be held for sufficient time to bridge the transition time of CCLK.

16. For f_{sck} < 1 MHz.

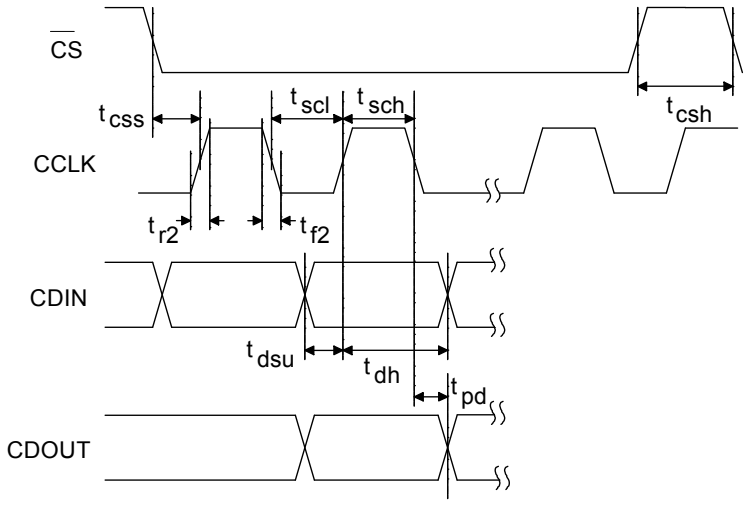


Figure 3. SPI Mode timing

SWITCHING CHARACTERISTICS - CONTROL PORT - I²C MODE

Note 17, Inputs: Logic 0 = 0 V, Logic 1 = VL+; C_L = 20 pF.

Parameter	Symbol	Min	Typ	Max	Units
SCL Clock Frequency	f_{scl}	-	-	100	kHz
Bus Free Time Between Transmissions	t_{buf}	4.7	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	-	µs
Clock Low Time	t_{low}	4.7	-	-	µs
Clock High Time	t_{high}	4.0	-	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	-	µs
SDA Hold Time from SCL Falling (Note 18)	t_{hdd}	0	-	-	µs
SDA Setup Time to SCL Rising	t_{sud}	250	-	-	ns
Rise Time of Both SDA and SCL Lines	t_r	-	-	25	ns
Fall Time of Both SDA and SCL Lines	t_f	-	-	25	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	-	µs

Notes: 17. I²C protocol is supported only in VL+ = 5.0 V mode.

18. Data must be held for sufficient time to bridge the 25 ns transition time of SCL.

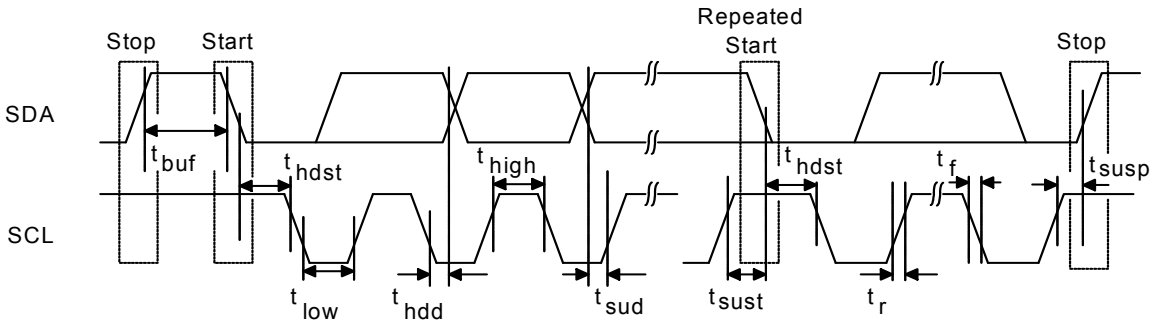
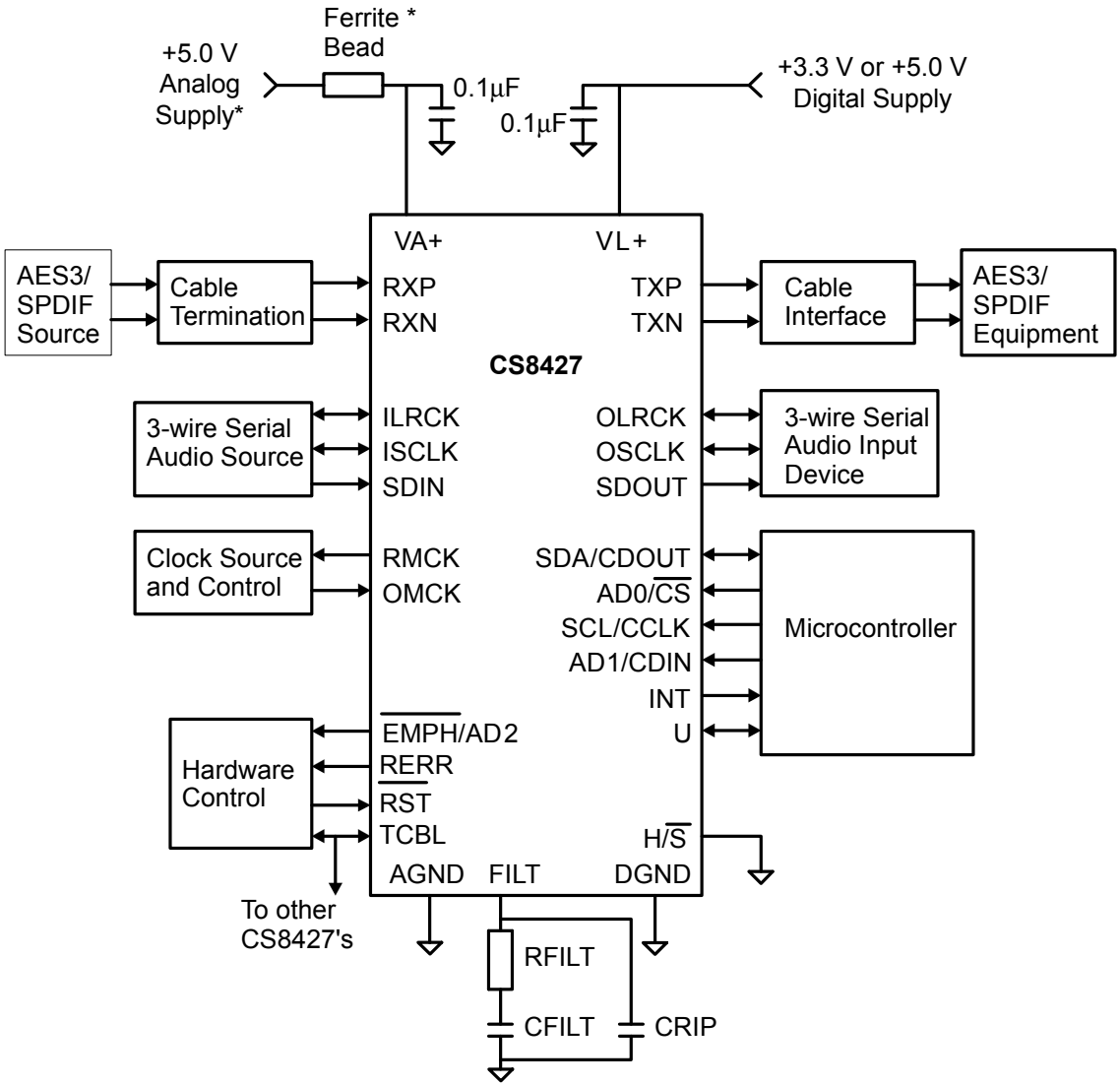


Figure 4. I²C Mode timing

2. TYPICAL CONNECTION DIAGRAM



* A separate analog supply is only necessary in applications where RMCK is used for a jitter sensitive task. For applications where RMCK is not used for a jitter sensitive task, connect VA+ to VD+ via a ferrite bead. Keep the decoupling capacitor between VA+ and AGND.

Figure 5. Recommended Connection Diagram for Software Mode

3. GENERAL DESCRIPTION

The CS8427 is an AES3 transceiver intended to be used in digital audio systems. Such systems include digital mixing consoles, effects processors, digital recorders, and computer multimedia systems.

3.1 Audio Input/Output Ports

The CS8427 has the following Audio ports:

- Serial Audio Input Port
- Serial Audio Output Port
- AES3 or S/PDIF Receiver
- AES3 or S/PDIF Transmitter

The Serial Audio ports use a three-wire format. This consists of a serial audio data stream, a left-right clock defining the boundaries of the audio sample frames, and a serial clock signal clocking the data bits.

A Serial Audio port may operate in either Master or Slave mode. When a port is a Master, it supplies the left-right clock and the serial clock to the external device that is sending or receiving the serial data. A port in slave mode must have its left-right clock and its serial clock supplied by an external device so that it may send or receive serial audio data.

The input sample rate is determined by the stream applied to the Serial Audio Input or to the AES3 Receiver. A phase-locked loop recovers RMCK, the input master clock signal, from the chosen input stream.

The output from the device may be through the Serial Audio Output, the AES3 Transmitter, or from both simultaneously. In some configurations, all audio ports of the device may be in use at the same time.

3.2 Serial Control Port

Besides the functional blocks already described, the device also has a control port that allows the user to read and write the control registers that configure the part. The control port is capable of operating in either SPI or I²C serial mode. This port also has access to buffer memory that allows the user to control what is transmitted in the Channel Status and User bits of the outgoing AES3 stream.

The control port is clocked by the serial clock signal that the user's microcontroller sends it. The MCU can read and write the registers even when the RMCK and OMCK clocks are not running. The Channel Status and User bit buffer memories depend on clocking from RMCK and OMCK. They will not function unless the clocks are running, and the RUN bit in the Clock Source Control register is set.

There is also an interrupt signal associated with the Serial Control Port and the internal registers. The format of the interrupt may be chosen by a register setting. There are two interrupt status registers and their associated interrupt mask registers.

3.3 Channel Status and User bit Memory

The memory architecture consists of three buffers to handle the Channel Status information, and another three buffers to handle the User bits. The data recovery logic extracts the Channel Status and User bits from the AES3 stream and places them in their respective D buffers. Each buffer contains 384 bits.

This is enough memory to hold a complete block of Channel Status bits from both A and B channels and a complete block of User bits.

When the D buffers are full, the chip transfers their contents into the E buffers. While in the E buffers the Channel Status and User bits may be read or written through the control port. This allows the user to alter them to suit the needs of the application. The control bit BSEL, in the Channel Status Data Buffer Control register, determines whether the control port has access to the Channel Status bits or the User bits. The AES3 encoder reads the Channel Status and User bits from the F buffers and inserts them into the outgoing AES3 stream. After the F buffers bits are transmitted, the device transfers the current contents of the E buffers into the F buffers.

In applications using AES3 in and AES3 out, the CS8427 can automatically transceive user data that conforms to the IEC60958 format. The CS8427 also gives the user access to the bits necessary to comply with the serial copy management system (SCMS).

In applications where the user want to read/modify/write the Channel Status information that requires a microcontroller to actively manage the

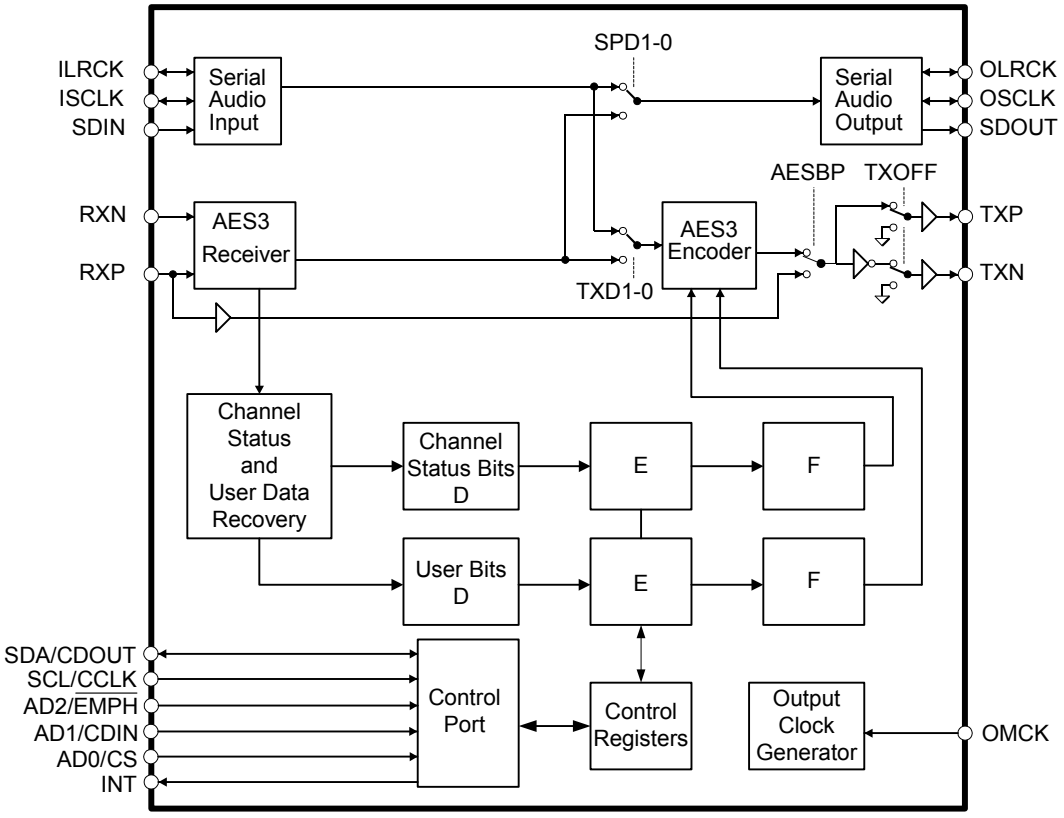


Figure 6. CS8427 Internal Block Diagram

Channel Status bits. The part also has a feature that allows the first five bytes of Channel Status memory to be configured and transmitted in each channel status block without change. See "Appendix A: External AES3/SPDIF/IEC60958 Transmitter and Receiver Components" on page 50 for a tutorial in Channel Status and User bit management.

3.4 AES3 and S/PDIF Standards Documents

This data sheet assumes that the user is familiar with the AES3 and S/PDIF data formats. It is advisable to have current copies of the AES3 and IEC60958 specifications on hand for easy reference.

The latest AES3 standard is available from the Audio Engineering Society or ANSI at www.aes.org or www.ansi.org. Obtain the latest IEC60958 standard from ANSI or from the International Electrotechnical Commission at www.iec.ch. The latest EIAJ CP-1201 standard is available from the Japanese Electronics Bureau.

Crystal Application Note AN22: *Overview of Digital Audio Interface Data Structures* contains a useful tutorial on digital audio specifications, but it should not be considered a substitute for the standards.

The paper, *An Understanding and Implementation of the SCMS Serial Copy Management System for Digital Audio Transmission*, by Clifton Sanchez, is an excellent tutorial on SCMS. It is available from the AES as preprint 3518.

4. DATA I/O FLOW AND CLOCKING OPTIONS

The CS8427 can be configured for several connectivity alternatives, called data flows. Figure 7. "Software Mode Audio Data Flow Switching Options" on page 19 shows the data flow switching, along with the control register bits which control the switches; this drawing only shows the audio data paths for simplicity. This drawing only shows the audio data paths for simplicity. Figure 8 shows the internal

clock routing and the associated control register bits. The clock routing constraints determine which data routing options are actually usable. Users should note that not all the possible data flow switch setting combinations are valid, because of the clock distribution architecture.

The AESBP switch, shown in Figure 7, allows a TTL level bi-phase, mark-encoded data stream connected to RXP to be routed to the TXP and TXN pin drivers. The TXOFF switch causes the TXP and TXN outputs to be driven to ground.

There are two possible clock sources. The first, designated the recovered clock, is the output of the PLL, and is output through the RMCK pin. The input to the PLL can be either the incoming AES3 data stream or the ILRCK word rate clock from the serial audio input port. The second clock is input through the OMCK pin and would normally be a crystal derived stable clock. The Clock Source Control Register bits determine which clock is used to operate the CS8427.

The CS8427 has another constraint related to the state machine that governs the startup of the part. The startup state machine doesn't complete its process until the PLL has locked unless one is in the transmitter dataflow (See Figure 10). The consequence of this is that the transmitter will not transmit until the PLL has locked. If you wish to use the part in transceiver mode and this constraint is a problem, there is a work around. Start the part up in its default configuration and allow the PLL to lock to a signal on the ILRCK pin, then without stopping the part, reconfigure it to the transceiver mode.

By studying the following drawings and appropriately setting the Data Flow Control and Clock Source Control register bits, the CS8427 can be configured to fit a variety of customer requirements. Please note that applications implementing both the Serial Audio Output Port and the AES3 Transmitter must operate at the same sample rate because they are both controlled by the same clock source.

Figure 9 shows the entire data path clocked by the PLL generated recovered clock. Figure 10 illustrates a standard AES3 receiver function. Figure 11 shows a standard AES3 transmitter function without PLL. Figure 12 shows a standard AES3 transmitter function with PLL.

5. THREE-WIRE SERIAL AUDIO PORTS

A 3-wire serial audio input port and a 3-wire serial audio output port is provided. Each port can be adjusted to suit the attached device by setting the control registers. The following parameters are adjustable: master or slave, serial clock frequency, audio data resolution, left or right justification of the data relative to left/right clock, optional 1-bit cell delay of the 1st data bit, the polarity of the bit clock, and the polarity of the left/right clock. By setting the appropriate control bits, many formats are possible.

Figure 15 shows a selection of common input formats, along with the control bit settings. It should be noted that in right justified mode, the serial audio output data is “MSB extended”. This means that in a sub-frame where the MSB of the data is '1', all bits preceding the MSB in the sub-frame will also be '1'. Conversely, in a sub-frame where the MSB of the data is '0', all bits preceding the MSB in the sub-frame will also be '0'.

The clocking of the input section of the CS8427 may be derived from the incoming ILRCK word rate clock, using the on-chip PLL. The PLL operation is described in “AES3 Receiver” on page 16. In the case of use with the serial audio input port, the PLL locks onto the leading edges of the ILRCK clock.

Figure 16 shows a selection of common output formats, along with the control bit settings. A special AES3 direct output format is included, which allows serial output port access to the V, U, and C bits embedded in the serial audio data stream. The P bit is replaced by a Z bit that marks the subframe just prior to the start of each block. This format is only available when the serial audio output port is being clocked by the AES3 receiver recovered clock.

In master mode, the left/right clock and the serial bit clock are outputs, derived from the appropriate clock domain master clock.

In slave mode, the left/right clock and the serial bit clock are inputs. The left/right clock must be synchronous to the appropriate master clock, but the serial bit clock can function in asynchronous burst mode if desired. By appropriate phasing of the left/right clock and control of the serial clocks, CS8427’s can be multiplexed to share one serial port. The left/right clock should be continuous, but the duty cycle does not have to be 50%, provided that enough serial clocks are present in each phase to clock all the data bits. When in slave mode, the serial audio output port must not be set to right justified data.

When using the serial audio output port in slave mode with an OLRCK input which is asynchronous to the port’s data source, an interrupt bit (OSLIP) is provided to indicate when repeated or dropped samples occur.

6. AES3 RECEIVER

The CS8427 includes an AES3 digital audio receiver and an AES3 digital audio transmitter. A comprehensive buffering scheme provides read/write access to the channel status and user data. This buffering scheme is described in "Appendix B: Channel Status and User Data Buffer Management".

The AES3 receiver accepts and decodes audio and digital data according to the AES3, IEC60958 (S/PDIF), and EIAJ CP-1201 interface standards. The receiver consists of a differential input stage, accessed through pins RXP and RXN, a PLL based clock recovery circuit, and a decoder which separates the audio data from the channel status and user data.

External components are used to terminate and isolate the incoming data cables from the CS8427. These components are detailed in "Appendix A: External AES3/SPDIF/IEC60958 Transmitter and Receiver Components" on page 50.

6.1 OMCK System Clock Mode

A special mode is available that allows the clock that is being input through the OMCK pin to be output through the RMCK pin. This feature is controlled by the SWCLK bit in control register 1. When the PLL loses lock, the frequency of the VCO drops to 300 kHz. The SWCLK function allows the clock from RMCK to be used as a clock in the system without any disruption when input is removed from the Receiver. This clock switching is performed glitch free. None of the internal circuitry that is clocked from the PLL is driven by the OMCK being output from RMCK. This function is available only in software mode.

6.2 PLL, Jitter Attenuation, and Varispeed

Please see Appendix C for general description of the PLL, selection of recommended PLL filter components, and layout considerations. Figure 5 shows the recommended configuration of the two capacitors and one resistor that comprise the PLL filter.

6.3 Error Reporting and Hold Function

While decoding the incoming AES3 data stream, the CS8427 can identify several kinds of error, indicated in the Receiver Error register. The UNLOCK bit indicates whether the PLL is locked to the incoming AES3 data. The V bit reflects the current validity bit status. The BIP (bi-phase) error bit indicates an error in incoming bi-phase coding. The PAR (parity) bit indicates a received parity error.

The error bits are "sticky": they are set on the first occurrence of the associated error and will remain set until the user reads the register through the control port. This enables the register to log all unmasked errors that occurred since the last time the register was read.

The Receiver Error Mask register allows masking of individual errors. The bits in this register serve as masks for the corresponding bits of the Receiver Error Register. If a mask bit is set to 1, the error is unmasked, which implies the following: its occurrence will be reported in the receiver error register, induce a pulse on RERR, invoke the occurrence of a RERR interrupt, and affect the current audio sample according to the status of the HOLD bits. The HOLD bits allow a choice of holding the previous sample, replacing the current sample with zero (mute), or not changing the current audio sample. If a mask bit is set to 0, the error is masked, which implies the following: its occurrence will not be reported in the receiver error register, will not induce a pulse on RERR or generate a RERR interrupt, and will not affect the current audio sample. The QCRC and CCRC errors do not affect the current audio sample, even if unmasked

6.4 Channel Status Data Handling

The first two bytes of the Channel Status block are decoded into the Receiver Channel Status register. The setting of the CHS bit in the Channel Status Data Buffer Control register determines whether the channel status decodes are from the A channel (CHS = 0) or B channel (CHS = 1).

The PRO (professional) bit is extracted directly. For consumer data, the COPY (copyright) bit is extracted, and the category code and L bits are decoded to determine SCMS status, indicated by the ORIG (original) bit. If the category code is set to

General on the incoming AES3 stream, copyright will always be indicated even when the stream indicates no copyright. Finally, the AUDIO bit is extracted and used to set an AUDIO indicator, as described in the Non-Audio Auto-Detection section below.

If 50/15 µs pre-emphasis is detected, the state of the EMPH pin is adjusted accordingly.

The encoded channel status bits which indicate sample word length are decoded according to AES3-1992 or IEC 60958. Audio data routed to the serial audio output port is unaffected by the word length settings - all 24 bits are passed on as received.

"Appendix B: Channel Status and User Data Buffer Management" on page 52 describes the overall handling of Channel Status and User bit data.

6.5 User Data Handling

The incoming user data is buffered in a user accessible buffer. Various automatic modes of re-transmitting received User data are provided. The Appendix: Channel Status and User Data Buffer Management describes the overall handling of CS and U data.

Received User data may also be output to the U pin, under the control of a control register bit. Depending on the data flow and clocking options selected, there may not be a clock available to qualify the U data output. Figure 13 illustrates the timing.

If the incoming user data bits have been encoded as Q-channel subcode, the data is decoded and presented in ten consecutive register locations. An interrupt may be enabled to indicate the decoding of a new Q-channel block, which may be read through the control port.

6.6 Non-Audio Auto Detection

An AES3 data stream may be used to convey non-audio data, thus it is important to know whether the incoming AES3 data stream is digital audio or not. This information is typically conveyed in channel status bit 1 (AUDIO), which is extracted automatically by the CS8427. However, certain non-audio sources, such as AC3® or MPEG encoders, may not adhere to this convention, and the bit may not be properly set. The CS8427 AES3 receiver can detect such non-audio data. This is accomplished by looking for a 96-bit sync code, consisting of 0x0000, 0x0000, 0x0000, 0x0000, 0xF872, and 0x4E1F. When the sync code is detected, an internal AUTODETECT signal will be asserted. If no additional sync codes are detected within the next 4096 frames, AUTODETECT will be de-asserted until another sync code is detected. The AUDIO bit in the Receiver Channel Status register is the logical OR of AUTODETECT and the received channel status bit 1. If non-audio data is detected, the data is still processed exactly as if it were normal audio. It is up to the user to mute the outputs as required.

7. AES3 TRANSMITTER

The AES3 transmitter encodes and transmits audio and digital data according to the AES3, IEC60958 (S/PDIF), and EIAJ CP-1201 interface standards. Audio and control data are multiplexed together and bi-phase, mark encoded. The resulting bit stream is driven to an output connector either directly or through a transformer.

The transmitter clock may be derived from the clock input pin OMCK, or from the incoming data. If OMCK is asynchronous to the data source, an interrupt bit (TSLIP) is provided that will go high every time a data sample is dropped or repeated. Be aware that the pattern of slips does not have hysteresis and so the occurrence of the interrupt condition is not deterministic.

The channel status (C) and user channel (U) bits in the transmitted data stream are taken from storage areas within the CS8427. The user can manually access the internal storage or configure the CS8427 to run in one of several automatic modes. The Appendix: Channel Status and User Data Buffer Management provides detailed descriptions of each automatic mode and describes methods of manually accessing the storage areas. The transmitted user data can optionally be input through the U pin, under the control of a control port register bit. Figure 13 shows the timing requirements for clocking U data through the U pin.

7.1 Transmitted Frame and Channel Status Boundary Timing

The TCBL pin is used to control or indicate the start of transmitted channel status block boundaries and may be used as an input or output.

In some applications, it may be necessary to control the precise timing of the transmitted AES3 frame boundaries. This may be achieved in three ways:

1) With TCBL set to input, driving TCBL high for >3 OMCK clocks will cause a frame start, as well as a new channel status block start.
2) If the AES3 output comes from the AES3 input, setting TCBL as output will cause AES3 output frame boundaries to align with AES3 input frame boundaries.
3) If the AES3 output comes from the serial audio input port while the port is in slave mode and TCBL is set to output, the start of the A channel sub-frame will be aligned with the leading edge of IL-CK.

7.2 TXN and TXP Drivers

The line drivers are low skew, low impedance, differential outputs capable of driving cables directly. Both drivers are set to ground during reset ($\overline{RST}$ = low), when no AES3 transmit clock is provided, and optionally under the control of a register bit. The CS8427 also allows immediate mute of the AES3 transmitter audio data through a control register bit.

External components are used to terminate and isolate the external cable from the CS8427. These components are detailed in Appendix A: External AES3/SPDIF/IEC60958 Transmitter and Receiver Components.

8. MONO MODE OPERATION

An AES3 stream may be used in more than one way to transmit 96-kHz sample rate data. One method is to double the frame rate of the current format. This results in a stereo signal with a sample rate of 96 kHz, carried over a single twisted pair cable. An alternate method is implemented using the two sub-frames in a 48-kHz frame rate AES3 signal to carry consecutive samples of a mono signal, resulting in a 96-kHz sample rate stream. This allows older equipment, whose AES3 transmitters and receivers are not rated for 96-kHz frame rate operation, to handle 96-kHz sample rate information. In this “mono mode”, two AES3 cables are needed for stereo data transfer. The CS8427 offers mono mode operation for the AES3 receiver and the AES3 transmitter. The receiver and transmitter sections may be independently set to mono mode through the MMR and MMT control bits.

8.1 Receiver Mono Mode

The receiver mono mode effectively doubles the input frame rate, Fsi. The clock output on the RMCK pin tracks Fsi, and thus is doubled in frequency compared to stereo mode. The receiver will run at a frame rate of Fsi/2, and the serial audio output port will run at Fsi. Sub-frame A data will be routed to both the left and right data fields on SD-OUT. Similarly, sub-frame B data will be routed to both the left and right data fields of the next word clock cycle of SDOUT.

Using receiver mono mode is only necessary if the serial audio output port must run at 96 kHz. If the CS8427 is kept in normal stereo mode and receives AES3 data arranged in mono mode, the serial audio output port will run at 48 kHz, with left and right data fields representing consecutive audio samples.

8.2 Transmitter Mono Mode

In transmitter mono mode, the input port will run at the audio sample rate (Fso), while the AES3 transmitter frame rate will be at Fso/2. Consecutive left or right channel serial audio data samples may be selected for transmission on the A and B subframes, and the channel status block transmitted is also selectable.

Using transmitter mono mode is only necessary if the incoming audio sample rate is already at 96 kHz and contains both left and right audio data words. The “mono mode” AES3 output stream may also be achieved by keeping the CS8427 in normal stereo mode and placing consecutive audio samples in the left and right positions of an incoming data stream with a 48-kHz word rate.

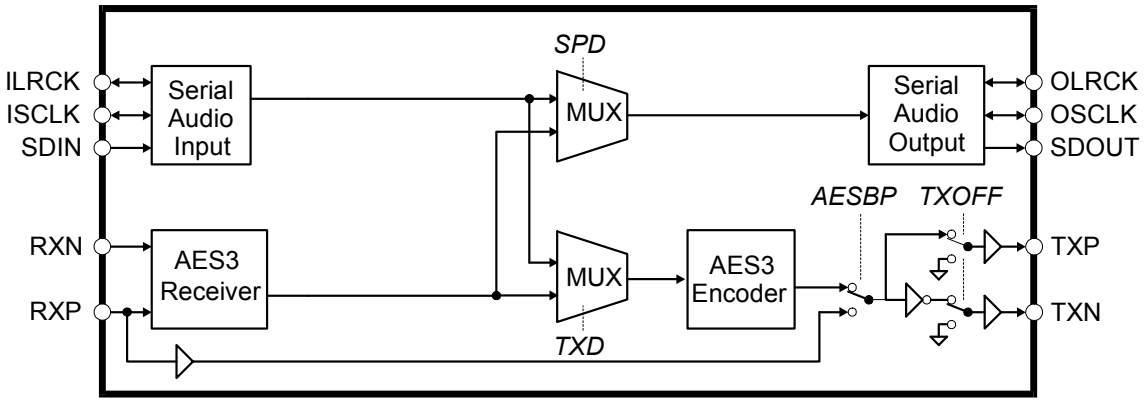
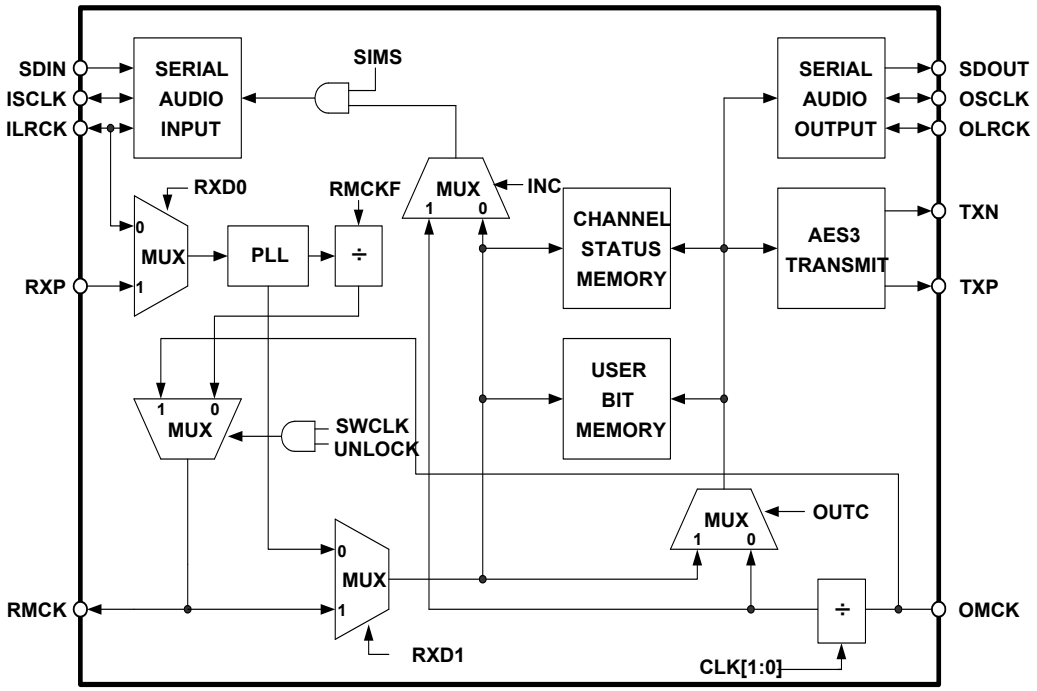
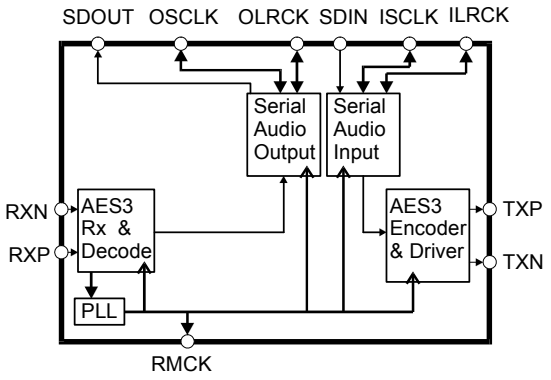


Figure 7. Software Mode Audio Data Flow Switching Options



* Note: When SWCLK mode is enabled, signal input on OMCK is only output through RMCK and not routed back through the RXD1 multiplexer; RMCK is not bi-directional in this mode.

Figure 8. CS8427 Clock Routing

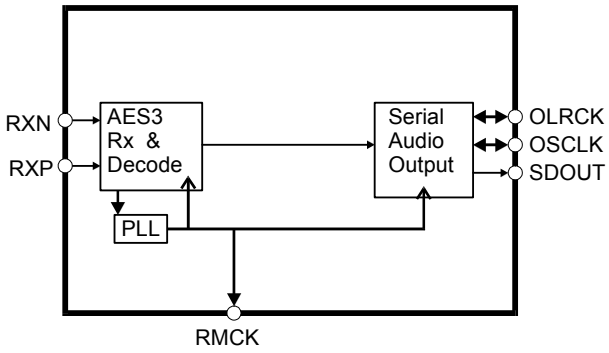


Data Flow Control Bits
TXD1-0: 01
SPD1-0: 10

Clock Source Control Bits
OUTC: 1
INC: 0
RXD1-0: 01

Figure 9. AES3 Input to Serial Audio Output, Serial Audio Input to AES3 Out

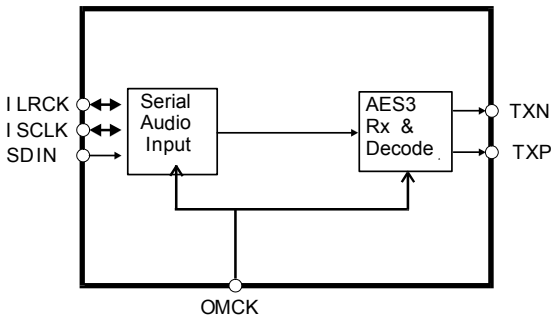
NOTE: Applications implementing both the Serial Audio Output Port and the AES3 Transmitter must operate at the same sample rate because they are both controlled by the same clock source.



Data Flow Control Bits
TXD1-0: 10
SPD1-0: 10
TXOFF : 1

Clock Source Control Bits
OUTC: 1
INC: 0
RXD1-0: 01

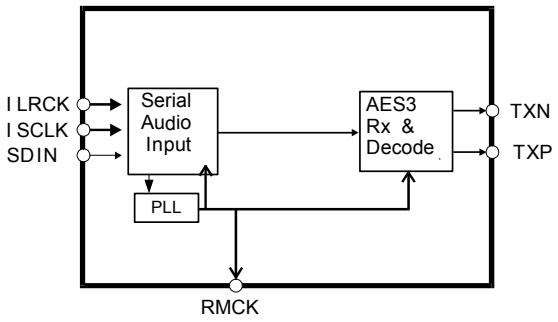
Figure 10. AES3 Input to Serial Audio Output Only



Data Flow Control Bits
TXD1-0: 01
SPD1-0: 01

Clock Source Control Bits
OUTC: 0
INC: 1
RXD1-0: 00

Figure 11. Input Serial Port to AES3 Transmitter without PLL

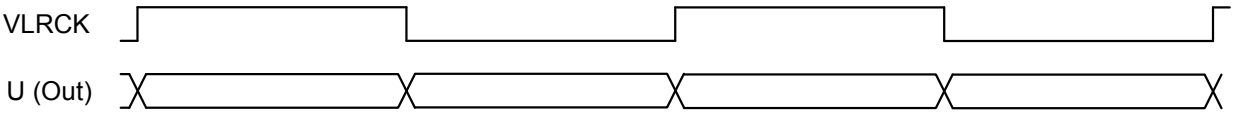


Data Flow Control Bits
TXD1-0: 01
SPD1-0: 01

Clock Source Control Bits
OUTC: 1
INC: 0
RXD1-0: 00

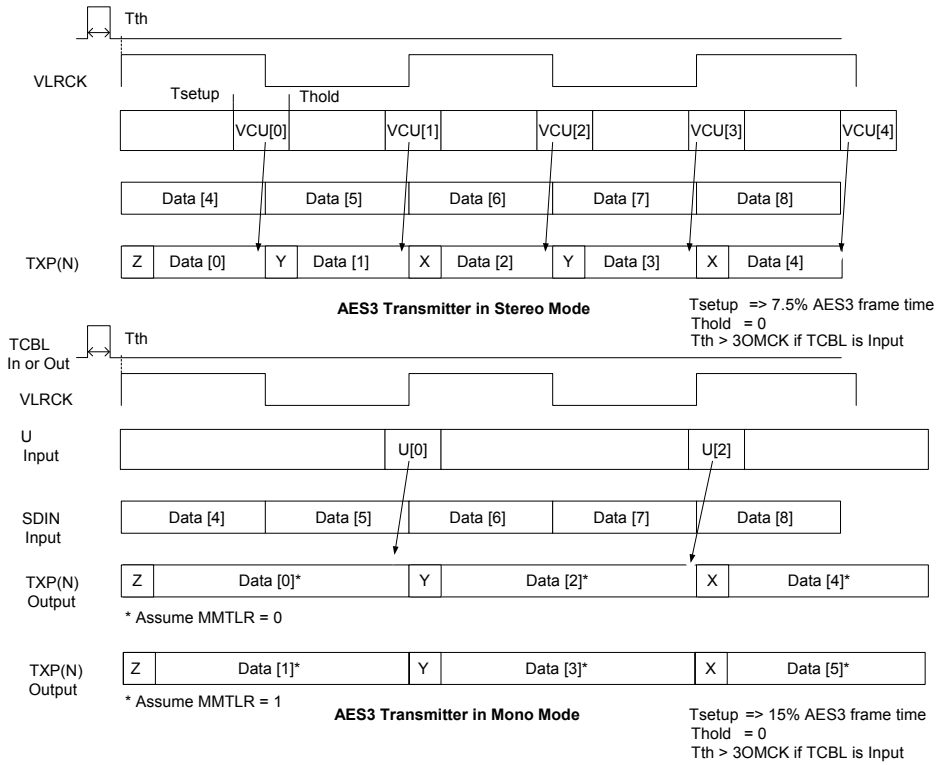
Figure 12. Input Serial Port to AES3 Transmitter with PLL

NOTE: In this mode, ILRCK and ISCLK are inputs only.



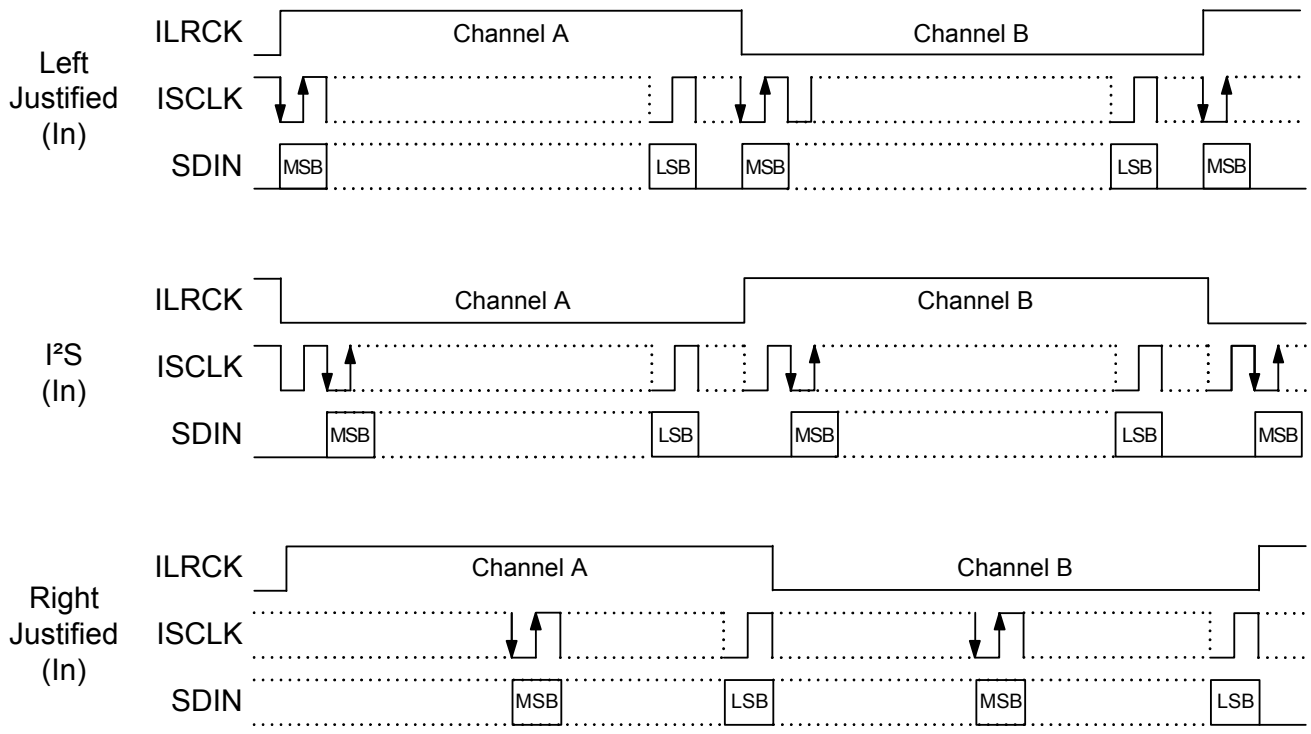
VLRCK is a virtual word clock, which may not exist, but is used to illustrate the U timing.
VLRCK duty cycle is 50%. VLRCK frequency is always equal to the incoming frame rate.
If the serial audio output port is in master mode, VLRCK = OLRCK.
If the serial audio output port is in slave mode, then VLRCK needs to be externally created, if required.
U transitions are aligned within ±1% of VLRCK period to VLRCK edges

Figure 13. AES3 Receiver Timing for U pin output data



VLRCK is a virtual word clock, which may not exist, is used to illustrate the CUV timing.
VLRCK duty cycle is 50%.
In stereo mode, VLRCK frequency = AES3 frame rate. In mono mode, ALRCK frequency = 2xAES3 frame rate.
If the serial audio input port is on slave mode and TCBL is an output, then VLRCK=ILRCK if SILRPOL=0 and VLRCK= $\overline{\text{ILRCK}}$ if SILRPOL =1.
If the serial audio input port is in master mode and TCBL is an input, then VLRCK=ILRCK if SILRPOL=0 and VLRCK= $\overline{\text{ILRCK}}$ if SILRPOL =1.

Figure 14. AES3 Transmitter Timing for C, U and V pin input data



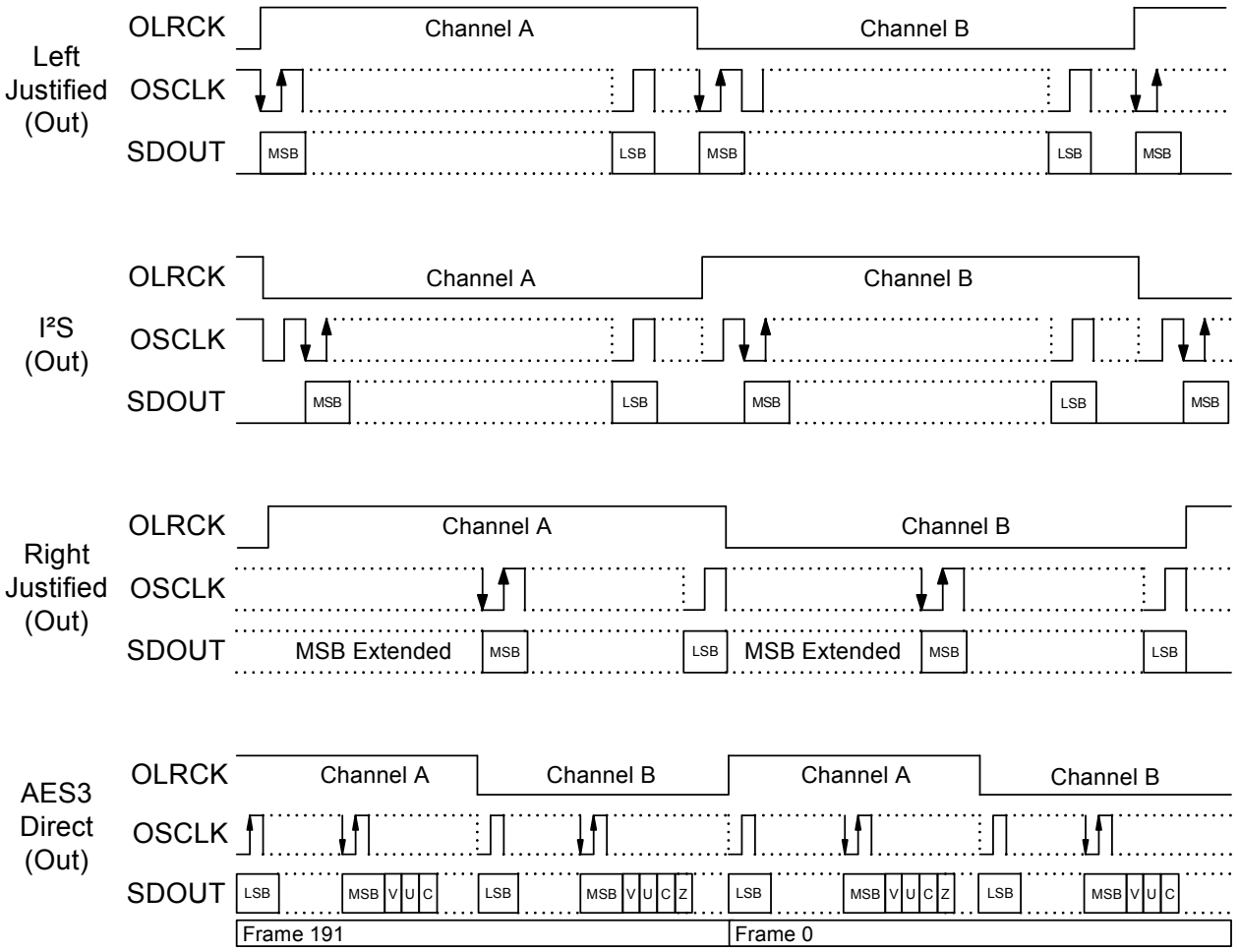
	SIMS*	SISF*	SIRES*[1:0]	SIJUST*	SIDEL*	SISPOL*	SILRPOL*
Left Justified	X	X	00+	0	0	0	0
I²S	X	X	00+	0	1	0	1
Right Justified	X	X	XX	1	0	0	0

X = don't care to match format, but does need to be set to the desired setting

+ I²S can accept an arbitrary number of bits, determined by the number of ISCLK cycles

* See Serial Input Port Data Format Register Bit Descriptions for an explanation of the meaning of each bit

Figure 15. Serial Audio Input Example Formats



	SOMS*	SOSF*	SORES[1:0]*	SOJUST*	SODEL*	SOSPOL*	SOLRPOL*
Left Justified	X	X	XX	0	0	0	0
I²S	X	X	XX	0	1	0	1
Right Justified	1	X	XX	1	0	0	0
AES3 Direct	X	X	11	0	0	0	0

X = don't care to match format, but does need to be set to the desired setting

* See Serial Output Data Format Register Bit Descriptions for an explanation of the meaning of each bit

Figure 16. Serial Audio Output Example Formats

9. CONTROL PORT DESCRIPTION AND TIMING

The control port is used to access the registers, allowing the CS8427 to be configured for the desired operational modes and formats. In addition, Channel Status and User data may be read and written through the control port. The operation of the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has two modes: SPI and I²C, with the CS8427 acting as a slave device. SPI mode is selected if there is a high to low transition on the AD0/CS pin after the RST pin has been brought high. I²C mode is selected by connecting the AD0/CS pin to VL+ or DGND, thereby permanently selecting the desired AD0 bit address state.

9.1 SPI™ Mode

In SPI mode, CS is the CS8427 chip select signal; CCLK is the control port bit clock (input into the CS8427 from the microcontroller); CDIN is the input data line from the microcontroller; CDOUT is the output data line to the microcontroller. Data is clocked in on the rising edge of CCLK and out on the falling edge.

Figure 17 shows the operation of the control port in SPI mode. To write to a register, bring CS low. The first seven bits on CDIN form the chip address and must be 0010000b. The eighth bit is a read/write indicator (R/W), which should be low to write. The next eight bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data which will be placed into the register designated by the MAP. During writes, the CDOUT output stays in the Hi-Z state. It may be externally pulled high or low with a 47 kΩ resistor, if desired.

There is a MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, the MAP will stay constant for successive read or writes. If INCR is set to a 1, then the MAP will autoincrement after each byte is read or written, allowing block reads or writes of successive registers.

To read a register, the MAP has to be set to the correct address by executing a partial write cycle which finishes (CS high) immediately after the MAP byte. The MAP auto increment bit (INCR) may be set or not, as desired. To begin a read, bring CS low, send out the chip address, and set the read/write bit (R/W) high. The next falling edge of CCLK will clock out the MSB of the addressed register (CDOUT will leave the high impedance state). If the MAP auto increment bit is set to 1, the data for successive registers will appear consecutively.

9.2 I²C Mode

In I²C mode, SDA is a bidirectional data line. Data is clocked into and out of the part by SCL, with the clock to data relationship as shown in Figure 18. There is no CS pin. Each individual CS8427 is given a unique address. Pins AD0 and AD1 form the two least significant bits of the chip address and should be connected to VL+ or DGND as desired. The EMPH pin is used to set the AD2 bit, by connecting a resistor from the EMPH pin to VL+ or to DGND. The state of the pin is sensed while the CS8427 is being reset. The upper four bits of the seven bit address field are fixed at 0010b. To communicate with a CS8427, the chip address field, which is the first byte sent to the CS8427, should be 0010b followed by the settings of the EMPH, AD1, and AD0. The eighth bit of the address is the R/W bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit, ACK, which is output from the CS8427 after each input byte is read. The ACK bit is input to the CS8427 from the microcontroller after each transmitted byte. I²C mode is supported only with VL+ = 5.0 V.

9.3 Interrupts

The CS8427 has a comprehensive interrupt capability. The INT output pin is intended to drive the interrupt input pin on the host microcontroller. The INT pin may be set to be active low, active high, or active low with no active pull-up transistor. This last