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CS8900A

Product Data Sheet

FEATURES

- **Single-Chip IEEE 802.3 Ethernet Controller with Direct ISA-Bus Interface**
- **Maximum Current Consumption = 55 mA (5V Supply)**
- **3 V or 5 V Operation**
- **Industrial Temperature Range**
- **Comprehensive Suite of Software Drivers Available**
- **Efficient PacketPage™ Architecture Operates in I/O and Memory Space, and as DMA Slave**
- **Full Duplex Operation**
- **On-Chip RAM Buffers Transmit and Receive Frames**
- **10BASE-T Port with Analog Filters, Provides:**
  - Automatic Polarity Detection and Correction
- **AUI Port for 10BASE2, 10BASE5 and 10BASE-F**
- **Programmable Transmit Features:**
  - Automatic Re-transmission on Collision
  - Automatic Padding and CRC Generation
- **Programmable Receive Features:**
  - Stream Transfer for Reduced CPU Overhead
  - Auto-Switch Between DMA and On-Chip Memory
  - Early Interrupts for Frame Pre-Processing
  - Automatic Rejection of Erroneous Packets
- **EEPROM Support for Jumperless Configuration**
- **Boot PROM Support for Diskless Systems**
- **Boundary Scan and Loopback Test**
- **LED Drivers for Link Status and LAN Activity**
- **Standby and Suspend Sleep Modes**

Crystal LAN™ *Ethernet Controller*

DESCRIPTION

The CS8900A is a low-cost Ethernet LAN Controller optimized for the Industry Standard Architecture (ISA) bus and general purpose microcontroller busses. Its highly-integrated design eliminates the need for costly external components required by other Ethernet controllers. The CS8900A includes on-chip RAM, 10BASE-T transmit and receive filters, and a direct ISA-Bus interface with 24 mA Drivers.

In addition to high integration, the CS8900A offers a broad range of performance features and configura-tionoptions. Its unique PacketPage architecture automatically adapts to changing network traffic pat-terns and available system resources. The result is increased system efficiency.

The CS8900A is available in a 100-pin LQFP package ideally suited for small form-factor, cost-sensitive Ether-net applications. With the CS8900A, system engineers can design a complete Ethernet circuit that occupies less than 1.5 square inches (10 sq. cm) of board space.

ORDERING INFORMATION

CS8900A-CQZ	0° to 70° C	5V	LQFP-100	Lead free
CS8900A-IQZ	-40° to 85° C	5V	LQFP-100	Lead free
CS8900A-CQ3Z	0° to 70° C	3.3V	LQFP-100	Lead free
CS8900A-IQ3Z	-40° to 85° C	3.3V	LQFP-100	Lead free

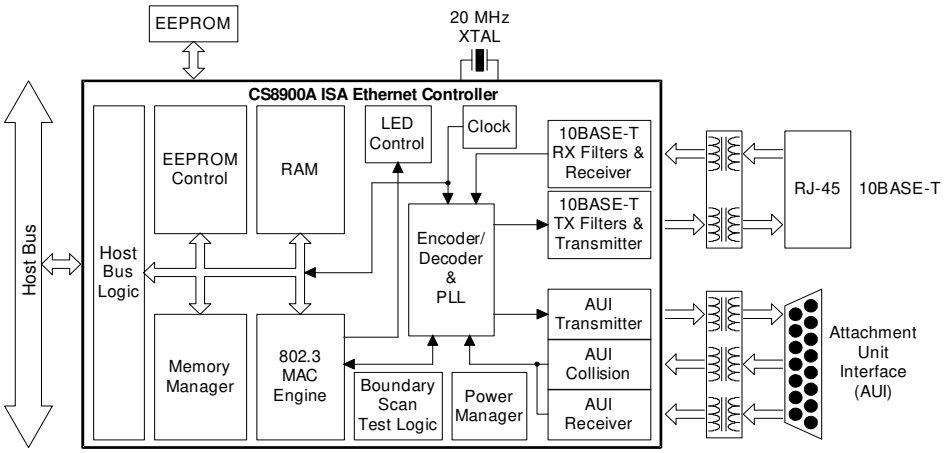

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Table 1. Revision History

Release	Date	Changes
PP4	APR 2001	Preliminary Release, revision 4 Page 13: **INTRQ[0:2]** changed to **INTRQ[0..3]** Page 41: Added bit definitions for Revisions C and D Page 56: **PacketPage base + 0218h** changed to **PacketPage base + 0128h** Page 81: Table 19: **Register 5, LRxCTL** changed to **Register 5, RxCTL** Page 86: Table 23: **0410h to 011h** changed to **0410h to 0411h**
F2	JUL 2004	Added ordering information for the -CQ3Z lead free part
F3	SEP 2004	Added ordering information for the -CQZ lead free part
F4	AUG 2007	Added industrial temperature range Pb-free devices
F5	SEP 2010	Page 1: Removed lead-containing device ordering information Page 113, 124: Updated Power Supply Current & AUI interface DC characteristics Page 119, 130: Updated AUI interface switching characteristics
F6	JUN 2015	Page 1, 10: Section 1.3.4: Removed evaluation kit ordering information Page 25: Table 8: Erase Register Opcode format updated Page 51: Section 4.4.4 edited to reference section 4.4.3 for detailed description Page 112, 123: Table 7.2, 8.2: Updated part numbers for Operating Conditions Page 112, 123: Table 7.3, 8.3: Updated Hardware Standby Mode Current for 3.3V and 5.0V power supplies Page 119, 130: Reference Notes numbering corrected Page 135: Acronym for Carrier Sense Signal corrected

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to www.cirrus.com

1.0 INTRODUCTION

1.1 General Description

The CS8900A is a true single-chip, full-duplex, Ethernet solution, incorporating all of the analog and digital circuitry needed for a complete Ethernet circuit. Major functional blocks include: a direct ISA-bus interface; an 802.3 MAC engine; integrated buffer memory; a serial EEPROM interface; and a complete analog front end with both 10BASE-T and AUI.

1.1.1 General Purpose and ISA-Bus Interface

Included in the CS8900A is a direct ISA-bus interface with full 24 mA drive capability. Its configuration options include a choice of four interrupts and three DMA channels (one of each selected during initialization). In Memory Mode, it supports Standard or Ready Bus cycles without introducing additional wait states. The bus can be configured to support many microcontroller and microcomputer busses.

1.1.2 Integrated Memory

The CS8900A incorporates a 4-Kbyte page of on-chip memory, eliminating the cost and board area associated with external memory chips. Unlike most other Ethernet controllers, the CS8900A buffers entire transmit and receive frames on chip, eliminating the need for complex, inefficient memory management schemes. In addition, the CS8900A operates in either Memory space, I/O space, or with external DMA controllers, providing maximum design flexibility.

1.1.3 802.3 Ethernet MAC Engine

The CS8900A's Ethernet Media Access Control (MAC) engine is fully compliant with the IEEE 802.3 Ethernet standard (ISO/IEC 8802-3, 1993), and supports full-duplex operation. It handles all aspects of Ethernet frame transmission and reception, including: collision detection, preamble generation and detection, and CRC generation and test. Programmable MAC features include automatic retransmission on collision, and automatic padding of transmitted frames.

1.1.4 EEPROM Interface

The CS8900A provides a simple and efficient serial EEPROM interface that allows configuration information to be stored in an optional EEPROM, and then loaded automatically at power-up. This eliminates the need for costly and cumbersome switches and jumpers.

1.1.5 Complete Analog Front End

The CS8900A's analog front end incorporates a Manchester encoder/decoder, clock recovery circuit, 10BASE-T transceiver, and complete Attachment Unit Interface (AUI). It provides manual and automatic selection of either 10BASE-T or AUI, and offers three on-chip LED drivers for link status, bus status, and Ethernet line activity.

The 10BASE-T transceiver includes drivers, receivers, and analog filters, allowing direct connection to low-cost isolation transformers. It supports 100, 120, and 150 Ω shielded and unshielded cables, extended cable lengths, and automatic receive polarity reversal detection and correction.

The AUI port provides a direct interface to 10BASE-2, 10BASE-5, and 10BASE-FL networks, and is capable of driving a full 50-meter AUI cable.

1.2 System Applications

The CS8900A is designed to work well in either motherboard or adapter applications.

1.2.1 Motherboard LANs

The CS8900A requires the minimum number of external components needed for a full Ethernet node. Its small-footprint package and

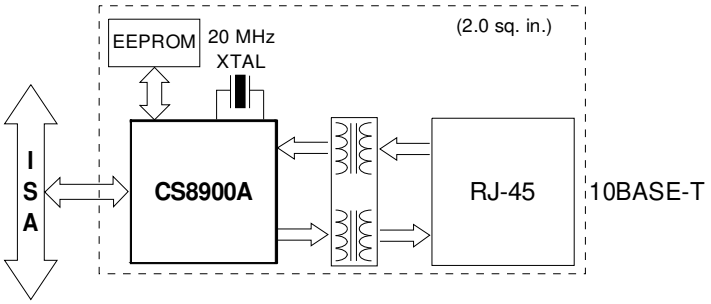


Figure 1. Complete Ethernet Motherboard Solution

high level of integration allow System Engineers to design a complete Ethernet circuit that occupies as little as 1.5 square inches of PCB area (Figure 1). In addition, the CS8900A's power-saving features and CMOS design make it a perfect fit for power-sensitive portable and desktop PCs. Motherboard design options include:

- An EEPROM can be used to store node-specific information, such as the Ethernet Individual Address and node configuration.
- The 20 MHz crystal oscillator may be replaced by a 20 MHz clock signal.

1.2.2 Ethernet Adapter Cards

The CS8900A's highly efficient PacketPage architecture, with StreamTransfer™ and Auto-Switch DMA options, make it an excellent choice for high-performance, low-cost ISA adapter cards (Figure 2). The CS8900A's wide range of configuration options and performance features allow engineers to design Ethernet solutions that meet their particular system requirements. Adapter card design options include:

- A Boot PROM can be added to support diskless applications.
- The 10BASE-T transmitter and receiver impedance can be adjusted to support 100, 120, or 150 Ohm twisted pair cables.
- An external Latchable-Address-bus decode circuit can be added to operate the CS8900A in Upper-Memory space.

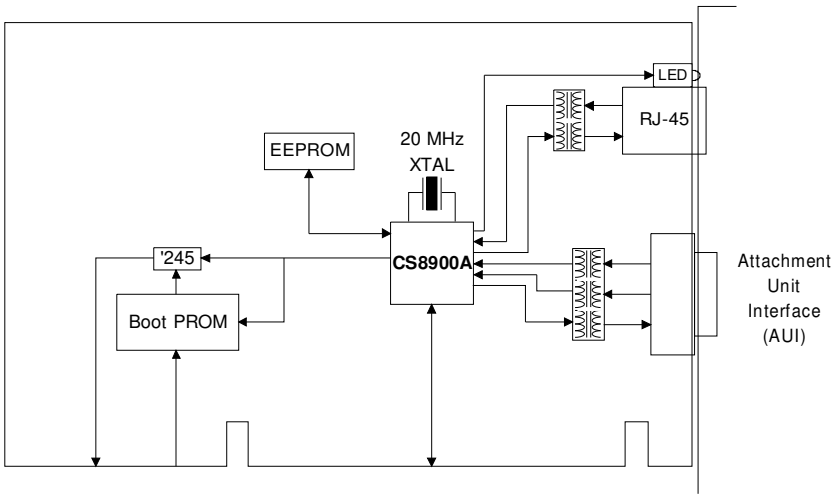


Figure 2. Full-Featured ISA Adapter Solution

- On-chip LED ports can be used for either optional LEDs, or as programmable outputs.

1.3 Key Features and Benefits

1.3.1 Very Low Cost

The CS8900A is designed to provide the lowest-cost Ethernet solution available for embedded applications, portable motherboards, non-ISA bus systems and adapter cards. Cost-saving features include:

- Integrated RAM eliminates the need for expensive external memory chips.
- On-chip 10BASE-T filters allow designers to use simple isolation transformers instead of more costly filter/transformer packages.
- The serial EEPROM port, used for configuration and initialization, eliminates the need for expensive switches and jumpers.
- The CS8900A is designed to be used on a 2-layer circuit board instead of a more expensive multilayer board.
- The 8900A-based solution offers the smallest footprint available, saving valuable printed circuit board area.
- A set of certified software drivers is available at no charge, eliminating the need for costly software development.

1.3.2 High Performance

The CS8900A is a full 16-bit Ethernet controller designed to provide optimal system performance by minimizing time on the ISA bus and CPU overhead per frame. It offers equal or superior performance for less money when compared to other Ethernet controllers. The CS8900A's PacketPage architecture allows software to select whichever access method is best suited to each particular CPU/ISA-bus configuration. When compared to older I/O-space designs, PacketPage is faster, simpler and more efficient.

To boost performance further, the CS8900A includes several key features that increase throughput and lower CPU overhead, including:

- StreamTransfer cuts up to 87% of interrupts to the host CPU during large block transfers.
- Auto-Switch DMA allows the CS8900A to maximize throughput while minimizing missed frames.
- Early interrupts allow the host to preprocess incoming frames.
- On-chip buffering of full frames cuts the amount of host bandwidth needed to manage Ethernet traffic.

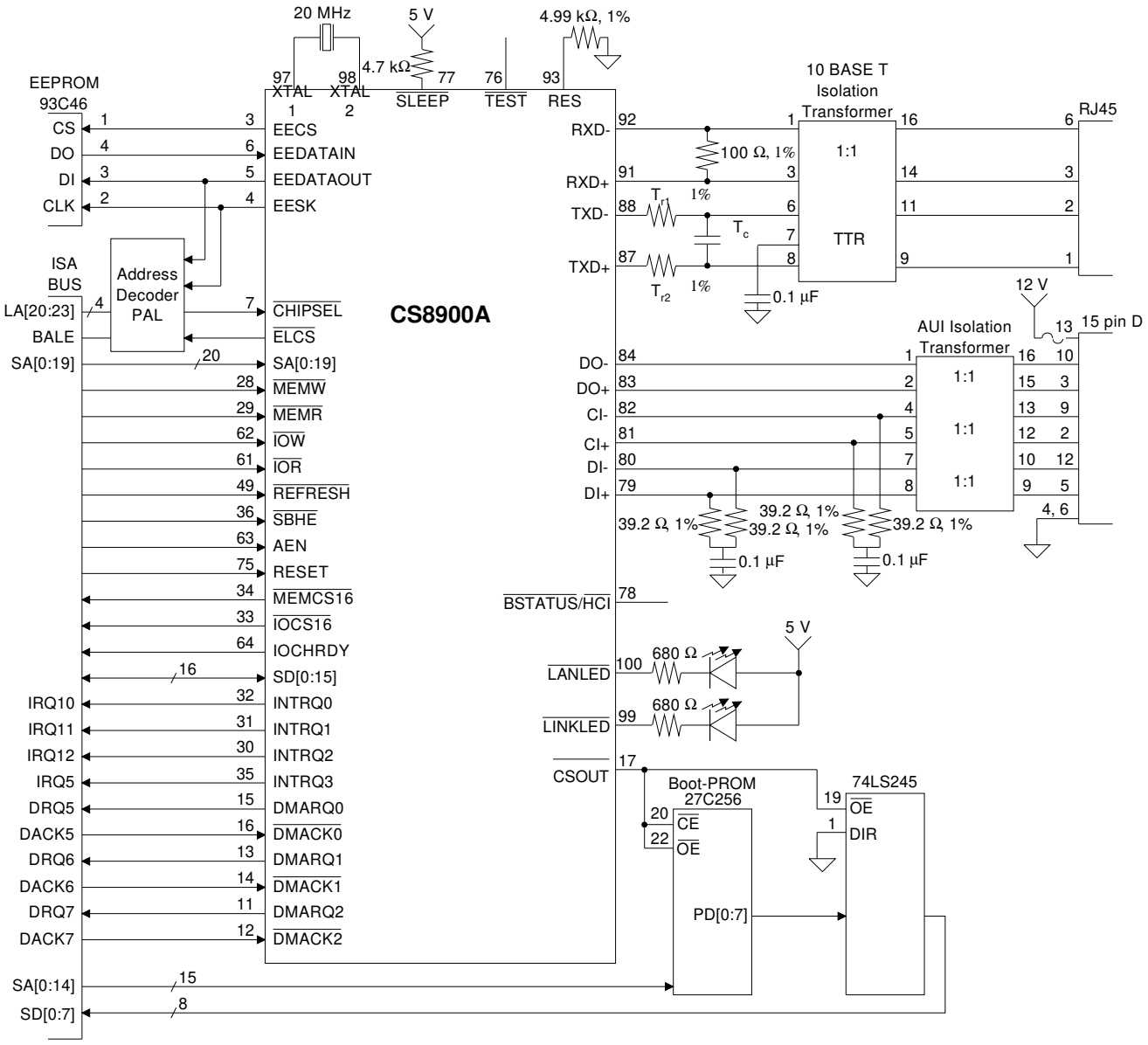
1.3.3 Low Power and Low Noise

For low power needs, the CS8900A offers three power-down options: Hardware Standby, Hardware Suspend, and Software Suspend. In Standby mode, the chip is powered down with the exception of the 10BASE-T receiver, which is enabled to listen for link activity. In either Hardware or Software Suspend mode, the receiver is disabled and power consumption drops to the micro-ampere range.

In addition, the CS8900A has been designed for very low noise emission, thus shortening the time required for EMI testing and qualification.

1.3.4 Complete Support

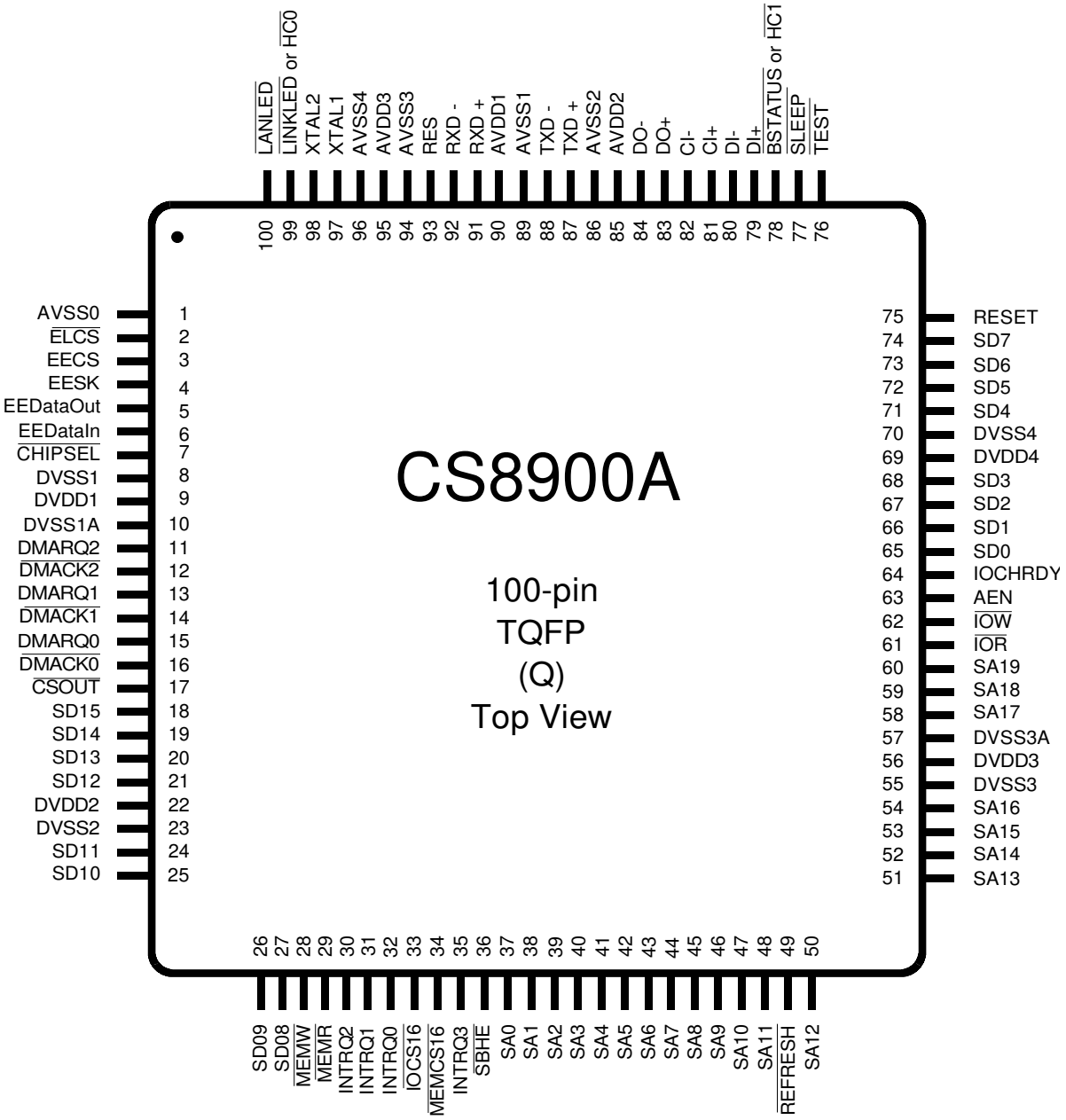
The CS8900A comes with a suite of software drivers for immediate use with most industry standard network operating systems. In addition, complete manufacturing packages are available, significantly reducing the cost and time required to produce new Ethernet products.



	5 Volt	3 Volt
TTR	1 : 1.414	1 : 2.5
T_{r1} and T_{r2}	24.3 Ω	8.0 Ω
T_c	69 pF	560 pF

Figure 3. Typical ISA Bus Connection Diagram

2.0 PIN DESCRIPTION



ISA Bus Interface

SA[0:19] - System Address Bus, Input PINS 37-48, 50-54, 58-60.

Lower 20 bits of the 24-bit System Address Bus used to decode accesses to CS8900A I/O and Memory space, and attached Boot PROM. SA0-SA15 are used for I/O Read and Write operations. SA0-SA19 are used in conjunction with external decode logic for Memory Read and Write operations.

SD[0:15] - System Data Bus, Bi-Directional with 3-State Output PINS 65-68, 71-74, 27-24, 21-18.

Bi-directional 16-bit System Data Bus used to transfer data between the CS8900A and the host.

RESET - Reset, Input PIN 75.

Active-high asynchronous input used to reset the CS8900A. Must be stable for at least 400 ns before the CS8900A recognizes the signal as a valid reset.

AEN - Address Enable, Input PIN 63.

When $\overline{\text{TEST}}$ is high, this active-high input indicates to the CS8900A that the system DMA controller has control of the ISA bus. When AEN is high, the CS8900A will not perform slave I/O space operations. When $\overline{\text{TEST}}$ is low, this pin becomes the shift clock input for the Boundary Scan Test. AEN should be inactive when performing an IO or memory access and it should be active during a DMA cycle.

$\overline{\text{MEMR}}$ - Memory Read, Input PIN 29.

Active-low input indicates that the host is executing a Memory Read operation.

$\overline{\text{MEMW}}$ - Memory Write, Input PIN 28.

Active-low input indicates that the host is executing a Memory Write operation.

$\overline{\text{MEMCS16}}$ - Memory Chip Select 16-bit, Open Drain Output PIN 34.

Open-drain, active-low output generated by the CS8900A when it recognizes an address on the ISA bus that corresponds to its assigned Memory space (CS8900A must be in Memory Mode with the MemoryE bit (Register 17, BusCTL, Bit A) set for MEMCS16 to go active). 3-Stated when not active.

$\overline{\text{REFRESH}}$ - Refresh, Input PIN 49.

Active-low input indicates to the CS8900A that a DRAM refresh cycle is in progress. When REFRESH is low, MEMR, MEMW, IOR, IOW, DMACK0, DMACK1, and DMACK2 are ignored.

$\overline{\text{IOR}}$ - I/O Read, Input PIN 61.

When $\overline{\text{IOR}}$ is low and a valid address is detected, the CS8900A outputs the contents of the selected 16-bit I/O register onto the System Data Bus. IOR is ignored if REFRESH is low.

$\overline{\text{IOW}}$ - I/O Write, Input PIN 62.

When $\overline{\text{IOW}}$ is low and a valid address is detected, the CS8900A writes the data on the System Data Bus into the selected 16-bit I/O register. $\overline{\text{IOW}}$ is ignored if REFRESH is low.

$\overline{\text{IOCS16}}$ - I/O Chip Select 16-bit, Open Drain Output PIN 33.

Open-drain, active-low output generated by the CS8900A when it recognizes an address on the ISA bus that corresponds to its assigned I/O space. 3-Stated when not active.

IOCHRDY - I/O Channel Ready, Open Drain Output PIN 64.

When driven low, this open-drain, active-high output extends I/O Read and Memory Read cycles to the CS8900A. This output is functional when the IOCHRDYE bit in the Bus Control register (Register 17) is clear. This pin is always 3-Stated when the IOCHRDYE bit is set.

$\overline{\text{SBHE}}$ - System Bus High Enable, Input PIN 36.

Active-low input indicates a data transfer on the high byte of the System Data Bus (SD8-SD15). After a hardware or a software reset, the CS8900A will be in 8-bit mode. Provide a HIGH to LOW and then LOW to HIGH transition on the SBHE signal before any 16-bit IO or memory access is done to the CS8900A.

INTRQ[0:3] - Interrupt Request, 3-State PINS 30-32, 35.

Active-high output indicates the presence of an interrupt event. Interrupt Request goes low once the Interrupt Status Queue (ISQ) is read as all 0's. Only one Interrupt Request output is used (one is selected during configuration). All non-selected Interrupt Request outputs are placed in a high-impedance state. (Section 3.2 on page 18 and Section 5.1 on page 78.)

DMARQ[0:2] - DMA Request, 3-State PINS 11, 13, and 15.

Active-high, 3-Stateable output used by the CS8900A to request a DMA transfer. Only one DMA Request output is used (one is selected during configuration). All non-selected DMA Request outputs are placed in a high-impedance state.

$\overline{\text{DMACK}}$[0:2] - DMA Acknowledge, Input PINS 12, 14, and 16.

Active-low input indicates acknowledgment by the host of the corresponding DMA Request output.

$\overline{\text{CHIPSEL}}$ - Chip Select, Input PIN 7.

Active-low input generated by external Latchable Address bus decode logic when a valid memory address is present on the ISA bus. If Memory Mode operation is not needed, CHIPSEL should be tied low. The CHIPSEL is ignored for IO and DMA mode of the CS8900A.

EEPROM and Boot PROM Interface

EESK - EEPROM Serial Clock, PIN 4.

Serial clock used to clock data into or out of the EEPROM.

EECS - EEPROM Chip Select, PIN 3.

Active-high output used to select the EEPROM.

EEDataIn - EEPROM Data In, Input Internal Weak Pullup PIN 6.

Serial input used to receive data from the EEPROM. Connects to the DO pin on the EEPROM. EEDataIn is also used to sense the presence of the EEPROM.

$\overline{\text{ELCS}}$ - External Logic Chip Select, Internal Weak Pullup PIN 2.

Bi-directional signal used to configure external Latchable Address (LA) decode logic. If external LA decode logic is not needed, ELCS should be tied low.

EEDataOut - EEPROM Data Out, PIN 5.

Serial output used to send data to the EEPROM. Connects to the DI pin on the EEPROM. When TEST is low, this pin becomes the output for the Boundary Scan Test.

$\overline{\text{CSOUT}}$ - Chip Select for External Boot PROM, PIN 17.

Active-low output used to select an external Boot PROM when the CS8900A decodes a valid Boot PROM memory address.

10BASE-T Interface

TXD+/TXD- - 10BASE-T Transmit, Differential Output Pair PINS 87 and 88.

Differential output pair drives 10 Mb/s Manchester-encoded data to the 10BASE-T transmit pair.

RXD+/RXD- - 10BASE-T Receive, Differential Input Pair PINS 91 and 92.

Differential input pair receives 10 Mb/s Manchester-encoded data from the 10BASE-T receive pair.

Attachment Unit Interface (AUI)

DO+/DO- - AUI Data Out, Differential Output Pair PINS 83 and 84.

Differential output pair drives 10 Mb/s Manchester-encoded data to the AUI transmit pair.

DI+/DI- - AUI Data In, Differential Input Pair PINS 79 and 80.

Differential input pair receives 10 Mb/s Manchester-encoded data from the AUI receive pair.

CI+/CI- - AUI Collision In, Differential Input Pair PINS 81 and 82.

Differential input pair connects to the AUI collision pair. A collision is indicated by the presence of a 10 MHz ± 15% signal with duty cycle no worse than 60/40.

General Pins

XTAL[1:2] - Crystal, Input/Output PINS 97 and 98.

A 20 MHz crystal should be connected across these pins. If a crystal is not used, a 20 MHz signal should be connected to XTAL1 and XTAL2 should be left open. (See Section 7.3 on page 112 and Section 7.7 on page 122.)

$\overline{\text{SLEEP}}$ - Hardware Sleep, Input Internal Weak Pullup PIN 77.

Active-low input used to enable the two hardware sleep modes: Hardware Suspend and Hardware Standby. (See Section 3.7 on page 27.)

$\overline{\text{LINKLED}}$ or $\overline{\text{HC0}}$ - Link Good LED or Host Controlled Output 0, Open Drain Output PIN 99.

When the HCE0 bit of the Self Control register (Register 15) is clear, this active-low output is low when the CS8900A detects the presence of valid link pulses. When the HC0E bit is set, the host may drive this pin low by setting the HCBO in the Self Control register.

$\overline{\text{BSTATUS}}$ or $\overline{\text{HC1}}$ - Bus Status or Host Controlled Output 1, Open Drain Output PIN 78.

When the HC1E bit of the Self Control register (Register 15) is clear, this active-low output is low when receive activity causes an ISA bus access. When the HC1E bit is set, the host may drive this pin low by setting the HCB1 in the Self Control register.

$\overline{\text{LANLED}}$ - LAN Activity LED, Open Drain Output PIN 100.

During normal operation, this active-low output goes low for 6 ms whenever there is a receive packet, a transmit packet, or a collision. During Hardware Standby mode, this output is driven low when the receiver detects network activity.

$\overline{\text{TEST}}$ - Test Enable, Input Internal Weak Pullup PIN 76.

Active-low input used to put the CS8900A in Boundary Scan Test mode. For normal operation, this pin should be high.

RES - Reference Resistor, Input PIN 93.

This input should be connected to a 4.99KΩ ± 1% resistor needed for biasing of internal analog circuits.

DVDD[1:4] - Digital Power, Power PINS 9, 22, 56, and 69.

Provides 5 V ± 5% power to the digital circuits of the CS8900A.

DVSS[1:4} and DVSS1A, DVSS3A - Digital Ground, Ground PINS 8, 10, 23, 55, 57, and 70.

Provides ground reference (0 V) to the digital circuits of the CS8900A.

AVDD[1:3] - Analog Power, Power PINS 90, 85, and 95.

Provides 5 V ± 5% power to the analog circuits of the CS8900A.

AVSS[0:4] - Analog Ground, Ground PINS 1, 89, 86, 94, 96.

Provide ground reference (0 V) to the analog circuits of the CS8900A.

3.0 FUNCTIONAL DESCRIPTION

3.1 Overview

During normal operation, the CS8900A performs two basic functions: Ethernet packet transmission and reception. Before transmission or reception is possible, the CS8900A must be configured.

3.1.1 Configuration

The CS8900A must be configured for packet transmission and reception at power-up or reset. Various parameters must be written into its internal Configuration and Control registers such as Memory Base Address; Ethernet Physical Address; what frame types to receive; and which media interface to use. Configuration data can either be written to the CS8900A by the host (across the ISA bus), or loaded automatically from an external EEPROM. Operation can begin after configuration is complete.

Section 3.3 on page 19 and Section 3.4 on page 21 describe the configuration process in detail. Section 4.4 on page 49 provides a detailed description of the bits in the Configuration and Control Registers.

3.1.2 Packet Transmission

Packet transmission occurs in two phases. In the first phase, the host moves the Ethernet frame into the CS8900A's buffer memory. The first phase begins with the host issuing a Transmit Command. This informs the CS8900A that a frame is to be transmitted and tells the chip when to start transmission (i.e. after 5, 381, 1021 or all bytes have been transferred) and how the frame should be sent (i.e. with or without CRC, with or without pad bits, etc.). The Host follows the Transmit Command with the Transmit Length, indicating how much buffer space is required. When buffer space is available, the host writes the Ethernet frame into the CS8900A's internal memory, either as a Memory or I/O space operation.

In the second phase of transmission, the CS8900A converts the frame into an Ethernet packet then transmits it onto the network. The second phase begins with the CS8900A transmitting the preamble and Start-of-Frame delimiter as soon as the proper number of bytes has been transferred into its transmit buffer (5, 381, 1021 bytes or full frame, depending on configuration). The preamble and Start-of-Frame delimiter are followed by the Destination Address, Source Address, Length field and LLC data (all supplied by the host). If the frame is less than 64 bytes, including CRC, the CS8900A adds pad bits if configured to do so. Finally, the CS8900A appends the proper 32-bit CRC value.

The Section 5.6 on page 99 provides a detailed description of packet transmission.

3.1.3 Packet Reception

Like packet transmission, packet reception occurs in two phases. In the first phase, the CS8900A receives an Ethernet packet and stores it in on-chip memory. The first phase of packet reception begins with the receive frame passing through the analog front end and Manchester decoder where Manchester data is converted to NRZ data. Next, the preamble and Start-of-Frame delimiter are stripped off and the receive frame is sent through the address filter. If the frame's Destination Address matches the criteria programmed into the address filter, the packet is stored in the CS8900A's internal memory. The CS8900A then checks the CRC, and depending on the configuration, informs the processor that a frame has been received.

In the second phase, the host transfers the receive frame across the ISA bus and into host memory. Receive frames can be transferred

as Memory space operations, I/O space operations, or as DMA operations using host DMA. Also, the CS8900A provides the capability to switch between Memory or I/O operation and DMA operation by using Auto-Switch DMA and StreamTransfer.

The Section 5.2 on page 78 through Section 5.5 on page 96 provide a detailed description of packet reception.

3.2 ISA Bus Interface

The CS8900A provides a direct interface to ISA buses running at clock rates from 8 to 11 MHz. Its on-chip bus drivers are capable of delivering 24 mA of drive current, allowing the CS8900A to drive the ISA bus directly, without added external “glue logic”.

The CS8900A is optimized for 16-bit data transfers, operating in either Memory space, I/O space, or as a DMA slave.

Note that ISA-bus operation below 8 MHz should use the CS8900A’s Receive DMA mode to minimize missed frames. See Section 5.3 on page 90 for a description of Receive DMA operation.

3.2.1 Memory Mode Operation

When configured for Memory Mode operation, the CS8900A’s internal registers and frame buffers are mapped into a contiguous 4-Kbyte block of host memory, providing the host with direct access to the CS8900A’s internal registers and frame buffers. The host initiates Read operations by driving the $\overline{\text{MEMR}}$ pin low and Write operations by driving the $\overline{\text{MEMW}}$ pin low.

For additional information about Memory Mode, see Section 4.9 on page 73.

3.2.2 I/O Mode Operation

When configured for I/O Mode operation, the CS8900A is accessed through eight, 16-bit I/O ports that are mapped into sixteen contiguous I/O locations in the host system’s I/O space. I/O Mode is the default configuration for the CS8900A and is always enabled.

For an I/O Read or Write operation, the AEN pin must be low, and the 16-bit I/O address on the ISA System Address bus (SA0 - SA15) must match the address space of the CS8900A. For a Read, $\overline{\text{IOR}}$ must be low, and for a Write, $\overline{\text{IOW}}$ must be low.

For additional information about I/O Mode, see Section 4.10 on page 75.

3.2.3 Interrupt Request Signals

The CS8900A has four interrupt request output pins that can be connected directly to any four of the ISA bus Interrupt Request signals. Only one interrupt output is used at a time. It is selected during initialization by writing the interrupt number (0 to 3) into PacketPage Memory base + 0022h. Unused interrupt request pins are placed in a high-impedance state. The selected interrupt request pin goes high when an enabled interrupt is triggered. The pin goes low after the Interrupt Status Queue (ISQ) is read as all 0’s (see Section 5.1 on page 78 for a description of the ISQ).

Table 2 presents one possible way of connecting the interrupt request pins to the ISA bus that utilizes commonly available interrupts and facilitates board layout.

CS8900A Interrupt Request Pin	ISA Bus Interrupt	PacketPage base + 0022h
INTRQ3 (Pin 35)	IRQ5	0003h
INTRQ0 (Pin 32)	IRQ10	0000h
INTRQ1 (Pin 31)	IRQ11	0001h
INTRQ2 (Pin 30)	IRQ12	0002h

Table 2. Interrupt Assignments

3.2.4 DMA Signals

The CS8900A interfaces directly to the host DMA controller to provide DMA transfers of receive frames from CS8900A memory to host

memory. The CS8900A has three pairs of DMA pins that can be connected directly to the three 16-bit DMA channels of the ISA bus. Only one DMA channel is used at a time. It is selected during initialization by writing the number of the desired channel (0, 1 or 2) into PacketPage Memory base + 0024h. Unused DMA pins are placed in a high-impedance state. The selected DMA request pin goes high when the CS8900A has received frames to transfer to the host memory via DMA. If the DMABurst bit (register 17, BusCTL, Bit B) is clear, the pin goes low after the DMA operation is complete. If the DMABurst bit is set, the pin goes low 32 µs after the start of a DMA transfer.

The DMA pin pairs are arranged on the CS8900A to facilitate board layout. Crystal recommends the configuration in Table 3 when connecting these pins to the ISA bus.

CS8900A DMA Signal (Pin #)	ISA DMA Signal	PacketPage base + 0024h
DMARQ0 (Pin 15)	DRQ5	0000h
$\overline{\text{DMACK0}}$ (Pin 16)	DACK5	
DMARQ1 (Pin 13)	DRQ6	0001h
$\overline{\text{DMACK1}}$ (Pin 14)	DACK6	
DMARQ2 (Pin 11)	DRQ7	0002h
$\overline{\text{DMACK2}}$ (Pin 12)	DACK7	

Table 3. DMA Assignments

For a description of DMA mode, see Section 5.3 on page 90.

3.3 Reset and Initialization

3.3.1 Reset

Seven different conditions cause the CS8900A to reset its internal registers and circuits.

3.3.1.1 External Reset, or ISA Reset

There is a chip-wide reset whenever the RESET pin is high for at least 400 ns. During a chip-wide reset, all circuitry and registers in the CS8900A are reset.

3.3.1.2 Power-Up Reset

When power is applied, the CS8900A maintains reset until the voltage at the supply pins reaches approximately 2.5 V. The CS8900A comes out of reset once Vcc is greater than approximately 2.5 V *and* the crystal oscillator has stabilized.

3.3.1.3 Power-Down Reset

If the supply voltage drops below approximately 2.5 V, there is a chip-wide reset. The CS8900A comes out of reset once the power supply returns to a level greater than approximately 2.5 V *and* the crystal oscillator has stabilized.

3.3.1.4 EEPROM Reset

There is a chip-wide reset if an EEPROM checksum error is detected (see Section 3.4 on page 21).

3.3.1.5 Software Initiated Reset

There is a chip-wide reset whenever the RESET bit (Register 15, SelfCTL, Bit 6) is set.

3.3.1.6 Hardware (HW) Standby or Suspend

The CS8900A goes though a chip-wide reset whenever it enters or exits either HW Standby mode or HW Suspend mode (see Section 3.7 on page 27 for more information about HW Standby and Suspend).

3.3.1.7 Software (SW) Suspend

Whenever the CS8900A enters SW Suspend mode, all registers and circuits are reset except for the ISA I/O Base Address register (located at PacketPage base + 0020h) and the SelfCTL register (Register 15). Upon exit, there is a chip-wide reset (see Section 3.7 on page 27 for more information about SW Suspend).

3.3.2 Allowing Time for Reset Operation

After a reset, the CS8900A goes through a self configuration. This includes calibrating on-chip analog circuitry, and reading EEPROM for validity and configuration. Time required for the reset calibration is typically 10 ms. Software drivers should not access registers internal to the CS8900A during this time. When calibration is done, bit INITD in the Self Status Register (register 16) is set indicating that initialization is complete, and the SIBUSY bit in the same register is cleared indicating the EEPROM is no longer being read or programmed.

3.3.3 Bus Reset Considerations

After reset, the CS8900A packet page pointer register (IObase+0Ah) is set to 3000h. The 3000h value can be used as part of the CS8900A signature when the system scans for the CS8900A. See Section 4.10 on page 75.

After a reset, the ISA bus outputs INTRx and DMARQx are 3-Stated, thus avoiding any interrupt or DMA channel conflicts on the ISA bus at power-up time.

3.3.4 Initialization

After each reset (except EEPROM Reset), the CS8900A checks the sense of the EEDataIn pin to see if an external EEPROM is present. If EEDI is high, an EEPROM is present and the CS8900A automatically loads the configuration data stored in the EEPROM into its internal registers (see next section). If EEDI is low, an EEPROM is not present and the CS8900A comes out of reset with the default configuration shown in Table 4.

A low-cost serial EEPROM can be used to store configuration information that is automatically loaded into the CS8900A after each reset (except EEPROM reset). The use of an EEPROM is optional.

The CS8900A operates with any of six standard EEPROM's shown in Table 5.

PacketPage Address	Register Contents	Register Descriptions
0020h	0300h	I/O Base Address*
0022h	XXXX XXXX XXXX X100	Interrupt Number
0024h	XXXX XXXX XXXX XX11	DMA Channel
0026h	0000h	DMA Start of Frame Offset
0028h	X000h	DMA Frame Count
002Ah	0000h	DMA Byte Count
002Ch	XXX0 0000h	Memory Base Address
0030h	XXX0 0000h	Boot PROM Base Address
0034h	XXX0 0000h	Boot PROM Address Mask
0102h	0003h	Register 3 - RxCFG
0104h	0005h	Register 5 - RxCTL
0106h	0007h	Register 7 - TxCFG
0108h	0009h	Register 9 - TxCMD
010Ah	000Bh	Register B - BufCFG
010Ch	Undefined	Reserved
010Eh	Undefined	Reserved
0110h	Undefined	Reserved
0112h	00013h	Register 13 - LineCTL
0114h	0015h	Register 15 - SelfCTL
0116h	0017h	Register 17 - BusCTL
0118h	0019h	Register 19 - TestCTL

* I/O base address is unaffected by Software Suspend mode.

Table 4. Default Configuration

EEPROM Type	Size (16-bit words)
‘C46 (non-sequential)	64
‘CS46 (sequential)	64
‘C56 (non-sequential)	128
‘CS56 (sequential)	128
‘C66 (non-sequential)	256
‘CS66 (sequential)	256

Table 5. Supported EEPROM Types

3.4 Configurations with EEPROM

3.4.1 EEPROM Interface

The interface to the EEPROM consists of the four signals shown in Table 6.

CS8900A Pin (Pin #)	CS8900A Function	EEPROM Pin
EECS (Pin 3)	EEPROM Chip Select	Chip Select
EESK (PIN 4)	1 MHz EEPROM Serial Clock output	Clock
EEDO (Pin 5)	EEPROM Data Out (data to EEPROM)	Data In
EEDI (Pin 6)	EEPROM Data in (data from EEPROM)	Data Out

Table 6. EEPROM Interface

3.4.2 EEPROM Memory Organization

If an EEPROM is used to store initial configuration information for the CS8900A, the EEPROM is organized in one or more blocks of 16-bit words. The first block in EEPROM, referred to as the Configuration Block, is used to configure the CS8900A after reset. An example of a typical Configuration Block is shown in Table 7. Additional blocks containing user data may be stored in the EEPROM. However, the Configuration Block must always start at address 00h and be stored in contiguous memory locations.

3.4.3 Reset Configuration Block

The first block in EEPROM, referred to as the Reset Configuration Block, is used to automatically program the CS8900A with an initial configuration after a reset. Additional user data may also be stored in the EEPROM if space is available. The additional data are stored as 16-bit words and can occupy any EEPROM address space beginning immediately after the end of the Reset Configuration Block up to address 7Fh, depending on EEPROM size. This additional data can only be accessed through software control (refer to Section 3.5 on page 25 for more information on accessing

Word Address	Value	Description
FIRST WORD in DATA BLOCK		
00h	A120h	Configuration Block Header. The high byte, A1h, indicates a 'C46 EEPROM is attached. The Link Byte, 20h, indicates the number of bytes to be used in this block of configuration data.
FIRST GROUP of WORDS		
01h	2020h	Group Header for first group of words. Three words to be loaded, beginning at 0020h in PacketPage memory.
02h	0300h	I/O Base Address
03h	0003h	Interrupt Number
04h	0001h	DMA Channel Number
SECOND GROUP of WORDS		
05h	502Ch	Group Header for second group of words. Six words to be loaded, beginning at 002Ch in PacketPage memory.
06h	E000h	Memory Base Address - low word
07h	000Fh	Memory Base Address - high word
08h	0000h	Boot PROM Base Address - low word
09h	000Dh	Boot PROM Base Address - high word
0Ah	C000h	Boot PROM Address Mask - low word
0Bh	000Fh	Boot PROM Address Mask - high word
THIRD GROUP of WORDS		
0Ch	2158h	Group Header for third group of words. Three words to be loaded, beginning at 0158 in PacketPage memory.
0Dh	0010h	Individual Address - Octet 0 and 1
0Eh	0000h	Individual Address - Octet 2 and 3
0Fh	0000h	Individual Address - Octet 4 and 5
CHECKSUM Value		
10h	2800h	The high byte, 28h, is the Checksum Value. In this example, the checksum includes word addresses 00h through 0Fh. The hexadecimal sum of the bytes is D8h, resulting in a 2's complement of 28h. The low byte, 00h, provides a pad to the word boundary.

* FFFFh is a special code indicating that there are no more words in the EEPROM.

Table 7. EEPROM Configuration Block Example

the EEPROM). Address space 80h to AFh is reserved.

3.4.3.1 Reset Configuration Block Structure

The Reset Configuration Block is a block of contiguous 16-bit words starting at EEPROM address 00h. It can be divided into three logical sections: a header, one or more groups of configuration data words, and a checksum value. All of the words in the Reset Configuration Block are read sequentially by the CS8900A after each reset, starting with the header and ending with the checksum. Each group of configuration data is used to program a PacketPage register (or set of PacketPage registers in some cases) with an initial non-default value.

3.4.3.2 Reset Configuration Block Header

The header (first word of the block located at EEPROM address 00h) specifies the type of EEPROM used, whether or not a Reset Configuration block is present, and if so, how many

bytes of configuration data are stored in the Reset Configuration Block.

3.4.3.3 Determining the EEPROM Type

The LSB of the high byte of the header indicates the type of EEPROM attached: sequential or non-sequential. An LSB of 0 (XXXX-XXX0) indicates a sequential EEPROM. An LSB of 1 (XXXX-XXX1) indicates a non-sequential EEPROM. The CS8900A works equally well with either type of EEPROM. The CS8900A will automatically generate sequential addresses while reading the Reset Configuration Block if a non-sequential EEPROM is used.

3.4.3.4 Checking EEPROM for presence of Reset Configuration Block

The read-out of either a binary 101X-XXX0 or 101X-XXX1 (X = do not care) from the high byte of the header indicates the presence of configuration data. Any other readout value terminates initialization from the EEPROM. If an EEPROM is attached but not used for configuration, Cirrus Logic recommends that the high byte of the first word be programmed with 00h in order to ensure that the CS8900A will not attempt to read configuration data from the EEPROM.

3.4.3.5 Determining Number of Bytes in the Reset Configuration Block

The low byte of the Reset Configuration Block header is known as the link byte. The value of the Link Byte represents the number of bytes of configuration data in the Reset Configuration Block. The two bytes used for the header are excluded when calculating the Link Byte value.

For example, a Reset Configuration Block header of A104h indicates a non-sequential EEPROM programmed with a Reset Configuration Block containing 4 bytes of configuration data. This Reset Configuration Block occupies 6 bytes (3 words) of EEPROM space (2 bytes for the header and 4 bytes of configuration data).

3.4.4 Groups of Configuration Data

Configuration data are arranged as groups of words. Each group contains one or more words of data that are to be loaded into PacketPage registers. The first word of each group is referred to as the Group Header. The Group Header indicates the number of words in the group and the address of the PacketPage register into which the first data word in the group is to be loaded. Any remaining words in the group are stored in successive PacketPage registers.

3.4.4.1 Group Header

Bits F through C of the Group Header specify the number of words in each group that are to be transferred to PacketPage registers (see Figure 4). This value is two less than the total number of words in the group, including the Group Header. For example, if bits F through C contain 0001, there are three words in the group (a Group Header and two words of configuration data).

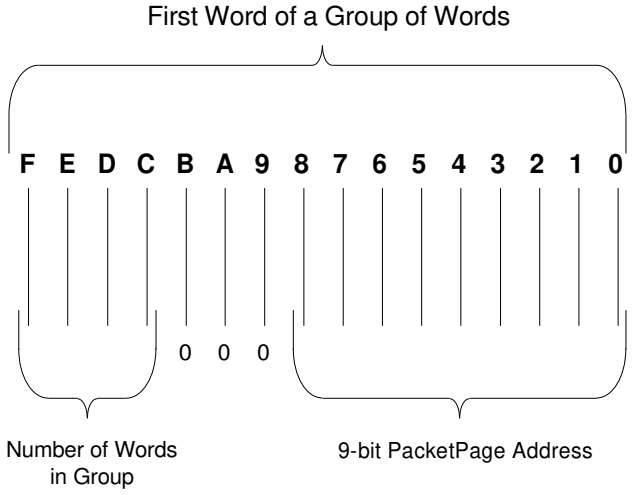


Figure 4. Group Header

Bits 8 through 0 of the Group Header specify a 9-bit PacketPage Address. This address defines the PacketPage register that will be loaded with the first word of configuration data from the group. Bits B though 9 of the Group Header are forced to 0, restricting the destination address range to the first 512 bytes of PacketPage memory. Figure 4 shows the format of the Group header.

3.4.5 Reset Configuration Block Checksum

A checksum is stored in the high byte position of the word immediately following the last group of data in the Reset Configuration Block. (The EEPROM address of the checksum value can be determined by dividing the value stored in the Link Byte by two). The checksum value is the 2's complement of the 8-bit sum (any carry out of eighth bit is ignored) of all the bytes in the Reset Configuration Block, excluding the checksum byte. This sum includes the Reset Configuration Block header at address 00h. Since the checksum is calculated as the 2's complement of the sum of all preceding bytes in the Reset Configuration Block, a total of 0 should result when the checksum value is added to the sum of the previous bytes.

3.4.6 EEPROM Example

Table 7 shows an example of a Reset Configuration Block stored in a C46 EEPROM. Note that little-endian word ordering is used, i.e., the least significant word of a multiword datum is located at the lowest address.

3.4.7 EEPROM Read-out

If the EEDI pin is asserted high at the end of reset, the CS8900A reads the first word of EEPROM data by:

1) Asserting EECS
2) Clocking out a Read-Register-00h command on EEDO (EESK provides a 1MHz serial clock signal)
3) Clocking the data in on EEDI.

If the EEDI pin is low at the end of the reset signal, the CS8900A does not perform an EEPROM read-out (uses its default configuration).

3.4.7.1 Determining EEPROM Size

The CS8900A determines the size of the EEPROM by checking the sense of EEDI on the tenth rising edge of EESK. If EEDI is low, the EEPROM is a 'C46 or 'CS46. If EEDI is high, the EEPROM is a 'C56, 'CS56, 'C66, or 'CS66.

3.4.7.2 Loading Configuration Data

The CS8900A reads in the first word from the EEPROM to determine if configuration data is contained in the EEPROM. If configuration data is not stored in the EEPROM, the CS8900A terminates initialization from EEPROM and operates using its default configuration (See Table 4). If configuration data is stored in EEPROM, the CS8900A automatically loads all configuration data stored in the Reset Configuration Block into its internal PacketPage registers.

3.4.8 EEPROM Read-out Completion

Once all the configuration data are transferred to the appropriate PacketPage registers, the CS8900A performs a checksum calculation to verify the Reset Configuration Blocks data are valid. If the resulting total is 0, the read-out is considered valid. Otherwise, the CS8900A initiates a partial reset to restore the default configuration.

If the read-out is valid, the EEPROMOK bit (Register 16, SelfST, bit A) is set. EEPROMOK is cleared if a checksum error is detected. In this case, the CS8900A performs a partial reset and is restored to its default. Once

initialization is complete (configuration loaded from EEPROM or reset to default configuration) the INITD bit is set (Register 16, SelfST, bit 7).

3.5 Programming the EEPROM

After initialization, the host can access the EEPROM through the CS8900A by writing one of seven commands to the EEPROM Command register (PacketPage base + 0040h). Figure 5 shows the format of the EEPROM Command register.

3.5.1 EEPROM Commands

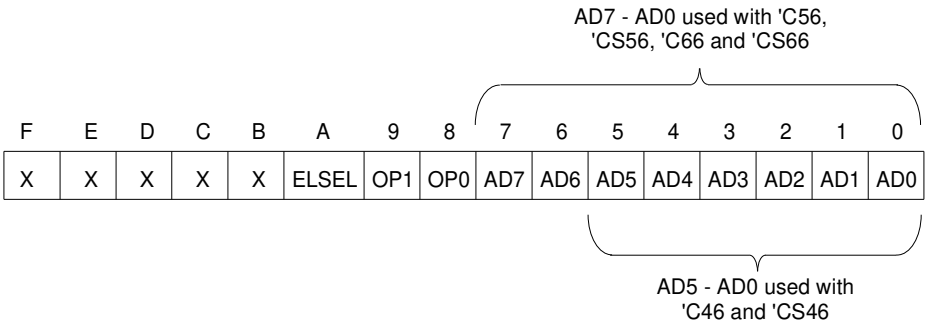
The seven commands used to access the EEPROM are: Read, Write, Erase, Erase/Write Enable, Erase/Write Disable, Erase-All, and Write-All. They are described in Table 8.

Command	Opcode (bits 9,8)	EEPROM Address (bits 7 to 0)	Data	EEPROM Type	Execution Time
Read Register	1,0	word address	yes	all	25 µs
Write Register	0,1	word address	yes	all	10 ms
Erase Register	1,1	word address	no	all	10 ms
Erase/Write Enable	0,0	XX11-XXXX	no	‘CS46, ‘C46	9 µs
		11XX-XXXX	no	‘CS56, ‘C56, ‘CS66, ‘C66	9 µs
Erase/Write Disable	0,0	XX00-XXXX	no	‘CS46, ‘C46	9 µs
	0,0	00XX-XXXX	no	‘CS56, ‘C56, ‘CS66, ‘C66	9 µs
Erase-All Registers	0,0	XX10-XXXX	no	‘CS46, ‘C46	10 ms
	0,0	10XX-XXXX	no	‘CS56, ‘C56, ‘CS66, ‘C66	9 µs
Write-All Register	0,0	XX01-XXXX	yes	‘CS46, ‘C46	10 ms
	0,0	01XX-XXXX	yes	‘CS56, ‘C56, ‘CS66, ‘C66	10 ms

Table 8. EEPROM Commands

3.5.2 EEPROM Command Execution

During the execution of a command, the two Opcode bits, followed by the six bits of address (for a ’C46 or ’CS46) or eight bits of address



Bit	Name	Description
[F:B]		Reserved
[A]	ELSEL	External Logic Select: When clear, the EECS pin is used to select the EEPROM. When set, the ELCS pin is used to select the external LA decode circuit.
[9:8]	OP1, OP0	Opcode: Indicates what command is being executed (see next section).
[7:0]	AD7 to AD0	EEPROM Address: Address of EEPROM word being accessed.

Figure 5. EEPROM Command Register Format