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CS8952

CrystalLAN™ 100BASE-X and 10BASE-T Transceiver

Features

- Single-Chip IEEE 802.3 Physical Interface IC for 100BASE-TX, 100BASE-FX and 10BASE-T
- Adaptive Equalizer provides Extended Length Operation (>160 m) with Superior Noise Immunity and NEXT Margin
- Extremely Low Transmit Jitter (<400 ps)
- Low Common Mode Noise on TX Driver for Reduced EMI Problems
- Integrated RX and TX Filters for 10BASE-T
- Compensation for Back-to-Back "Killer Packets"
- Digital Interfaces Supported
  - Media Independent Interface (MII) for 100BASE-X and 10BASE-T
  - Repeater 5-bit code-group interface (100BASE-X)
  - 10BASE-T Serial Interface
- Register Set Compatible with DP83840A
- IEEE 802.3 Auto-Negotiation with Next Page Support
- Six LED drivers (LNK, COL, FDX, TX, RX, and SPD)
- Low power (135 mA Typ) CMOS design operates on a single 5 V supply

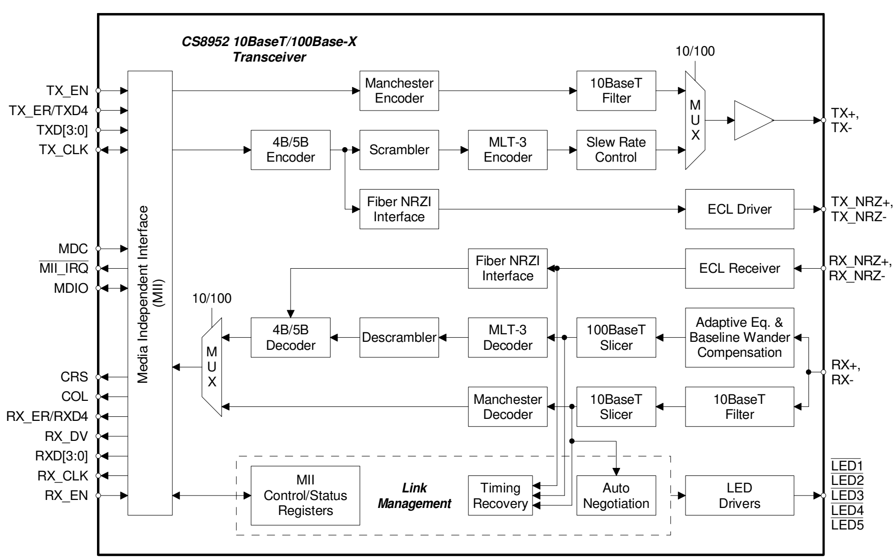
Description

The CS8952 uses CMOS technology to deliver a high-performance, low-cost 100BASE-X/10BASE-T Physical Layer (PHY) line interface. It makes use of an adaptive equalizer optimized for noise and near end crosstalk (NEXT) immunity to extend receiver operation to cable lengths exceeding 160 m. In addition, the transmit circuitry has been designed to provide extremely low transmit jitter (<400 ps) for improved link partner performance. Transmit driver common mode noise has been minimized to reduce EMI for simplified FCC certification.

The CS8952 incorporates a standard Media Independent Interface (MII) for easy connection to a variety of 10 and 100 Mb/s Media Access Controllers (MACs). The CS8952 also includes a pseudo-ECL interface for use with 100Base-FX fiber interconnect modules.

ORDERING INFORMATION

See "Ordering Information" on page 80.



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1. SPECIFICATIONS AND CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (AVSS, DVSS = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Max	Unit
Power Supply		V_{DD} V_{DD_MII}	-0.3 -0.3	6.0 6.0	V
Input Current	Except Supply Pins		-	+/-10.0	mA
Input Voltage			-0.3	V_{DD} + 0.3	V
Ambient Temperature	Power Applied		-55	+125	°C
Storage Temperature			-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AVSS, DVSS = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Max	Unit
Power Supply	Core MII	V_{DD} V_{DD_MII}	4.75 3.0	5.25 5.25	V V
Operating Ambient Temperature		T_A	0	70	°C

QUARTZ CRYSTAL REQUIREMENTS (If a 25 MHz quartz crystal is used, it must meet the following specifications.)

Parameter	Min	Typ	Max	Unit
Parallel Resonant Frequency	-	25.0	-	MHz
Resonant Frequency Error (CL = 15 pF)	-50	-	+50	ppm
Resonant Frequency Change Over Operating Temperature	-40	-	+40	ppm
Crystal Load Capacitance	-	15	-	pF
Motional Crystal Capacitance	-	0.021	-	pF
Series Resistance	-	-	18	Ω
Shunt Capacitance	-	-	7	pF

DC CHARACTERISTICS (Over recommended operating conditions)

Parameter	Symbol	Min	Typ	Max	Unit
External Oscillator					
XTAL_I Input Low Voltage	V_{IXH}	-0.3	-	0.5	V
XTAL_I Input High Voltage	V_{IXH}	3.5	-	VDD+0.5	V
XTAL_I Input Low Current	I_{IXL}	-40	-	-	µA
XTAL_I Input High Current	I_{IXH}	-	-	40	µA
XTAL_I Input Capacitance	C_L		-	35	pF
XTAL_I Input Cycle Time	t_{IXC}	39.996	-	40.004	ns
XTAL_I Input Low Time	t_{IXL}	18	-	22	ns
XTAL_I Input High Time	t_{XH}	18	-	22	ns
Power Supply					
Power Supply Current 100BASE-TX (Note **1**) 100BASE-FX (Note **1**) 10BASE-T (Note **1**)	I_{DD}	- - -	135 90 80	145 - -	mA
Hardware Power-Down (Note **1**)	I_{DDHPDN}	-	900	-	µA
Software Power-Down (Note **1**)	I_{DDSPDN}	-	20	-	mA
Low Power Power-Up (Note **1**)	$I_{DDSLPUP}$	-	900	-	µA
Digital I/O					
Output Low Voltage CLK25, MII_IRQ, SPD10, SPD100 I_{OL} = 4.0mA LED[4:0] I_{OL} = 10.0mA	V_{OL}	- -	- -	0.4 0.4	V
Output Low Voltage (MII_DRV = 1) COL, CRS, MDIO, RXD[3:0], RX_CLK, RX_DV, RX_ER, TX_CLK I_{OL} = 4.0mA VDD_MII = 5V; I_{OL} = 43.0mA VDD_MII = 3.3V, I_{OL} = 26.0mA	V_{OL}	- - -	- - -	0.4 3.05 2.1	V
Output Low Voltage (MII_DRV = 0) COL, CRS, MDIO, RXD[3:0], RX_CLK, RX_DV, RX_ER, TX_CLK I_{OL} = 4.0mA	V_{OL}	-	-	0.4	V
Output High Voltage CLK25, SPD10, SPD100 I_{OH} = -4.0mA	V_{OH}	2.4	-	-	V
Output High Voltage (MII_DRV = 1) COL, CRS, MDIO, RXD[3:0], RX_CLK, RX_DV, RX_ER, TX_CLK I_{OH}= -4.0mA VDD_MII = 5V; I_{OH} = -20.0mA VDD_MII = 3.3V, I_{OH} = -20.0mA	V_{OH}	2.4 1.1 1.1	- - -	- - -	V

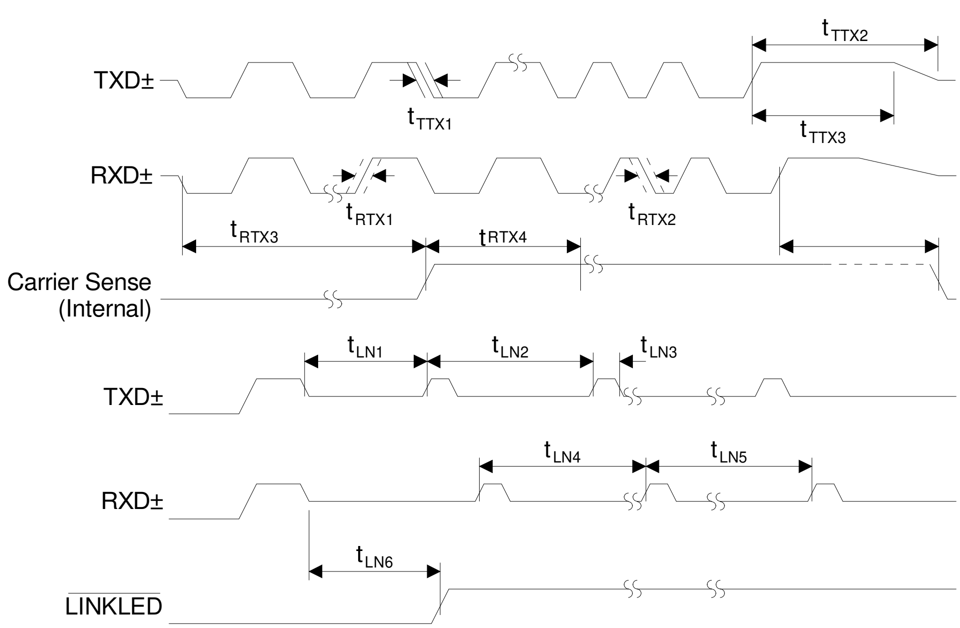
DC CHARACTERISTICS *(CONTINUED)* (Over recommended operating conditions)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (MII_DRV = 0) COL, CRS, MDIO, RXD[3:0], RX_CLK, RX_DV, RX_ER, TX_CLK I_{OH} = -4.0mA	V_{OH}	2.4	-	-	V
Input Low Voltage All Inputs Except AN[1:0], TCM, TXSLEW[1:0]	V_{IL}	-	-	0.8	V
Input High Voltage All Inputs Except AN[1:0], TCM, TXSLEW[1:0]	V_{IH}	2.0	-	-	V
Tri-Level Input Voltages AN[1:0], TCM, TXSLEW[1:0]	V_{IL}	-	-	1/3 V_{DD_MII} - 20%	V
	V_{IM}	1/3 V_{DD_MII} + 20%	-	2/3 V_{DD_MII} - 20%	
	V_{IH}	2/3 V_{DD_MII} + 20%	-	-	
Input Low Current MDC, TXD[3:0], TX_CLK, TX_EN, TX_ER V_I = 0.0V	I_{IL}	-20	-	-	µA
MDIO V_I = 0.0V		-3800	-	-	
Input High Current MDC, TXD[3:0], TX_CLK, TX_EN, TX_ER V_I = 5.0V	I_{IH}	-	-	200	µA
MDIO V_I = 5.0V		-	-	20	
Input Leakage Current All Other Inputs 0<=V<=V_{DD}	I_{LEAK}	-10	-	+10	µA

Notes: 1. With digital outputs connected to CMOS loads.

10BASE-T CHARACTERISTICS

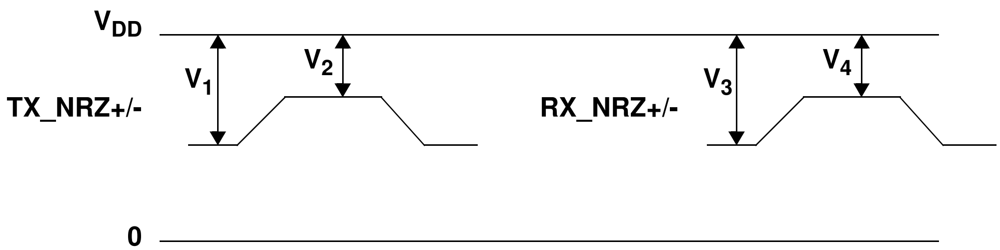
Parameter	Symbol	Min	Typ	Max	Unit
10BASE-T Interface					
Transmitter Differential Output Voltage (Peak)	V_{OD}	2.2	-	2.8	V
Receiver Normal Squelch Level (Peak)	V_{ISQ}	300	-	525	mV
Receiver Low Squelch Level (LoRxSquelch bit set)	V_{SQL}	125	-	290	mV
10BASE-T Transmitter					
TXD Pair Jitter into 100 Ω Load	t_{TTX1}	-	-	8	ns
TXD Pair Return to ≤ 50 mV after Last Positive Transition	t_{TTX2}	-	-	4.5	µs
TXD Pair Positive Hold Time at End of Packet	t_{TTX3}	250	-	-	ns
10BASE-T Receiver					
Allowable Received Jitter at Bit Cell Center	t_{TRX1}	-	-	+/-13.5	ns
Allowable Received Jitter at Bit Cell Boundary	t_{TRX2}	-	-	+/-13.5	ns
10BASE-T Link Integrity					
First Transmitted Link Pulse after Last Transmitted Packet	t_{LN1}	15	16	17	ms
Time Between Transmitted Link Pulses	t_{LN2}	15	16	17	ms
Width of Transmitted Link Pulses	t_{LN3}	60	-	200	ns
Minimum Received Link Pulses Separation	t_{LN4}	2	5	7	ms
Maximum Received Link Pulse Separation	t_{LN5}	25	52	150	ms
Last Receive Activity to Link Fail (Link Loss Timer)	t_{LN6}	50	52	150	ms
10Base-T Jabber/Unjabber Timing					
Maximum Transmit Time		-	105	-	ms
Unjabber Time		-	406	-	ms



100BASE-X CHARACTERISTICS

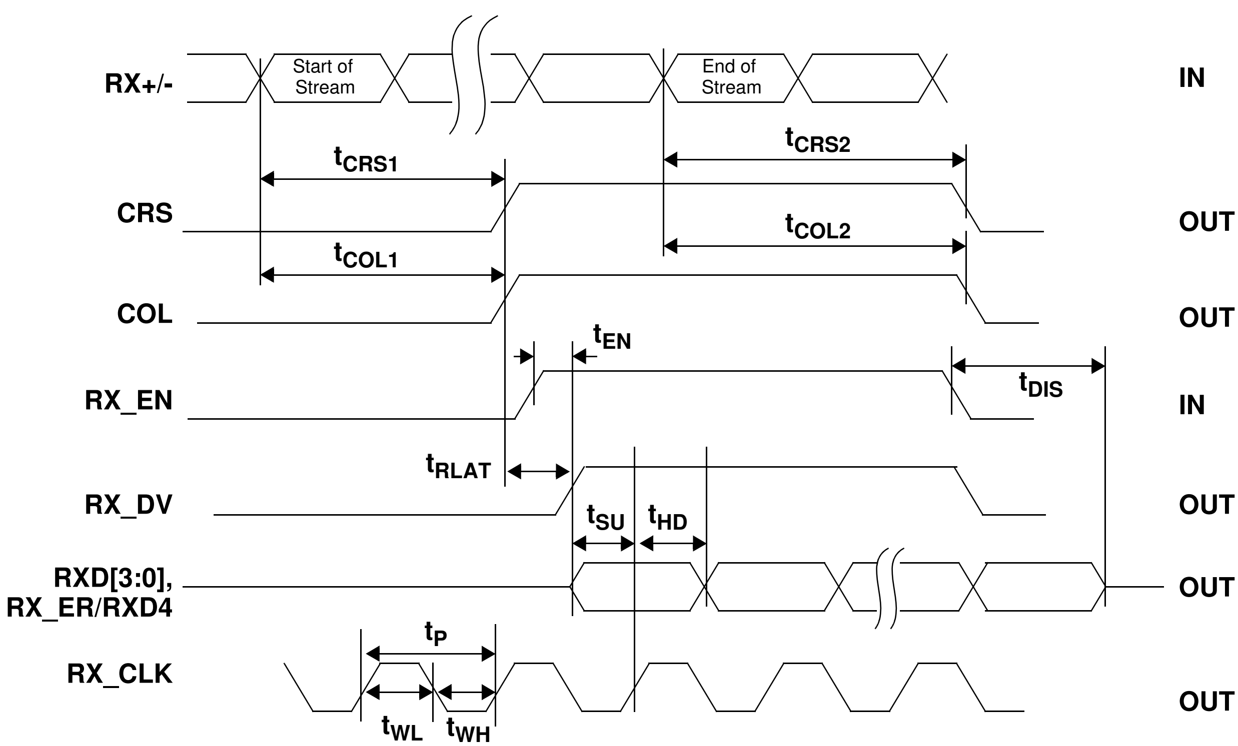
Parameter	Symbol	Min	Typ	Max	Unit
100BASE-TX Transmitter					
TX Differential Output Voltage (Peak)	V_{OP}	0.95	-	1.05	V
Signal Amplitude Symmetry	V_{SYM}	98	-	102	%
Signal Rise/Fall Time	t_{RF}	3.0	-	5.0	ns
Rise/Fall Symmetry	t_{RFS}	-	-	0.5	ns
Duty Cycle Distortion	t_{DCD}	-	-	+/-0.5	ns
Overshoot/Undershoot	t_{OS}	-	-	5	%
Transmit Jitter	t_{JT}	-	400	1400	ps
TX Differential Output Impedance	Z_{OUT}	-	100	-	ohms
100BASE-TX Receiver					
Receive Signal Detect Assert Threshold		-	-	1.0	V_{p-p}
Receive Signal Detect De-assert Threshold		0.2	-	-	V_{p-p}
Receive Signal Detect Assert Time		-	-	1000	µs
Receive Signal Detect De-assert Time		-	-	350	µs
100BASE-FX Transmitter					
TX_NRZ+/- Output Voltage - Low	V_1	-1.830	-	-1.605	V
TX_NRZ+/- Output Voltage - High	V_2	-1.035	-	-0.880	V
Signal Rise/Fall Time	T_{RF}	-	-	1.6	ns
100Base-FX Receiver					
RX_NRZ+/- Input Voltage - Low	V_3	-1.830	-	-1.605	V
RX_NRZ+/- Input Voltage - High	V_4	-1.035	-	-0.880	V
Common Mode Input Range	V_{CMIP}	-	3.56	-	V

RX/TX Signaling for 100Base-FX



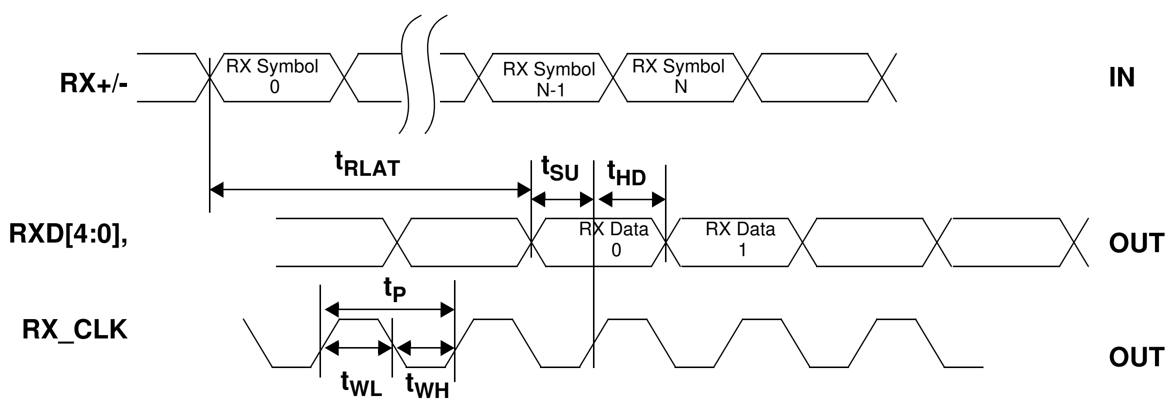
100BASE-TX MII RECEIVE TIMING - 4B/5B ALIGNED MODES

Parameter		Symbol	Min	Typ	Max	Unit
RX_CLK Period		t_P	-	40	-	ns
RX_CLK Pulse Width		t_{WL}, t_{WH}	-	20	-	ns
RXD[3:0],RX_ER/RXD4,RX_DV setup to rising edge of RX_CLK		t_{SU}	10	-	-	ns
RXD[3:0],RX_ER/RXD4,RX_DV hold from rising edge of RX_CLK		t_{HD}	10	-	-	ns
CRS to RXD latency	4B Aligned 5B Aligned	t_{DLAT}	2 2	3 - 6 3 - 6	8 8	BT
"Start of Stream" to CRS asserted		t_{CRS1}	-	10	11	BT
"End of Stream" to CRS de-asserted		t_{CRS2}	-	-	21	BT
"Start of Stream" to COL asserted		t_{COL1}	-	-	11	BT
"End of Stream" to COL de-asserted		t_{COL2}	-	-	21	BT
RX_EN asserted to RX_DV, RXD[3:0] valid		t_{EN}	-	TBD	-	ns
RX_EN de-asserted to RX_DV, RXD[3:0]. RX_ER/RXD4 in high impedance state		t_{DIS}	-	TBD	-	ns



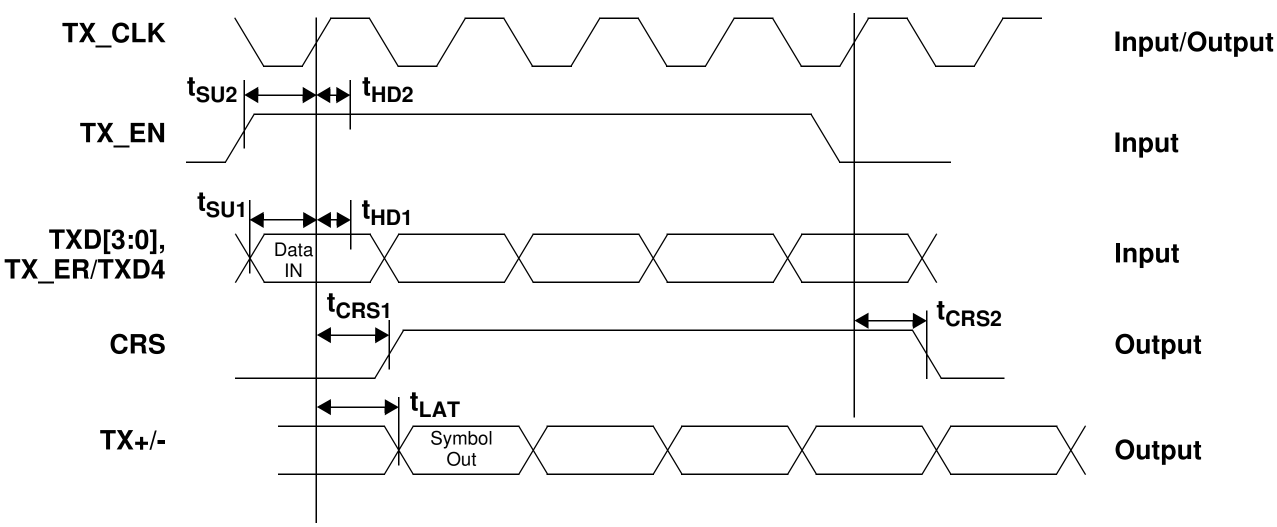
100BASE-TX MII RECEIVE TIMING - 5B BYPASS ALIGN MODE

Parameter	Symbol	Min	Typ	Max	Unit
RX_CLK Period	t_P	-	40	-	ns
RX_CLK Pulse Width	t_{WL}, t_{WH}	-	20	-	ns
RXD[4:0] setup to rising edge of RX_CLK	t_{SU}	10	-	-	ns
RXD[4:0] hold after rising edge of RX_CLK	t_{HD}	10	-	-	ns
Start of 5B symbol to symbol output on RX[4:0] 5B Mode	t_{RLAT}	5	-	9	BT



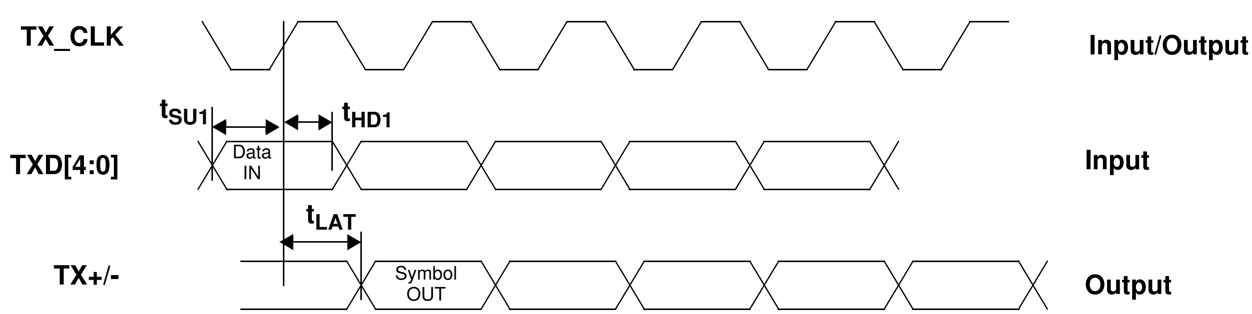
100BASE-TX MII TRANSMIT TIMING - 4B/5B ALIGN MODES

Parameter	Symbol	Min	Typ	Max	Unit
TXD[3:0] Setup to TX_CLK High	t_{SU1}	10	-	-	ns
TX_EN Setup to TX_CLK High	t_{SU2}	10	-	-	ns
TXD[3:0] Hold after TX_CLK High	t_{HD1}	0	-	-	ns
TX_ER Hold after TX_CLK High	t_{HD2}	0	-	-	ns
TX_EN Hold after TX_CLK High	t_{HD3}	0	-	-	ns
TX_EN “high” to CRS asserted latency	t_{CRS1}	-		8	BT
TX_EN “low” to CRS de-asserted latency	t_{CRS2}	-		8	BT
TX_EN “high” to TX+/- output (TX Latency)	t_{LAT}	6	7	8	BT



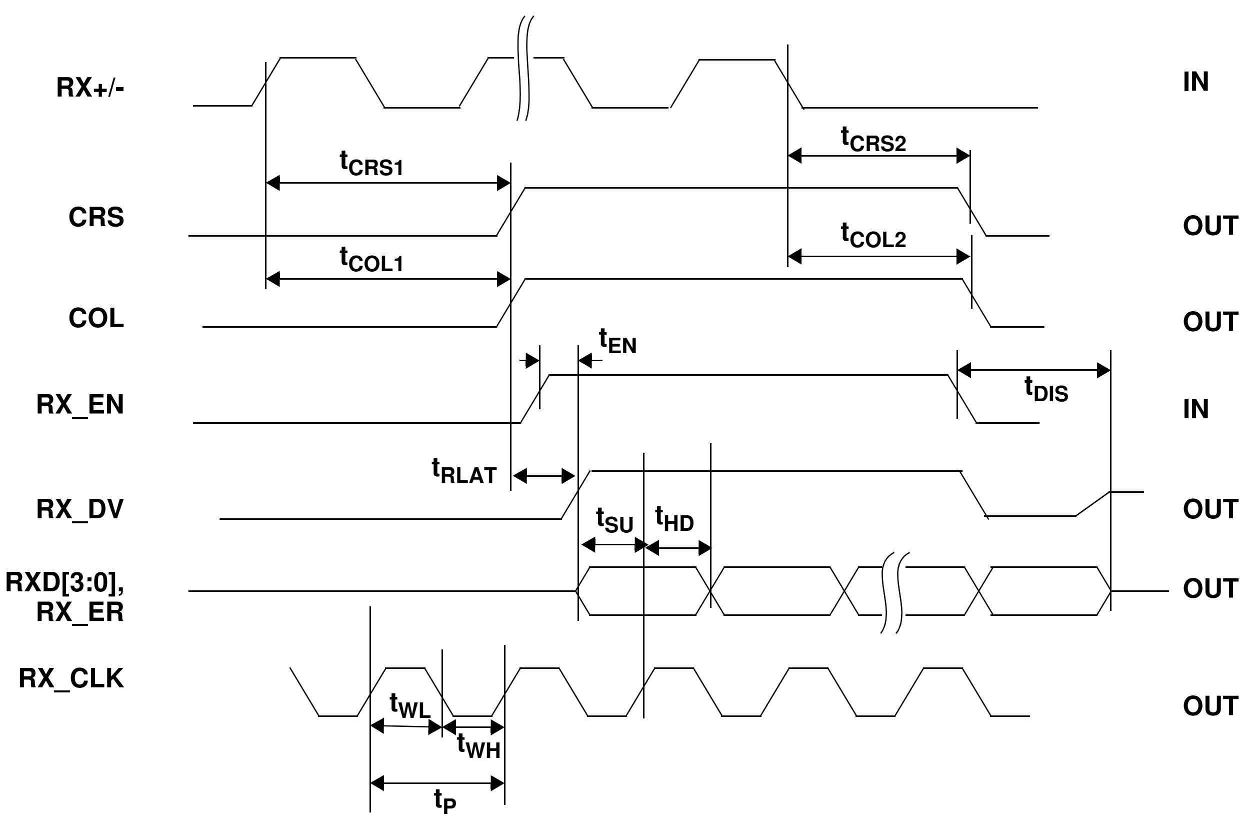
100BASE-TX MII TRANSMIT TIMING - 5B BYPASS ALIGN MODE

Parameter	Symbol	Min	Typ	Max	Unit
TXD[4:0] Setup to TX_CLK High	t_{SU1}	10	-	-	ns
TXD[4:0] Hold after TX_CLK High	t_{HD1}	0	-	-	ns
TX_ER Hold after TX_CLK High	t_{HD2}	0	-	-	ns
TXD[4:0] Sampled to TX+/- output (TX Latency)	t_{LAT}	-	6	7	ns



10BASE-T MII RECEIVE TIMING

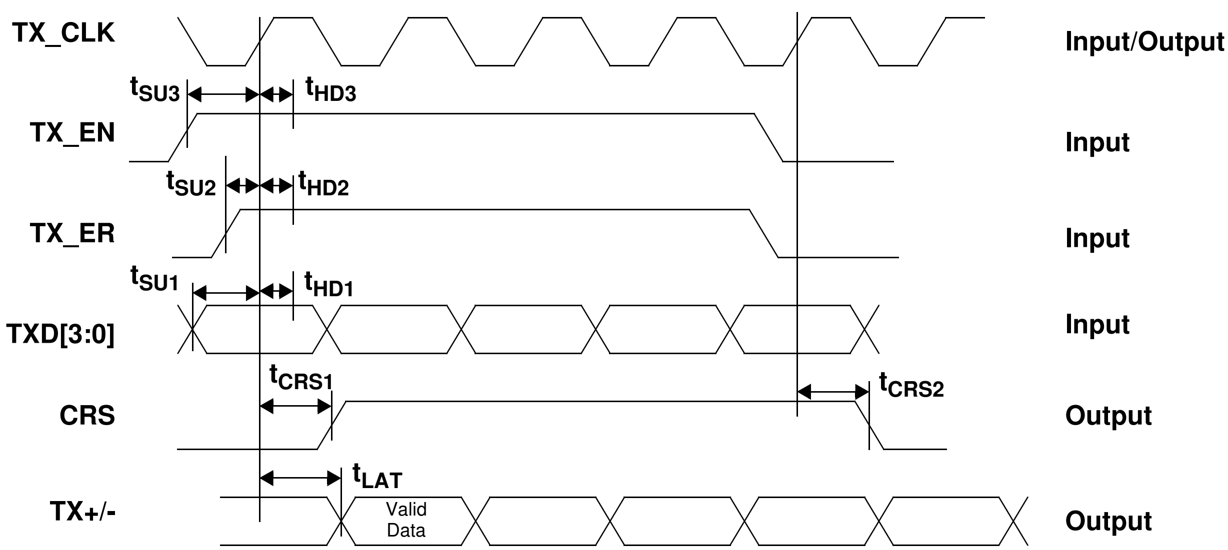
Parameter	Symbol	Min	Typ	Max	Unit
RX_CLK Period	t_P	-	400	-	ns
RX_CLK Pulse Width	t_{WL}, t_{WH}	-	200	-	ns
RXD[3:0], RX_ER, RX_DV setup to rising edge of RX_CLK	t_{SU}	30	-	-	ns
RXD[3:0], RX_ER, RX_DV hold from rising edge of RX_CLK	t_{HD}	30	-	-	ns
RX data valid from CRS	t_{RLAT}	-	8	10	BT
RX+/- preamble to CRS asserted	t_{CRS1}	-	5	7	BT
RX+/- end of packet to CRS de-asserted	t_{CRS2}		2.5	3	BT
RX+/- preamble to COL asserted	t_{COL1}	0	-	7	BT
RX+/- end of packet to COL de-asserted	t_{COL2}	-	-	3	BT
RX_EN asserted to RX_DV, RXD[3:0], RX_ER valid	t_{EN}	-	-	60	ns
RX_EN de-asserted to RX_DV, RXD[3:0]. RX_ER in high impedance state	t_{DIS}	-	-	60	ns



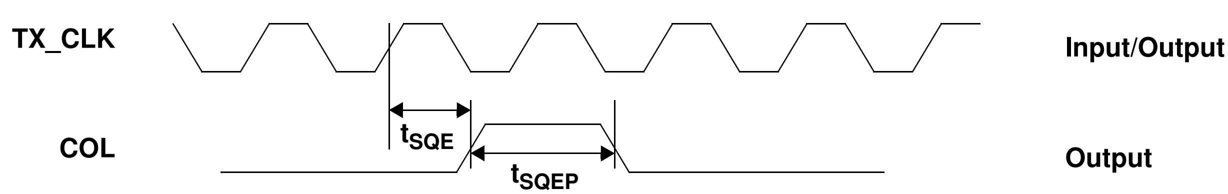
10BASE-T MII TRANSMIT TIMING

Parameter	Symbol	Min	Typ	Max	Unit
TXD[3:0] Setup to TX_CLK High	t_{SU1}	10	-	-	ns
TX_ER Setup to TX_CLK High	t_{SU2}	10	-	-	ns
TX_EN Setup to TX_CLK High	t_{SU3}	10	-	-	ns
TXD[3:0] Hold after TX_CLK High	t_{HD1}	0	-	-	ns
TX_ER Hold after TX_CLK High	t_{HD2}	0	-	-	ns
TX_EN Hold after TX_CLK High	t_{HD3}	0	-	-	ns
TX_EN "high" to CRS asserted latency	t_{CRS1}	0	-	4	BT
TX_EN "low" to CRS de-asserted latency	t_{CRS2}	0	-	16	BT
TX_EN "high" to TX+/- output (TX Latency)	t_{LAT}	6	-	14	BT
SQE Timing					
COL (SQE) Delay after CRS de-asserted	t_{COL}	0.65	0.9	1.6	µs
COL (SQE) Pulse Duration	t_{COLP}	0.65	1.0	1.6	µs

10BASE-T Transmit Timing

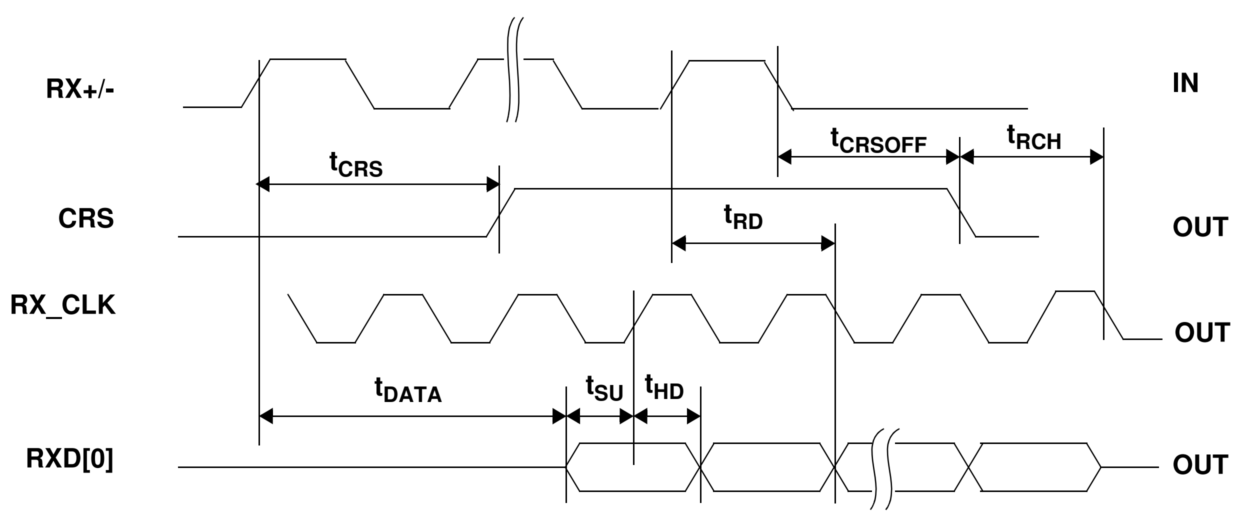


SQE Timing



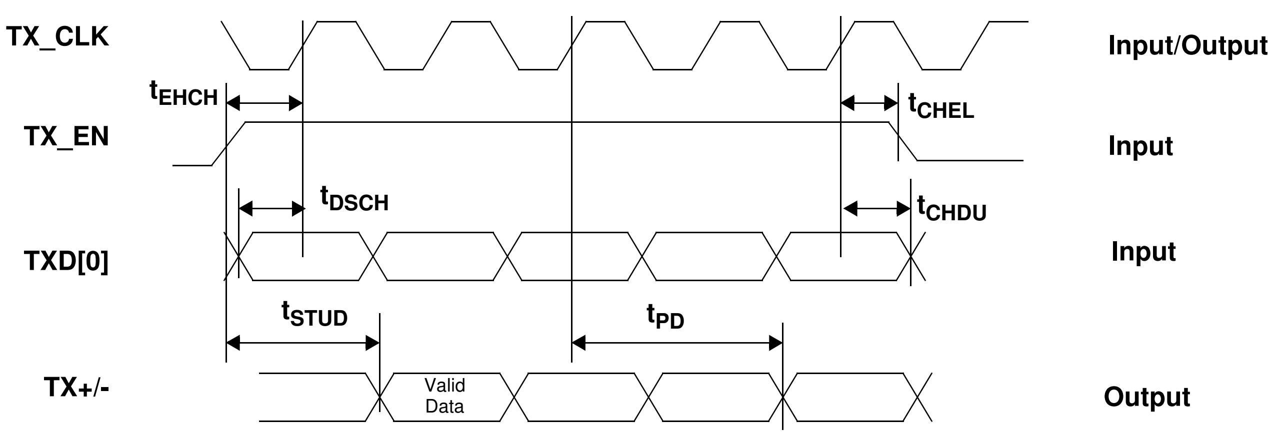
10BASE-T SERIAL RECEIVE TIMING

Parameter	Symbol	Min	Typ	Max	Unit
RX+/- active to RXD[0] active	t_{DATA}	-	-	1200	ns
RX+/- active to CRS active	t_{CRS}	-	-	600	ns
RXD[0] setup from RX_CLK	t_{RDS}	35	-	-	ns
RXD[0] hold from RX_CLK	t_{RDH}	50	-	-	ns
RX_CLK hold after CRS off	t_{RCH}	5	-	-	ns
RXD[0] throughput delay	t_{RD}	-	-	250	ns
CRS turn off delay	t_{CRSOFF}	-	-	400	ns



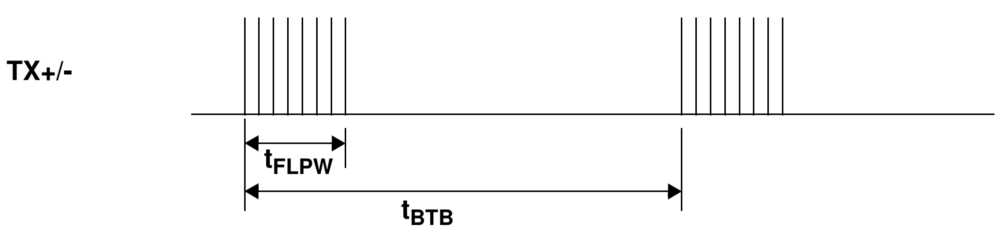
10BASE-T SERIAL TRANSMIT TIMING

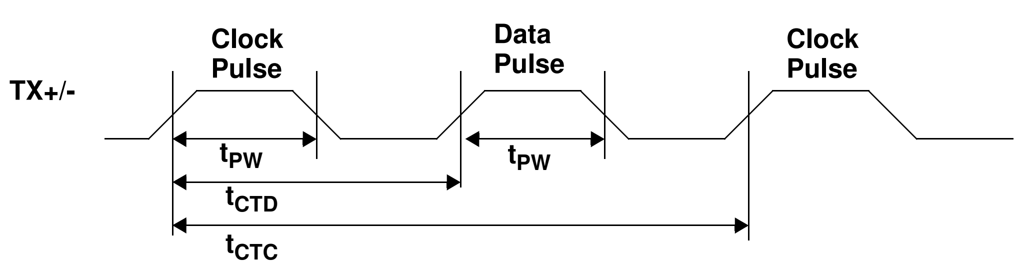
Parameter	Symbol	Min	Typ	Max	Unit
TX_EN Setup from TX_CLK	t_{EHCH}	10	-	-	ns
TX_EN Hold after TX_CLK	t_{CHEL}	10	-	-	ns
TXD[0] Setup from TX_CLK	t_{DSCH}	10	-	-	ns
TXD[0] Hold after TX_CLK	t_{CHDU}	10	-	-	ns
Transmit start-up delay	t_{STUD}	-	-	500	ns
Transmit throughput delay	t_{TPD}	-	-	500	ns



AUTO NEGOTIATION / FAST LINK PULSE TIMING

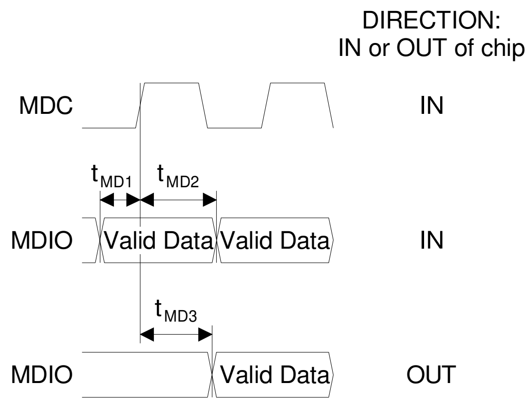
Parameter	Symbol	Min	Typ	Max	Unit
FLP burst to FLP burst	t_{BTB}	15	16	17	ms
FLP burst width	t_{FLPW}	-	2	-	ms
Clock/Data pulses per burst	-	17	-	33	ea.
Clock/Data pulse width	t_{PW}	-	100	-	ns
Clock pulse to Data pulse	t_{CTD}	55.5	64	69.5	µs
Clock pulse to clock pulse	t_{CTC}	111	128	139	µs





SERIAL MANAGEMENT INTERFACE TIMING

Parameter	Symbol	Min	Typ	Max	Unit
MDC Period	t_p	60	-	-	ns
MDC Pulse Width	t_{WL}, t_{WH}	40	-	60	%
MDIO Setup to MDC (MDIO as input)	t_{MD1}	10	-	-	ns
MDIO Hold after MDC (MDIO as input)	t_{MD2}	10	-	-	ns
MDC to MDIO valid (MDIO as output)	t_{MD3}	0	-	40	ns



2. INTRODUCTION

The CS8952 is a complete physical-layer transceiver for 100BASE-TX and 10BASE-T applications. Additionally, the CS8952 can be used with an external optical module for 100BASE-FX.

2.1 High Performance Analog

The highly integrated mixed-signal design of the CS8952 eliminates the need for external analog circuitry such as external transmit or receive filters. The CS8952 builds upon Cirrus Logic's experience in pioneering the high-volume manufacturing of 10BASE-T integrated circuits with "true" internal filters. The CS8952, CS8920, CS8904, and CS8900 include fifth-order, continuous-time Butterworth 10BASE-T transmit and receive filters, allowing those products to meet 10BASE-T wave shape, emission, and frequency content requirements without external filters.

2.2 Low Power Consumption

The CS8952 is implemented in low power CMOS, consuming only 135 mA typically. Three low-power modes are provided to make the CS8952 ideal for power sensitive applications such as CardBus.

2.3 Application Flexibility

The CS8952's digital interface and operating modes can be tailored to efficiently support a wide variety of applications. For example, the Media Independent Interface (MII) supports 100BASE-TX, 100BASE-FX and 10BASE-T NIC cards, switch ports and router ports. Additionally, the low-latency "repeater" interface mode minimizes data delay through the CS8952, facilitating system compliance with overall network delay budgets. To support 10BASE-T applications, the CS8952 provides a 10BASE-T serial port (Seven-wire ENDEC interface).

2.4 Typical Connection Diagram

Figure 1 illustrates a typical MII to CS8952 application with twisted-pair and fiber interfaces. Refer to the Analog Design Considerations section for detailed information on power supply requirements and decoupling, crystal and magnetics requirements, and twisted-pair and fiber transceiver connections.

3. FUNCTIONAL DESCRIPTION

The CS8952 is a complete physical-layer transceiver for 100BASE-TX and 10BASE-T applications. It provides a Physical Coding Sub-layer for communication with an external MAC (Media Access Controller). The CS8952 also includes a complete Physical Medium Attachment layer and a 100BASE-TX and 10BASE-T Physical Medium Dependent layer. Additionally, the CS8952 provides a PECL interface to an external optical module for 100BASE-FX applications.

The primary digital interface to the CS8952 is an enhanced IEEE 802.3 Media Independent Interface (MII). The MII supports parallel data transfer, access to the CS8952 Control and Status registers, and several status and control pins. The CS8952's operating modes can be tailored to support a wide variety of applications, including low-latency 100BASE-TX repeaters, switches and MII-based network interface cards.

For 100BASE-TX applications, the digital data interface can be either 4-bit parallel (nibbles) or 5-bit parallel (code-groups). For 10BASE-T applications, the digital data format can be either 4-bit parallel (nibbles) or one-bit serial.

The CS8952 is controlled primarily by configuration registers via the MII Management Interface. Additionally, a number of the most fundamental register bits can be set at power-up and reset time by connecting pull-up or pull-down resistors to external pins.

The CS8952's MII interface is enhanced beyond IEEE requirements by register extensions and the addition of pins for $\overline{\text{MII\_IRQ}}$, RX_EN, and ISODEF signals. The $\overline{\text{MII\_IRQ}}$ pin provides an inter-

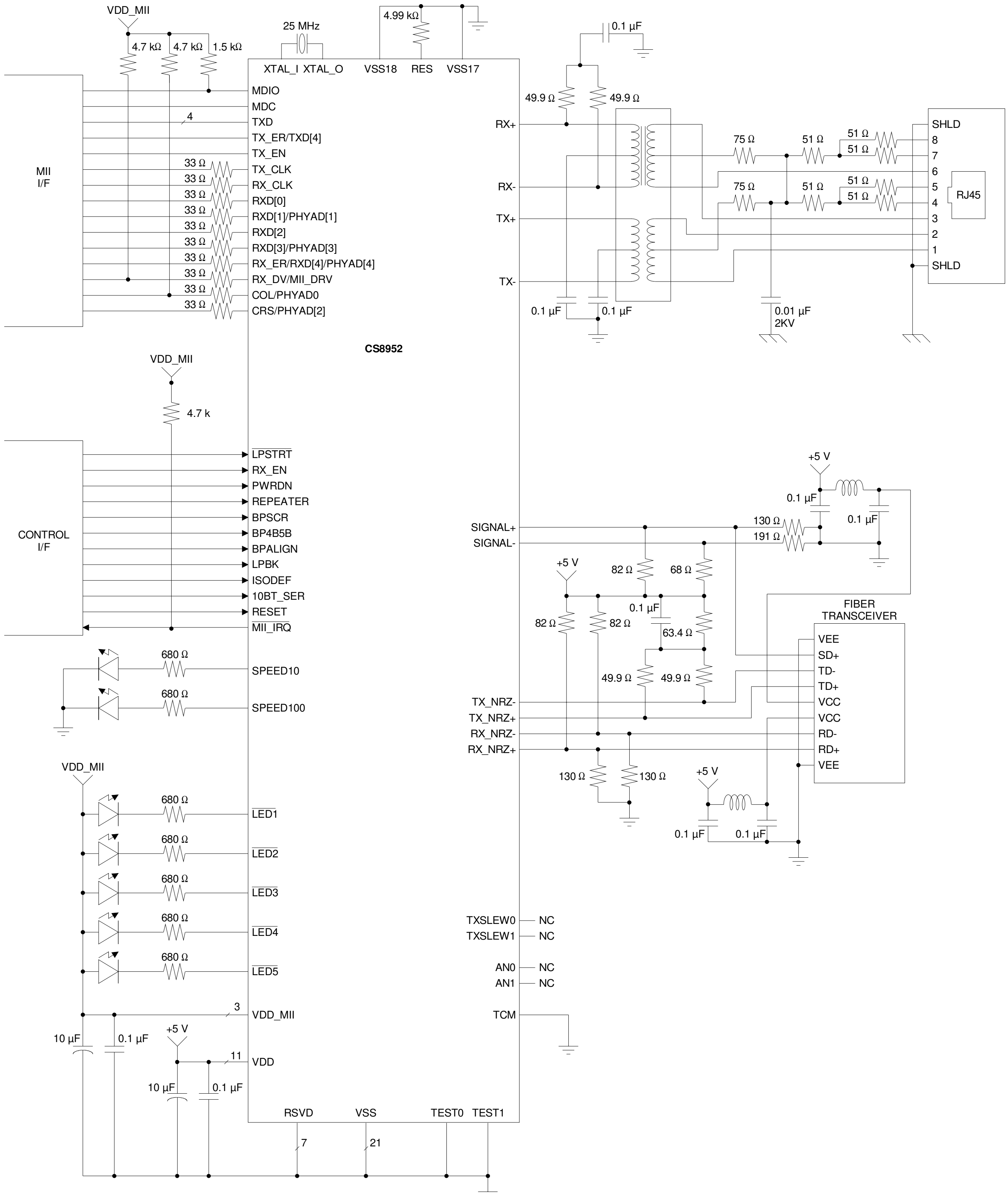


Figure 1. Typical Connection Diagram

rupt signal to the controller when a change of state has occurred in the CS8952, eliminating the need for the system to poll the CS8952 for state changes. The RX_EN signal allows the receiver outputs to be electrically isolated. The ISODEF pin controls the value of register bit ISOLATE in the Basic Mode Control Register (address 00h) which in turn electrically isolates the CS8952's MII data path.

3.1 Major Operating Modes

The following sections describe the four major operating modes of the CS8952:

- 100BASE-X MII Modes (TX and FX)
- 100BASE-X Repeater Modes
- 10BASE-T MII Mode
- 10BASE-T Serial Mode

The choice of operating speed (10 Mb/s versus 100 Mb/s) is made using the auto-negotiation input pins (AN0, AN1) and/or the auto-negotiation MII registers. The auto-negotiation capability also is used to select a duplex mode (full or half duplex). Both speed and duplex modes can either be forced or negotiated with the far-end link partner.

The digital interface mode (MII, repeater, or 10BASE-T serial) is selected by input pins BPALIGN, BP4B5B and 10BT_SER as shown in Table **1**. Speed and duplex selection are made through the AN[1:0] pins as shown in Table **5**.

Operating Mode	BPALIGN	BP4B5B	10BT_SER
100BASE-X MII	0	0	0
10BASE-T MII	0	0	0
100BASE-X Repeater	1	Don't Care	0
	0	1	0
10BASE-T Serial	Don't Care	Don't Care	1

Table 1.

3.1.1 100BASE-X MII Application (TX and FX)

The CS8952 provides an IEEE 802.3-compliant MII interface. Data is transferred across the MII in four-bit parallel (nibble) mode. TX_CLK and RX_CLK are nominally 25 MHz for 100BASE-X.

The 100BASE-X mode includes both the TX and FX modes, as determined by pin BPSCR (bypass scrambler), or the BPSCR bit (bit 13) in the Loopback, Bypass, and Receiver Error Mask Register (address 18h). In FX mode, an external optical module is connected to the CS8952 via pins TX_NRZ+, TX_NRZ-, RX_NRZ+, RX_NRZ-, SIGNAL+, and SIGNAL-. In FX mode, the MLT-3/NRZI conversion blocks and the scrambler/descrambler are bypassed.

3.1.1.1 Symbol Encoding and Decoding

In 100BASE-X modes, 4-bit nibble transmit data is encoded into 5-bit symbols for transmission onto the media as shown in Tables **2** and **3**. The encoding is necessary to allow data and control symbols to be sent consecutively along the same media transparent to the MAC layer. This encoding causes the symbol rate transmitted across the wire (125 symbols/second) to be greater than the actual data rate of the system (100 symbols/second).

DATA and CONTROL Codes (RX_ER = 0 or TX_ER = 0)			
Name	**5-bit Symbol**	**4-bit Nibble**	**Comments**
DATA (Note **1**)			
0	11110	0000	
1	01001	0001	

DATA and CONTROL Codes (RX_ER = 0 or TX_ER = 0)			
Name	**5-bit Symbol**	**4-bit Nibble**	**Comments**
2	10100	0010	
3	10101	0011	
4	01010	0100	
5	01011	0101	
6	01110	0110	
7	01111	0111	
8	10010	1000	
9	10011	1001	
A	10110	1010	
B	10111	1011	
C	11010	1100	
D	11011	1101	
E	11100	1110	
F	11101	1111	
CONTROL (Note **2**)			
I	11111	0101	IDLE (Note **3**)
J	11000	0101	First Start of Stream Symbol
K	10001	0101	Second Start of Stream Symbol
T	01101	0000	First End of Stream Symbol
R	00111	0000	Second End of Stream Symbol

1. DATA code groups are indicated by RX_DV = 1
2. CONTROL code groups are inserted automatically during transmission in response to TX_EN. They are not generated through any combination of TXD[3:0] or TX_ER.
3. IDLE is indicated by RX_DV = 0.

Table 2. 4B5B Symbol Encoding/Decoding

Code Violations (RX_ER = 1 or TX_ER = 1)				
Name	**5-bit Symbol**	**Normal Mode 4-bit Nibble**	**Error Report Mode 4-bit Nibble**	**Comments**
CONTROL (Note **1**)				
I	11111	0000	0000	This portion of the table relates received 5-bit symbols to received 4-bit nibbles only. The control code groups may not be transmitted in the data portion of the frame.
J	11000	0000	0000	
K	10001	0000	0000	
T	01101	0000	0000	
R	00111	0000	0000	
CODE VIOLATIONS				
H	00100	0000	0000	
V0	00000	0110 or 0101 (Note **2**)	0001	
V1	00001	0110 or 0101 (Note **2**)	0111	
V2	00010	0110 or 0101 (Note **2**)	1000	
V3	00011	0110 or 0101 (Note **2**)	1001	
V4	00101	0110 or 0101 (Note **2**)	1010	
V5	00110	0110 or 0101 (Note **2**)	1011	

Code Violations (RX_ER = 1 or TX_ER = 1)				
Name	**5-bit Symbol**	**Normal Mode 4-bit Nibble**	**Error Report Mode 4-bit Nibble**	**Comments**
V6	01000	0110 or 0101 (Note **2**)	1100	
V7	01100	0110 or 0101 (Note **2**)	1101	
V8	10000	0110 or 0101 (Note **2**)	1110	
V9	11001	0110 or 0101 (Note **2**)	1111	

1. CONTROL code groups become violations when found in the data portion of the frame.
2. Invalid code groups are mapped to 5h unless the Code Error Report select bit in the Loopback, Bypass, and Receiver Error Mask Register (address 18h) is set, in which case invalid code groups are mapped to 6h.

Table 3. 4B5B Code Violation Decoding

3.1.1.2 100 Mb/s Loopback

One of two internal 100BASE-TX loopback modes can be selected. Local loopback redirects the TXD[3:0] input data to RXD[3:0] data outputs through the 4B5B coders and scramblers. Local loopback is selected by asserting pin LPBK, by setting the LPBK bit (bit 14) in the Basic Mode Control Register (address 00h) or by setting bits 8 and 11 in the Loopback, Bypass, and Receiver Error Mask Register (address 18h) as shown in Table **4**.

Remote loopback redirects the analog line interface inputs to the analog line driver outputs. Remote loopback is selected by setting bit 9 in the Loopback, Bypass, and Receiver Error Mask Register (address 18h) as shown in Table **4**.

Remote Loopback (bit 9)	PMD Loopback (bit 8)	Function
0	0	No Loopback
0	1	Local Loopback (toward MII)
1	0	Remote Loopback (toward line)
1	1	Operation is undefined

Table 4.

When changing between local and non-loopback modes, the data on RXD[3:0] will be undefined for approximately 330 µs.

3.1.2 100BASE-X Repeater Application

The CS8952 provides two low latency modes for repeater applications. These are selected by asserting either pin BPALIGN or BP4B5B. Both pins have the effect of bypassing the 4B5B encoder and decoder. Bypassing the coders decreases latency, and uses a 5-bit wide parallel code group interface on pins RXD[4:0] and TXD[4:0] instead of the 4-bit wide MII nibble interface on pins RXD[3:0] and TXD[3:0]. In repeater mode, pin RX_ER is redefined as the fifth receive data bit (RXD4), and pin TX_ER is redefined as the fifth transmit data bit (TXD4).

BPALIGN can also be selected by setting bit 12 in Loopback, Bypass, and Receiver Error Mask Register (address 18h). BP4B5B can be selected by setting bit 14 of the same register.

Pin BPALIGN causes more of the CS8952 to be bypassed than the BP4B5B pin. BPALIGN also bypasses the scrambler/descrambler, and the NRZI to NRZ converters (see Figure **1**). Also, for repeater applications, pin REPEATER should be asserted to redefine the function of the CRS (carrier sense) pin. The REPEATER function may also be invoked by setting bit 12 in the PCS Sublayer Configuration Register (address 17h).

For repeater applications, the RX_EN pin can be used to gate the receive data pins (RXD[4:0], RX_CLK, RX_DV, COL, and CRS) onto a shared, external repeater system bus.

3.1.3 10BASE-T MII Application

The digital interface used in this mode is the same as that used in the 100BASE-X MII mode except that TX_CLK and RX_CLK are nominally 2.5 MHz.

The CS8952 includes a full-featured 10BASE-T interface, as described in the following sections.

3.1.3.1 Full and Half Duplex operation

The 10BASE-T function supports full and half duplex operation as determined by pins AN[1:0] and/or the corresponding MII register bits. (See Table **5**).

3.1.3.2 Collision Detection

If half duplex operation is selected, the CS8952 detects a 10BASE-T collision whenever the receiver and transmitter are active simultaneously. When a collision is present, the collision is reported on pin COL. Collision detection is undefined for full-duplex operation.

3.1.3.3 Jabber

The jabber timer monitors the transmitter and disables the transmission if the transmitter is active for greater than approximately 105 ms. The transmitter stays disabled until approximately 406 ms after the internal transmit request is no longer enabled.

3.1.3.4 Link Pulses

To prevent disruption of network operation due to a faulty link segment, the CS8952 continually monitors the 10BASE-T receive pair (RXD+ and RXD-) for packets and link pulses. After each packet or link pulse is received, an internal Link-Loss timer is started. As long as a packet or link pulse is received before the Link-Loss timer finishes (between 50 and 100 ms), the CS8952 maintains normal operation. If no receive activity is detected, the CS8952 disables packet transmission to prevent “blind” transmissions onto the network (link pulses are still sent while packet transmission is disabled). To reactivate transmission, the receiver must detect a single packet (the packet itself is ignored), or two normal link pulses separated by more than 6 ms and no more than 50 ms.

The CS8952 automatically checks the polarity of the receive half of the twisted pair cable. To detect a reversed pair, the receiver examines received link pulses and the End-of-Frame (EOF) sequence of incoming packets. If it detects at least one reversed link pulse and at least four frames in a row with negative polarity after the EOF, the receive pair is considered reversed. If the polarity is reversed and bit 1 of the 10BASE-T Configuration Register (address 1Ch), is set, the CS8952 automatically corrects a reversal.

In the absence of transmit packets, the transmitter generates link pulses in accordance with Section 14.2.1.1 of the Ethernet standard. Transmitted link pulses are positive pulses, one bit time wide, typically generated at a rate of one every 16 ms. The 16 ms timer also starts whenever the transmitter completes an End-of-Frame (EOF) sequence. Thus, a link pulse will be generated 16 ms after an EOF unless there is another transmitted packet.

3.1.3.5 Receiver Squelch

The 10BASE-T squelch circuit determines when valid data is present on the RXD+/RXD- pair. Incoming signals passing through the receive filter are tested by the squelch circuit. Any signal with amplitude less than the squelch threshold (either positive or negative, depending on polarity) is rejected.

3.1.3.6 10BASE-T Loopback

When Loopback is selected, the TXD[3:0] pins are looped back into the RXD[3:0] pins through the

Manchester Encoder and Decoder. Selection is made via:

- setting bit 14 in the Basic Mode Control Register (address 00h) or
- setting bits 8 and 11 in the Loopback, Bypass, and Receiver Error Mask Register (address 18h) or
- asserting the LPBK pin.

3.1.3.7 Carrier Detection

The carrier detect circuit informs the MAC that valid receive data is present by asserting the Carrier Sense signal (CRS) as soon it detects a valid bit pattern (1010b or 0101b for 10BASE-T). During normal packet reception, CRS remains asserted while the frame is being received, and is de-asserted within 2.3 bit times after the last low-to-high transition of the End-of-Frame (EOF) sequence. Whenever the receiver is idle (no receive activity), CRS is de-asserted.

3.1.4 10BASE-T Serial Application

This mode is selected when pin 10BT_SERis asserted during power-up or reset, and operates similar to the 10BASE_T MII mode except that data is transferred serially on pins RXD0 and TXD0 using a 10 MHz RX_CLK and TX_CLK. Receive data is framed by CRS rather than RX_DV.

3.2 Auto-Negotiation

The CS8952 supports auto-negotiation, which is the mechanism that allows the two devices on either end of an Ethernet link segment to share information and automatically configure both devices for maximum performance. When configured for auto-negotiation, the CS8952 will detect and automatically operate full-duplex at 100 Mb/s if the device on the other end of the link segment also supports full-duplex, 100 Mb/s operation, and auto-negotiation. The CS8952 auto-negotiation capability is fully compliant with the relevant portions of section 28 of the IEEE 802.3u standard.

The CS8952 can auto-negotiate both operating speed (10 versus 100 Mb/s), duplex mode (half duplex versus full duplex), and flow control (pause frames), or alternatively can be set not to negotiate. At power-up and reset times, the auto-negotiation mode is selected via the auto-negotiation input pins (AN[1:0]). This selection can later be changed using the Auto-Negotiation Advertisement Register (address 04h).

Pins AN[1:0] are three level inputs, and have the function shown in Table **5**.

AN1	AN0	Forced/ Auto	Speed (Mb/s)	Full/Half Duplex
Low	Floating	Forced	10	Half
High	Floating	Forced	10	Full
Floating	Low	Forced	100	Half
Floating	High	Forced	100	Full
Floating	Floating	Auto-Neg	100/10	Full/Half
Low	Low	Auto-Neg	10	Half
Low	High	Auto-Neg	10	Full
High	Low	Auto-Neg	100	Half
High	High	Auto-Neg	100	Full

Table 5.

Auto-Negotiation encapsulates information within a burst of closely spaced Link Integrity Test Pulses, referred to as a Fast Link Pulse (FLP) Burst. The FLP Burst consists of a series of Link Integrity Pulses which form an alternating clock / data sequence. Extraction of the data bits from the FLP Burst yields a Link Code Word which identifies the capability of the remote device.

In order to support legacy 10 and 100 Mb/s devices, the CS8952 also supports parallel detection. In parallel detection, the CS8952 monitors activity on the media to determine the capability of the link partner even without auto-negotiation having occurred.

3.3 Reset Operation

Reset occurs in response to six different conditions:

1) There is a chip-wide reset whenever the RESET pin is high for at least 200 ns. During a chip-wide reset, all circuitry and registers in the CS8952 are reset.

2) When power is applied, the CS8952 maintains reset until the voltage at the VDD supply pins reaches approximately 3.6 V. The CS8952 comes out of reset once VDD is greater than approximately 3.6 V and the crystal oscillator has stabilized.

3) There is a chip-wide reset whenever the RESET bit (bit 15 of the Basic Mode Control Register (address 00h)) is set.

4) Digital circuitry is reset whenever bit 0 of the PCS Sub-Layer Configuration Register (address 17h) is set. Analog circuitry is unaffected.

5) Analog circuitry is reset and recalibrated whenever the CS8952 enters or exits the power-down state, as requested by pin PWRDN.

6) Analog circuitry is reset and recalibrated whenever the CS8952 changes between 10 Mb/s and 100 Mb/s modes.

After a reset, the CS8952 latches the signals on various input pins in order to initialize key registers and goes through a self configuration. This includes calibrating on-chip analog circuitry. Time required for the reset calibration is typically 40 ms. External circuitry may access registers internal to the CS8952 during this time. Reset and calibration complete is indicated when bit 15 of the Basic Mode Control Register (address 00h) is clear.

3.4 LED Indicators

The $\overline{\text{LEDx}}$, SPD100, and SPD10 output pins provide status information that can be used to drive LEDs or can be used as inputs to external control circuitry. Indication options include: receive activity, transmit activity, collision, carrier sense, polarity OK, descrambler synchronization status, auto-negotiation status, speed (10 vs. 100), and duplex mode.

4. MEDIA INDEPENDENT INTERFACE (MII)

The Media Independent Interface (MII) provides a simple interconnect to an external Media Access Controller (MAC). This connection may be chip to chip, motherboard to daughterboard, or a connection between two assemblies attached by a limited length of shielded cable and an appropriate connector.

The MII interface uses the following pins: