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CTSLV363

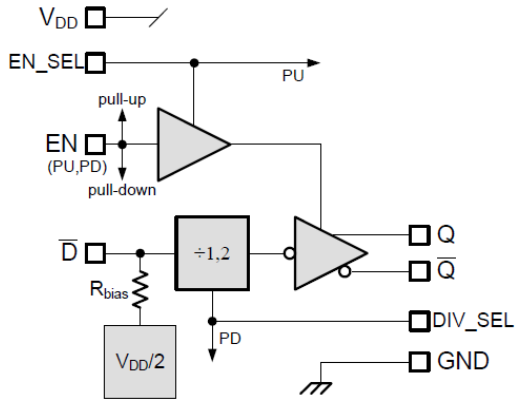
Low Phase Noise LVPECL Buffer and Translator

SON8

FEATURES

- LVPECL Outputs Optimized for Very Low Phase Noise (-165dBc/Hz)
- Up to 1GHz Bandwidth
- Selectable ÷1, ÷2 Output
- Selectable Enable Logic
- 3.0V to 3.6V Operation
- RoHS Compliant Pb Free Packages

BLOCK DIAGRAM



DESCRIPTION

The CTSLV363 is a sine wave/CMOS to LVPECL buffer/translator optimized for very low phase noise (-165dBc/Hz). It is particularly useful in converting crystal or SAW based oscillators into LVPECL outputs for greater than 1GHz of bandwidth.

The CTSLV363 is one of a family of parts that provide options of fixed ÷1, fixed ÷2 and selectable ÷1, ÷2 modes as well as active high enable or active low enable to oscillator designers. Refer to Table 1 for the comparison of parts within the CTSLV35x and CTSLV363 family.

ENGINEERING NOTES

Functionality

Table 1 details the differences between the family parts to assist designers in selecting the optimal part for their design.

Table 2 lists the specific CTSLV363 functional operation.

Figure 1 plots the S-parameters of the D input.

Table 1

Part Number	Divide Ratio	EN Logic	EN Pull-Up / Pull-Down	Bandwidth
CTSLV351	÷1	active HIGH	Pull-up	> 800MHz
CTSLV353	Selectable ÷1 or ÷2	selectable	selectable	> 800MHz
CTSLV363	Selectable ÷1 or ÷2	selectable	selectable	≥ 1GHz

Table 2 – CTSLV363 Functional Operation, ÷1 mode

	Inputs			Outputs	
Part Number	**EN_SEL**	**EN**	**D**	**Q**	**`Q**
CTSLV363	High, NC	Low, NC	Low	Low	High
			High	High	Low
		High	X	Z	Z
	Low	High, NC	Low	Low	High
			High	High	Low
		Low	X	Z	Z

DIV_SEL	**Divide Ratio**
Low, NC	÷1
High	÷2

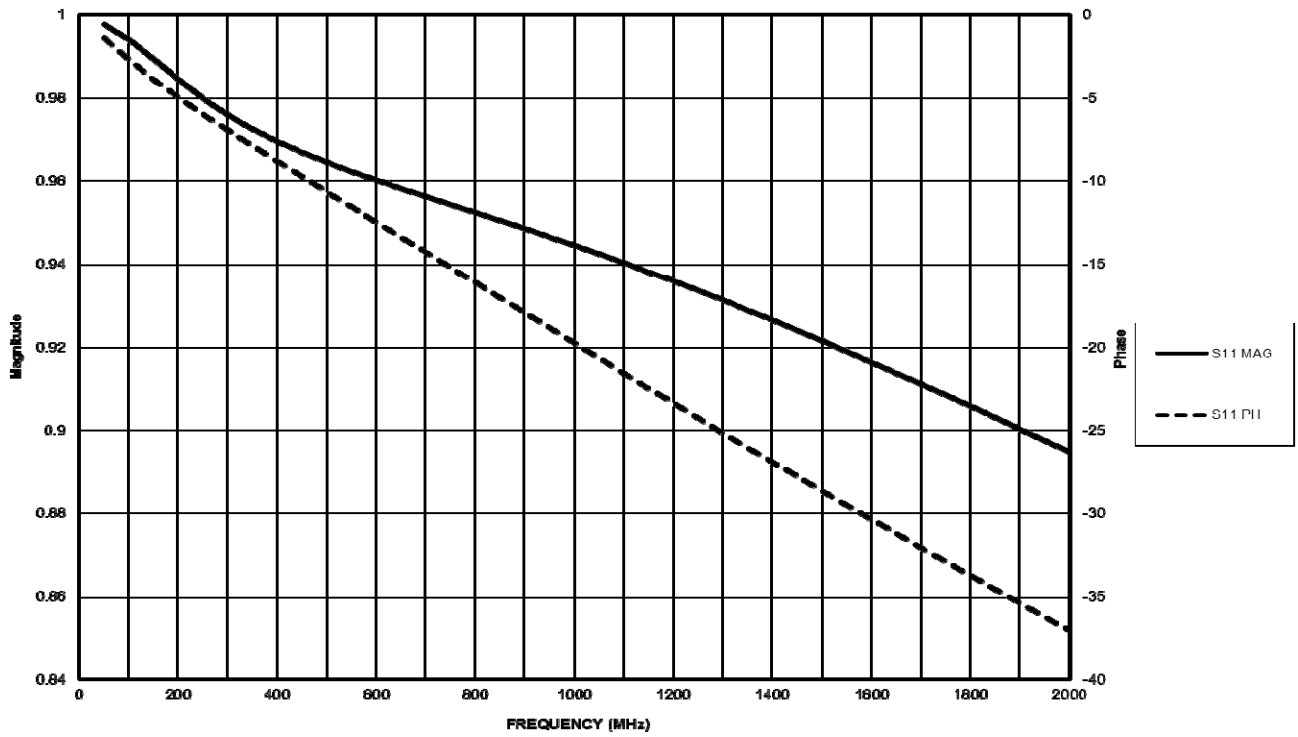


Figure 1- S11, Parameters, $\overline{D}$ Input

Input Termination

The D input bias is $V_{DD}/2$ fed through an internal 10kΩ resistor. For clock applications, an input signal of at least 750mV_{PP} ensures the CTSLV363 meets AC specifications. The input should also be AC coupled to maintain a 50% duty cycle on the outputs. The input can be driven to any voltage between 0V and V_{DD} without damage or waveform degradation.

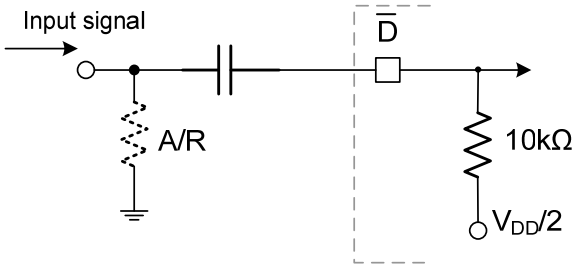


Figure 2 - Input Termination

Output Termination Techniques

The LVPECL compatible output stage of the CTSLV363 uses a current drive topology to maximize switching speed as illustrated below in Figure 3. Two current source PMOS transistors (M1-M2) feed the output pins. M5 is an NMOS current source which is switched by M3 and M4. When M4 is on, M5 takes current from M2. This produces an output current of 5.1mA (low output state). M3 is off, and the entire 21.1mA flows through the output pin. The associated output voltage swings match LVPECL levels when external 50Ω resistors terminate the outputs.

Both Q and $\overline{Q}$ should always be terminated identically to avoid waveform distortion and circulating current caused by unsymmetrical loads. This rule should be followed even if only one output is in use.

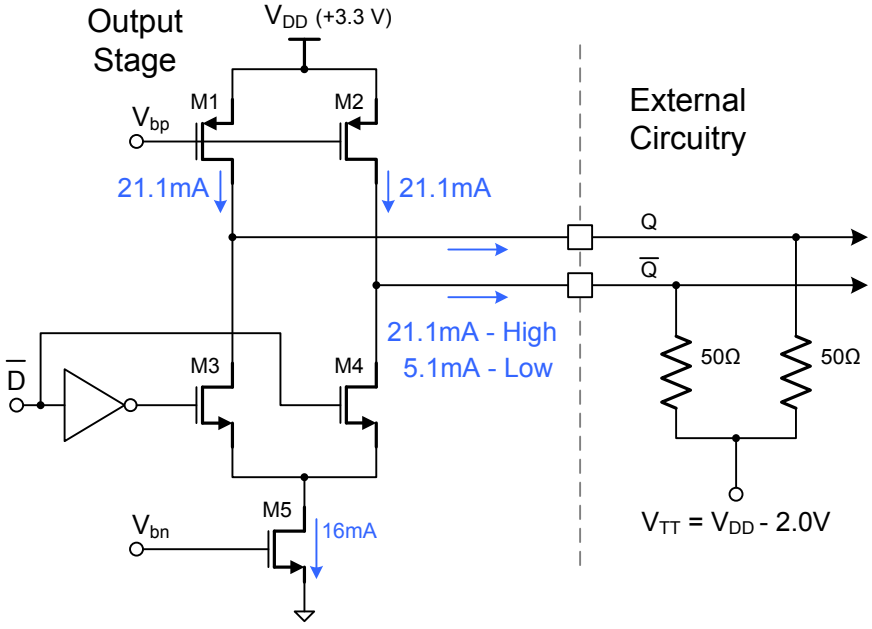


Figure 3 - Typical Output Termination

Dual Supply LVPECL Output Termination

The standard LVPECL loads are a pair of 50Ω resistors connected between the outputs and V_{DD} -2.0V (Figure 3). The resistors provide both the DC and the AC loads, assuming 50Ω interconnect. If an additional supply is available within the application, a four resistor termination configuration is possible (Figure 4).

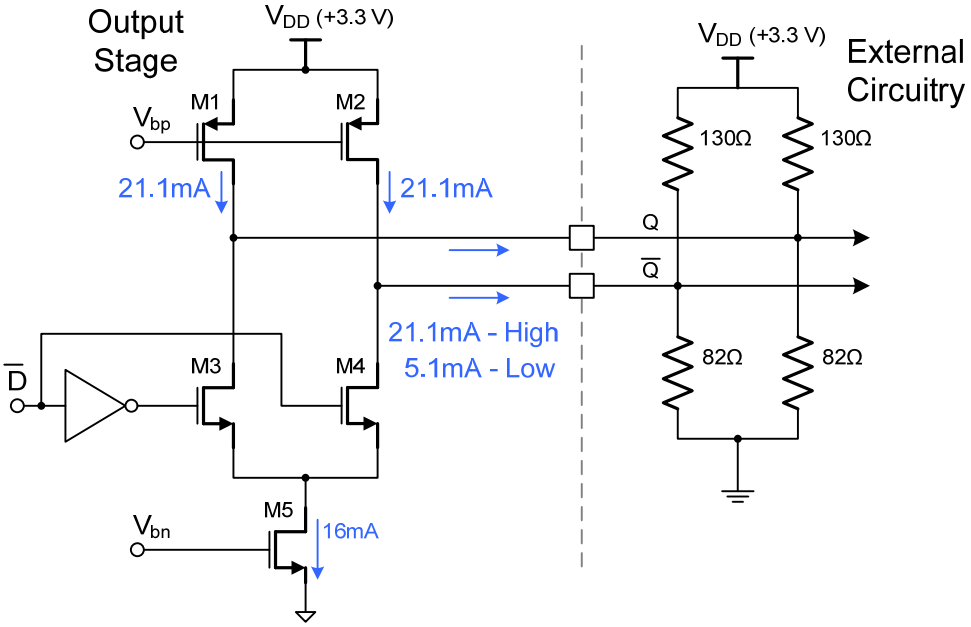


Figure 4 - Dual Supply Output Termination

Three Resistor Termination

Another termination variant eliminates the need for the additional supply (Figure 5). Alternately three resistors and one capacitor accomplish the same termination and reduce power consumption.

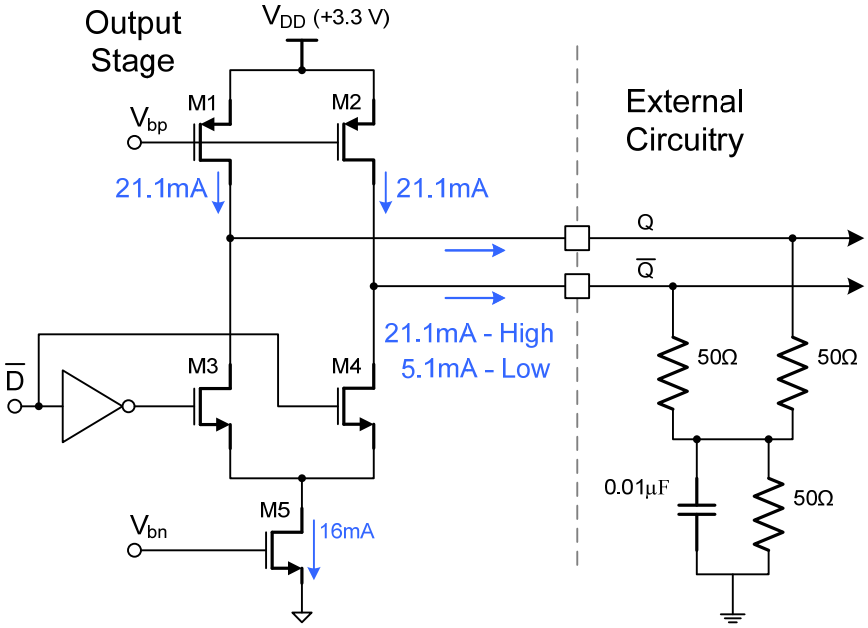


Figure 5 - Three Resistor Termination

Evaluation Board (EBP63)

CTS's evaluation board EBP63 provides the most convenient way to test and prototype CTSLV363 series circuits. Built for the CTSLV363Q 1.5x1.0 mm package, it is designed to support both dual and single supply operation. Dual supply operation (V_{DD}=+2.0V, V_{SS}=-1.3V) enables direct coupling to 50Ω time domain test equipment (Figure 6).

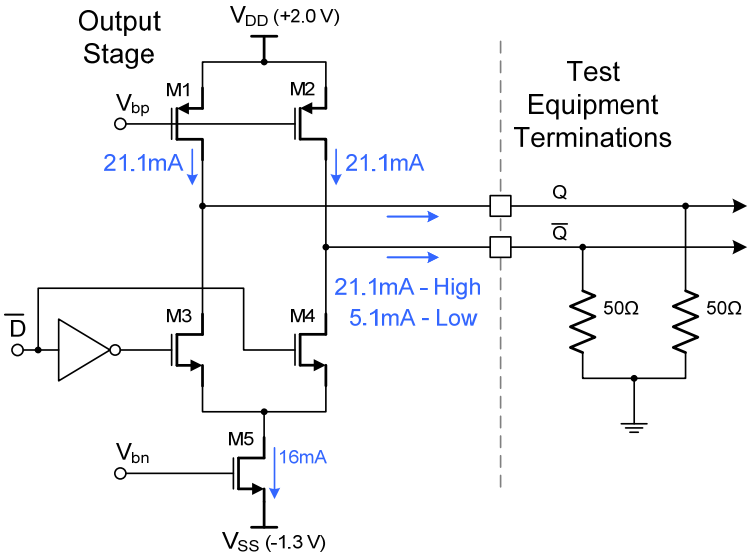


Figure 6 - Split Supply LVPECL Output Termination

AC Termination

Clock applications or phase noise/frequency domain testing scenarios typically require AC coupling. Figure 7 below shows the AC coupling technique. The 200Ω resistors form the required DC loads, and the 50Ω resistors provide the AC termination. The parallel combination of the 200Ω and 50Ω resistors results in a net 40Ω AC load termination. In many cases this will work well. If necessary, the 50Ω resistors can be increased to about 56Ω. Alternately, bias tees combined with current setting resistors will eliminate the lowered AC load impedance. The 50Ω resistors are typically connected to ground but can be connected to the bias level needed by the succeeding stage.

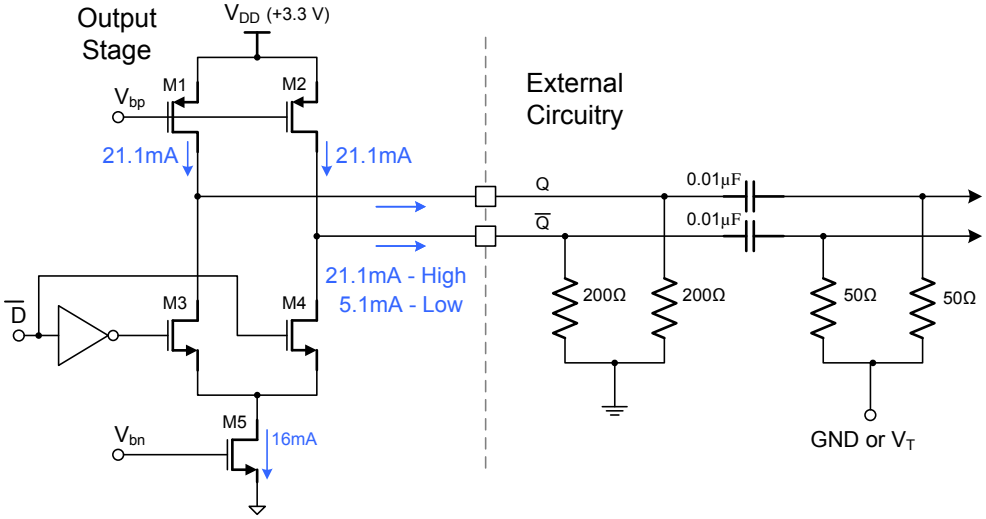


Figure 7 - AC Termination

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Rating	Unit
V_{DD}	Power Supply	0 to +5.5	V
V_I	Input Voltage	-0.5 to V_{DD} + 0.5	V
T_A	Operating Temperature Range	-40 to +85	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
ESD_{HBM}	Human Body Model	2500	V
ESD_{MM}	Machine Model	200	V
ESD_{CDM}	Charged Device Model	2500	V

DC Characteristics

DC Characteristics (V_{DD} = 3.0V to 3.6V unless otherwise specified, T_A = -40°C to +85°C)

Symbol	Characteristic	Conditions		Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage[1]	-40°C	V_{DD} = 3.3V	2.05		2.415	V
		+25°C		2.05		2.48	
		+85°C		2.05		2.54	
V_{OL}	Output LOW Voltage[1]	-40°C	V_{DD} = 3.3V	1.365		1.615	V
		+25°C		1.43		1.68	
		+85°C		1.49		1.74	
I_Z	Output Leakage Current, Tri-state[2]	EN=Disable		-10		10	µA
V_{IH}	High Level Input Voltage	EN_SEL		2			V
		DIV_SEL					
V_{IL}	Low Level Input Voltage	EN				0.8	V
I_{PU}	Pull-up Current	EN_SEL			2.2		µA
I_{PD}	Pull-down Current	DIV_SEL			-2.2		µA
I_P	Pull-up / Pull-down Current	EN			±2.2		µA
R_{BIAS}	Bias Resistor	$\overline{D}$ Input to Internal $V_{DD}/2$ Reference			10k		Ω
I_{DD}	Power Supply Current				22	35	mA
I_{DDZ}	Power Supply Current –	$\overline{D}$ Input ≤ V_{IL}				8	mA
	Outputs Tri-state[1]	EN=Disable					

[1] Specified with outputs terminated through 50Ω resistors to V_{DD} -2V or Thevenin equivalent.

[2] Measured at Q / $\overline{Q}$ pins.

AC Characteristics

AC Characteristics (V_{DD} = 3.0V to 3.6V, T_A = -40°C to +85°C)

AC Specifications guaranteed by design

Symbol	Characteristic	Min	Typ	Max	Unit
t_r / t_f	Output Rise/Fall[1, 2] (20% - 80%)	80		250	ps
f_{MAX}	Maximum Input Frequency - Sine wave[2]				MHz
	÷1			800	
	÷2			1300	
V_{INMAX}	Maximum Recommended Input Signal			V_{DD}	V_{PP}
V_{INMIN}	Minimum Recommended Input Signal	0.2			V_{PP}
t_{PLH}	Propagation Delay	938		1614	ps
t_{PHL}	Propagation Delay	938		1614	ps
j_{RMS}	RMS Jitter: 12kHz - 20MHz, 155MHz Center Freq		36		fs
n_P	Phase Noise[1, 2] - 1MHz offset		-165		dBc/Hz

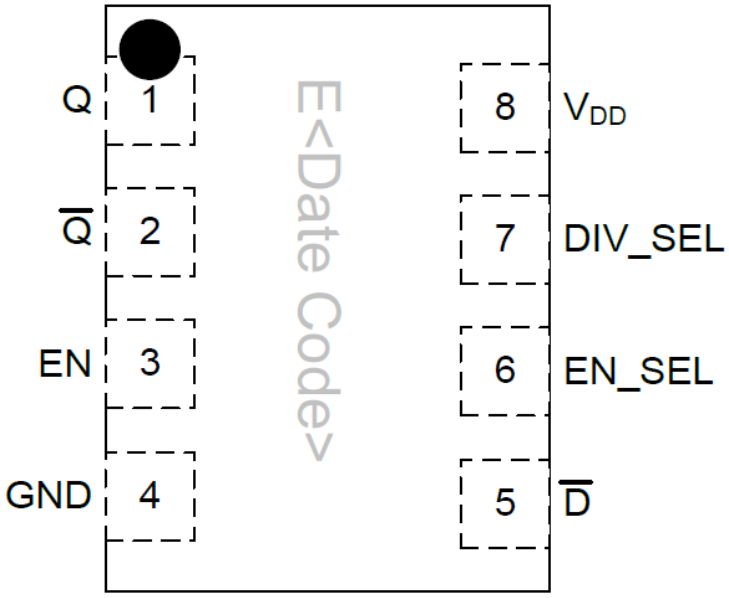
[1] Specified with outputs terminated through 50W resistors to V_{CC} -2V or Thevenin equivalent.

[2] 1.5 V_{P-P} sine wave input, AC coupled to D pin.

Pin Description and Configuration

Pin Assignments

Pin	Name	Type	Function
1	Q	Output	LVPECL Output
2	$\overline{Q}$	Output	LVPECL Output
3	EN	Input	Enable
4	GND	Power	Negative Supply
5	$\overline{D}$	Input	Sine or CMOS Input
6	EN_SEL	Input	Enable Select
7	DIV_SEL	Input	Divide Select
8	V_{DD}	Power	Positive Supply

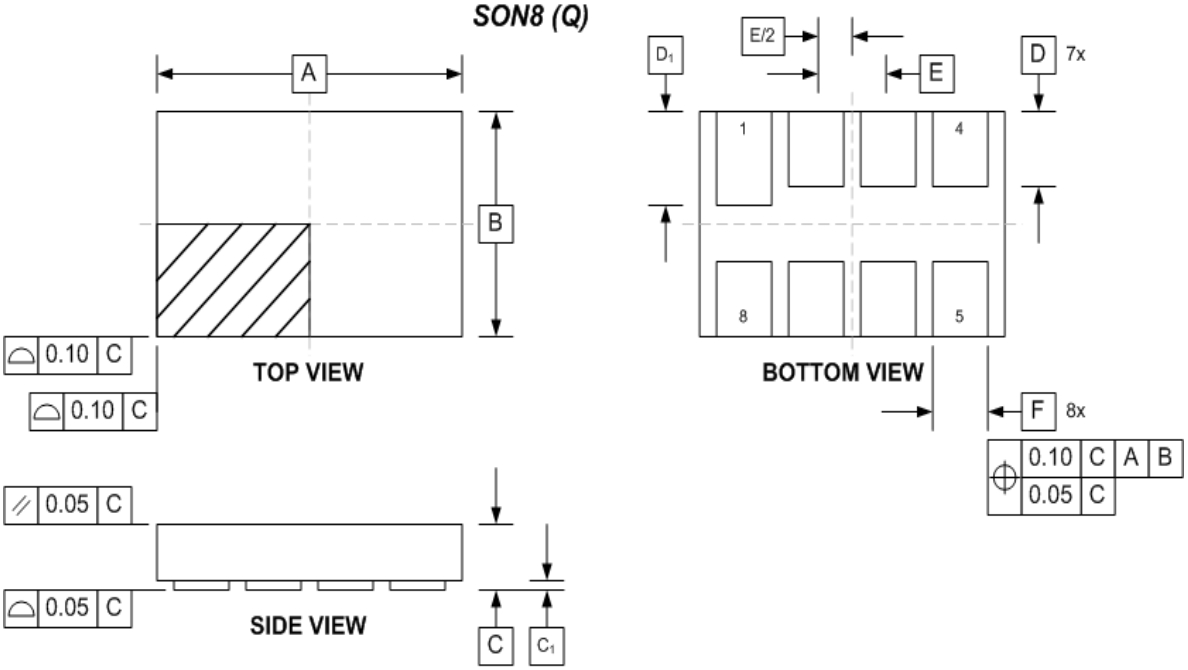


PART ORDERING INFORMATION

Part Number	Package	Marking
CTSLV363QG	SON8	E YW

PACKAGE DIMENSIONS

SON8 (Q)



	MILLIMETERS	
DIM	MIN	MAX
A	1.50 BSC	
B	1.00 BSC	
C	---	0.40
C_1	0.00	0.05
D	0.25	0.35
D_1	0.30	0.40
E	0.35 BSC	
F	0.15	0.25

PCB LAND PATTERN/FOOTPRINT