Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

CTSLVEL16VV

Dual Frequency PECL/ECL Oscillator Gain Stage & Buffer with Enable

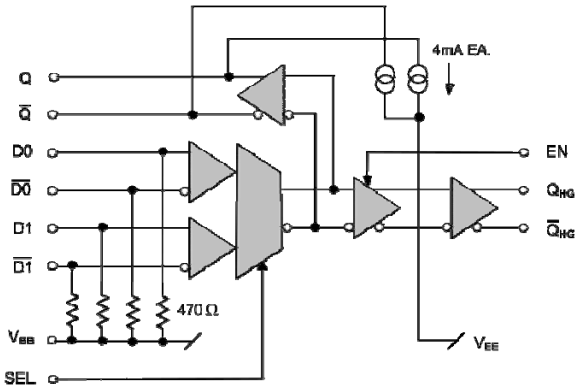
MLP16

Not recommended for new designs

FEATURES

- Minimizes External Components
- Similar Operation as CTSLVEL16VR except with Selectable Data Input Pairs
- High Bandwidth for ≥1GHz
- -147 dBc/Hz Typical Noise Floor

BLOCK DIAGRAM



DESCRIPTION

The CTSLVEL16VV is a specialized oscillator gain stage with two selectable data input pairs and a high gain output buffer including an enable. Selectable data input pairs permit switching between two different oscillator frequencies. The $Q_{HG}/\overline{Q}_{HG}$ outputs have a voltage gain several times greater than the $Q/\overline{Q}$ outputs. An enable allows continuous oscillator operation by only controlling the Q_{HG} outputs.

The CTSLVEL16VV also provides a reference voltage (V_{BB}) with internal biasing resistors to each input to minimize external components.

ENGINEERING NOTES

The CTSLVEL16VV is a specialized oscillator gain stage with two selectable data input pairs and a high gain output buffer including an enable. The $Q_{HG}/\overline{Q}_{HG}$ outputs have a voltage gain several times greater than the $Q/\overline{Q}$ outputs.

The CTSLVEL16VV provides two selectable data input pairs that permit switching between two different oscillator frequencies. When the select pin (SEL) is LOW or open (NC) data from the D0/$\overline{D0}$ is selected. When the SEL pin is HIGH data from the D1/$\overline{D1}$ is selected. Allowing continuous oscillator operation, the (EN) enable works with either data input pair. When EN is HIGH or open (NC), input data is passed to both sets of outputs. When EN is LOW, the $Q_{HG}/\overline{Q}_{HG}$ outputs will be forced LOW/HIGH respectively, while input data will continue to be passed to the $Q/\overline{Q}$ outputs. The EN and SEL inputs can be driven with an ECL/PECL signal or a full supply swing CMOS type logic signal.

The CTSLVEL16VV also provides a V_{BB} with a 1.5mA sink/source current. Each data input is separately connected to V_{BB} with a 470Ω internal bias resistor. Bypassing VBB to ground with a 0.01µF capacitor is recommended.

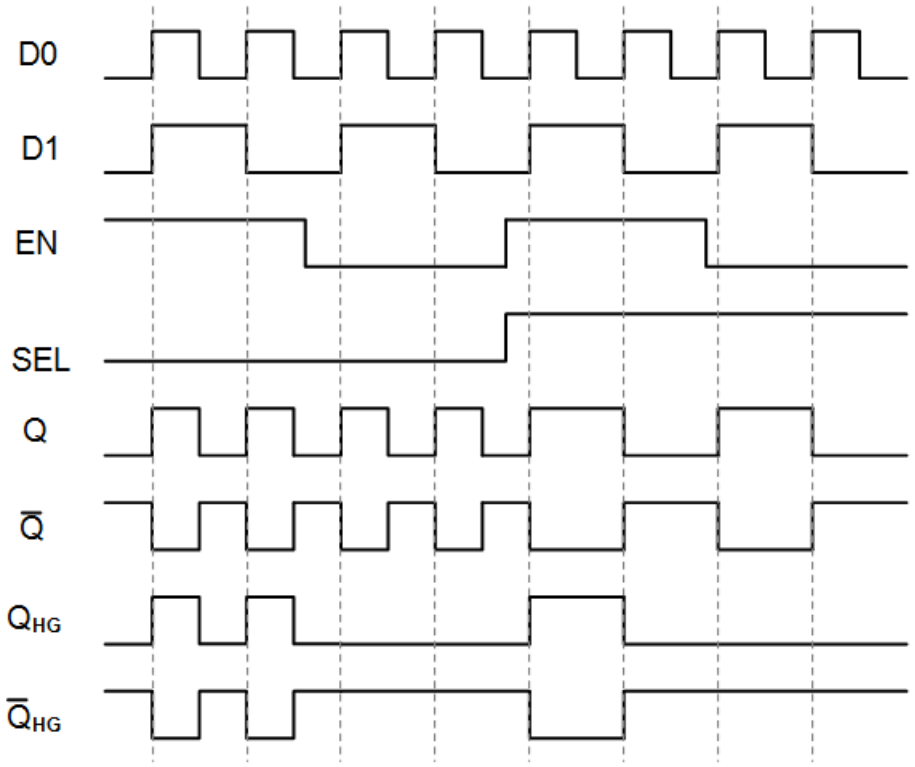
Each $Q/\overline{Q}$ output has a 4mA on-chip pull-down current source. External resistors may also be used to increase pull-down current of the $Q/\overline{Q}$ to a maximum of 25mA each (includes a 4mA on-chip current source).

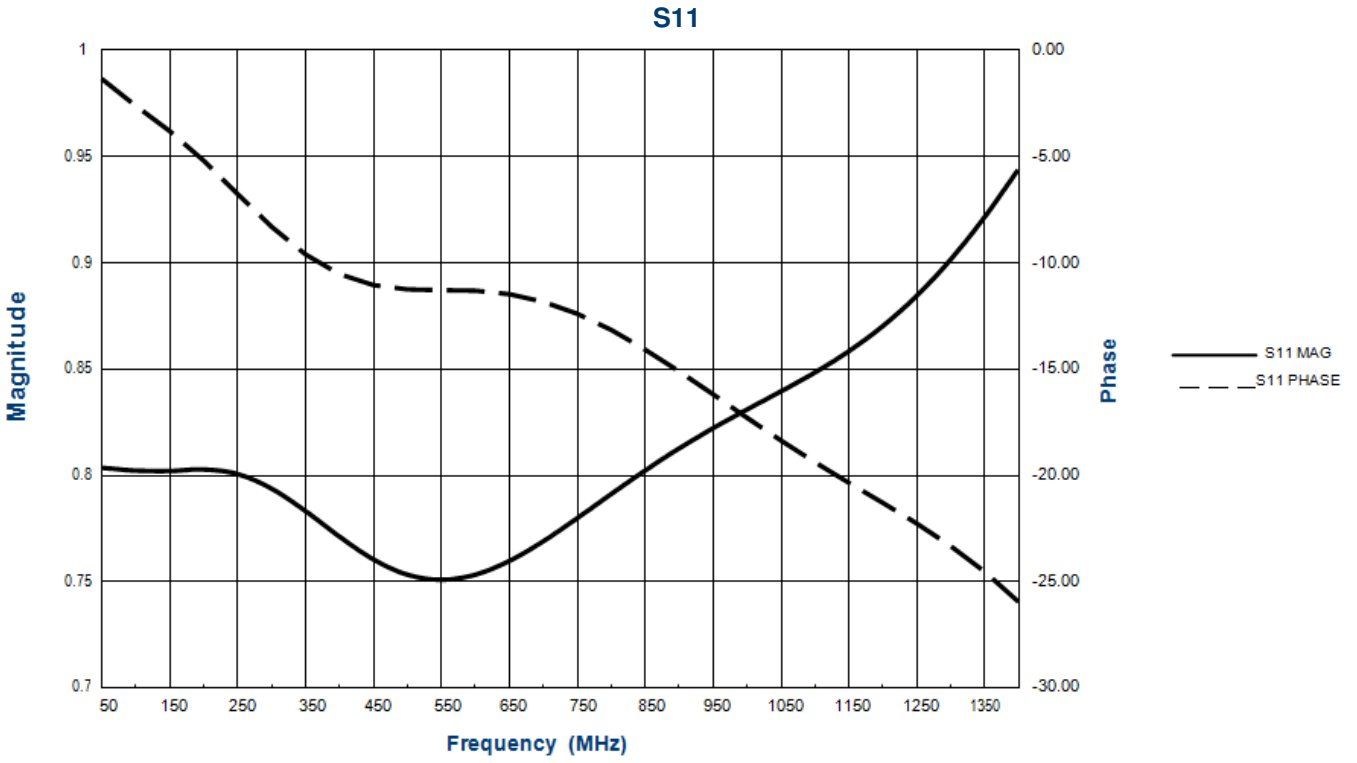
Not recommended for new designs

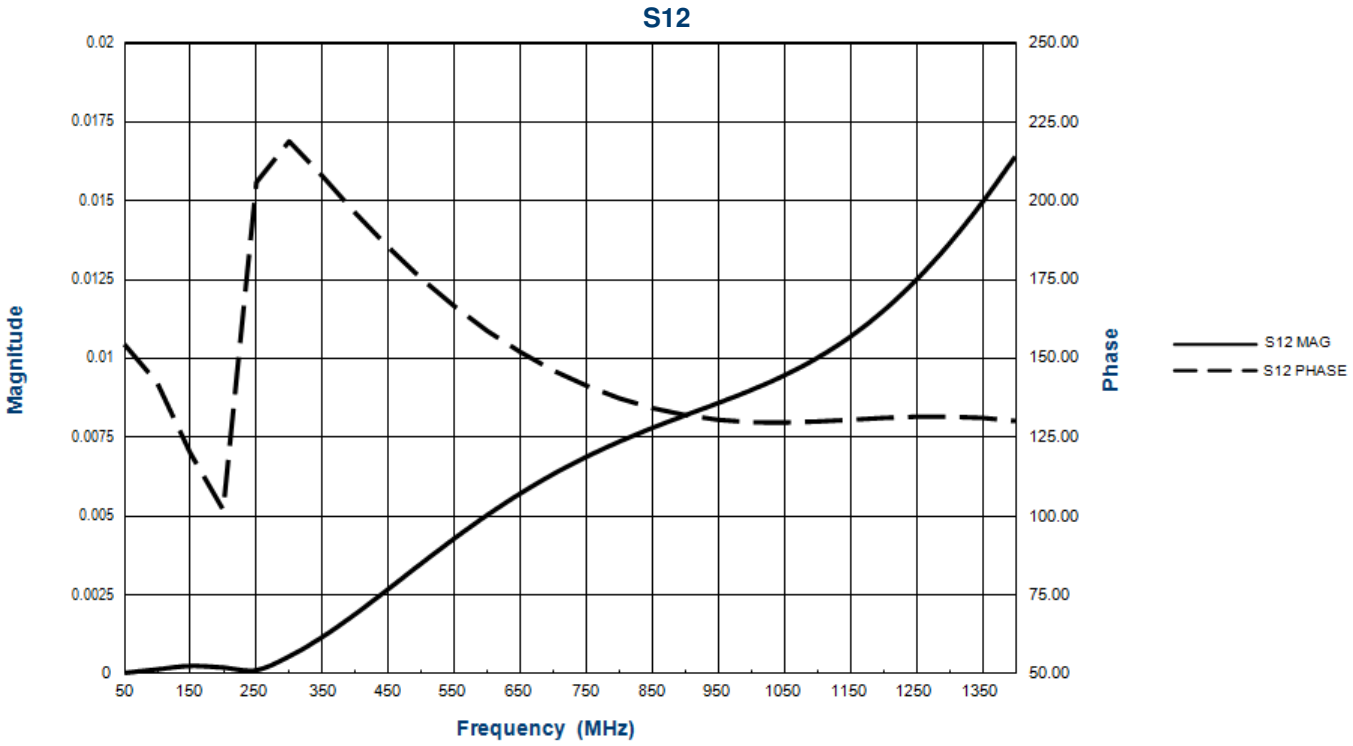
Truth Table

EN	CS-SEL	Q	Q_{HG}	$\overline{Q}_{HG}$
High/Open	Low/Open	D0/$\overline{D0}$	D0/$\overline{D0}$	D0/$\overline{D0}$
High/Open	High	D1/$\overline{D1}$	D1/$\overline{D1}$	D1/$\overline{D1}$
Low	Low/Open	D0/$\overline{D0}$	Low	High
Low	High	D1/$\overline{D1}$	Low	High

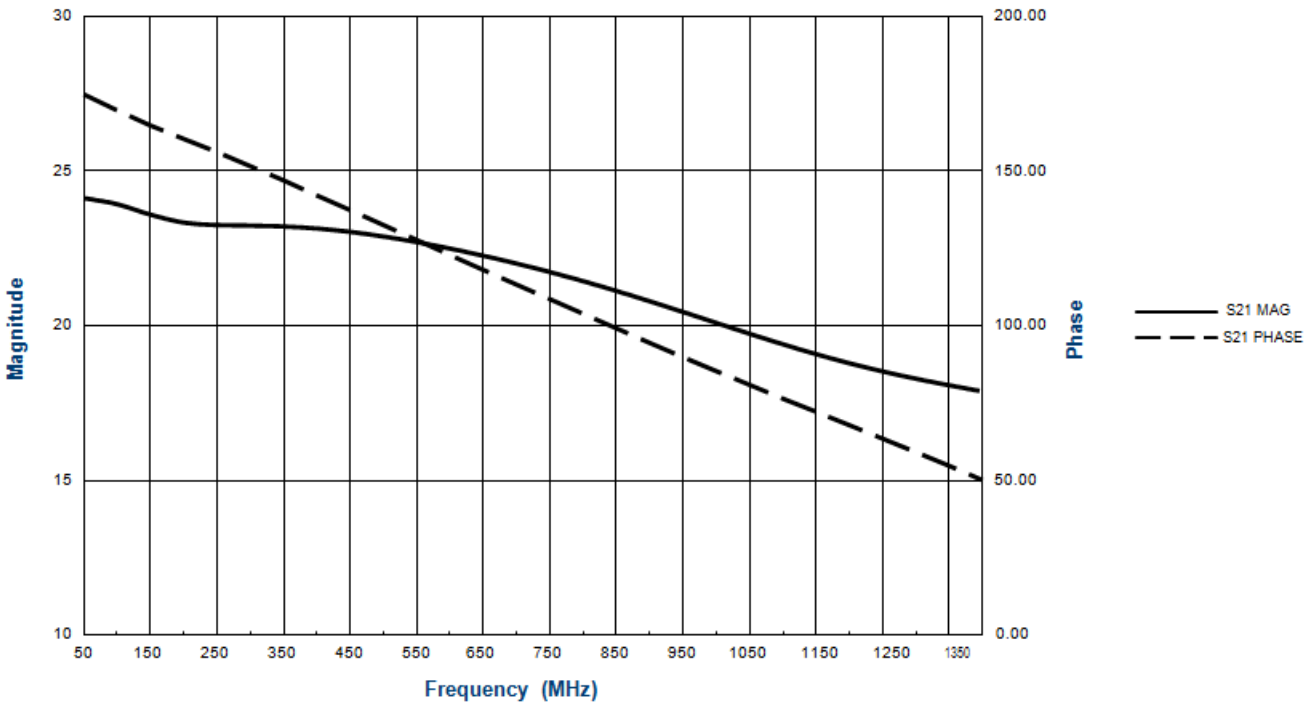
Timing Diagram



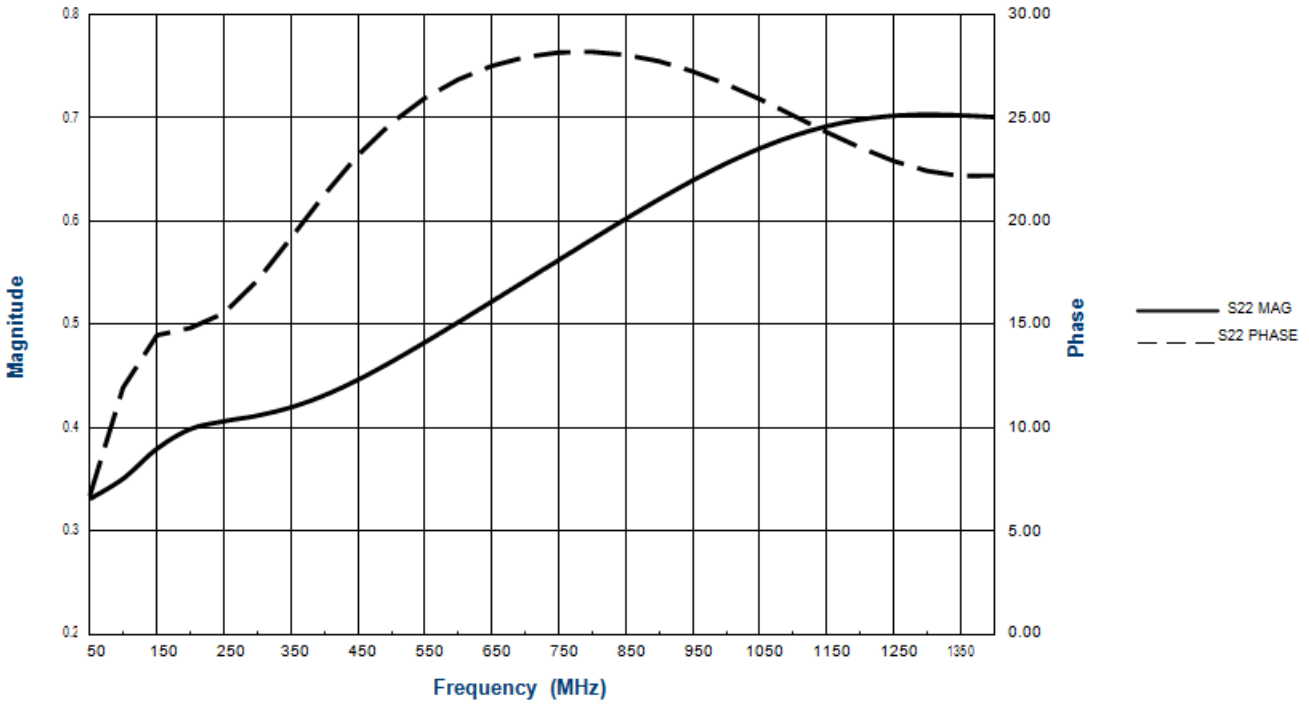

S11
Magnitude
Phase
Frequency (MHz)
1
0.95
0.9
0.85
0.8
0.75
0.7
0.00
-5.00
-10.00
-15.00
-20.00
-25.00
-30.00
50
150
250
350
450
550
650
750
850
950
1050
1150
1250
1350
S11 MAG
S11 PHASE


S12
Magnitude
Phase
Frequency (MHz)
0.02
0.0175
0.015
0.0125
0.01
0.0075
0.005
0.0025
0
250.00
225.00
200.00
175.00
150.00
125.00
100.00
75.00
50.00
50
150
250
350
450
550
650
750
850
950
1050
1150
1250
1350
S12 MAG
S12 PHASE

S21


Magnitude
30
25
20
15
10
Phase
200.00
150.00
100.00
50.00
0.00
50
150
250
350
450
550
650
750
850
950
1050
1150
1250
1350
Frequency (MHz)
S21 MAG
S21 PHASE

S22


Magnitude
0.8
0.7
0.6
0.5
0.4
0.3
0.2
Phase
30.00
25.00
20.00
15.00
10.00
5.00
0.00
50
150
250
350
450
550
650
750
850
950
1050
1150
1250
1350
Frequency (MHz)
S22 MAG
S22 PHASE

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Condition	Rating	Unit
V_{CC}	PECL Power Supply	V_{EE} = 0V	0 to + 6.0	V
V_{D_PECL}	PECL D Input	Referenced to V_{BB}	±0.75	V
V_{EN_PECL}	PECL D Input Voltage	V_{EE} = 0V	0 to + 6.0	V
V_{EE}	ECL Power	V_{CC} = 0V	-6.0 to 0	V
V_{D_ECL}	ECL D Input Voltage	Referenced to V_{BB}	±0.75	V
V_{EN_ECL}	ECL D Input Voltage	V_{CC} = 0V	-6.0 to 0	V
I_{OUT}	Output Current	Continuous Q	25	mA
		Surge Q	50	
		Continuous Q_{HG}	50	
		Surge Q_{HG}	100	
T_A	Operating Temperature Range	-	-40 to +85	°C
T_{STG}	Storage Temperature Range	-	-65 to +150	°C
ESD_{HBM}	Human Body Model Electro Static Discharge	-	2500	V
ESD_{MM}	Machine Model Electro Static Discharge	-	200	V
ESD_{CDM}	Charged Device Model Electro Static Discharge	-	2000	V

ECL DC Characteristics (V_{EE} = -3.0V to -5.5V, V_{CC} = GND)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1]	-1045	-835	-1025	-835	-1025	-835	-1025	-835	mV
V_{OL}	Output LOW Voltage[1]	-1925	-1555	-1900	-1620	-1900	-1620	-1900	-1620	mV
V_{IH}	Input HIGH Voltage D	-1165	-740	-1165	-740	-1165	-740	-1165	-740	mV
	Input HIGH Voltage EN,SEL	-1165	V_{CC}	-1165	V_{CC}	-1165	V_{CC}	-1165	V_{CC}	
V_{IL}	Input LOW Voltage D	-1900	-1475	-1900	-1475	-1900	-1475	-1900	-1475	mV
	Input LOW Voltage EN,SEL	V_{EE}	-1475	V_{EE}	-1475	V_{EE}	-1475	V_{EE}	-1475	
V_{BB}	Reference Voltage	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV
I_{IH}	Input HIGH Current EN,SEL		150		150		150		150	µA
I_{IL}	Input LOW Current EN,SEL	-100		-100		-100		-100		µA
I_{EE}	Power Supply Current[1]		47		47		47		51	mA

[1] Specified with each output terminated through 50Ω resistors to V_{CC} –2V.

LVPECL DC Characteristics (V_{EE} = GND, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	2255	2465	2275	2465	2275	2465	2275	2465	mV
V_{OL}	Output LOW Voltage[1,2]	1375	1745	1400	1680	1400	1680	1400	1680	mV
V_{IH}	Input HIGH Voltage D	2135	2560	2135	2560	2135	2560	2135	2560	mV
	Input HIGH Voltage EN,SEL	2135	V_{CC}	2135	V_{CC}	2135	V_{CC}	2135	V_{CC}	
V_{IL}	Input LOW Voltage D	1050	1825	1400	1825	1400	1825	1400	1825	mV
	Input LOW Voltage EN,SEL	V_{EE}	1825	V_{EE}	1825	V_{EE}	1825	V_{EE}	1825	
V_{BB}	Reference Voltage[1]	1910	2050	1910	2050	1910	2050	1910	2050	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	µA
I_{IL}	Input LOW[3] Current EN	-400		-400		-400		-400		µA
I_{EE}	Power Supply Current[2]		47		47		47		51	mA

1 Voltage levels vary 1:1 with V_{CC}.

2 Specified with each output terminated through 50Ω resistors to V_{CC} –-2V.

3 Specified with EN and SEL forced to V_{EE}.

PECL DC Characteristics (V_{EE} = GND, V_{CC} = +5.0V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	3955	4165	3975	4165	3975	4165	3975	4165	mV
V_{OL}	Output LOW Voltage[1,2]	3075	3445	3100	3380	3100	3380	3100	3380	mV
V_{IH}	Input HIGH Voltage D	3835	4260	3835	4260	3835	4260	3835	4260	mV
	Input HIGH Voltage EN,SEL	3835	V_{CC}	3835	V_{CC}	3835	VCC	3835	V_{CC}	
V_{IL}	Input LOW Voltage D	3100	3525	3100	3525	3100	3525	3100	3525	mV
	Input LOW Voltage EN,SEL	V_{EE}								
V_{BB}	Reference Voltage[1]	3610	3750	3610	3750	3610	3750	3610	3750	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	µA
I_{IL}	Input LOW[3] Current EN	-1000		-1000		-1000		-1000		µA
I_{EE}	Power Supply Current[2]		47		47		47		51	mA

1 Voltage levels vary 1:1 with V_{CC}.

2 Specified with each output terminated through 50Ω resistors to V_{CC} –-2V.

3 Specified with EN and SEL forced to V_{EE}.

LVPECL DC Characteristics (V_{EE} = GND, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}/t_{PHL}	Propagation Delay	2255	2465	2275	2465	2275	2465	2275	2465	mV
t_{SKEW}	D to Q/Qb	1375	1745	1400	1680	1400	1680	1400	1680	mV
V_{PP} (AC)	D to Q_{HG}/Qb_{HG}	2135	2560	2135	2560	2135	2560	2135	2560	mV
	Duty Cycle Skew1	2135	V_{CC}	2135	V_{CC}	2135	V_{CC}	2135	V_{CC}	
t_R/t_F	Input Swing2	1050	1825	1400	1825	1400	1825	1400	1825	mV
	Output Rise and Fall (20% - 80%)	V_{EE}	1825	V_{EE}	1825	V_{EE}	1825	V_{EE}	1825	

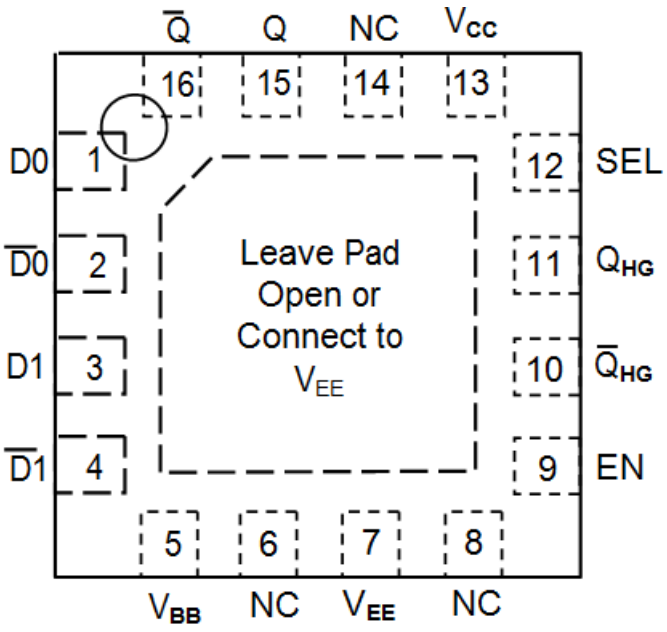
1 Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.

2 V_{PP} is the peak-to-peak differential input swing for which AC parameters are guaranteed. The device has a voltage gain of ≈20 to Q/$\overline{Q}$ outputs and a voltage gain of ≈100 to $Q_{HG}/\overline{Q}_{HG}$ outputs.

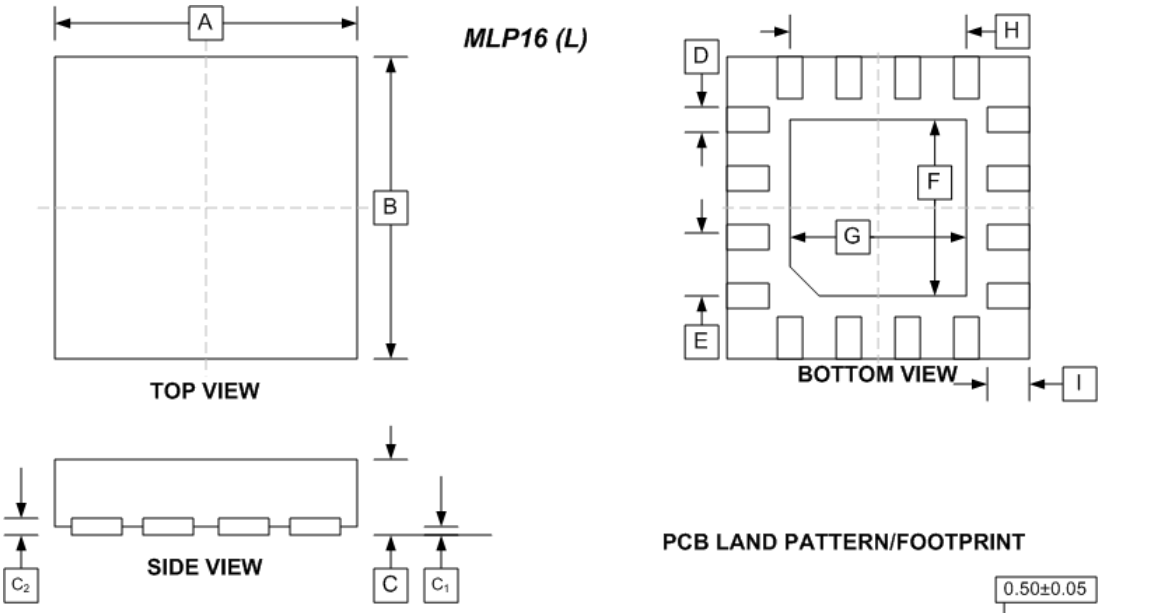
Pin Description and Configuration

Pin Assignments

Pin	Name	Type	Function
1	D0	Input	Data Input
2	$\overline{D0}$	Input	Inverting Data Input
3	D1	Input	Data Input
4	$\overline{D1}$	Input	Inverting Data Input
5	V_{BB}	Output	Reference Voltage
6	NC	-	N/A
7	V_{EE}	Power	Negative Supply
8	NC	-	N/A
9	EN	Input	Output Enable
10	$\overline{Q}_{HG}$	Output	High Gain Inverting PECL Output
11	Q_{HG}	Output	High Gain PECL Output
12	SEL	Input	Data Input Select
13	V_{CC}	Power	Positive Supply
14	NC	-	N/A
15	Q	Output	PECL Output
16	$\overline{Q}$	Output	Inverting PECL Output

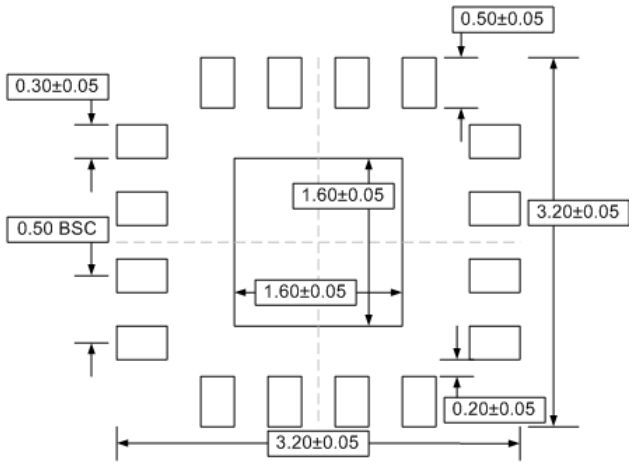


PACKAGE DIMENSIONS



	MILLIMETERS	
DIM	MIN	MAX
A	3.00±0.050	
B	3.00±0.050	
C	0.85±0.050	
C_1	0.00	0.05
C_2	0.203 REF	
D	0.23±0.050	
E	0.50 BSC	
F	1.55±0.050	
G	1.55±0.050	
H	1.500 Ref	
I	0.40±0.050	

PCB LAND PATTERN/FOOTPRINT



PART ORDERING INFORMATION

Part Number	Package	Marking
CTSLVEL16VVRLG	MLP16	CTSG 16K YYWW