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CX24109

Digital Satellite Tuner

Rev. 01 — 13 November 2008 Product data sheet

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01	20081113	First NXP version based on the Conexant 102031A data sheet.

Contact information

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For sales office addresses, please send an email to: **salesaddresses@nxp.com**

General description

The CX24109 is a highly integrated, direct down-conversion satellite tuner intended for high-volume digital video, audio, and data receivers. When combined with the CX24121 QPSK demodulator/FEC decoder, the chip set provides a complete broadband satellite front-end solution capable of operating from 1–45 MSps in the most demanding satellite environments. It is compatible with international standards such as DVB and DSS. The highly integrated CX24109 reduces the tuner BOM cost and simplifies the RF layout.

Features

- Zero-IF architecture eliminates the need for image reject filtering
- Integrated LNA
- Integrated LO with onboard VCO and synthesizer
- Single +5 V supply
- Reference oscillator output for demodulator

Applications

- DBS set-top boxes
- Commercial digital video, audio, and data receivers
- Digital VCRs

Block diagram

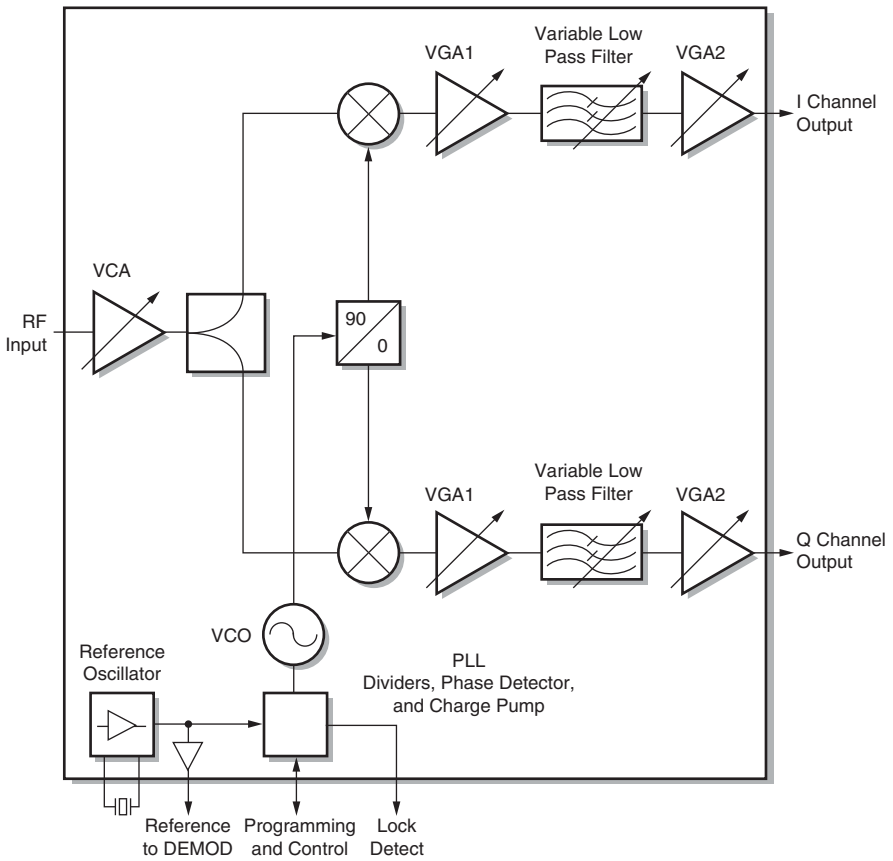

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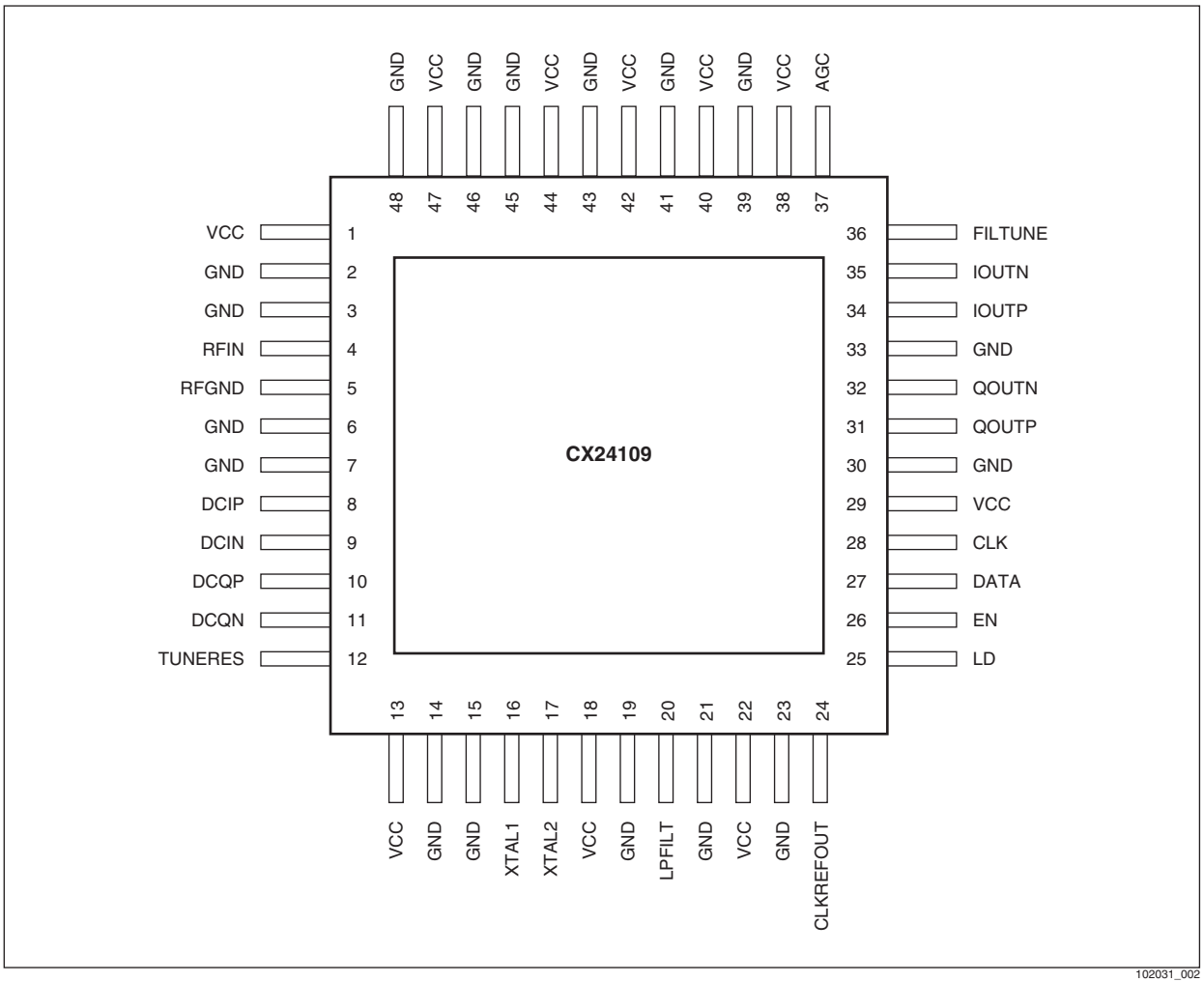
Figure 1. CX24109 Pin Diagram



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1.2 Pin Description

Table 1. Pin Description

Pin Name	Pin No.	I/O	Description
RFIN	4	I	RF input signal pin.
AGC	37	I	AGC control input from the demodulator/FEC IC. It controls the gain of the RF attenuator and both baseband amplifiers. Minimum gain occurs at minimum voltage. Input impedance zin = 1 MΩ//20 pF..
FILTUNE	36	I	Baseband filter control input from the demodulator/FEC IC. Minimum BW occurs at minimum voltage. Zin = 17 kΩ//20 pF.

Table 1. Pin Description

Pin Name	Pin No.	I/O	Description
TUNERES	12	—	Filter reference. A resistor to ground from this pin sets the reference current for the tunable filter. See Figure 6 and Figure 7.
IOUTP, IOUTN	34, 35	O	I channel output to the demodulator/FEC IC. Can be used balanced or single-ended. Zout = 1 kΩ//10 pF.
QOUTP, QOUTN	31, 32	O	Q channel output to the demodulator/FEC IC. Can be used balanced or single-ended. Zout = 1 kΩ//10 pF.
DCIP, DCIN	8, 9	—	I channel DC offset cancellation. A capacitor must be placed between these pins. See Figure 6 and Figure 7.
DCQP, DCQN	10, 11	—	Q channel DC offset cancellation. A capacitor must be placed between these pins. See Figure 6 and Figure 7.
LPFILT	20	—	Loop filter. A network with a capacitor in parallel with a series resistor and capacitor connected from this pin to ground determines the loop filter bandwidth. See Figure 6 and Figure 7.
CLKREFOUT	24	O	Clock reference output. This pin provides the reference clock for the demodulator/FEC IC. The maximum load allowed at this node is Z_{LOAD} = 10 kΩ//20 pF.
XTAL1, XTAL2	16, 17	—	Crystal inputs. A 10.111 MHz, series-resonant, fundamental crystal is placed between these two pins to create the system clock. See Figure 6 and Figure 7.
CLK	28	I	Serial bus clock signal.
EN	26	I	Serial bus latch enable.
DATA	27	I	Serial bus data pin.
LD	25	O	The lock detect signal to the demodulator/FEC IC. Z_{LOAD} = 10 kΩ//20 pF. High is the locked state.

Table 2. Power Supply and Ground Pins

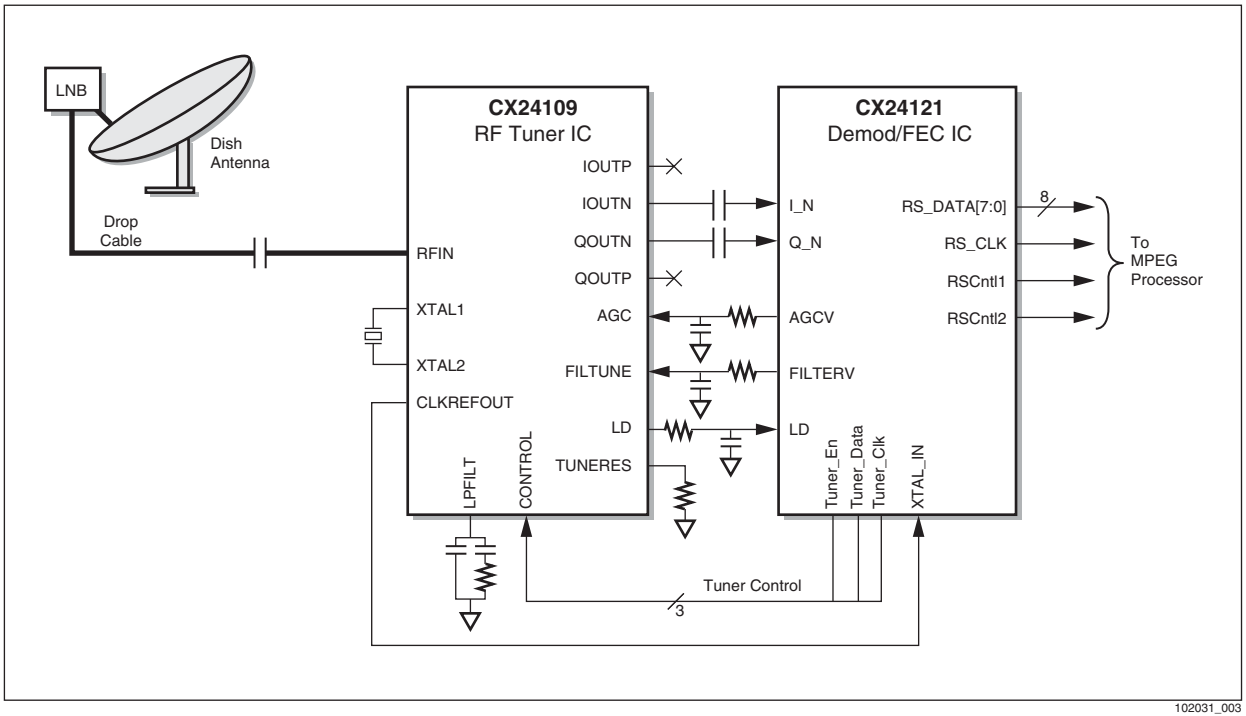
Pin Name	Pin No.	I/O	Description
VCC	1, 13, 18, 22, 29, 38, 40, 42, 44, 47	P	+5 V power supply
GND	2, 3, 5, 6, 7, 14, 15, 19, 21, 23, 30, 33, 39, 41, 43, 45, 46, 48	P	Ground

1.3 Application Overview

Several million Satellite Set-Top Boxes (STBs) are deployed in many different entertainment networks around the world today. The standards for each network may vary a little but the requirements for the tuner in the STB are essentially the same. Each receiver system in the

network requires an antenna, a Low Noise Block (LNB) downconverter, a drop cable, and an STB. The LNB converts the satellite downlink frequency to an intermediate L-band frequency where it is passed to the STB via the drop cable. The STB front end consists of a tuner and a demodulator/FEC IC. The satellite tuner must tune to the L-band frequency, downconvert the carrier, and separate it to baseband I and Q signals. The demodulator/FEC IC includes QPSK Demodulation, carrier tracking, AGC control, bit timing, and the required FEC for a given network service. Figure 2 illustrates a typical application block diagram for the CX24109/CX24121 chip set in an STB front end.

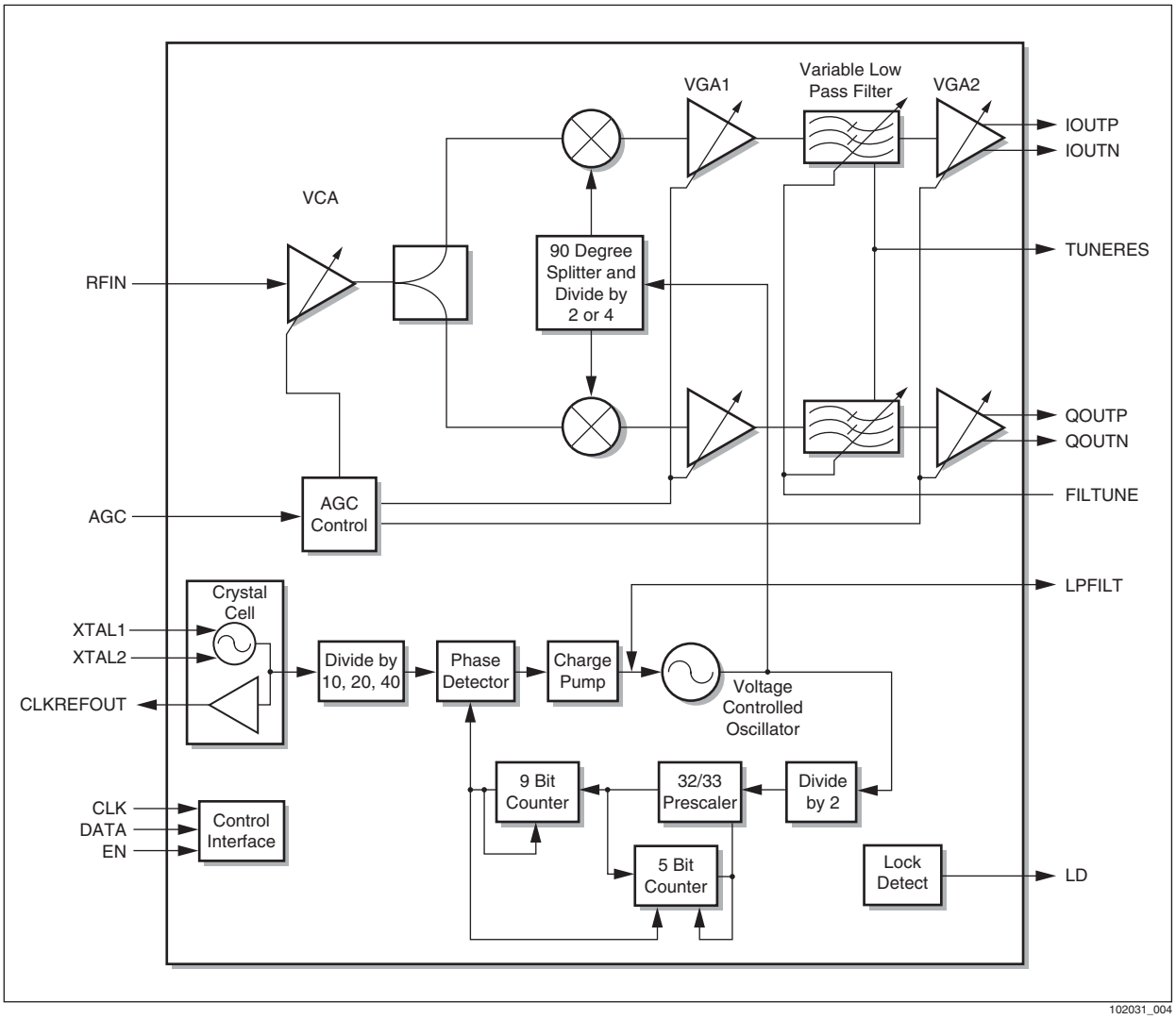
Figure 2. QPSK Demodulation Typical Application Block Diagram



1.4 Signal Path

The CX24109 is a highly integrated, direct-down conversion satellite tuner. It consists of an LNA, variable RF attenuator, quadrature downconverter, variable IF gain amplifiers, variable low-pass filters, VCO, and synthesizer. A detailed block diagram of the IC is illustrated in Figure 3.

Figure 3. Detailed Functional Block Diagram



The L-band output from the LNB enters the IC through the RFIN pin and is immediately amplified by the Voltage Controlled Attenuator block (VCA). The VCA functions as a variable gain LNA. The noise figure and gain of the VCA are the dominant factors for the tuner's noise figure. The signal is then quadrature downconverted to I and Q baseband channels. Additional amplifiers at baseband provide more variable gain for the AGC loop. Also at baseband, variable low-pass filters provide anti-alias filtering and eliminate noise power from adjacent carriers and spurious signals before they can impact the A/Ds in the demodulator IC.

1.5 AGC and Control

The AGC functionality for the CX24109 is split between the RF and baseband sections, and provides 80 dB of variable gain. The primary control for the AGC is an analog voltage from the demodulator IC. Programmable adjustments to the slope and offset of each variable gain component in the tuner are available through the AGC control registers. Programming information for the VGA and VCA is provided in Tables 4 and 5, respectively. The recommended default values for the programmable control bits versus symbol rate are listed in Table 8.

1.6 Local Oscillator

The local oscillator consists of a synthesizer and a VCO block, and is contained entirely within the CX24109. The VCO block uses an innovative architecture that requires only a 5 V source, eliminating the need for a 28 V power supply. It includes the required tank circuit.

The VCO block consists of a bank of eight oscillators operating at twice and four times the input frequency with a continuous range from 2200 MHz to 4400 MHz. The VCOs overlap to cover the frequency range from 950 MHz to 2150 MHz under all voltage, temperature, and process variations. The VCO tuning range, combined with programmable ÷2 or ÷4 frequency dividers, creates the continuous frequencies from 950 MHz to 2150 MHz for the local oscillator. A simple tuning algorithm must be run by the host processor one time at power-up to calibrate the VCO block. Conexant provides this program.

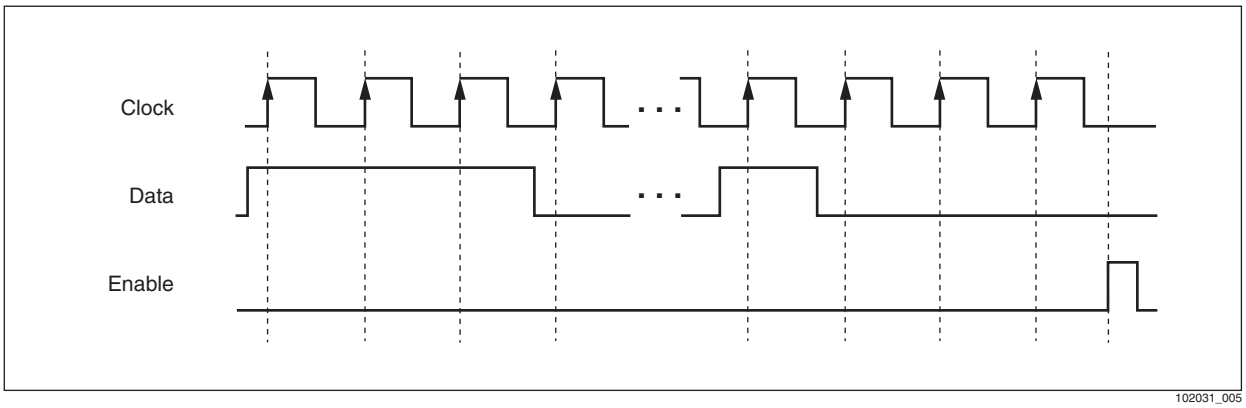
The synthesizer is also contained within the CX24109. It uses a 10.111 MHz reference frequency and a reference divider, ÷R, to set the phase comparison frequency. Two programming bits are used to configure the reference divider to divide by 10, 20, or 40, which in turn sets the comparison frequency to 1.0111 MHz, 505 kHz, or 253 kHz, respectively. A reference divider of 10 is recommended. The comparison frequency also determines the frequency step size of the local oscillator. Another programmable divider is provided for the VCO output. It consists of a 32/33 prescaler, a 9-bit N-counter (N-divider), a 5-bit A-counter (A-divider), and a fixed ÷ 2 block. The programmable divider divides the VCO output from its highest frequency to the minimum phase comparison frequency. The programmable charge pump includes output currents of 1 mA, 2 mA, 3 mA, and 4 mA. Programming information for the synthesizer can be found in Table 7**.** The recommended values for charge pump current, polarity, and referenced dividers are listed in Tables 9 and 10.

The typical loop filter bandwidth is set with external passive components and should be set between 8 kHz and 15 kHz.

1.7 Programming Interface

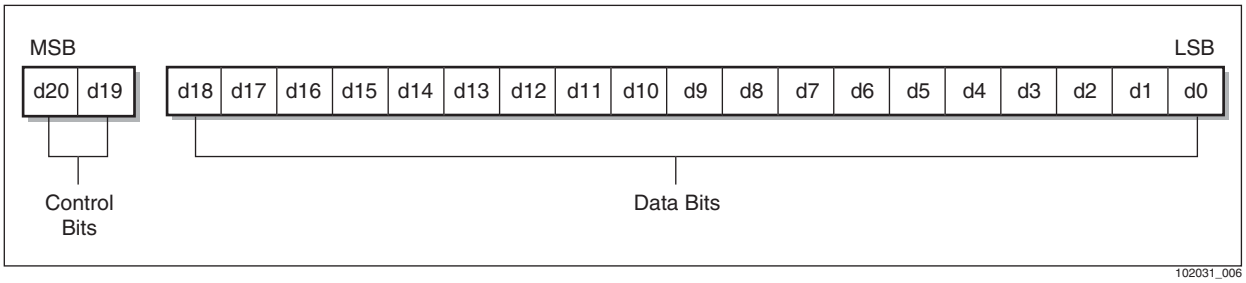
A three-wire serial interface with Clock, Data, and Enable lines is used to program the CX24109. All digital signals are CMOS-compatible. The serial data carries the binary settings for the programmable dividers, the VCO band select, the voltage-controlled attenuator, and the voltage-controlled amplifiers. When the Enable line is low, data is shifted into an internal shift register on the rising edge of the clock, and when the Enable line goes high, the stored data is latched. The clock signal should be kept low when inactive. The maximum clock rate is 1 MHz. Figure 4 illustrates the relationship between the Clock, Data, and Enable signals.

Figure 4. Serial Interface Programming Example



The internal shift register in the CX24109 is 21 bits long. When the data is latched into the IC, the two MSBs act as control bits, and the lower 19 bits are the data bits as illustrated in Figure 5. Data must be entered MSB first.

Figure 5. Programming Word Configuration



The control bits determine the functional block that is being programmed, while the data bits contain the specific control information. Table 3 provides a detail mapping of the control and data bits.

Table 3. Programming Bit Mapping (Sheet 1 of 2)

Programming Bit Mapping																				
20 MSB	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 LSB
Band Select																				
0	0	R	R	R	R	R	R	R	R(1)	R	V	R(1)	Band Select							
VGA Programming																				
0	1	R	VGA2 Offset										VGA1 Offset							
VCA Programming																				
1	0	R	VCA Offset										VCA Slope							
PLL Programming																				

Table 3. Programming Bit Mapping (Sheet 2 of 2)

Programming Bit Mapping										
1	1	÷R Divider	P	Charge Pump Current	MSB	÷ N Divider(2)	LSB	MSB	÷A Divider(2)	LSB

GENERAL NOTES:

1. R means Reserved except for ÷R which means reference divider.
   P means Charge Pump Polarity
   V means VCO Divide Select

FOOTNOTES:

(1) These Reserved locations must be set to zero. All other Reserved location values do not matter.

(2) These Divide ratios are binary coded.

Table 4. Band Select Programming

Band Select										
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Typical Receive Frequency Range (MHz)	VCO Number	VCO Divider
0	1	0	0	0	0	0	0	950–1019	7	4
1	0	0	0	0	0	0	0	1019–1075	8	4
0	0	0	0	0	0	0	1	1075–1178	1	2
0	0	0	0	0	0	1	0	1178–1296	2	2
0	0	0	0	0	1	0	0	1296–1432	3	2
0	0	0	0	1	0	0	0	1432–1576	4	2
0	0	0	1	0	0	0	0	1576–1718	5	2
0	0	1	0	0	0	0	0	1718–1856	6	2
0	1	0	0	0	0	0	0	1856–2036	7	2
1	0	0	0	0	0	0	0	2036–2150	8	2

VCO Divide Select	
Bit 9	Function
0	÷4
1	÷2

Table 5. VGA Programming

VGA1 Offset									
Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Offset in dB
1	1	1	1	1	1	1	1	0	–27.0
1	1	1	1	1	1	1	0	0	–28.5
1	1	1	1	1	1	0	0	0	–30.0
1	1	1	1	1	0	0	0	0	–31.5
1	1	1	1	0	0	0	0	0	–33.0
1	1	1	0	0	0	0	0	0	–34.5
1	1	0	0	0	0	0	0	0	–36.0
1	0	0	0	0	0	0	0	0	–37.5
0	0	0	0	0	0	0	0	0	–39.0
VGA2 Offset									
Bit 17	Bit 16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Offset in dB
1	1	1	1	1	1	1	1	0	35
1	1	1	1	1	1	1	0	0	32
1	1	1	1	1	1	0	0	0	29
1	1	1	1	1	0	0	0	0	26
1	1	1	1	0	0	0	0	0	23
1	1	1	0	0	0	0	0	0	20
1	1	0	0	0	0	0	0	0	17
1	0	0	0	0	0	0	0	0	14
0	0	0	0	0	0	0	0	0	11

Table 6. VCA Programming

VCA Slope									
Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Slope in dB/V
0	0	0	0	0	0	0	0	1	47.0
0	0	0	0	0	0	0	1	1	49.5
0	0	0	0	0	0	1	1	1	52.0
0	0	0	0	0	1	1	1	1	54.5
0	0	0	0	1	1	1	1	1	57.0
0	0	0	1	1	1	1	1	1	59.5
0	0	1	1	1	1	1	1	1	62.0
0	1	1	1	1	1	1	1	1	64.5
1	1	1	1	1	1	1	1	1	67.0
VCA Offset									
Bit 17	Bit 16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Offset in dB
0	0	0	0	0	0	0	0	1	90.00
0	0	0	0	0	0	0	1	1	94.25
0	0	0	0	0	0	1	1	1	98.50
0	0	0	0	0	1	1	1	1	102.75
0	0	0	0	1	1	1	1	1	107.00
0	0	0	1	1	1	1	1	1	111.25
0	0	1	1	1	1	1	1	1	115.50
0	1	1	1	1	1	1	1	1	119.75
1	1	1	1	1	1	1	1	1	124.00

Table 7. PLL Programming

Charge Pump Current		
Bit 15	**Bit 14**	**Current (mA)**
0	0	1
0	1	2
1	0	3
1	1	4
Charge Pump Polarity		
Bit 16		**Function**
0		Positive
1		Negative
Reference Dividers		
Bit 18	**Bit 17**	**Function**
0	0	—
0	1	Reserved
1	0	Reserved
1	1	÷10

1.7.1 Gain Equations

The RF block voltage gain (G_{RF}) is equal to the VCA gain + the mixer gain.

$$G_{RF} = V_{AGC} \times \text{VCA Slope} - \text{VCA Offset (in dB)} + 23$$

where the maximum value of G_{RF} is 23 dB, regardless of voltage

VGA1 voltage gain (G_{VGA1}) is equal to

$$G_{VGA1} = V_{AGC} \times 26 + \text{VGA1 Offset (in dB)}$$

VGA2 voltage gain (G_{VGA2}) is equal to

$$G_{VGA2} = \text{VGA2 Offset (in dB)}$$

The total baseband voltage gain ($G_{Baseband}$) is equal to

$$G_{Baseband} = G_{VGA1} + G_{Filter} + G_{VGA2}$$
$$= G_{VGA1} + 3 + G_{VGA2}$$

1.7.2 Frequency Equations

The VCO frequency is determined by

$$F_{VCO} = (F_{Crystal} \div R) \times (N + (A \div 32)) \times 32 \times 2$$
$$= (10.111 \div R) \times (N + (A \div 32)) \times 32 \times 2$$

NOTE: If A = 0, then N = N + 1

Remember, the incoming receive frequency is always lower than the VCO frequency, such that:

$$F_{Receive} = F_{VCO} \div 2 \text{ or } F_{VCO} \div 4$$

1.7.3 Recommended Default Values

Table 8. Recommended AGC Programming Values

VCA and VGA Slope and Offset vs. Symbol Rate							Condition
Symbol Rate	**VCA Slope (dB/V)**	**VCA Offset (dB)(1)**	**VGA1 Slope (dB/V)(2)**	**VGA1 Offset (dB)**	**VGA2 Slope (dB/V)(2)**	**VGA2 Offset (dB)**	**FILTUNE Voltage (V)**
1 to 5 MSps	52	98.5 (102.75)	26	–30	0	29	0.41
5 to 15 MSps	57	98.5 (107)	26	–33	0	17	0.90
15 to 45 MSps	59.5	98.5 (111.25)	26	–36	0	14	2.70

FOOTNOTES:

(1) There is an interaction between the offset and slope settings in the RF block, so the actual settings will be different from the theoretical setting. Theoretical settings are given in parentheses.

(2) These values are for reference only. They are not programmable.

Table 9. Recommended VCO Frequency vs. Charge Pump Current

VCO Frequency	Charge Pump Current
Lower 50% VCO Frequency Range	2 mA
Upper 50% of VCO Frequency Range	3 mA

Table 10. Recommended Charge Pump Polarity and Reference Divider Values

Feature	Specification
Charge Pump Polarity	Negative
Reference Divider	÷10

2.1 AGC Input

To prevent excessive current draw, a 10 kΩ resistor on the AGC pin is recommended. See Figure 6.

2.2 VCO Power Pin Ripple Requirement

Care must be taken to reduce the power supply ripple on pin 13 (VCO power supply) in order to reduce phase noise. The power supply conditioning circuitry given in Figure 6 is suitable for most circumstances.

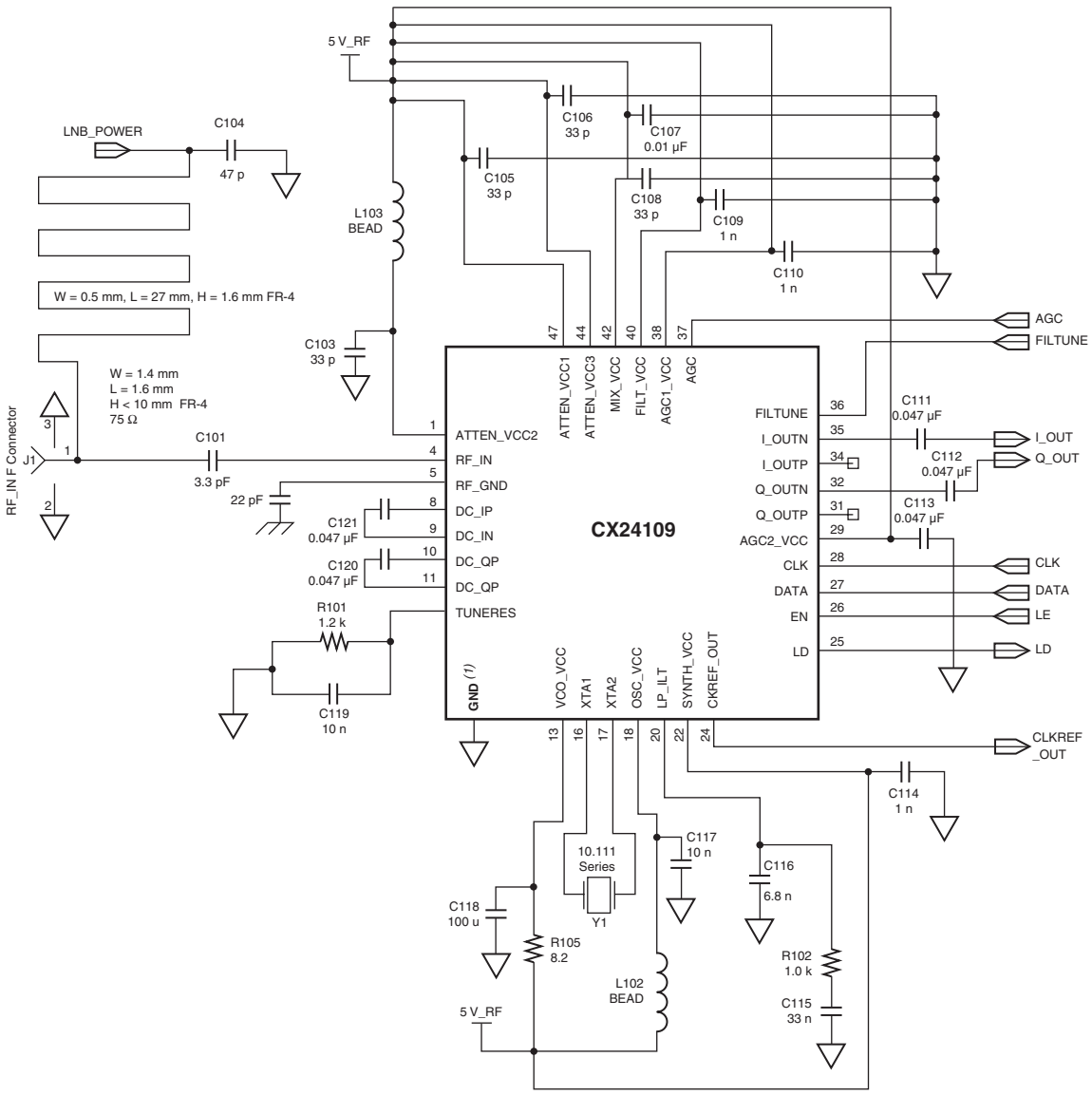
2.3 Transmission Lines

Though the CX24109's RF layout is simple, there are two transmission lines that must be designed. The first transmission line is the LNB power line, which is located at the connector. The second transmission line is between the connector and the RF IN pin. The input transmission line must have a characteristic impedance of 75 Ω**.** The schematic gives recommended dimensions assuming a two-layer FR-4 board.

2.4 Example Schematic

Figure 6 provides a simplified version of the CX24109/CX24121 reference design. For complete and current reference design information, contact your local Conexant sales office.

Figure 6. Simplified Application Schematic (Page 1 of 2)



FOOTNOTE:

(1) Ground pins include: 2, 3, 5, 6, 7, 14, 15, 19, 21, 23, 30, 33, 39, 41, 43, 45, 46, and 48

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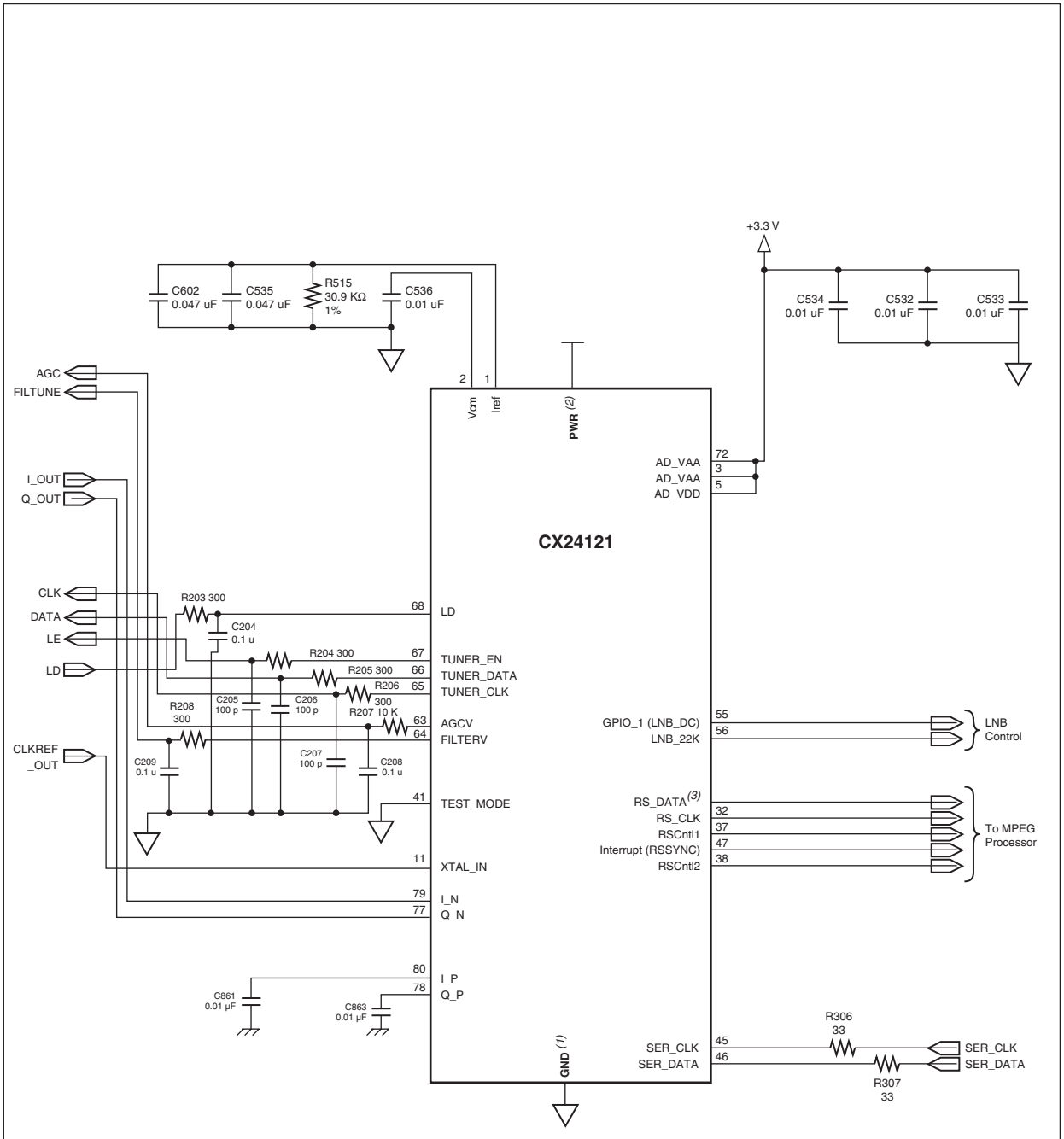
Figure 7. Simplified Application Schematic (Page 2 of 2)



FOOTNOTE:

(1) Ground Pins include: 4, 6, 8, 10, 15, 26, 30, 34, 50, 52, 62, 70, and 71.

(2) Core (1.8 V) power pins include: 7, 9, 14, 29, 49, and 69.
3.3 V power pins include: 25, 33, 51, and 61.

(3) RS_DATA includes RS_DATA0–RS_DATA7 pins 35, 31, 28, 27, 24, 23, 22, and 21.

102031_008