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## Features

- 20 ns, 25 ns, and 45 ns access times
- Internally organized as 128 K × 8 (CY14B101LA) or 64 K × 16 (CY14B101NA)
- Hands off automatic STORE on power-down with only a small capacitor
- STORE to QuantumTrap nonvolatile elements initiated by software, device pin, or AutoStore on power-down
- RECALL to SRAM initiated by software or power-up
- Infinite read, write, and RECALL cycles
- 1 million STORE cycles to QuantumTrap
- 20 year data retention
- Single 3 V +20% to -10% operation
- Industrial temperature

## ■ Packages

- 32-pin small-outline integrated circuit (SOIC)
- 44-/54-pin thin small outline package (TSOP) Type II
- 48-pin shrink small-outline package (SSOP)
- 48-ball fine-pitch ball grid array (FBGA)

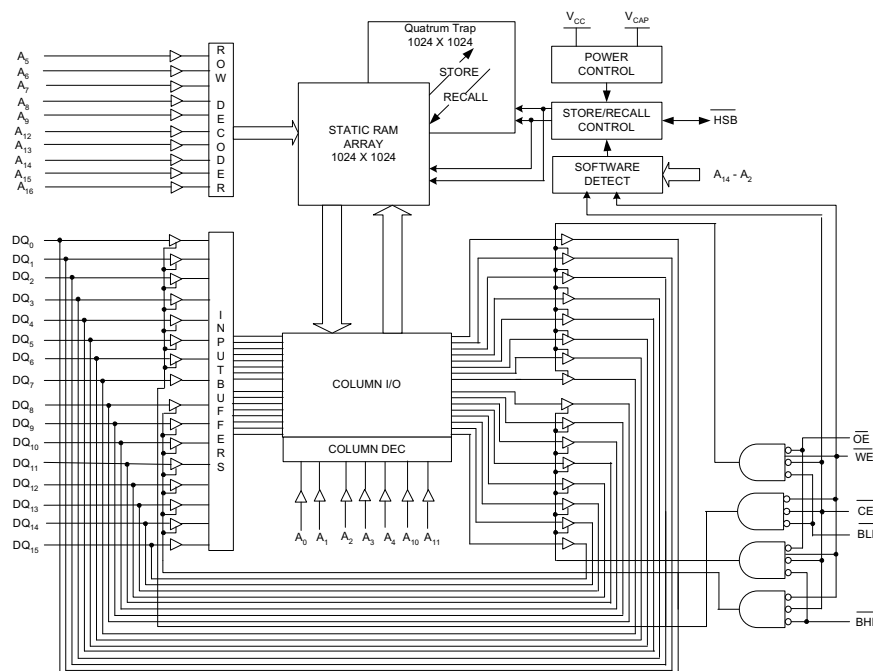
- Pb-free and restriction of hazardous substances (RoHS) compliant

## Functional Description

The Cypress CY14B101LA/CY14B101NA is a fast static RAM (SRAM), with a nonvolatile element in each memory cell. The memory is organized as 128 K bytes of 8 bits each or 64 K words of 16 bits each. The embedded nonvolatile elements incorporate QuantumTrap technology, producing the world's most reliable nonvolatile memory. The SRAM provides infinite read and write cycles, while independent nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power-down. On power-up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control.

For a complete list of related resources, click [here](#).

## Logic Block Diagram [1, 2, 3]



### Notes

1. Address A<sub>0</sub>-A<sub>16</sub> for × 8 configuration and Address A<sub>0</sub>-A<sub>15</sub> for × 16 configuration.
2. Data DQ<sub>0</sub>-DQ<sub>7</sub> for × 8 configuration and Data DQ<sub>0</sub>-DQ<sub>15</sub> for × 16 configuration.
3. BHE and BLE are applicable for × 16 configuration only.

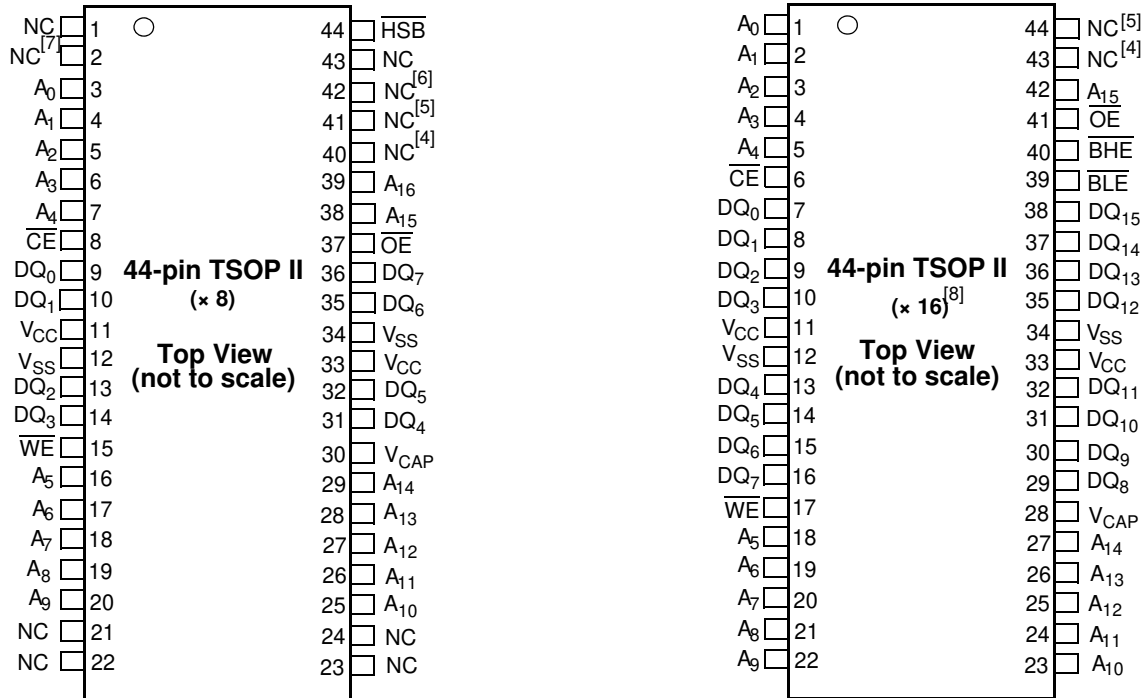
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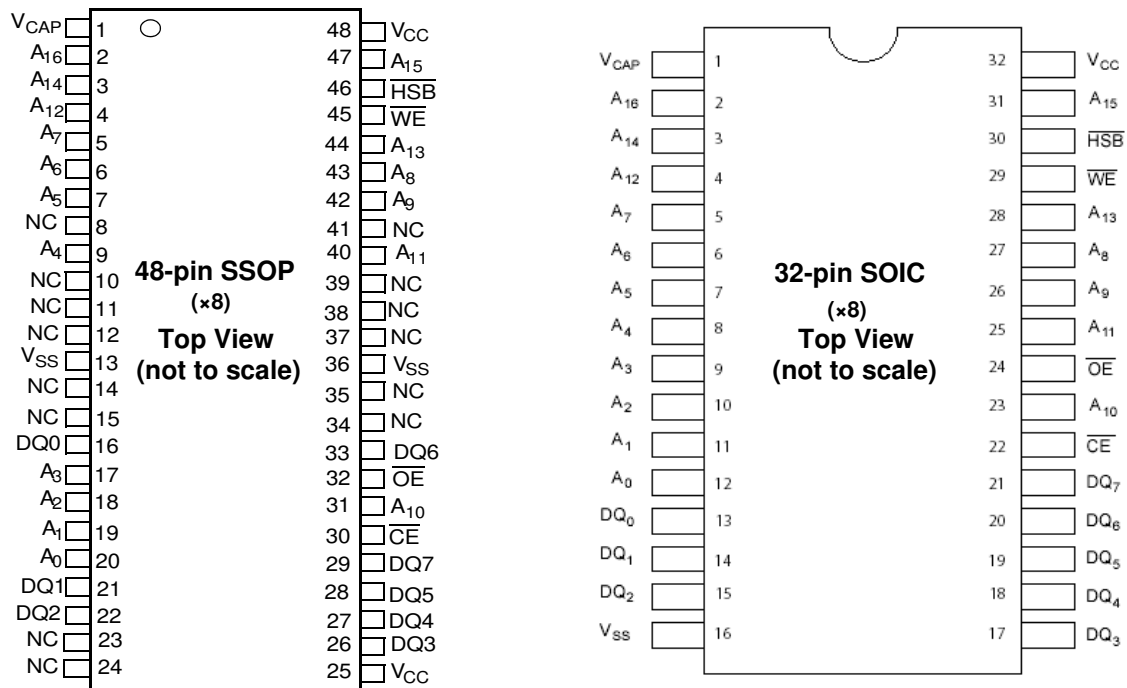


**Pinouts**

**Figure 1. Pin Diagram – 44-pin TSOP II**



**Figure 2. Pin Diagram – 48-pin SSOP and 32-pin SOIC**

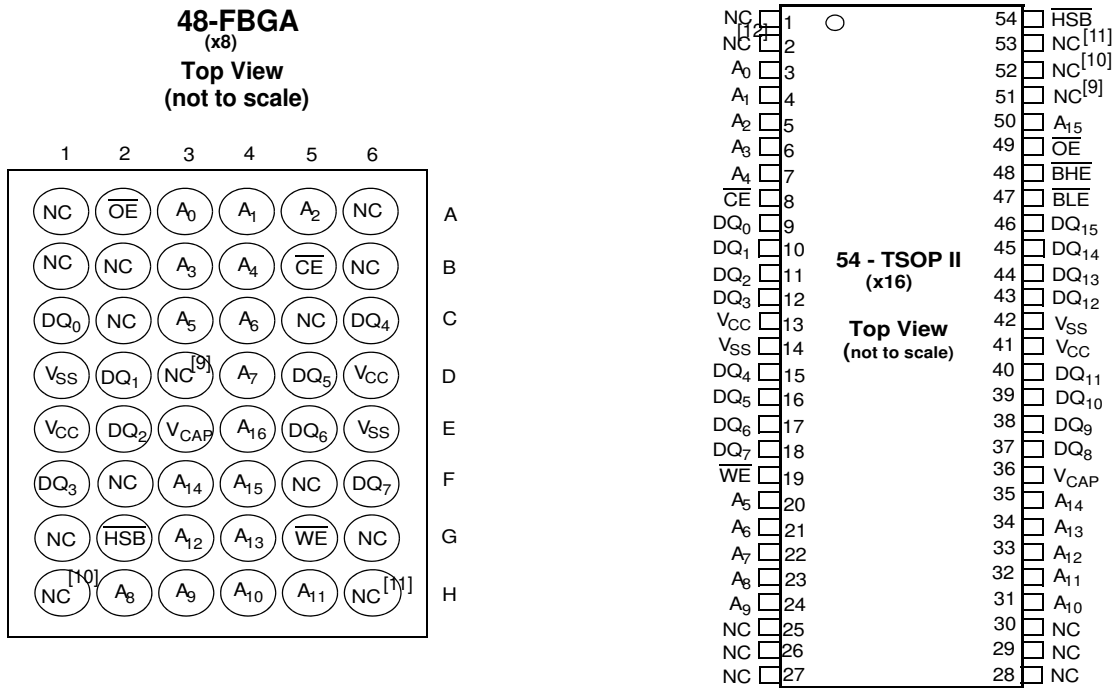


**Notes**

4. Address expansion for 2-Mbit. NC pin not connected to die.
5. Address expansion for 4-Mbit. NC pin not connected to die.
6. Address expansion for 8-Mbit. NC pin not connected to die.
7. Address expansion for 16-Mbit. NC pin not connected to die.
8. HSB pin is not available in 44-pin TSOP II (x 16) package.

**Pinouts** (continued)

**Figure 3. 48-ball FBGA and 54-pin TSOP II pinout**



**Notes**

- 9. Address expansion for 2-Mbit. NC pin not connected to die.
- 10. Address expansion for 4-Mbit. NC pin not connected to die.
- 11. Address expansion for 8-Mbit. NC pin not connected to die.
- 12. Address expansion for 16-Mbit. NC pin not connected to die.

## Pin Definitions

Pin Name	I/O Type	Description
A <sub>0</sub> -A <sub>16</sub>	Input	Address inputs. Used to select one of the 131,072 bytes of the nvSRAM for × 8 configuration.
A <sub>0</sub> -A <sub>15</sub>		Address inputs. Used to select one of the 65,536 words of the nvSRAM for × 16 configuration.
DQ <sub>0</sub> -DQ <sub>7</sub>	Input/Output	Bidirectional data I/O lines for × 8 configuration. Used as input or output lines depending on operation.
DQ <sub>0</sub> -DQ <sub>15</sub>		Bidirectional Data I/O Lines for × 16 configuration. Used as input or output lines depending on operation.
$\overline{WE}$	Input	Write Enable input, Active LOW. When the chip is enabled and $\overline{WE}$ is LOW, data on the I/O pins is written to the specific address location.
$\overline{CE}$	Input	Chip Enable input, Active LOW. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{OE}$	Input	Output Enable, Active LOW. The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. I/O pins are tristated on deasserting $\overline{OE}$ HIGH.
$\overline{BHE}$	Input	Byte High Enable, Active LOW. Controls DQ <sub>15</sub> -DQ <sub>8</sub> .
$\overline{BLE}$	Input	Byte Low Enable, Active LOW. Controls DQ <sub>7</sub> -DQ <sub>0</sub> .
V <sub>SS</sub>	Ground	Ground for the device. Must be connected to the ground of the system.
V <sub>CC</sub>	Power supply	Power supply inputs to the device. 3.0 V +20%, -10%
$\overline{HSB}^{[13]}$	Input/Output	Hardware STORE Busy ( $\overline{HSB}$ ). When LOW, this output indicates that a Hardware STORE is in progress. When pulled LOW, external to the chip, it initiates a nonvolatile STORE operation. After each Hardware and Software STORE operation $\overline{HSB}$ is driven HIGH for a short time (t <sub>HHD</sub> ) with standard output high current and then a weak internal pull-up resistor keeps this pin HIGH (external pull-up resistor connection optional).
V <sub>CAP</sub>	Power supply	AutoStore capacitor. Supplies power to the nvSRAM during power loss to store data from SRAM to nonvolatile elements.
NC	No connect	No connect. This pin is not connected to the die.

**Note**

13. HSB pin is not available in 44-pin TSOP II (× 16) package.

## Device Operation

The CY14B101LA/CY14B101NA nvSRAM is made up of two functional components paired in the same physical cell. They are an SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation), or from the nonvolatile cell to the SRAM (the RECALL operation). Using this unique architecture, all cells are stored and recalled in parallel. During the STORE and RECALL operations, SRAM read and write operations are inhibited. The CY14B101LA/CY14B101NA supports infinite reads and writes similar to a typical SRAM. In addition, it provides infinite RECALL operations from the nonvolatile cells and up to 1 million STORE operations. See the [Truth Table For SRAM Operations on page 18](#) for a complete description of read and write modes.

### SRAM Read

The CY14B101LA/CY14B101NA performs a read cycle when  $\overline{CE}$  and  $\overline{OE}$  are LOW and  $\overline{WE}$  and HSB are HIGH. The address specified on pins  $A_{0-16}$  or  $A_{0-15}$  determines which of the 131,072 data bytes or 65,536 words of 16 bits each are accessed. Byte enables (BHE, BLE) determine which bytes are enabled to the output, in the case of 16-bit words. When the read is initiated by an address transition, the outputs are valid after a delay of  $t_{AA}$  (read cycle 1). If the read is initiated by  $\overline{CE}$  or  $\overline{OE}$ , the outputs are valid at  $t_{ACE}$  or at  $t_{DOE}$ , whichever is later (read cycle 2). The data output repeatedly responds to address changes within the  $t_{AA}$  access time without the need for transitions on any control input pins. This remains valid until another address change or until  $\overline{CE}$  or  $\overline{OE}$  is brought HIGH, or  $\overline{WE}$  or HSB is brought LOW.

### SRAM Write

A write cycle is performed when  $\overline{CE}$  and  $\overline{WE}$  are LOW and HSB is HIGH. The address inputs must be stable before entering the write cycle and must remain stable until  $\overline{CE}$  or  $\overline{WE}$  goes HIGH at the end of the cycle. The data on the common I/O pins  $DQ_{0-15}$  are written into the memory if the data is valid  $t_{SD}$  before the end of a  $\overline{WE}$ -controlled write or before the end of a  $\overline{CE}$ -controlled write. The Byte Enable inputs (BHE, BLE) determine which bytes are written, in the case of 16-bit words. Keep  $\overline{OE}$  HIGH during the entire write cycle to avoid data bus contention on common I/O lines. If  $\overline{OE}$  is left LOW, internal circuitry turns off the output buffers  $t_{HZWE}$  after  $\overline{WE}$  goes LOW.

### AutoStore Operation

The CY14B101LA/CY14B101NA stores data to the nvSRAM using one of the following three storage operations: Hardware STORE activated by HSB; Software STORE activated by an address sequence; AutoStore on device power-down. The AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14B101LA/CY14B101NA.

During a normal operation, the device draws current from  $V_{CC}$  to charge a capacitor connected to the  $V_{CAP}$  pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the  $V_{CC}$  pin drops below  $V_{SWITCH}$ , the part automatically disconnects the  $V_{CAP}$  pin from  $V_{CC}$ . A STORE operation is initiated with power provided by the  $V_{CAP}$  capacitor.

#### Note

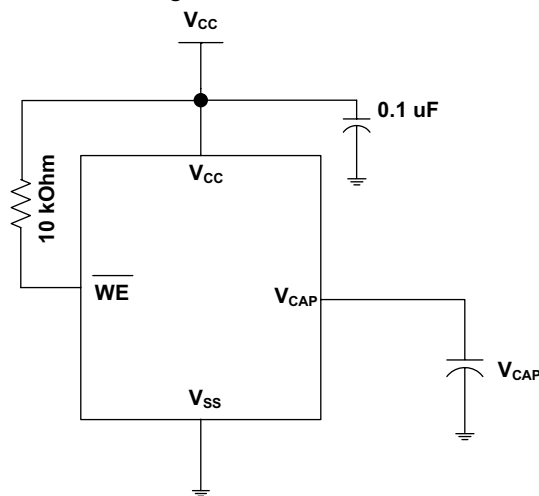
14. HSB pin is not available in 44-pin TSOP II ( $\times 16$ ) package.

**Note** If the capacitor is not connected to  $V_{CAP}$  pin, AutoStore must be disabled using the soft sequence specified in [Preventing AutoStore on page 8](#). In case AutoStore is enabled without a capacitor on  $V_{CAP}$  pin, the device attempts an AutoStore operation without sufficient charge to complete the store. This corrupts the data stored in nvSRAM.

Figure 4 shows the proper connection of the storage capacitor ( $V_{CAP}$ ) for automatic STORE operation. See the [DC Electrical Characteristics on page 9](#) for the size of  $V_{CAP}$ . The voltage on the  $V_{CAP}$  pin is driven to  $V_{CC}$  by a regulator on the chip. A pull-up should be placed on  $\overline{WE}$  to hold it inactive during power-up. This pull-up is effective only if the  $\overline{WE}$  signal is tristate during power-up. Many MPUs tristate their controls on power-up. This should be verified when using the pull-up. When the nvSRAM comes out of power-on-RECALL, the MPU must be active or the  $\overline{WE}$  held inactive until the MPU comes out of reset.

To reduce unnecessary nonvolatile stores, AutoStore and Hardware STORE operations are ignored unless at least one write operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a write operation has taken place. The HSB signal is monitored by the system to detect if an AutoStore cycle is in progress.

Figure 4. AutoStore Mode



### Hardware STORE Operation

The CY14B101LA/CY14B101NA provides the  $\overline{HSB}^{14}$  pin to control and acknowledge the STORE operations. Use the HSB pin to request a Hardware STORE cycle. When the HSB pin is driven LOW, the CY14B101LA/CY14B101NA conditionally initiates a STORE operation after  $t_{DELAY}$ . An actual STORE cycle only begins if a write to the SRAM has taken place since the last STORE or RECALL cycle. The HSB pin also acts as an open drain driver (internal 100 k $\Omega$  weak pull-up resistor) that is internally driven LOW to indicate a busy condition when the STORE (initiated by any means) is in progress.

**Note** After each Hardware and Software STORE operation  $\overline{HSB}$  is driven HIGH for a short time ( $t_{HHHD}$ ) with standard output high current and then remains HIGH by internal 100 k $\Omega$  pull-up resistor.

SRAM write operations that are in progress when  $\overline{\text{HSB}}$  is driven LOW by any means are given time ( $t_{\text{DELAY}}$ ) to complete before the STORE operation is initiated. However, any SRAM write cycles requested after  $\overline{\text{HSB}}$  goes LOW are inhibited until  $\overline{\text{HSB}}$  returns HIGH. In case the write latch is not set,  $\overline{\text{HSB}}$  is not driven LOW by the CY14B101LA/CY14B101NA. But any SRAM read and write cycles are inhibited until  $\overline{\text{HSB}}$  is returned HIGH by MPU or other external source.

During any STORE operation, regardless of how it is initiated, the CY14B101LA/CY14B101NA continues to drive the  $\overline{\text{HSB}}$  pin LOW, releasing it only when the STORE is complete. Upon completion of the STORE operation, the nvSRAM memory access is inhibited for  $t_{\text{LZHSB}}$  time after  $\overline{\text{HSB}}$  pin returns HIGH. Leave the  $\overline{\text{HSB}}$  unconnected if it is not used.

### Hardware RECALL (Power-up)

During power-up or after any low power condition ( $V_{\text{CC}} < V_{\text{SWITCH}}$ ), an internal RECALL request is latched. When  $V_{\text{CC}}$  again exceeds the  $V_{\text{SWITCH}}$  on power up, a RECALL cycle is automatically initiated and takes  $t_{\text{HRECALL}}$  to complete. During this time, the  $\overline{\text{HSB}}$  pin is driven LOW by the  $\overline{\text{HSB}}$  driver and all reads and writes to nvSRAM are inhibited.

### Software STORE

Data is transferred from the SRAM to the nonvolatile memory by a software address sequence. The CY14B101LA/CY14B101NA Software STORE cycle is initiated by executing sequential  $\overline{\text{CE}}$  or  $\overline{\text{OE}}$  controlled read cycles from six specific address locations in exact order. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. After a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other read or write accesses intervene in the sequence, or the sequence is aborted and no STORE or RECALL takes place.

To initiate the Software STORE cycle, the following read sequence must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x8FC0 Initiate STORE cycle

The software sequence may be clocked with  $\overline{\text{CE}}$  controlled reads or  $\overline{\text{OE}}$  controlled reads, with  $\overline{\text{WE}}$  kept HIGH for all the six READ sequences. After the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled.  $\overline{\text{HSB}}$  is driven LOW. After the  $t_{\text{STORE}}$  cycle time is fulfilled, the SRAM is activated again for the read and write operation.

### Software RECALL

Data is transferred from the nonvolatile memory to the SRAM by a software address sequence. A Software RECALL cycle is initiated with a sequence of read operations in a manner similar to the Software STORE initiation. To initiate the RECALL cycle, the following sequence of  $\overline{\text{CE}}$  or  $\overline{\text{OE}}$  controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x4C63 Initiate RECALL cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared. Next, the nonvolatile information is transferred into the SRAM cells. After the  $t_{\text{RECALL}}$  cycle time, the SRAM is again ready for read and write operations. The RECALL operation does not alter the data in the nonvolatile elements.

**Table 1. Mode Selection**

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}, \overline{\text{BLE}}^{[15]}$	$\text{A}_{15}\text{-A}_0^{[16]}$	Mode	I/O	Power
H	X	X	X	X	Not selected	Output high Z	Standby
L	H	L	L	X	Read SRAM	Output data	Active
L	L	X	L	X	Write SRAM	Input data	Active
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8B45	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Disable	Output data Output data Output data Output data Output data Output data	Active <sup>[17]</sup>

**Notes**

15.  $\overline{\text{BHE}}$  and  $\overline{\text{BLE}}$  are applicable for x16 configuration only.

16. While there are 17 address lines on the CY14B101LA (16 address lines on the CY14B101NA), only the 13 address lines ( $\text{A}_{14} - \text{A}_2$ ) are used to control software modes. Rest of the address lines are do not care.

17. The six consecutive address locations must be in the order listed.  $\overline{\text{WE}}$  must be HIGH during all six cycles to enable a nonvolatile cycle.



**Table 1. Mode Selection** (continued)

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}, \overline{BLE}^{[15]}$	$A_{15}-A_0^{[16]}$	Mode	I/O	Power
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4B46	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Enable	Output data Output data Output data Output data Output data Output data	Active <sup>[18]</sup>
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile STORE	Output data Output data Output data Output data Output data Output high Z	Active $I_{CC2}^{[18]}$
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile RECALL	Output data Output data Output data Output data Output data Output high Z	Active <sup>[18]</sup>

**Preventing AutoStore**

The AutoStore function is disabled by initiating an AutoStore disable sequence. A sequence of read operations is performed in a manner similar to the Software STORE initiation. To initiate the AutoStore disable sequence, the following sequence of CE or OE controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x8B45 AutoStore Disable

The AutoStore is reenabled by initiating an AutoStore enable sequence. A sequence of read operations is performed in a manner similar to the Software RECALL initiation. To initiate the AutoStore enable sequence, the following sequence of CE or OE controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x4B46 AutoStore Enable

If the AutoStore function is disabled or reenabled, a manual STORE operation (Hardware or Software) must be issued to save the AutoStore state through subsequent power-down cycles. The part comes from the factory with AutoStore enabled and 0x00 written in all cells.

**Data Protection**

The CY14B101LA/CY14B101NA protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and write operations. The low voltage condition is detected when  $V_{CC}$  is less than  $V_{SWITCH}$ . If the CY14B101LA/CY14B101NA is in a write mode (both CE and WE are LOW) at power-up, after a RECALL or STORE, the write is inhibited until the SRAM is enabled after  $t_{LZHSB}$  (HSB to output active). This protects against inadvertent writes during power-up or brown out conditions.

**Note**

18. The six consecutive address locations must be in the order listed.  $\overline{WE}$  must be HIGH during all six cycles to enable a nonvolatile cycle.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature .....	-65 °C to +150 °C
Maximum accumulated storage time:	
At 150 °C ambient temperature .....	1000 h
At 85 °C ambient temperature .....	20 Years
Maximum junction temperature .....	150 °C
Supply voltage on V <sub>CC</sub> relative to V <sub>SS</sub> .....	-0.5 V to 4.1 V
Voltage applied to outputs in High Z state .....	-0.5 V to V <sub>CC</sub> + 0.5 V
Input voltage .....	-0.5 V to V <sub>CC</sub> + 0.5 V
Transient voltage (< 20 ns) on any pin to ground potential .....	-2.0 V to V <sub>CC</sub> + 2.0 V

Package power dissipation capability (T <sub>A</sub> = 25 °C) .....	1.0 W
Surface mount Pb soldering temperature (3 Seconds) .....	+260 °C
DC output current (1 output at a time, 1s duration) ....	15 mA
Static discharge voltage (per MIL-STD-883, Method 3015) .....	> 2001 V
Latch up current .....	> 200 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40 °C to +85 °C	2.7 V to 3.6 V

## DC Electrical Characteristics

Over the [Operating Range](#)

Parameter	Description	Test Conditions	Min	Typ <sup>[19]</sup>	Max	Unit
V <sub>CC</sub>	Power supply voltage		2.7	3.0	3.6	V
I <sub>CC1</sub>	Average V <sub>CC</sub> current	t <sub>RC</sub> = 20 ns t <sub>RC</sub> = 25 ns t <sub>RC</sub> = 45 ns Values obtained without output loads (I <sub>OUT</sub> = 0 mA)	-	-	70 70 52	mA mA mA
I <sub>CC2</sub>	Average V <sub>CC</sub> current during STORE	All inputs don't care, V <sub>CC</sub> = Max Average current for duration t <sub>STORE</sub>	-	-	10	mA
I <sub>CC3</sub>	Average V <sub>CC</sub> current at t <sub>RC</sub> = 200 ns, V <sub>CC(Typ)</sub> , 25 °C	All inputs cycling at CMOS levels. Values obtained without output loads (I <sub>OUT</sub> = 0 mA)	-	35	-	mA
I <sub>CC4</sub>	Average V <sub>CAP</sub> current during AutoStore cycle	All inputs don't care. Average current for duration t <sub>STORE</sub>	-	-	5	mA
I <sub>SB</sub>	V <sub>CC</sub> standby current	CE ≥ (V <sub>CC</sub> - 0.2 V). V <sub>IN</sub> ≤ 0.2 V or ≥ (V <sub>CC</sub> - 0.2 V). Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz	-	-	5	mA
I <sub>IX</sub> <sup>[20]</sup>	Input leakage current (except HSB)	V <sub>CC</sub> = Max, V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1	-	+1	μA
	Input leakage current (for HSB)	V <sub>CC</sub> = Max, V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-100	-	+1	μA
I <sub>OZ</sub>	Off-state output leakage current	V <sub>CC</sub> = Max, V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , CE or OE ≥ V <sub>IH</sub> or BHE/BLE ≥ V <sub>IH</sub> or WE ≤ V <sub>IL</sub>	-1	-	+1	μA
V <sub>IH</sub>	Input HIGH voltage		2.0	-	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input LOW voltage		V <sub>SS</sub> - 0.5	-	0.8	V
V <sub>OH</sub>	Output HIGH voltage	I <sub>OUT</sub> = -2 mA	2.4	-	-	V
V <sub>OL</sub>	Output LOW voltage	I <sub>OUT</sub> = 4 mA	-	-	0.4	V

### Notes

19. Typical values are at 25 °C, V<sub>CC</sub> = V<sub>CC(Typ)</sub>. Not 100% tested.

20. The HSB pin has I<sub>OUT</sub> = -2 μA for V<sub>OH</sub> of 2.4 V when both active high and low drivers are disabled. When they are enabled standard V<sub>OH</sub> and V<sub>OL</sub> are valid. This parameter is characterized but not tested.

## DC Electrical Characteristics (continued)

Over the [Operating Range](#)

Parameter	Description	Test Conditions	Min	Typ <sup>[19]</sup>	Max	Unit
V <sub>CAP</sub> <sup>[21]</sup>	Storage capacitor	Between V <sub>CAP</sub> pin and V <sub>SS</sub>	61	68	180	μF
V <sub>V<sub>CAP</sub></sub> <sup>[22, 23]</sup>	Maximum voltage driven on V <sub>CAP</sub> pin by the device	V <sub>CC</sub> = Max	–	–	V <sub>CC</sub>	V

## Data Retention and Endurance

Over the [Operating Range](#)

Parameter	Description	Min	Unit
DATA <sub>R</sub>	Data retention	20	Years
NV <sub>C</sub>	Nonvolatile STORE operations	1,000	K

## Capacitance

Parameter <sup>[23]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance (except BHE, BLE and HSB)	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(Typ)</sub>	7	pF
	Input capacitance (for BHE, BLE and HSB)		8	pF
C <sub>OUT</sub>	Output capacitance (except HSB)		7	pF
	Output capacitance (for HSB)		8	pF

## Thermal Resistance

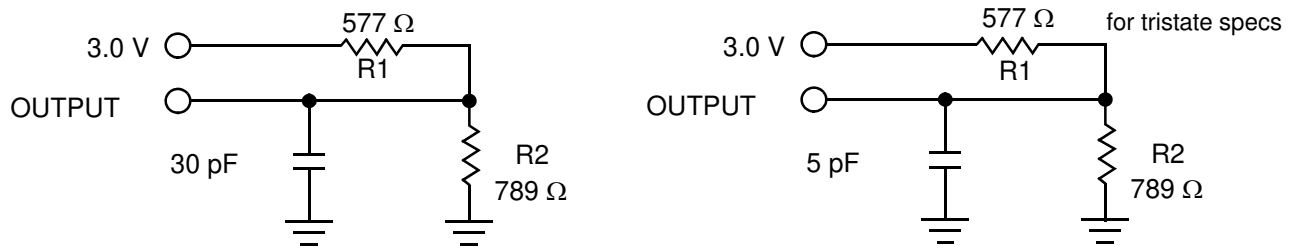
Parameter <sup>[23]</sup>	Description	Test Conditions	54-pin TSOP II	48-pin SSOP	48-ball FBGA	44-pin TSOP II	32-pin SOIC	Unit
θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	36.4	37.47	48.19	41.74	41.55	°C/W
θ <sub>JC</sub>	Thermal resistance (junction to case)		10.13	24.71	6.5	11.90	24.43	°C/W

### Notes

21. Min V<sub>CAP</sub> value guarantees that there is a sufficient charge available to complete a successful AutoStore operation. Max V<sub>CAP</sub> value guarantees that the capacitor on V<sub>CAP</sub> is charged to a minimum voltage during a Power-Up RECALL cycle so that an immediate power-down cycle can complete a successful AutoStore. Therefore it is always recommended to use a capacitor within the specified min and max limits. See application note [AN43593](#) for more details on V<sub>CAP</sub> options.
22. Maximum voltage on V<sub>CAP</sub> pin (V<sub>V<sub>CAP</sub></sub>) is provided for guidance when choosing the V<sub>CAP</sub> capacitor. The voltage rating of the V<sub>CAP</sub> capacitor across the operating temperature range should be higher than the V<sub>V<sub>CAP</sub></sub> voltage.
23. These parameters are guaranteed by design and are not tested.

**AC Test Loads**

**Figure 5. AC Test Loads**



**AC Test Conditions**

Input pulse levels .....0 V to 3 V  
 Input rise and fall times (10%–90%) ..... ≤ 3 ns  
 Input and output timing reference levels ..... 1.5 V



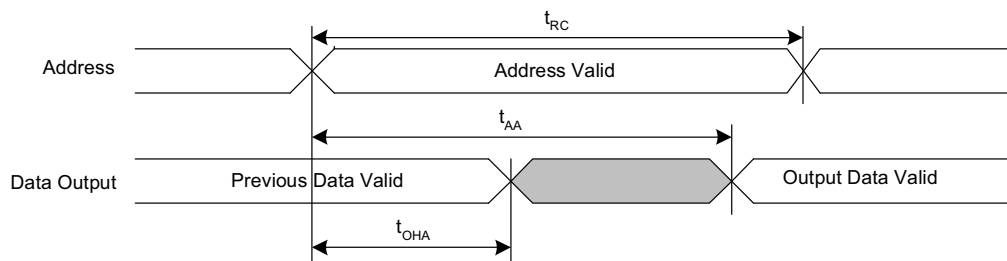
## AC Switching Characteristics

Over the [Operating Range](#)

Parameters <sup>[24]</sup>		Description	20 ns		25 ns		45 ns		Unit
Cypress Parameter	Alt Parameter		Min	Max	Min	Max	Min	Max	
<b>SRAM Read Cycle</b>									
t <sub>ACE</sub>	t <sub>ACS</sub>	Chip enable access time	–	20	–	25	–	45	ns
t <sub>RC</sub> <sup>[25]</sup>	t <sub>RC</sub>	Read cycle time	20	–	25	–	45	–	ns
t <sub>AA</sub> <sup>[26]</sup>	t <sub>AA</sub>	Address access time	–	20	–	25	–	45	ns
t <sub>DOE</sub>	t <sub>OE</sub>	Output enable to data valid	–	10	–	12	–	20	ns
t <sub>OHA</sub> <sup>[26]</sup>	t <sub>OH</sub>	Output hold after address change	3	–	3	–	3	–	ns
t <sub>LZCE</sub> <sup>[27, 28]</sup>	t <sub>LZ</sub>	Chip enable to output active	3	–	3	–	3	–	ns
t <sub>HZCE</sub> <sup>[27, 28]</sup>	t <sub>HZ</sub>	Chip disable to output inactive	–	8	–	10	–	15	ns
t <sub>LZOE</sub> <sup>[27, 28]</sup>	t <sub>OLZ</sub>	Output enable to output active	0	–	0	–	0	–	ns
t <sub>HZOE</sub> <sup>[27, 28]</sup>	t <sub>OHZ</sub>	Output disable to output inactive	–	8	–	10	–	15	ns
t <sub>PU</sub> <sup>[27]</sup>	t <sub>PA</sub>	Chip enable to power active	0	–	0	–	0	–	ns
t <sub>PD</sub> <sup>[27]</sup>	t <sub>PS</sub>	Chip disable to power standby	–	20	–	25	–	45	ns
t <sub>DBE</sub> <sup>[27]</sup>	–	Byte enable to data valid	–	10	–	12	–	20	ns
t <sub>LZBE</sub> <sup>[27]</sup>	–	Byte enable to output active	0	–	0	–	0	–	ns
t <sub>HZBE</sub> <sup>[27]</sup>	–	Byte disable to output inactive	–	8	–	10	–	15	ns
<b>SRAM Write Cycle</b>									
t <sub>WC</sub>	t <sub>WC</sub>	Write cycle time	20	–	25	–	45	–	ns
t <sub>PWE</sub>	t <sub>WP</sub>	Write pulse width	15	–	20	–	30	–	ns
t <sub>SCE</sub>	t <sub>CW</sub>	Chip enable to end of write	15	–	20	–	30	–	ns
t <sub>SD</sub>	t <sub>DW</sub>	Data setup to end of write	8	–	10	–	15	–	ns
t <sub>HD</sub>	t <sub>DH</sub>	Data hold after end of write	0	–	0	–	0	–	ns
t <sub>AW</sub>	t <sub>AW</sub>	Address setup to end of write	15	–	20	–	30	–	ns
t <sub>SA</sub>	t <sub>AS</sub>	Address setup to start of write	0	–	0	–	0	–	ns
t <sub>HA</sub>	t <sub>WR</sub>	Address hold after end of write	0	–	0	–	0	–	ns
t <sub>HZWE</sub> <sup>[27, 28, 29]</sup>	t <sub>WZ</sub>	Write enable to output disable	–	8	–	10	–	15	ns
t <sub>LZWE</sub> <sup>[27, 28]</sup>	t <sub>OW</sub>	Output active after end of write	3	–	3	–	3	–	ns
t <sub>BW</sub>	–	Byte enable to end of write	15	–	20	–	30	–	ns

## Switching Waveforms

Figure 6. SRAM Read Cycle #1 (Address Controlled) <sup>[25, 26, 30]</sup>



### Notes

24. Test conditions assume signal transition time of 3 ns or less, timing reference levels of  $V_{CC}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  and load capacitance shown in [Figure 5 on page 11](#).
25. WE must be HIGH during SRAM read cycles.
26. Device is continuously selected with CE, OE, and BHE/BLE LOW.
27. These parameters are guaranteed by design and are not tested.
28. Measured  $\pm 200$  mV from steady state output voltage.
29. If WE is low when CE goes low, the outputs remain in the high impedance state.
30. HSB must remain HIGH during Read and Write cycles.

Switching Waveforms (continued)

Figure 7. SRAM Read Cycle #2 ( $\overline{CE}$  and  $\overline{OE}$  Controlled) [31, 32, 33]

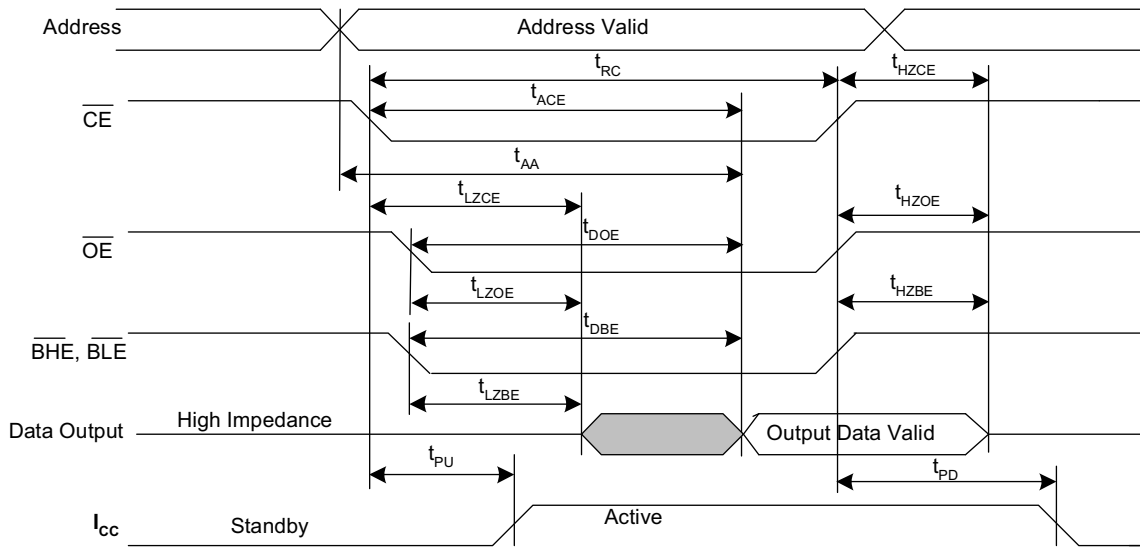
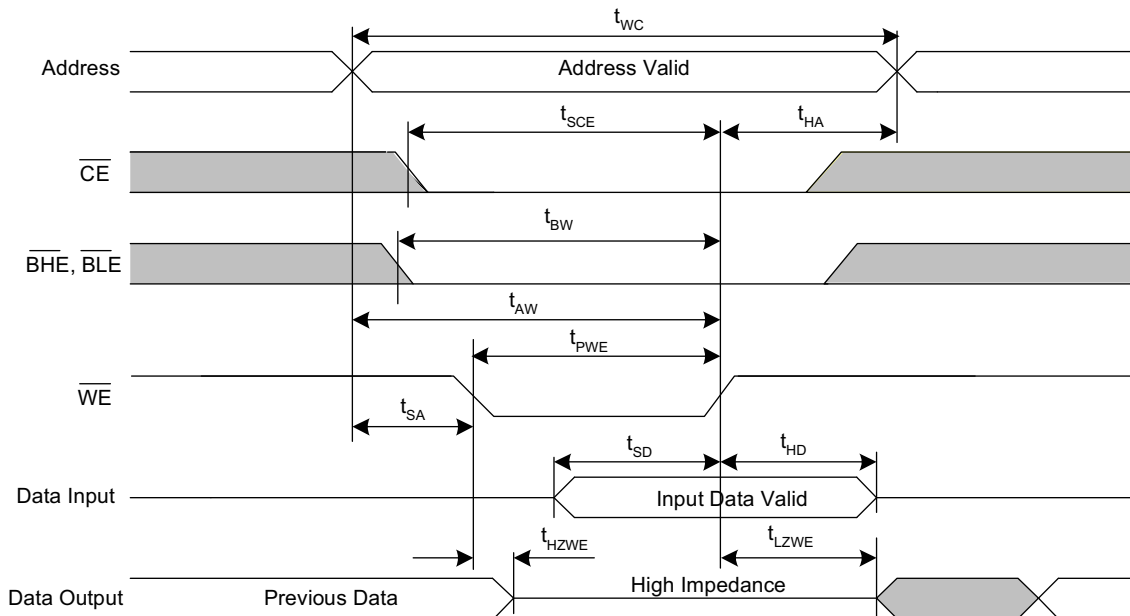


Figure 8. SRAM Write Cycle #1 ( $\overline{WE}$  Controlled) [31, 33, 34, 35]



Notes

- 31.  $\overline{BHE}$  and  $\overline{BLE}$  are applicable for  $\times 16$  configuration only.
- 32.  $\overline{WE}$  must be HIGH during SRAM read cycles.
- 33.  $\overline{HSB}$  must remain HIGH during Read and Write cycles.
- 34.  $\overline{CE}$  or  $\overline{WE}$  must be  $\geq V_{IH}$  during address transitions.
- 35. If  $\overline{WE}$  is low when  $\overline{CE}$  goes low, the outputs remain in the high impedance state.



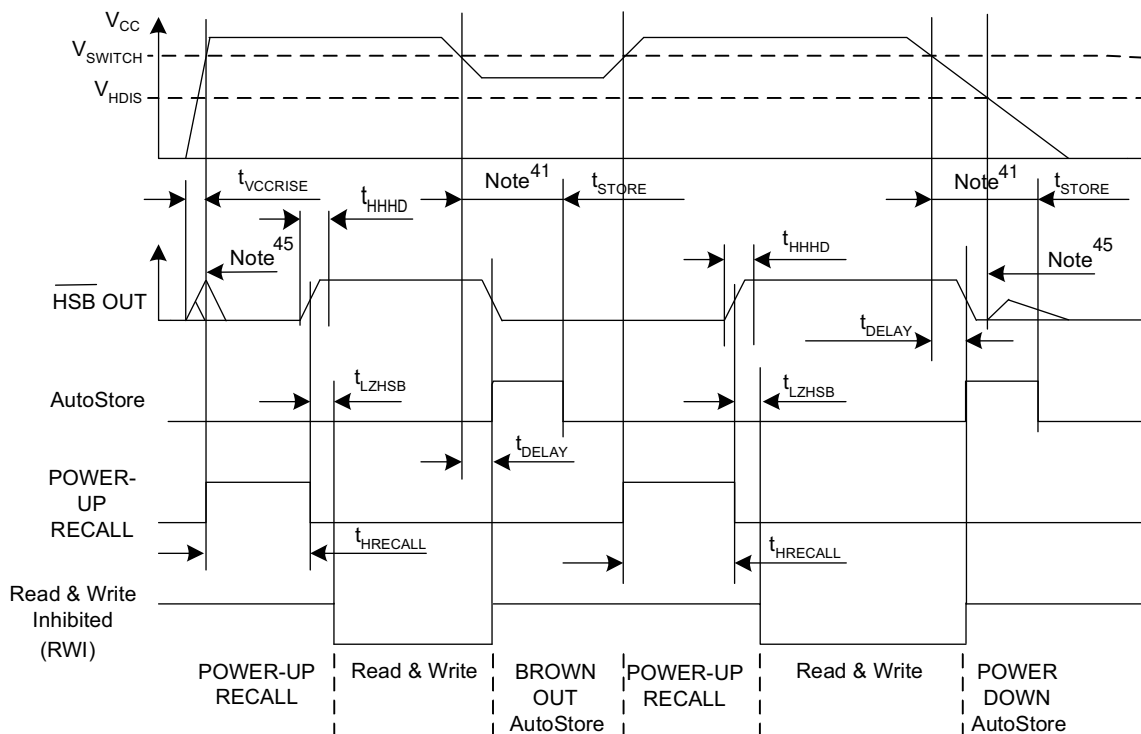
## AutoStore/Power-Up RECALL

Over the [Operating Range](#)

Parameter	Description	20 ns		25 ns		45 ns		Unit
		Min	Max	Min	Max	Min	Max	
$t_{HRECALL}^{[40]}$	Power-Up RECALL duration	–	20	–	20	–	20	ms
$t_{STORE}^{[41]}$	STORE cycle duration	–	8	–	8	–	8	ms
$t_{DELAY}^{[42]}$	Time allowed to complete SRAM write cycle	–	20	–	25	–	25	ns
$V_{SWITCH}$	Low voltage trigger level	–	2.65	–	2.65	–	2.65	V
$t_{VCCRRISE}^{[43]}$	$V_{CC}$ rise time	150	–	150	–	150	–	$\mu$ s
$V_{HDIS}^{[43]}$	HSB output disable voltage	–	1.9	–	1.9	–	1.9	V
$t_{LZHHSB}^{[43]}$	HSB to output active time	–	5	–	5	–	5	$\mu$ s
$t_{HHHD}^{[43]}$	HSB High active time	–	500	–	500	–	500	ns

## Switching Waveforms

Figure 11. AutoStore or Power-Up RECALL <sup>[44]</sup>



### Notes

- 40.  $t_{HRECALL}$  starts from the time  $V_{CC}$  rises higher than  $V_{SWITCH}$ .
- 41. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.
- 42. On a Hardware STORE and AutoStore initiation, SRAM write operation continues to be enabled for time  $t_{DELAY}$ .
- 43. These parameters are guaranteed by design and are not tested.
- 44. Read and Write cycles are ignored during STORE, RECALL, and while  $V_{CC}$  is lower than  $V_{SWITCH}$ .
- 45. During power-up and power-down, HSB glitches when HSB pin is pulled up through an external resistor.



## Software Controlled STORE/RECALL Cycle

Over the [Operating Range](#)

Parameter <sup>[46, 47]</sup>	Description	20 ns		25 ns		45 ns		Unit
		Min	Max	Min	Max	Min	Max	
$t_{RC}$	STORE/RECALL initiation cycle time	20	–	25	–	45	–	ns
$t_{SA}$	Address setup time	0	–	0	–	0	–	ns
$t_{CW}$	Clock pulse width	15	–	20	–	30	–	ns
$t_{HA}$	Address hold time	0	–	0	–	0	–	ns
$t_{RECALL}$	RECALL duration	–	200	–	200	–	200	$\mu$ s

## Switching Waveforms

Figure 12.  $\overline{CE}$  and  $\overline{OE}$  Controlled Software STORE/RECALL Cycle <sup>[47]</sup>

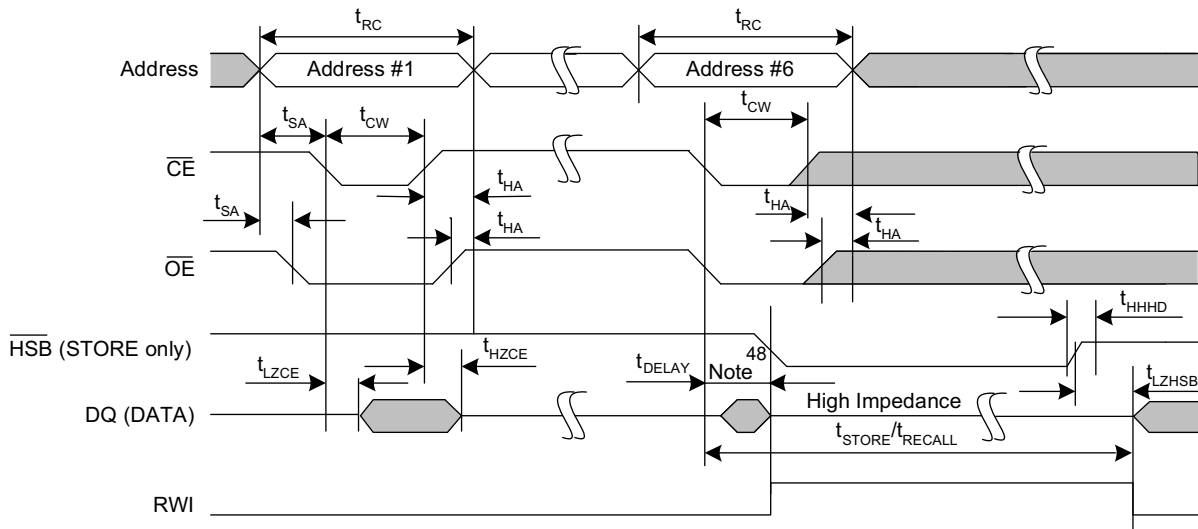
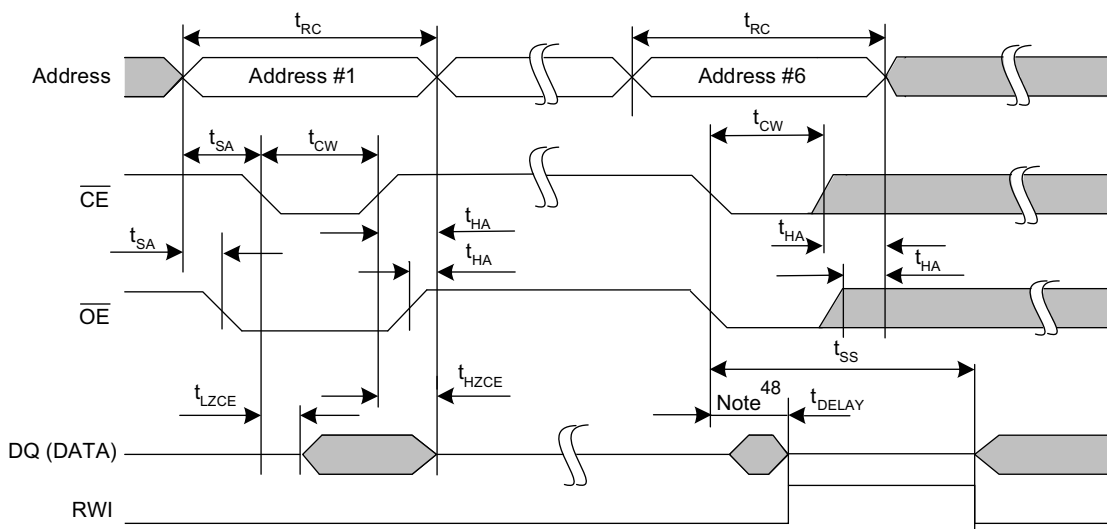


Figure 13. AutoStore Enable/Disable Cycle <sup>[47]</sup>



### Notes

46. The software sequence is clocked with  $\overline{CE}$  controlled or  $\overline{OE}$  controlled reads.

47. The six consecutive addresses must be read in the order listed in [Table 1 on page 7](#).  $\overline{WE}$  must be HIGH during all six consecutive cycles.

48. DQ output data at the sixth read may be invalid because the output is disabled at  $t_{DELAY}$  time.



## Truth Table For SRAM Operations

$\overline{\text{HSB}}$  must remain HIGH for SRAM operations

**Table 2. Truth Table for × 8 Configuration**

CE	WE	OE	Inputs/Outputs <sup>[52]</sup>	Mode	Power
H	X	X	High Z	Deselect/Power-down	Standby
L	H	L	Data Out (DQ <sub>0</sub> –DQ <sub>7</sub> );	Read	Active
L	H	H	High Z	Output disabled	Active
L	L	X	Data in (DQ <sub>0</sub> –DQ <sub>7</sub> );	Write	Active

**Table 3. Truth Table for × 16 Configuration**

CE	WE	OE	BHE <sup>[53]</sup>	BLE <sup>[53]</sup>	Inputs/Outputs <sup>[52]</sup>	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-down	Standby
L	X	X	H	H	High Z	Output disabled	Active
L	H	L	L	L	Data Out (DQ <sub>0</sub> –DQ <sub>15</sub> )	Read	Active
L	H	L	H	L	Data Out (DQ <sub>0</sub> –DQ <sub>7</sub> ); DQ <sub>8</sub> –DQ <sub>15</sub> in High Z	Read	Active
L	H	L	L	H	Data Out (DQ <sub>8</sub> –DQ <sub>15</sub> ); DQ <sub>0</sub> –DQ <sub>7</sub> in High Z	Read	Active
L	H	H	L	L	High Z	Output disabled	Active
L	H	H	H	L	High Z	Output disabled	Active
L	H	H	L	H	High Z	Output disabled	Active
L	L	X	L	L	Data In (DQ <sub>0</sub> –DQ <sub>15</sub> )	Write	Active
L	L	X	H	L	Data In (DQ <sub>0</sub> –DQ <sub>7</sub> ); DQ <sub>8</sub> –DQ <sub>15</sub> in High Z	Write	Active
L	L	X	L	H	Data In (DQ <sub>8</sub> –DQ <sub>15</sub> ); DQ <sub>0</sub> –DQ <sub>7</sub> in High Z	Write	Active

**Notes**

52. Data DQ<sub>0</sub>–DQ<sub>7</sub> for × 8 configuration and Data DQ<sub>0</sub>–DQ<sub>15</sub> for × 16 configuration.

53. BHE and BLE are applicable for × 16 configuration only.

**Ordering Information**

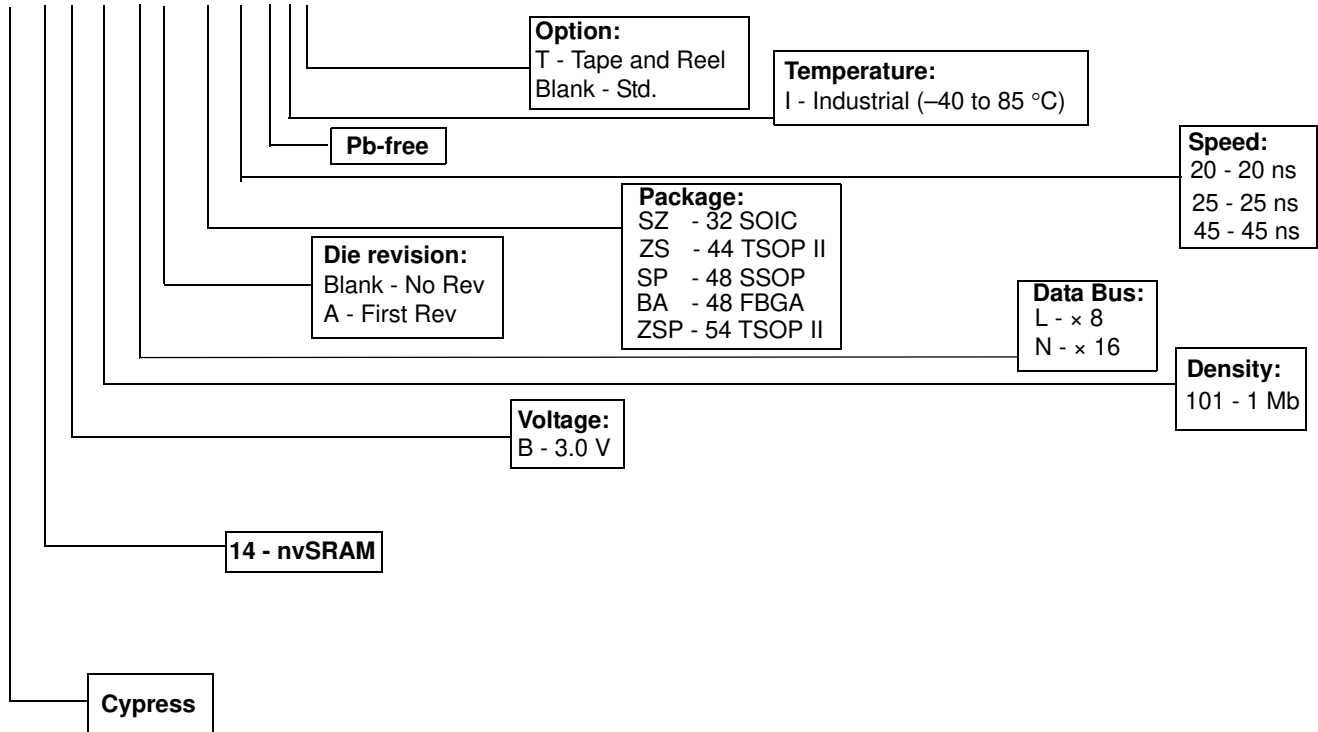
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
20	CY14B101LA-ZS20XIT	51-85087	44-pin TSOP II	Industrial
	CY14B101LA-ZS20XI	51-85087	44-pin TSOP II	
25	CY14B101LA-SZ25XIT	51-85127	32-pin SOIC	Industrial
	CY14B101LA-SZ25XI	51-85127	32-pin SOIC	
	CY14B101LA-ZS25XIT	51-85087	44-pin TSOP II	
	CY14B101LA-ZS25XI	51-85087	44-pin TSOP II	
	CY14B101LA-SP25XIT	51-85061	48-pin SSOP	
	CY14B101LA-SP25XI	51-85061	48-pin SSOP	
	CY14B101LA-BA25XIT	51-85128	48-ball FBGA	
	CY14B101LA-BA25XI	51-85128	48-ball FBGA	
	CY14B101NA-ZS25XIT	51-85087	44-pin TSOP II	
	CY14B101NA-ZS25XI	51-85087	44-pin TSOP II	
	45	CY14B101LA-SZ45XIT	51-85127	
CY14B101LA-SZ45XI		51-85127	32-pin SOIC	
CY14B101LA-ZS45XIT		51-85087	44-pin TSOP II	
CY14B101LA-ZS45XI		51-85087	44-pin TSOP II	
CY14B101LA-SP45XIT		51-85061	48-pin SSOP	
CY14B101LA-SP45XI		51-85061	48-pin SSOP	
CY14B101LA-BA45XIT		51-85128	48-ball FBGA	
CY14B101LA-BA45XI		51-85128	48-ball FBGA	
CY14B101NA-ZS45XIT		51-85087	44-pin TSOP II	
CY14B101NA-ZS45XI		51-85087	44-pin TSOP II	

All the above parts are Pb-free.



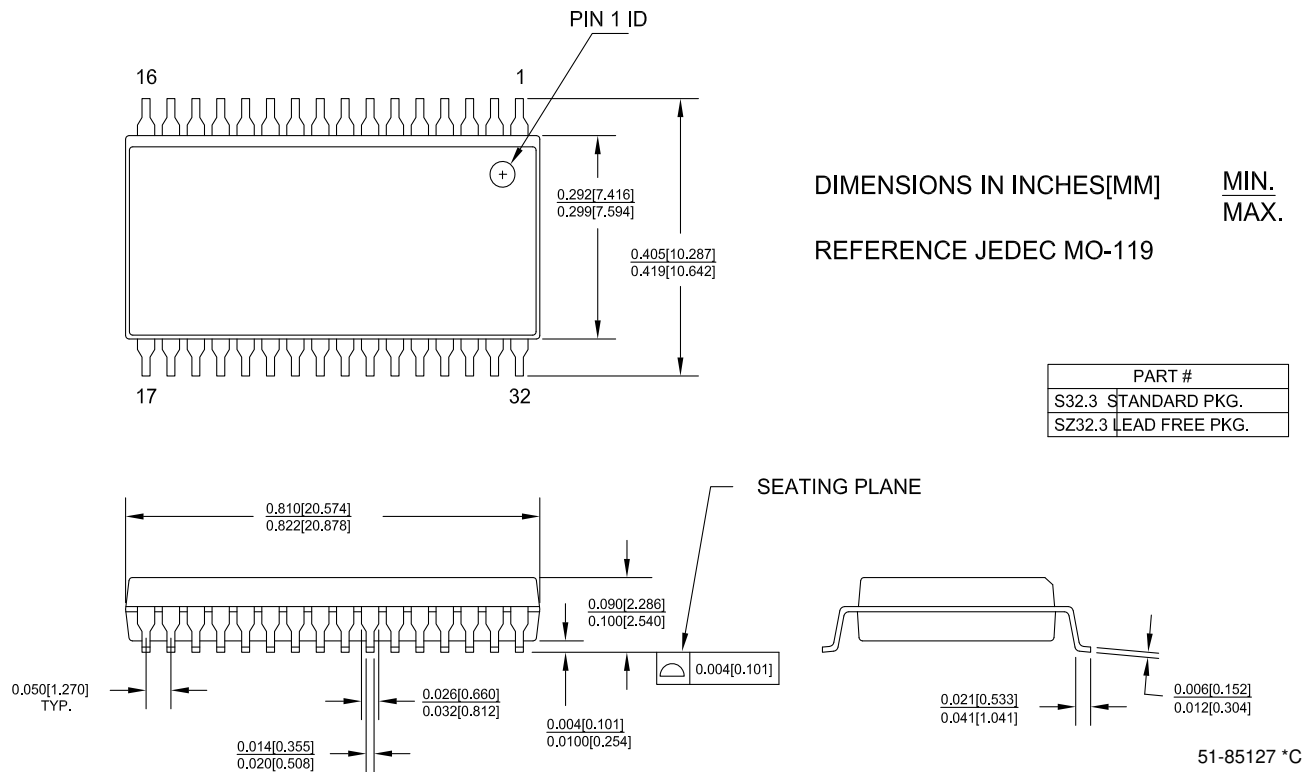
**Ordering Code Definitions**

**CY 14 B 101 L A - ZS 20 X I T**



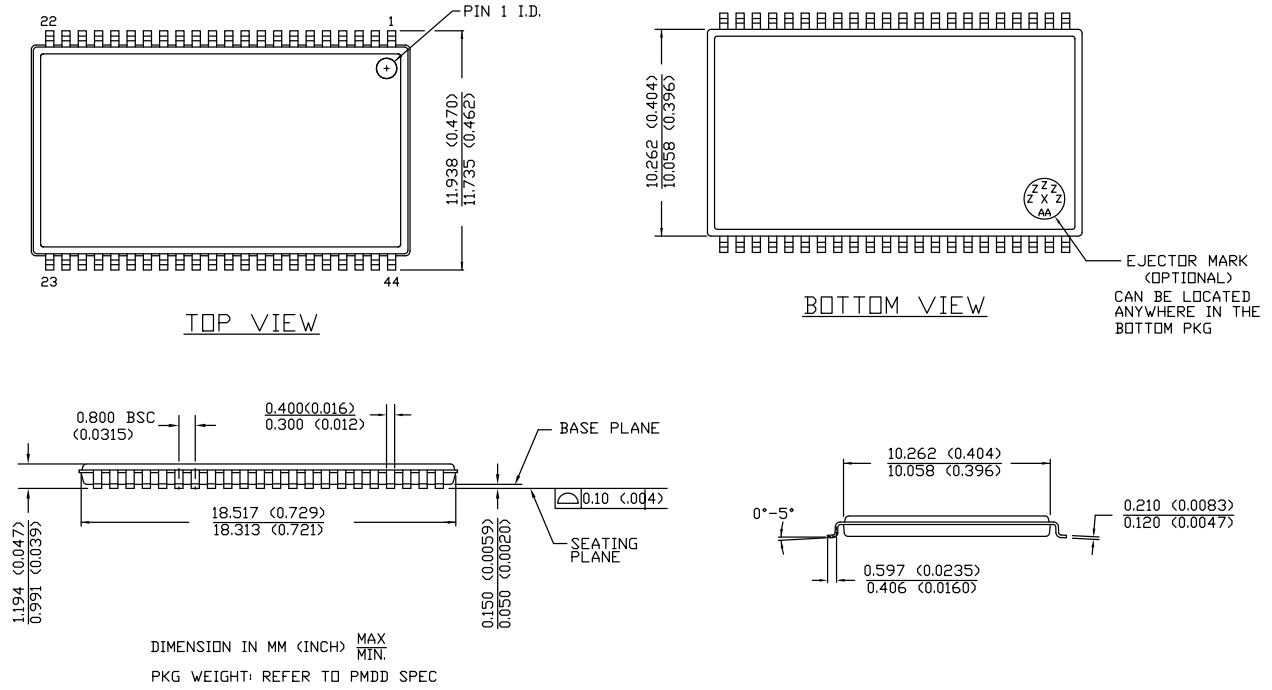
Package Diagrams

Figure 16. 32-pin SOIC (300 Mil) Package Outline, 51-85127



**Package Diagrams** (continued)

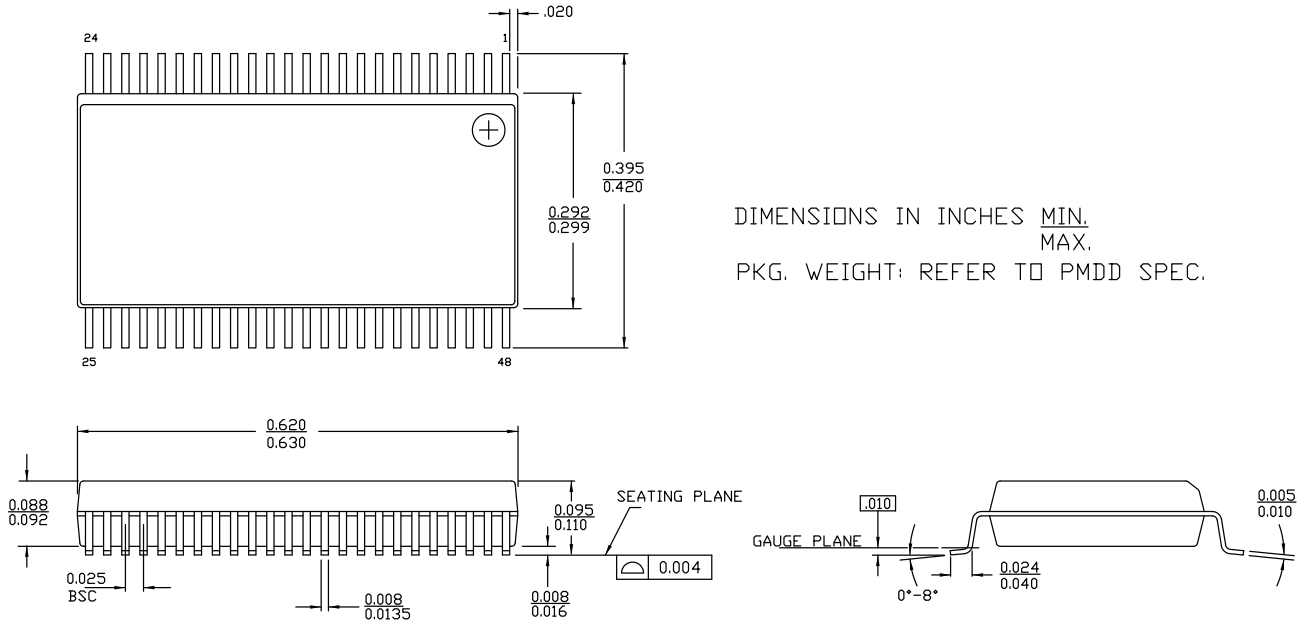
**Figure 17. 44-pin TSOP II Package Outline, 51-85087**



51-85087 \*E

**Package Diagrams** (continued)

**Figure 18. 48-pin SSOP (300 Mils) Package Outline, 51-85061**



DIMENSIONS IN INCHES MIN.  
MAX.  
PKG. WEIGHT: REFER TO PMDD SPEC.

51-85061 \*F





**Package Diagrams** (continued)

**Figure 20. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Package Outline, 51-85160**

