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MPEG Clock Generator with VCXO

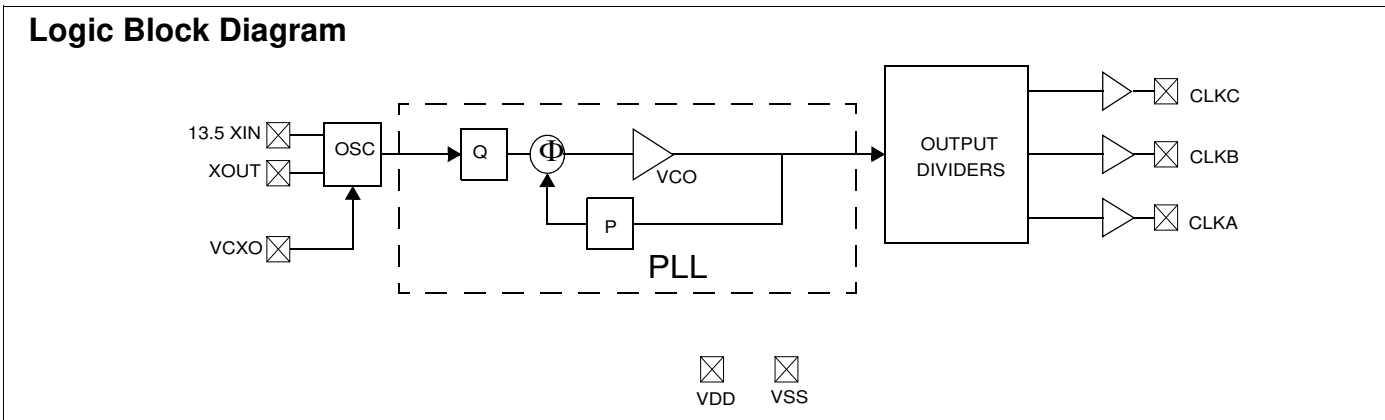
Features

- Integrated phase-locked loop (PLL)
- Low-jitter, high-accuracy outputs
- VCXO with analog adjust
- 3.3V operation
- 8-pin SOIC package

Benefits

- Highest-performance PLL tailored for multimedia applications
- Meets critical timing requirements in complex system designs
- Large ± 150 -ppm range, better linearity
- Enables application compatibility

| Part Number | Outputs | Input Frequency Range | Output Frequencies | VCXO Profile |
|-------------|---------|---|---------------------------------------|--------------|
| CY2412-1 | 3 | 13.5-MHz pullable crystal input per Cypress specification | Two 27 MHz outputs, one 54 MHz (3.3V) | Linear |
| CY2412-3 | 3 | 13.5-MHz pullable crystal input per Cypress specification | 27 MHz, 13.5 MHz, 54 MHz (3.3V) | Linear |



Pin Configuration

Figure 1. CY2412, 8-Pin SOIC

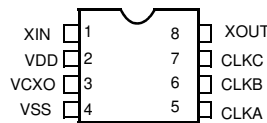


Table 1. Pin Definition - CY2412, 8-Pin SOIC

| Pin Name | Pin Number | Pin Description |
|---------------------------------|------------|-------------------------------|
| X _{IN} | 1 | Reference Crystal Input |
| V _{DD} | 2 | Voltage Supply |
| VCXO | 3 | Input Analog Control for VCXO |
| V _{SS} | 4 | Ground |
| CLKA | 5 | 54-MHz clock output |
| CLKB | 6 | 13.5-MHz clock output |
| CLKC | 7 | 27-MHz clock output |
| X _{OUT} ^[2] | 8 | Reference Crystal Output |

Pullable Crystal Specifications^[1]

| Parameter | Description | Condition | Min | Typ. | Max | Unit |
|--------------------------------|--|---|------|------|------|------|
| F _{NOM} | Nominal crystal frequency | Parallel resonance, fundamental mode, AT cut | – | 13.5 | – | MHz |
| C _{LNOM} | Nominal load capacitance | | – | 14 | – | pF |
| R ₁ | Equivalent series resistance (ESR) | Fundamental mode | – | – | 25 | Ω |
| R ₃ /R ₁ | Ratio of third overtone mode ESR to fundamental mode ESR | Ratio used because typical R ₁ values are much less than the maximum spec. | 3 | – | – | |
| DL | Crystal drive level | No external series resistor assumed | – | 0.5 | 2.0 | mW |
| F _{3SEPHI} | Third overtone separation from 3*F _{NOM} | High side | 300 | – | – | ppm |
| F _{3SEPLO} | Third overtone separation from 3*F _{NOM} | Low side | – | – | –150 | ppm |
| C ₀ | Crystal shunt capacitance | | – | – | 7 | pF |
| C ₀ /C ₁ | Ratio of shunt to motional capacitance | | 180 | – | 250 | |
| C ₁ | Crystal motional capacitance | | 14.4 | 18 | 21.6 | pF |

Absolute Maximum Conditions

| Parameter | Description | Min | Max | Unit |
|-----------------|---|-----------------------|-----------------------|------|
| V _{DD} | Supply Voltage | –0.5 | 7.0 | V |
| T _S | Storage Temperature ^[3] | –65 | 125 | °C |
| T _J | Junction Temperature | – | 125 | °C |
| | Digital Inputs | V _{SS} – 0.3 | V _{DD} + 0.3 | V |
| | Digital Outputs referred to V _{DD} | V _{SS} – 0.3 | V _{DD} + 0.3 | V |
| | Electrostatic Discharge | 2 | | kV |

Recommended Operating Conditions

| Parameter | Description | Min | Typ. | Max | Unit |
|-------------------|---|------|------|------|------|
| V _{DD} | Operating Voltage | 3.14 | 3.3 | 3.47 | V |
| T _A | Ambient Temperature | 0 | | 70 | °C |
| C _{LOAD} | Max. Load Capacitance | | | 15 | pF |
| f _{REF} | Reference Frequency | | 13.5 | | MHz |
| t _{PU} | Power up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic) | 0.05 | | 500 | ms |

DC Electrical Characteristics

| Parameter | Description | Test Conditions | Min | Typ. | Max | Unit |
|-----------------|-----------------------|---|-----|------|-----|------|
| I _{OH} | Output High Current | V _{OH} = V _{DD} – 0.5, V _{DD} = 3.3V | 12 | 24 | | mA |
| I _{OL} | Output Low Current | V _{OL} = 0.5, V _{DD} = 3.3V | 12 | 24 | | mA |
| C _{IN} | Input Capacitance | | | | 7 | pF |
| I _{Iz} | Input Leakage Current | | | 5 | | μA |

Notes

1. Crystals that meet this specification includes: Ecliptek ECX-5788-13.500M, Siward XTL001050A-13.5-14-400, Raltron A-13.500-14-CL, PDI HA13500XFSA14XC.
2. Float X_{OUT} if X_{IN} is externally driven.
3. Rated for ten years.

DC Electrical Characteristics (continued)

| Parameter | Description | Test Conditions | Min | Typ. | Max | Unit |
|-----------------|------------------------|--------------------------------|-----------|-----------|----------|------|
| $f_{\Delta XO}$ | VCXO pullability range | | ± 150 | | | ppm |
| V_{VCXO} | VCXO input range | | 0 | | V_{DD} | V |
| f_{VBW} | VCXO input bandwidth | | | DC to 200 | | kHz |
| I_{DD} | Supply Current | Sum of Core and Output Current | | | 35 | mA |

AC Electrical Characteristics

| Parameter ^[4] | Description | Test Conditions | Min | Typ. | Max | Unit |
|--------------------------|-------------------|--|-----|------|-----|------|
| DC | Output Duty Cycle | Duty Cycle is defined in Figure 2, 50% of V_{DD} | 45 | 50 | 55 | % |
| ER | Rising Edge Rate | Clock Edge Rate, Measured from 20% to 80% of V_{DD} , $C_{LOAD} = 15$ pF. See Figure 3. | 0.8 | 1.4 | | V/ns |
| EF | Falling Edge Rate | Output Clock Edge Rate, Measured from 80% to 20% of V_{DD} , $C_{LOAD} = 15$ pF. See Figure 3. | 0.8 | 1.4 | | V/ns |
| t_j | Clock Jitter | Peak to Peak period jitter | | 100 | 200 | ps |
| t_{10} | PLL Lock Time | | | | 3 | ms |

Figure 2. Duty Cycle Definition; $DC = t2/t1$

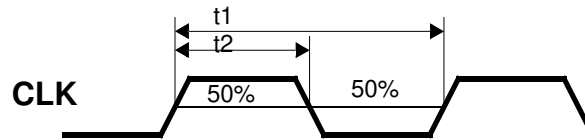


Figure 3. Rise and Fall Time Definitions: $ER = 0.6 \times VDD / t3$, $EF = 0.6 \times VDD / t4$

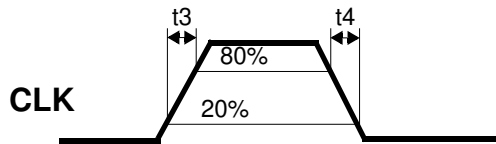
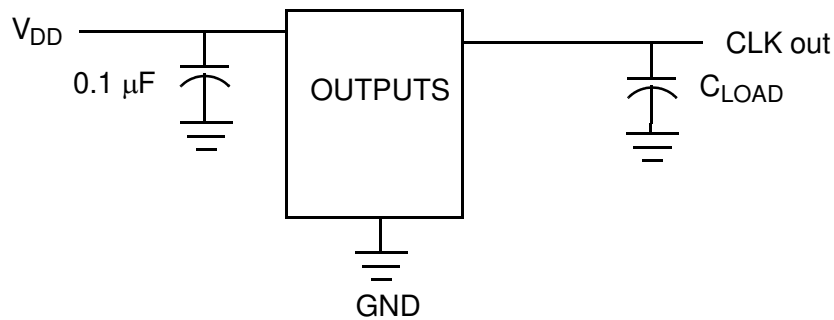


Figure 4. Test Circuit



Notes

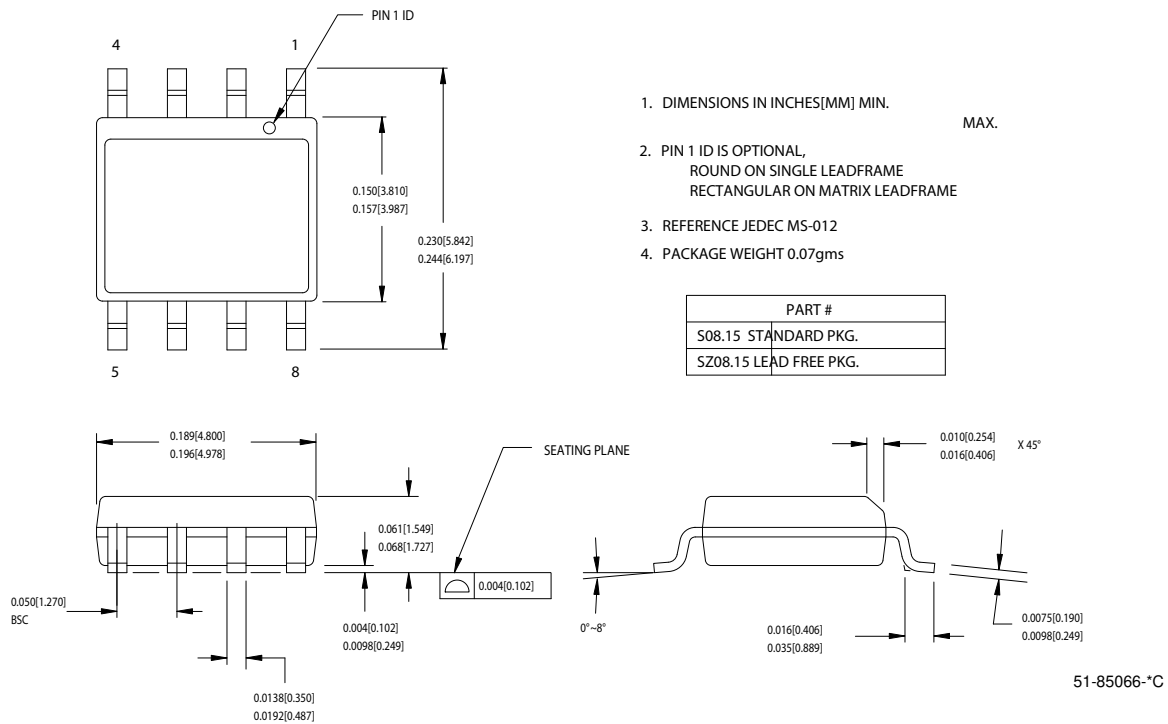
4. Not 100% tested.

Ordering Information

| Ordering Code | Package Type | Operating Range | Operating Voltage |
|-----------------------------|--------------------------|-----------------|-------------------|
| CY2412SC-1 ^[5] | 8-pin SOIC | Commercial | 3.3V |
| CY2412SC-1T ^[5] | 8-pin SOIC–Tape and Reel | Commercial | 3.3V |
| CY2412SC-3 ^[5] | 8-pin SOIC | Commercial | 3.3V |
| CY2412SC-3T ^[5] | 8-pin SOIC–Tape and Reel | Commercial | 3.3V |
| Pb-Free | | | |
| CY2412SXC-1 ^[5] | 8-pin SOIC | Commercial | 3.3V |
| CY2412SXC-1T ^[5] | 8-pin SOIC–Tape and Reel | Commercial | 3.3V |
| CY2412SXC-3 ^[5] | 8-pin SOIC | Commercial | 3.3V |
| CY2412SXC-3T ^[5] | 8-pin SOIC–Tape and Reel | Commercial | 3.3V |
| CY2412KSXC-1 | 8-pin SOIC | Commercial | 3.3V |
| CY2412KSXC-1T | 8-pin SOIC–Tape and Reel | Commercial | 3.3V |

Package Diagram

Figure 5. 8-Lead (150-Mil) SOIC S8



Note

5. Not recommended for new designs.

Document History Page

| Document Title: CY2412 MPEG Clock Generator with VCXO Document Number: 38-07227 | | | | |
|--|---------|-----------------|-----------------|---|
| REV. | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 110492 | SZV | 10/28/01 | Change from Spec number: 38-00898 to 38-07227 |
| *A | 112457 | CKN | 03/14/02 | Added CY2412-2 to data sheet |
| *B | 116961 | CKN | 08/06/02 | Removed CY2412-2 from the datasheet. Added CY2412-3 to data sheet |
| *C | 121879 | RBI | 12/14/02 | Power up requirements added to Operating Conditions Information |
| *D | 299735 | RGL | 02/15/05 | Added lead-free for CY2412-1 and CY2412-3 devices |
| *E | 2440866 | AESA | 04/25/08 | Updated template. Added Note "Not recommended for new designs." Added part number CY2412KSXC-1, and CY2412KSXC-1T in ordering information table. Replaced Lead-Free with Pb-Free. |
| *F | 2512734 | AESA | 06/05/08 | Added border to Logic Block Diagram. Added Sales, Solutions, and Legal Information. |

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