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CYPRESS

CY28331

## Clock Generator for AMD™ Hammer

## Features

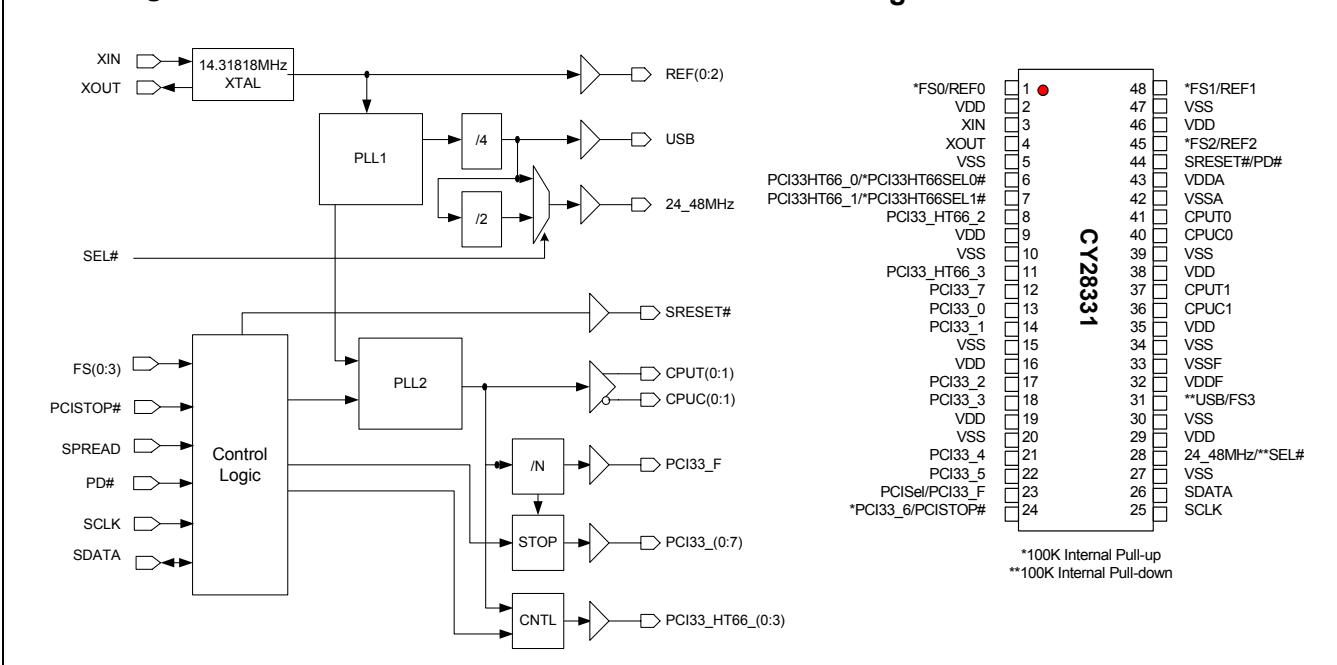
- Supports AMD™ Hammer CPU
- Two differential pairs of CPU clocks
- Eight low-skew/low-jitter PCI clocks
- One free-running PCI clock
- Four low-skew/low-jitter PCI/HyperTransport™ clocks
- One 48M output for USB
- One programmable 24M or 48M for FDC
- Three REF 14.318-MHz clocks
- Dial-a-Frequency® programmability
- Lexmark Spread Spectrum for optimal electromagnetic interference (EMI) reduction
- SMBus register-programmable options
- 5V-tolerance SCLK and SDATA lines
- 3.3V operation
- Power management control pins
- 48-pin SSOP package

Table 1. Frequency Table (MHz)<sup>[1]</sup>

| FS (3:0)       | PCI HT SEL | CPU  | HT66      | PCI  |
|----------------|------------|--|-----------|------|
| 0000           | X          | High-Z<br>(All outputs except XOUT are three-stated) |           |      |
| 0001           | 0/1        | 133.9  | 67.0/33.5 | 33.5 |
| 0010           | 0/1        | 166.9  | 66.8/33.4 | 33.4 |
| 0011           | 0/1        | 200.9  | 67.0/33.5 | 33.5 |
| 0100           | 0/1        | 100.0  | 66.7/33.3 | 33.3 |
| 0101           | 0/1        | 133.3  | 66.7/33.3 | 33.3 |
| 0110           | 0/1        | 166.7  | 66.7/33.3 | 33.3 |
| 0111 (default) | 0/1        | 200.0  | 66.7/33.3 | 33.3 |
| 1000           | 0/1        | 105.0  | 70.0/35.0 | 35.0 |
| 1001           | 0/1        | 110.0  | 73.3/36.7 | 36.7 |
| 1010           | 0/1        | 210.0  | 70.0/35.0 | 35.0 |
| 1011           | 0/1        | 240.0  | 60.0/30.0 | 30.0 |
| 1100           | 0/1        | 270.0  | 67.5/33.8 | 33.8 |
| 1101           | 0/1        | 233.3  | 58.3/29.2 | 29.2 |
| 1110           | 0/1        | 266.7  | 66.7/33.3 | 33.3 |
| 1111           | 0/1        | 300.0  | 75.0/37.5 | 37.5 |

## Block Diagram

## Pin Configuration



## Note:

1. HCLK, 66 MHz, and 33 MHz are in phase and synchronous at power-up.

**Pin Description**

| Pin                                     | Name                                     | PWR              | I/O | Description  |
|---|--|------------------|-----|--|
| 3                                       | XIN                                      | V <sub>DD</sub>  | I   | <b>Oscillator Buffer Input.</b> Connect to a crystal or to an external clock.  |
| 4                                       | XOUT                                     | V <sub>DD</sub>  | O   | <b>Oscillator Buffer Output.</b> Connect to a crystal. Do not connect when an external clock is applied at XIN.  |
| 41, 37                                  | CPUT(0:1)                                | V <sub>DDC</sub> | O   | <b>CPU clock outputs 0 and 1:</b> push-pull "true" output of differential pair.  |
| 40, 36                                  | CPUC(0:1)                                | V <sub>DDC</sub> | O   | <b>CPU clock outputs 0 and 1:</b> push-pull "complement" output of differential pair.  |
| 13, 14, 17,<br>18, 21, 22               | PCI33(0:5)                               |                  | O   | <b>3.3V PCI clock outputs controlled by PCISTOP#.</b>  |
| 23                                      | PCISel /<br>PCI33_F                      |                  | I/O | <b>PCISel is a strap option during power-up to select Pin 24 functionality:</b><br>0: Configure Pin 24 as PCI33_6<br>1: Configure Pin 24 as PCISTOP# (default 100k internal pull-up)<br>After power-up, this pin reverts to standard PCI33_F output.   |
| 8, 11                                   | PCI33_HT66(2:3)                          | V <sub>DDD</sub> | O   | <b>3.3V PCI 33-MHz or HyperTransport 66 clock outputs.</b> This group is selectable between 33 MHz and 66 MHz, based on the state of PCI33HT66SEL[0:1]#.   |
| 6, 7                                    | PCI33_HT66_[0:1]/<br>PCI33_HT66SEL[0:1]# | V <sub>DDD</sub> | I/O | <b>PCI33 or HT66 select.</b> This input strap selects the output frequency of PCI33_HT66 outputs to either 33 MHz or 66 MHz. There is an internal 100Kohm pull-up resistor. After power-up, this pin becomes PCI33_HT66_[0:1] output.<br>SEL1 SEL0 PIN6 PIN7 PIN8 PIN11<br>0 0 HT66_0 HT66_1 HT66_2 HT66_3<br>0 1 HT66_0 HT66_1 HT66_2 PCI33_3<br>1 0 HT66_0 HT66_1 PCI33_2 PCI33_3<br>1 1 HT66_0 PCI33_1 PCI33_2 PCI33_3        |
| 31                                      | USB/FS3                                  |                  | I/O | <b>3.3V USB clock output at 48 MHz.</b> At power-up this pin is sensed to determine the CPU output frequency. There is an internal 100K-ohm pull-down resistor.  |
| 28                                      | 24_48MHz/SEL#                            |                  | I/O | <b>3.3V super I/O clock output.</b> At power-up this pin is sensed to determine whether the output is 24 MHz or 48 MHz. There is an internal 100K-ohm pull-down resistor. This pin will be externally strapped high using a 10K-ohm resistor to V <sub>SS</sub> . 0 = 48 MHz, 1 = 24 MHz.  |
| 1, 48, 45                               | REF(0:2)/FS(0:2)                         |                  | I/O | <b>3.3V reference clock output.</b> At power-up this pin is sensed to determine the CPU output frequency. There is an internal 100K-ohm pull-up resistor for FS0, while FS(1:2) includes 100K ohm pull-up resistors.   |
| 44                                      | SRESET#/PD#                              |                  | I/O | <b>Watchdog Time-out Reset Output.</b> Power-down input (100K internal pull-up).   |
| 24                                      | PCI33_6/<br>PCISTOP#                     |                  | I/O | <b>When configured through pin 23 as PCI_STOP#, this pin controls the PCI33(0:5,7) and PCI33_HT66(1:3) outputs.</b> Active LOW control input to halt all 33-MHz PCI clocks except PCI33_F. Only the PCI33_HT66 outputs that are running at 33 MHz will be stopped. The outputs will be glitch-free when turning off and turning on (100K internal pull-up). When configured through pin 23 as PCI33_6, PCI_STOP# is unavailable. |
| 12                                      | PCI33_7                                  |                  | O   | <b>3.3V PCI clock outputs controlled by PCISTOP#.</b>  |
| 26                                      | SDATA                                    |                  | I/O | <b>Data pin for SMBus (rev2.0).</b> There is an internal 100K-ohm pull-up resistor.  |
| 25                                      | SCLK                                     |                  | I   | <b>Clock pin for SMBus (rev2.0).</b> There is an internal 100K-ohm pull-up resistor.   |
| 2, 9, 16,<br>19, 29, 35,<br>38, 46      | V <sub>DD</sub>                          |                  | PWR | <b>Power connection to 3.3V for the core.</b>  |
| 5, 10, 15,<br>20, 27, 30,<br>34, 39, 47 | V <sub>SS</sub>                          |                  | GND | <b>Power connection to GROUND for the CORE section of the chip.</b>  |
| 43                                      | V <sub>DDA</sub>                         |                  | PWR | <b>Power connection to 3.3V for the ANALOG section of the chip.</b>  |

**Pin Description** (continued)

| Pin | Name             | PWR | I/O | Description   |
|-----|------------------|-----|-----|---|
| 42  | V <sub>SSA</sub> |     | GND | <b>Power connection to GROUND for the analog section of the chip.</b>     |
| 32  | V <sub>DDF</sub> |     | PWR | <b>Power connection to 3.3V for the 48-MHz PLL section of the chip.</b>   |
| 33  | V <sub>SSF</sub> |     | GND | <b>Power connection to GROUND for the 48-MHz PLL section of the chip.</b> |

**Serial Data Interface**

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface (SDI), various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the SDI initialize to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions.

**Data Protocol**

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 2*.

The block write and block read protocol is outlined in *Table 3* while *Table 4* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

**Table 2. Command Code Definition**

| Bit   | Description  |
|-------|--|
| 7     | 0 = Block read or block write operation, 1 = Byte read or byte write operation.  |
| (6:0) | Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000.' |

**Table 3. Block Read and Block Write Protocol**

| Block Write Protocol |  | Block Read Protocol |  |
|----------------------|--|---------------------|--|
| Bit                  | Description  | Bit                 | Description  |
| 1                    | Start  | 1                   | Start  |
| 2:8                  | Slave address – 7 bits   | 2:8                 | Slave address – 7 bits   |
| 9                    | Write = 0  | 9                   | Write = 0  |
| 10                   | Acknowledge from slave   | 10                  | Acknowledge from slave   |
| 11:18                | Command Code – 8 bits<br>'00000000' stands for block operation | 11:18               | Command Code – 8 bits<br>'00000000' stands for block operation |
| 19                   | Acknowledge from slave   | 19                  | Acknowledge from slave   |
| 20:27                | Byte Count – 8 bits  | 20                  | Repeat start   |
| 28                   | Acknowledge from slave   | 21:27               | Slave address – 7 bits   |
| 29:36                | Data byte 1 – 8 bits   | 28                  | Read = 1   |
| 37                   | Acknowledge from slave   | 29                  | Acknowledge from slave   |
| 38:45                | Data byte 2 – 8 bits   | 30:37               | Byte count from slave – 8 bits                                 |
| 46                   | Acknowledge from slave   | 38                  | Acknowledge  |
| ....                 | .....  | 39:46               | Data byte from slave – 8 bits                                  |
| ....                 | Data Byte (N-1) – 8 bits                                       | 47                  | Acknowledge  |
| ....                 | Acknowledge from slave   | 48:55               | Data byte from slave – 8 bits                                  |
| ....                 | Data Byte N – 8 bits   | 56                  | Acknowledge  |
| ....                 | Acknowledge from slave   | ....                | Data bytes from slave/Acknowledge                              |
| ....                 | Stop   | ....                | Data byte N from slave – 8 bits                                |
|                      |  | ....                | Not Acknowledge  |
|                      |  | ....                | Stop   |

**Table 4. Byte Read and Byte Write Protocol**

| Byte Write Protocol |  | Byte Read Protocol |  |
|---------------------|--|--------------------|--|
| Bit                 | Description  | Bit                | Description  |
| 1                   | Start  | 1                  | Start  |
| 2:8                 | Slave address – 7 bits   | 2:8                | Slave address – 7 bits   |
| 9                   | Write = 0  | 9                  | Write = 0  |
| 10                  | Acknowledge from slave   | 10                 | Acknowledge from slave   |
| 11:18               | Command Code – 8 bits<br>'1xxxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed | 11:18              | Command Code – 8 bits<br>'1xxxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed |
| 19                  | Acknowledge from slave   | 19                 | Acknowledge from slave   |
| 20:27               | Data byte from master – 8 bits   | 20                 | Repeat start   |
| 28                  | Acknowledge from slave   | 21:27              | Slave address – 7 bits   |
| 29                  | Stop   | 28                 | Read = 1   |
|                     |  | 29                 | Acknowledge from slave   |
|                     |  | 30:37              | Data byte from slave – 8 bits  |
|                     |  | 38                 | Not Acknowledge  |
|                     |  | 39                 | Stop   |

## Serial Control Registers

### Byte 0: Frequency and Spread Spectrum Control Register

| Bit | @Pup         | Pin# | Name    | Description  |
|-----|--------------|------|---------|--|
| 7   | Inactive = 0 |      |         | Write Disable (write once). A 1 written to this bit after a 1 has been written to Byte0 bit0 will permanently disable modification of all configuration registers until the part has been powered off. Once the clock generator has been Write Disabled, the SMBus controller should still accept and acknowledge subsequent write cycles but it should not modify any of the registers.   |
| 6   | 0            |      |         | For Test, always program to '0'  |
| 5   | 1            | 12   | PCI33_7 | Enable (1 = Enabled, 0 = Disabled)   |
| 4   | FS3 pin      | 31   | FS3     | corresponds to Frequency Selection. See <i>Table 1</i> .   |
| 3   | FS2 pin      | 45   | FS2     | corresponds to Frequency Selection. See <i>Table 1</i> .   |
| 2   | FS1 pin      | 48   | FS1     | corresponds to Frequency Selection. See <i>Table 1</i> .   |
| 1   | FS0 pin      | 1    | FS0     | corresponds to Frequency Selection. See <i>Table 1</i> .   |
| 0   | Inactive = 0 |      |         | Write Enable. A 1 written to this bit after power-up will enable modification of all configuration registers and subsequent 0's written to this bit will disable modification of all configuration except this single bit. Note that block write transactions to the interface will complete, however unless the interface has been previously unlocked, the writes will have no effect. The effect of writing this bit does not take effect until the subsequent block write command. |

### Byte 1: PCI Clock Control Register

| Bit | @Pup | Pin# | Name    | Description                        |
|-----|------|------|---------|------------------------------------|
| 7   | 1    | 23   | PCI33_F | Enable (1 = Enabled, 0 = Disabled) |
| 6   | 1    | 24   | PCI33_6 | Enable (1 = Enabled, 0 = Disabled) |
| 5   | 1    | 22   | PCI33_5 | Enable (1 = Enabled, 0 = Disabled) |
| 4   | 1    | 21   | PCI33_4 | Enable (1 = Enabled, 0 = Disabled) |
| 3   | 1    | 18   | PCI33_3 | Enable (1 = Enabled, 0 = Disabled) |
| 2   | 1    | 17   | PCI33_2 | Enable (1 = Enabled, 0 = Disabled) |
| 1   | 1    | 14   | PCI33_1 | Enable (1 = Enabled, 0 = Disabled) |
| 0   | 1    | 13   | PCI33_0 | Enable (1 = Enabled, 0 = Disabled) |

**Byte 2: USB, 24–48MHz, REF(0:2) Control Register**

| Bit | @Pup       | Pin #  | Name      | Description  |
|-----|------------|--------|-----------|--|
| 7   | active = 1 | 37, 36 | CPUT/C(1) | CPUT/C(1) shutdown. This bit can be optionally used to disable the CPUT/C(1) clock pair. During shutdown, CPUT = low and CPUC = high |
| 6   | active = 1 | 41, 40 | CPUT/C(0) | CPUT/C(0) shutdown. This bit can be optionally used to disable the CPUT/C(0) clock pair. During shutdown, CPUT = low and CPUC = high |
| 5   | active = 1 | 45     | REF2      | Enable (1 = Enabled, 0 = Disabled)   |
| 4   | active = 1 | 48     | REF1      | Enable (1 = Enabled, 0 = Disabled)   |
| 3   | active = 1 | 1      | REF0      | Enable (1 = Enabled, 0 = Disabled)   |
| 2   | active = 1 | 28     | 24_48MHz  | Enable (1 = Enabled, 0 = Disabled)   |
| 1   | active = 1 | 31     | USB       | Enable (1 = Enabled, 0 = Disabled)   |
| 0   | 0          |        |           | For Test, always program to '0'  |

**Byte 3: PCI Clock Free Running Select Control Register**

| Bit | @Pup         | Pin # | Name         | Description  |
|-----|--------------|-------|--------------|--|
| 7   | Inactive = 0 |       |              | PCI_DRV<br>0 = Low Strength<br>1 = High Strength                   |
| 6   | Inactive = 0 |       |              | PCI33_HT66 Drive Strength<br>0 = Low Strength<br>1 = High Strength |
| 5   | Inactive = 0 | 22    | PCI5         | Free running enable (10 = Free running, 0 = Disabled)              |
| 4   | Inactive = 0 | 21    | PCI4         | Free running enable (1 = Free running, 0 = Disabled)               |
| 3   | Inactive = 0 | 18    | PCI3         | Free running enable (1 = Free running, 0 = Disabled)               |
| 2   | 1            | 11    | PCI33_HT66_3 | Enable (1 = Enabled, 0 = Disabled)                                 |
| 1   | 1            | 8     | PCI33_HT66_2 | Enable (1 = Enabled, 0 = Disabled)                                 |
| 0   | 1            | 7     | PCI33_HT66_1 | Enable (1 = Enabled, 0 = Disabled)                                 |

**Byte 4: Pin Latched/Real-time State**

| Bit | @Pup    | Pin# | Name          | Description  |
|-----|---------|------|---------------|--|
| 7   | 1       | 6    | PCI33_HT66_0  | Enable (1 = Enabled, 0 = Disabled)   |
| 6   | HW      |      | 24_48MHz/SEL# | Pin power-up latched state   |
| 5   | 0       |      | Reserved      | For Test, always program to '0'  |
| 4   | 1       |      | SSEN          | Spread Spectrum enable (0 = disable, 1 = enable).<br>This bit provides a SW programmable control for spread spectrum clocking. |
| 3   | FS3 pin | 31   | FS3           | Power-up latched state   |
| 2   | FS2 pin | 45   | FS2           | Power-up latched state   |
| 1   | FS1 pin | 48   | FS1           | Power-up latched state   |
| 0   | FS0 pin | 1    | FS0           | Power-up latched state   |

**Byte 5: SSCG, Dial-a-Skew™, and Dial-a-Ratio™ Register**

| Bit | @Pup | Description                |      |      |                  |
|-----|------|----------------------------|------|------|------------------|
| 7   | 0    | Spread Spectrum Selection: | bit7 | bit6 | bit5 % Spread    |
| 6   | 1    |                            | 0    | 0    | 0 -1.5           |
|     |      |                            | 0    | 0    | 1 -1.0           |
|     |      |                            | 0    | 1    | 0 -0.7           |
|     |      |                            | 0    | 1    | 1 -0.5 (default) |
| 5   | 1    |                            | 1    | 0    | 0 ±0.75          |
|     |      |                            | 1    | 0    | 1 ±0.50          |
|     |      |                            | 1    | 1    | 0 ±0.35          |
|     |      |                            | 1    | 1    | 1 ±0.25          |

**Byte 5: SSCG, Dial-a-Skew™, and Dial-a-Ratio™ Register (continued)**

| Bit | @Pup | Description  |                   |               |
|-----|------|--|-------------------|---------------|
| 4   | 0    | HT66 Frequency Fractional Aligner: These bits determine the HT66 fixed frequency when the HT66 Output Frequency Selection bit is set. It does not incorporate spread spectrum. |                   |               |
| 3   | 0    | Fract_Align  | PCI <sub>HT</sub> | PCI           |
| 2   | 0    | bit[4:0]   | (MHz)             | (MHz)         |
| 1   | 0    | 00000  | Off               | Off (default) |
| 0   | 0    | 00001  | 66.5              | 33.2          |
|     |      | 00010  | 67.5              | 33.7          |
|     |      | 00011  | 68.5              | 34.3          |
|     |      | 00100  | 69.5              | 34.8          |
|     |      | 00101  | 70.6              | 35.3          |
|     |      | 00110  | 71.6              | 35.8          |
|     |      | 00111  | 72.6              | 36.3          |
|     |      | 01000  | 73.6              | 36.8          |
|     |      | 01001  | 74.7              | 37.3          |
|     |      | 01010  | 75.7              | 37.8          |
|     |      | 01011  | 76.7              | 38.4          |
|     |      | 01100  | 77.7              | 38.9          |
|     |      | 01101  | 78.7              | 39.4          |
|     |      | 01110  | 79.8              | 39.9          |
|     |      | 01111  | 80.8              | 40.4          |
|     |      | 10000  | 81.8              | 40.9          |
|     |      | 10001  | 82.8              | 41.4          |
|     |      | 10010  | 83.9              | 41.9          |
|     |      | 10011  | 84.9              | 42.4          |
|     |      | 10100  | 85.9              | 43.0          |
|     |      | 10101  | 86.9              | 43.5          |
|     |      | 10110  | 88.0              | 44.0          |
|     |      | 10111  | 89.0              | 44.5          |
|     |      | 11000  | 90.0              | 45.0          |
|     |      | 11001  | 91.0              | 45.5          |
|     |      | 11010  | 92.0              | 46.0          |
|     |      | 11011  | 93.1              | 46.5          |
|     |      | 11100  | 94.1              | 47.0          |
|     |      | 11101  | 95.1              | 47.6          |
|     |      | 11110  | 96.1              | 48.1          |
|     |      | 11111  | 97.2              | 48.6          |

**Byte 6: Watchdog Control Register**

| Bit | @Pup | Name                            | Description   |
|-----|------|---------------------------------|---|
| 7   | 0    | HT66 Output Frequency Selection | HT66 Output Frequency Selection:<br>0: Set according to Frequency Selection Table<br>1: Set according to Fractional Aligner Table   |
| 6   | 0    | Pin 44 Mode Select              | Pin 44 Mode Select:<br>0 = Pin 12 is the output pin as SRESET# signal.<br>1 = Pin 12 is the input pin which functions as a PD# signal.  |
| 5   | 0    | Frequency Reversion             | Frequency Reversion:<br>This bit allows setting the Revert Frequency once the system is rebooted due to Watchdog time out only.<br>0 = Selects frequency of existing H/W setting<br>1 = Selects frequency of the second to last S/W setting. (the software setting prior to the one that caused a system reboot). |
| 4   | 0    | WD Time-out                     | WD Time-out:<br>This bit is set to "1" when the Watchdog times out. It is reset to "0" when the system clears the WD time stamps (WD3:0).   |

**Byte 6: Watchdog Control Register (continued)**

| Bit | @Pup | Name | Description   |   |   |               |
|-----|------|------|---|---|---|---------------|
| 3   | 0    | WD3  | WD3 .. .. WD0   |   |   |               |
| 2   | 0    | WD2  | This bit allows the selection of the time stamp for the Watchdog timer. After a Watchdog time-out, the frequency will revert to the original frequency.   |   |   |               |
| 1   | 0    | WD1  | 0 0 0 0 Off (default)<br>0 0 0 1 1 second<br>0 0 1 0 2 seconds<br>0 0 1 1 3 seconds<br>0 1 0 0 4 seconds<br>0 1 0 1 5 seconds<br>0 1 1 0 6 seconds<br>0 1 1 1 7 seconds<br>1 0 0 0 8 seconds<br>1 0 0 1 9 seconds<br>1 0 1 0 10 seconds<br>1 0 1 1 11 seconds<br>1 1 0 0 12 seconds<br>1 1 0 1 13 seconds<br>1 1 1 0 14 seconds<br>1 1 1 1 15 seconds |   |   |               |
| 0   | 0    | WD0  | 0   | 0 | 0 | Off (default) |
|     |      |      | 0   | 0 | 1 | 1 second      |
|     |      |      | 0   | 1 | 0 | 2 seconds     |
|     |      |      | 0   | 1 | 1 | 3 seconds     |
|     |      |      | 1   | 0 | 0 | 4 seconds     |
|     |      |      | 1   | 0 | 1 | 5 seconds     |
|     |      |      | 0   | 1 | 0 | 6 seconds     |
|     |      |      | 0   | 1 | 1 | 7 seconds     |
|     |      |      | 1   | 0 | 0 | 8 seconds     |
|     |      |      | 1   | 0 | 1 | 9 seconds     |
|     |      |      | 1   | 0 | 1 | 10 seconds    |
|     |      |      | 1   | 0 | 1 | 11 seconds    |
|     |      |      | 1   | 1 | 0 | 12 seconds    |
|     |      |      | 1   | 1 | 1 | 13 seconds    |
|     |      |      | 1   | 1 | 0 | 14 seconds    |
|     |      |      | 1   | 1 | 1 | 15 seconds    |

**Byte 7: Clock Vendor ID**

| Bit | @Pup | Description    |  |  |  |
|-----|------|----------------|--|--|--|
| 7   | 0    | Revision ID[1] |  |  |  |
| 6   | 1    | Revision ID[0] |  |  |  |
| 5   | 0    | Device ID[9]   |  |  |  |
| 4   | 1    | Device ID[8]   |  |  |  |
| 3   | 1    | Vendor ID[3]   |  |  |  |
| 2   | 0    | Vendor ID[2]   |  |  |  |
| 1   | 0    | Vendor ID[1]   |  |  |  |
| 0   | 0    | Vendor ID[0]   |  |  |  |

**Byte 8: Device ID**

| Bit | @Pup | Description |  |  |  |
|-----|------|-------------|--|--|--|
| 7   | 0    | Device ID   |  |  |  |
| 6   | 1    | Device ID   |  |  |  |
| 5   | 0    | Device ID   |  |  |  |
| 4   | 0    | Device ID   |  |  |  |
| 3   | 1    | Device ID   |  |  |  |
| 2   | 0    | Device ID   |  |  |  |
| 1   | 1    | Device ID   |  |  |  |
| 0   | 1    | Device ID   |  |  |  |

**Byte 9: Dial-a-Frequency Control Register N**

| Bit | @PUp | Description |  |  |  |
|-----|------|-------------|--|--|--|
| 7   | 0    | ATPG Pulse  |  |  |  |

**Byte 9: Dial-a-Frequency Control Register N (continued)**

| Bit | @PUp | Description  |
|-----|------|--|
| 6   | N6   | These bits are for programming the PLL's internal N register. This access allows the user to modify the CPU frequency with great accuracy. All other synchronous clocks (clocks that are generated from the same PLL, such as PCI, remain at their existing ratios relative to the CPU clock.) |
| 5   | N5   |  |
| 4   | N4   |  |
| 3   | N3   |  |
| 2   | N2   |  |
| 1   | N1   |  |
| 0   | N0   |  |

**Byte 10: Dial-a-Frequency Control Register M**

| Bit | @Pup  | Description  |
|-----|-------|--|
| 7   | 0     | ATPG Mode (default = 0)  |
| 6   | M5    | These bits are for programming the PLL's internal M register. This access allows the user to modify the CPU frequency with great accuracy. All other synchronous clocks (clocks that are generated from the same PLL, such as PCI, remain at their existing ratios relative to the CPU clock.) |
| 5   | M4    |  |
| 4   | M3    |  |
| 3   | M2    |  |
| 2   | M1    |  |
| 1   | M0    |  |
| 0   | DAFEN | When this bit = 1, it enables the Dial-a-Frequency N and M bits to be multiplexed into the internal N and M registers. When this bit = 0, the ROM based N and M values are loading into the internal N and M registers.  |

**Byte 11:**

| Bit | @Pup | Pin # | Name           | Description   |
|-----|------|-------|----------------|---|
| 7   | 0    |       |                | For Test, ALWAYS program to '0'   |
| 6   | HW   | 7     | PCI33HT66SEL1# | PCI33/HT66 Mode Select 1<br>Power-up Latched State of PCI33HT66SEL1# Mode Select 1 (read only). |
| 5   | HW   | 6     | PCI33HT66SEL0# | PCI33/HT66 Mode Select 0<br>Power-up Latched State of PCI33HT66SEL0# Mode Select 0 (read only). |
| 4   | 0    |       |                | Reserved Set = 0  |
| 3   | 0    |       |                | Reserved Set = 0  |
| 2   | 0    |       |                | Reserved Set = 0  |
| 1   | 0    |       |                | Reserved Set = 0  |
| 0   | 0    |       |                | Reserved Set = 0  |

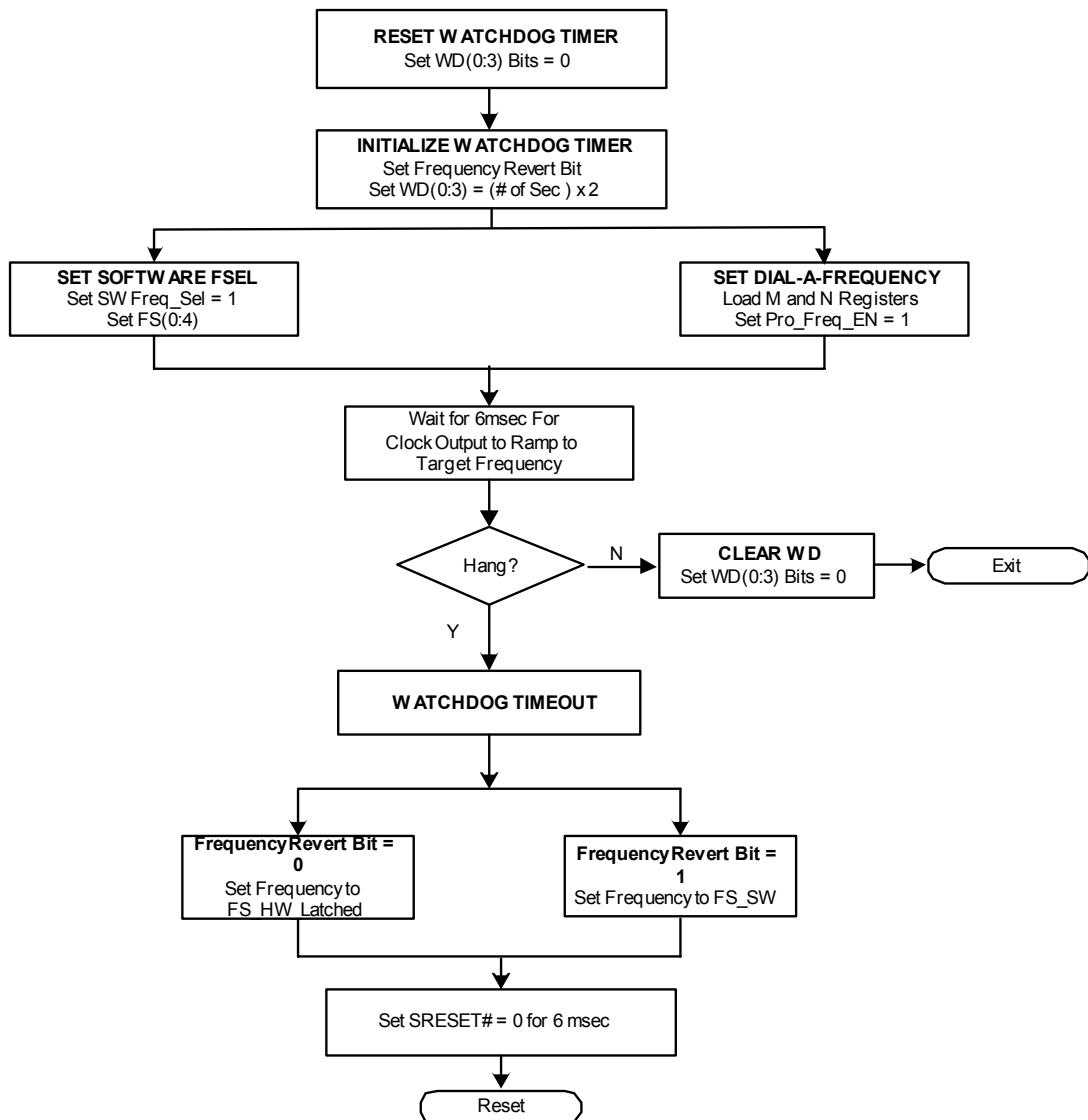
**System Self-Recovery Clock Management**

This feature is designed to allow the system designer to change frequency while the system is running and reboot the operation of the system in case of a hang up due to the frequency change.

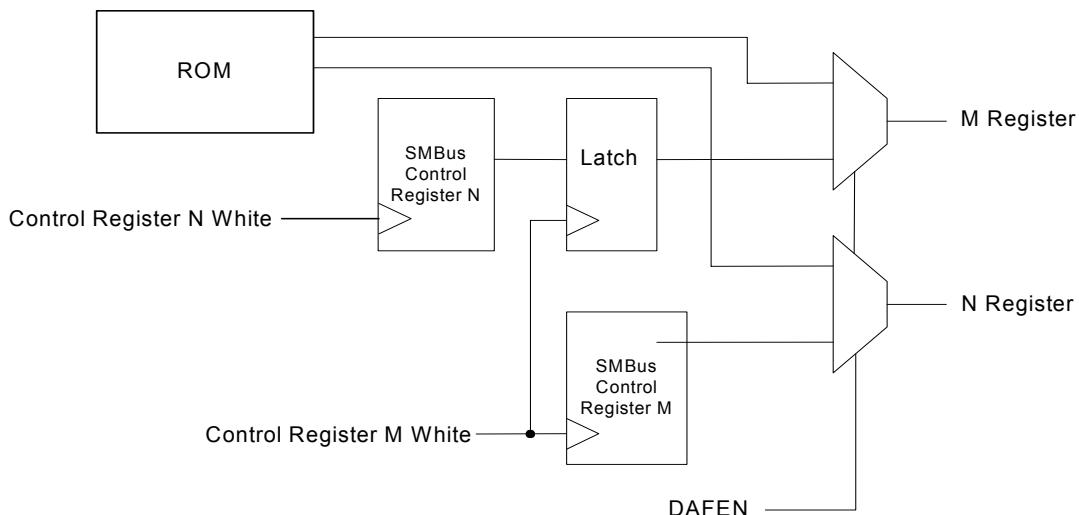
When the system sends an SMBus command requesting a frequency change through the Dial-a-Frequency Control Registers, it must have previously sent a command to the Watchdog Timer to select which time out stamp the Watchdog must perform, otherwise the System Self-Recovery feature will not be applicable. Consequently, this device will change frequency and then the Watchdog timer starts timing. Meanwhile, the system BIOS is running its operation with the

new frequency. If this device receives a new SMBus command to clear the bits originally programmed in Watchdog Timer bits (reprogram to 0000) before the Watchdog times out, then this device will keep operating in its normal condition with the new selected frequency.

The Watchdog timer will also be triggered if you program the software frequency select bits (FSEL) to a new frequency selection. If the Watchdog times out before the new SMBus reprograms the Watchdog Timer bits to (0000), then this device will send a low system reset pulse, on SRESET#, and changes WD Time-out bit to "1."



## Dial-a-Frequency



**Figure 1. Dial-a-Frequency Feature**

The SMBus controlled Dial-a-Frequency feature is available in this device via Dial-a-Frequency Control Register N and Dial-a-Frequency Control Register M. P is a PLL constant that depends on the frequency selection prior to accessing the Dial-a-Frequency feature.

**Table 5.**

| FS(3:0) | P         |
|---------|-----------|
| 0000    |           |
| 0001    | 127994667 |
| 0010    | 191992000 |
| 0011    | 191992000 |
| 0100    | 95996000  |
| 0101    | 127994667 |
| 0110    | 191992000 |
| 0111    | 191992000 |
| 1000    | 95966000  |
| 1001    | 95966000  |
| 1010    | 191992000 |
| 1011    | 191992000 |
| 1100    | 191992000 |
| 1101    | 191992000 |
| 1110    | 191992000 |
| 1111    | 191992000 |

The algorithm is the same for all P values, which is  $F_{CPU} = (P \cdot N) / M$  with the following conditions.  $M = (20..58)$ ,  $N = (21..125)$  and  $N > M > N/2$ .

## Operation

Pin strapping on any configuration pin is based on a 10K ohm resistor connected to either 3.3V ( $V_{DD}$ ) or ground ( $V_{SS}$ ). When the  $V_{DD}$  supply goes above 2.0V, the Power-on-Reset circuitry latches all of the configuration bits into their respective registers and then allows the outputs to be enabled. The output may not occur immediately after this time as the PLL needs to be locked and will not output an invalid frequency. The CPU frequencies are defined from the hardware-sampled inputs. Additional frequencies and operating states can be selected through the SMBus-programmable interface.

Spread spectrum modulation is required for all outputs derived from the internal CPU PLL2. This include the CPU(0:1), PCI33(0:6), PCI33\_F, and PCI33\_HT66(0:3). The REF (0:2), USB, and 24\_48 clocks are not affected by the spread spectrum modulation. The spread spectrum modulation is set for both center and down modes using a Lexmark profiles for amounts of 0.5% and 1.0% at a 33-KHz rate.

The CPU clock driver is of a push-pull type for the differential outputs, instead of the Athlon open-drain style. The CPU clock termination has been derived such that a 15-40 ohm, 3.3V output driver can be used for the CPU clock.

The PCISTOP# signal provides for synchronous control over the any output, except the PCI33\_F, that is running at 33 MHz. If the PCI33\_HT66 outputs are configured to run at 66 MHz will not be stopped by this signal. The PCISTOP# signal is sampled by an internal PCI clock such that once it is sensed low or active, the 33-MHz signals are stopped on the next high to low transition and remains low.

### Absolute Maximum Ratings

| Parameter                        | Description                       | Conditions                  | Min.    | Max.           | Unit |
|----------------------------------|-----------------------------------|-----------------------------|---------|----------------|------|
| $V_{DD}$ , $V_{DDA}$ , $V_{DDF}$ | Supply Voltage                    | Non-functional              | -0.5    | 4.6            | V    |
| $V_{IN}$                         | Input Voltage                     | Functional                  | -0.5    | $V_{DD} + 0.5$ | V    |
| $T_S$                            | Storage Temperature               | Non-functional              | -65     | +150           | °C   |
| $T_J$                            | Temperature, Junction             | Functional                  |         | +150           | °C   |
| $\theta_{JC}$                    | Dissipation, Junction to Case     | Mil-Spec 883E Method 1012.1 | 32.78   |                | °C/W |
| $\theta_{JA}$                    | Dissipation, Junction to Ambient  | JEDEC (JESD 51)             | 73.61   |                | °C/W |
| $ESD_h$                          | ESD Protection (Human Body Model) | MIL-STD-883, Method 3015    | > 2,000 |                | V    |
| UI-94                            | Flammability Rating               | $V=0$ @1/8 in.              |         | 10             | ppm  |
| MSL                              | Moisture Sensitivity Level        |                             | 1       |                |      |

### Recommended Operating Conditions

| Parameter                        | Description                            | Min.  | Typ.   | Max.  | Unit |
|----------------------------------|--|-------|--------|-------|------|
| $V_{DD}$ , $V_{DDA}$ , $V_{DDF}$ | Supply Voltage                         | 3.135 | 3.3    | 3.465 | V    |
| $T_A$                            | Operating Temperature, Ambient         | 0     |        | 70    | °C   |
| $f_{XIN}$                        | Input Frequency (Crystal or Reference) | 10    | 14.318 | 16    | MHz  |

### SCLK and SDATA Input Electrical Characteristics (5V-tolerant)

| Parameter           | Description            | Conditions            | Min.           | Typ. | Max.           | Unit |
|---------------------|------------------------|-----------------------|----------------|------|----------------|------|
| $V_{IL}$            | Input Low Voltage      |                       | $V_{SS} - 0.5$ |      | 0.8            | V    |
| $V_{IH}$            | Input High Voltage     |                       | 2.0            |      | $V_{DD} + 0.3$ | V    |
| $I_{IL}$ , $I_{IH}$ | Input High/Low Current | $0 < V_{IN} < V_{DD}$ |                |      | $\pm 5$        | µA   |
| $V_{OL}$            | Output High Voltage    | $I_{OL} = 1.75$ mA    | $V_{SS} - 0.3$ |      | 0.4            | V    |
| $I_{OL}$            | Output Low Current     | $V_O = 0.8V$          | 2              |      | 6              | mA   |

### DC Electrical Specifications (All outputs loaded)

| Parameter    | Description                 | Conditions                            | Min.           | Typ.       | Max.           | Unit |
|--------------|-----------------------------|---------------------------------------|----------------|------------|----------------|------|
| $V_{IL}$     | Input Low Voltage           |                                       | $V_{SS} - 0.5$ |            | 0.8            | V    |
| $V_{IH}$     | Input High Voltage          |                                       | 2.0            |            | $V_{DD} + 0.5$ | V    |
| $I_{IL}$     | Input Low Current           | $@V_{IL} = V_{SS}$ , except PU and PD |                |            | -5             | µA   |
| $I_{IH}$     | Input High Current          | $@V_{IH} = V_{DD}$ , except PU and PD |                |            | 5              | µA   |
| $I_{TSL}$    | Three-state Leakage Current |                                       |                |            | 10             | µA   |
| $I_{DD3.3V}$ | Dynamic Supply Current      | CPU(0:1) @ 200 MHz                    |                | 250        |                | mA   |
| $I_{PD3.3V}$ | Power-down Supply Current   |                                       |                |            | 2              | mA   |
| $C_{IN}$     | Input Pin Capacitance       | Except XIN and XOUT                   |                |            | 5              | pF   |
| $C_{OUT}$    | Output Pin Capacitance      |                                       |                |            | 6              | pF   |
| $L_{PIN}$    | Pin Inductance              |                                       |                |            | 7              | nH   |
| $C_{XTAL}$   | Crystal Pin Capacitance     | Measured from Pin to Ground.          | 27             | 36         | 45             | pF   |
| $V_{BIAS}$   | Crystal DC Bias Voltage     |                                       | $0.3V_{DD}$    | $V_{DD}/2$ | $0.7V_{DD}$    | V    |

**AC Electrical Specifications**

| Parameter                               | Description                           | Test Condition   | PCI133_HT66 = 66MHz |        |      |      |
|---|---------------------------------------|--|---------------------|--------|------|------|
|   |                                       |  | Min.                | Typ.   | Max. | Unit |
| <b>Hammer CPU</b>                       |                                       |  |                     |        |      |      |
| $T_R$                                   | Output Rise Edge Rate                 | Measured @ the Hammer test load using $V_{OCM} \pm 400$ mV, 0.850V to 1.650V | 2                   |        | 7    | V/ns |
| $T_F$                                   | Output Fall Edge Rate                 | Measured @ the Hammer test load using $V_{OCM} \pm 400$ mV, 1.650V to 0.850V | 2                   |        | 7    | V/ns |
| $V_{DIFF}$                              | Differential Voltage                  | Measured @ the Hammer test load (single-ended)                               | 0.4                 | 1.25   | 2.3  | V    |
| $\Delta_{DIFF}$                         | Change in $V_{DIFF\_DC}$ Magnitude    | Measured @ the Hammer test load (single-ended)                               | -150                |        | 150  | mV   |
| $V_{CM}$                                | Common Mode Voltage                   | Measured @ the Hammer test load (single-ended)                               | 1.05                | 1.25   | 1.45 | V    |
| $\Delta V_{CM}$                         | Change in $V_{CM}$                    | Measured @ the Hammer test load (single-ended)                               | -200                |        | 200  | mV   |
| $T_{DC}$                                | Duty Cycle                            | Measured at $V_{OX}$   | 45                  | 50     | 53   | %    |
| $T_{CYC}$                               | Jitter, Cycle to Cycle                | Measured at $V_{OX}$   | 0                   | 100    | 200  | ps   |
| $T_{ACCUM}$                             | Jitter, Accumulated                   | Measured at $V_{OX}$   | -1000               |        | 1000 | ps   |
| $T_{FS}$                                | Frequency Stabilization from Power-up | Measure from full supply voltage   | 0                   |        | 3    | ms   |
| $R_{ON}$                                | Output Impedance                      | Average value during switching transition                                    | 15                  | 35     | 55   | W    |
| <b>PCI/HyperTransport Clock Outputs</b> |                                       |  |                     |        |      |      |
| $V_{OL}$                                | Output Low Voltage                    | $I_{OL} = 9.0$ mA  |                     |        | 0.4  | V    |
| $V_{OH}$                                | Output High Voltage                   | $I_{OH} = -12.0$ mA  | 2.4                 |        |      | V    |
| $I_{OL}$                                | Output Low Current                    | $V_O = 0.8$ V  |                     | 10     |      | mA   |
| $I_{OH}$                                | Output High Current                   | $V_O = 2.0$ V  |                     |        | -15  | mA   |
| $F_{33}$                                | Frequency Actual                      |  |                     | 33.33  |      | MHz  |
| $F_{66}$                                |                                       |  |                     | 66.67  |      | MHz  |
| $T_R$                                   | Output Rise Edge Rate                 | Measured from 20% to 60%   | 0.5                 |        | 4    | V/ns |
| $T_F$                                   | Output Fall Edge Rate                 | Measured from 60% to 20%   | 0.5                 |        | 4    | V/ns |
| $T_{DC}$                                | Duty Cycle                            | Measured at 1.5V   | 45                  |        | 55   | %    |
| $T_{CCJ}$                               | Cycle-to-Cycle Jitter                 | Measured at 1.5V   | 0                   |        | 400  | ps   |
| $T_{LTJ}$                               | Long Term Jitter                      | Measured at 1.5V   | -1000               |        | 1000 | ps   |
| <b>REF(0:2) Clock Outputs</b>           |                                       |  |                     |        |      |      |
| $V_{OL}$                                | Output Low Voltage                    | $I_{OL} = 9.0$ mA  |                     |        | 0.4  | V    |
| $V_{OH}$                                | Output High Voltage                   | $I_{OH} = -12.0$ mA  | 2.4                 |        |      | V    |
| $I_{OL}$                                | Output Low Current                    | $V_O = 0.8$ V  |                     | 16     |      | mA   |
| $I_{OH}$                                | Output High Current                   | $V_O = 2.0$ V  |                     |        | -22  | mA   |
| $F$                                     | Frequency, Actual                     |  |                     | 14.318 |      | MHz  |
| $T_R$                                   | Output Rise Edge Rate                 | Measured from 20% to 60%   | 0.5                 |        | 2    | V/ns |
| $T_F$                                   | Output Fall Edge Rate                 | Measured from 60% to 20%   | 0.5                 |        | 2    | V/ns |
| $T_{DC}$                                | Duty Cycle                            | Measured at 1.5V   | 45                  |        | 55   | %    |
| $T_{CCJ}$                               | Cycle-to-Cycle Jitter                 | Measured at 1.5V   | 0                   | 500    | 1000 | ps   |
| $T_{LTJ}$                               | Long-term Jitter                      | Measured at 1.5V   | -1000               |        | 1000 | ps   |
| $T_{FS}$                                | Frequency Stabilization from Power-up | Measure from full supply voltage   | 0                   |        | 3    | mS   |
| $R_{ON}$                                | Output Impedance                      | Average value during switching transition                                    | 20                  | 24     | 60   | W    |

**AC Electrical Specifications (continued)**

| Parameter                       | Description                           | Test Condition                            | PCI133_HT66 = 66MHz |        |      |      |
|---------------------------------|---------------------------------------|---|---------------------|--------|------|------|
|                                 |                                       |   | Min.                | Typ.   | Max. | Unit |
| <b>USB, 24_48 Clock Outputs</b> |                                       |   |                     |        |      |      |
| V <sub>OL</sub>                 | Output Low Voltage                    | I <sub>OL</sub> = 9.0 mA                  |                     |        | 0.4  | V    |
| V <sub>OH</sub>                 | Output High Voltage                   | I <sub>OH</sub> = -12.0 mA                | 2.4                 |        |      | V    |
| I <sub>OL</sub>                 | Output Low Current                    | V <sub>O</sub> = 0.8V                     | 16                  |        |      | mA   |
| I <sub>OH</sub>                 | Output High Current                   | V <sub>O</sub> = 2.0V                     |                     |        | -22  | mA   |
| F <sub>33</sub>                 | Frequency Actual                      |   |                     | 24.004 |      | MHz  |
| F <sub>66</sub>                 |                                       |   |                     | 48.008 |      | MHz  |
| t <sub>R</sub>                  | Output Rise Edge Rate                 | Measured from 20% to 80%                  | 0.5                 |        | 2    | V/ns |
| t <sub>F</sub>                  | Output Fall Edge Rate                 | Measured from 80% to 20%                  | 0.5                 |        | 2    | V/ns |
| t <sub>D</sub>                  | Duty Cycle                            | Measured at 1.5V                          | 45                  |        | 55   | %    |
| T <sub>CCJ</sub>                | 24_48MHz Cycle-to-Cycle Jitter        | Measured at 1.5V                          | 0                   | 250    | 500  | ps   |
| T <sub>CCJ</sub>                | USB Cycle-to-Cycle Jitter             | Measured at 1.5V                          | 0                   |        | 200  | ps   |
| T <sub>LTJ</sub>                | Long-term Jitter                      | Measured at 1.5V                          | -1000               |        | 1000 | ps   |
| T <sub>STABLE</sub>             | Frequency Stabilization from Power-up | Measure from full supply voltage          | 0                   |        | 3    | ms   |
| R <sub>ON</sub>                 | Output Impedance                      | Average value during switching transition | 20                  | 24     | 60   | W    |

**Table 6. Skew** <sup>[2]</sup>

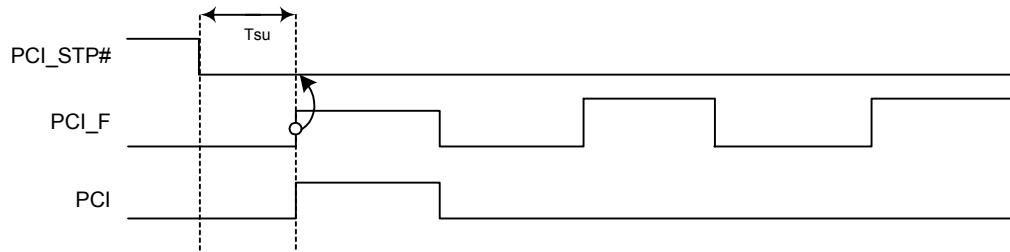
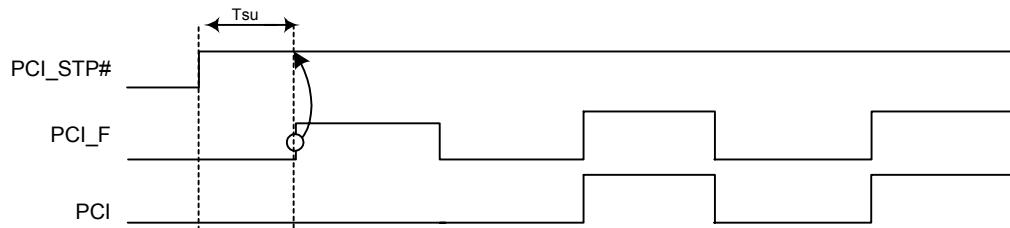
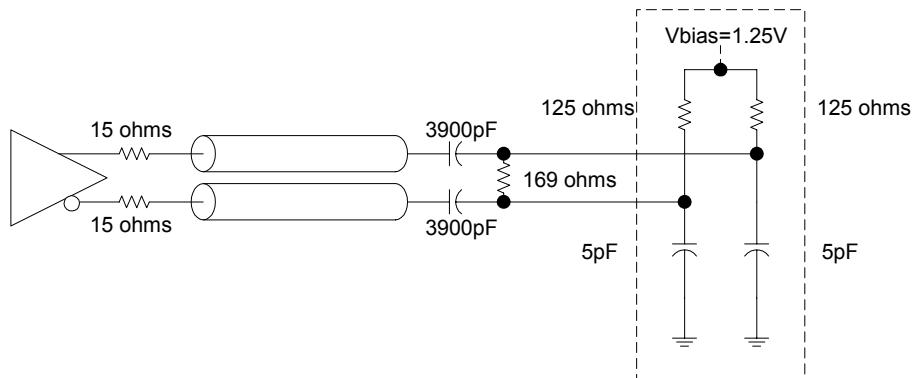
| Parameter       | Description                           | Conditions   | Skew Window | Unit |
|-----------------|---------------------------------------|--|-------------|------|
| TSK_CPU_CPU     | CPU to CPU skew, time independent     | Measured @ crossing points for CPUT rising edges1                                  | 250         | ps   |
| TSK_CPU_PCI33   | CPU to PCI33 skew, time independent   | Measured @ crossing points for CPUT rising edge and 1.5V PCI clocks                | 500         | ps   |
| TSK_PCI33_PCI33 | PCI33 to PCI33 skew, time independent | Measured between rising @ 1.5V   | 500         | ps   |
| TSK_PCI33_HT66  | PCI33 to HT66 skew, time independent  | Measured between rising @ 1.5V   | 500         | ps   |
| TSK_CPU_HT66    | CPU to HT66 skew, time independent    | Measured @ crossing points for CPUT rising edge and 1.5V for HyperTransport clocks | 500         | ps   |
| TSK_HT66_HT66   | HT66 to HT66 skew, time independent   | Measured between rising @ 1.5V   | 500         | ps   |
| TSK_CPU_CPU     | CPU to CPU skew, time variant         | Measured @ crossing points for CPUT rising edges                                   | 200         | ps   |
| TSK_CPU_PCI33   | CPU to PCI33 skew, time variant       | Measured @ crossing points for CPUT rising edge and 1.5V PCI clocks                | 200         | ps   |
| TSK_PCI33_PCI33 | PCI33 to PCI33 skew, time variant     | Measured between rising @ 1.5V   | 200         | ps   |
| TSK_PCI33_HT66  | PCI33 to HT66 skew, time variant      | Measured between rising @ 1.5V   | 200         | ps   |
| TSK_CPU_HT66    | CPU to HT66 skew, time variant        | Measured @ crossing points for CPUT rising edge and 1.5V for HyperTransport clocks | 200         | ps   |
| TSK_HT66_HT66   | HT66 to HT66 skew, time variant       | Measured between rising @ 1.5V   | 200         | ps   |

**Note:**

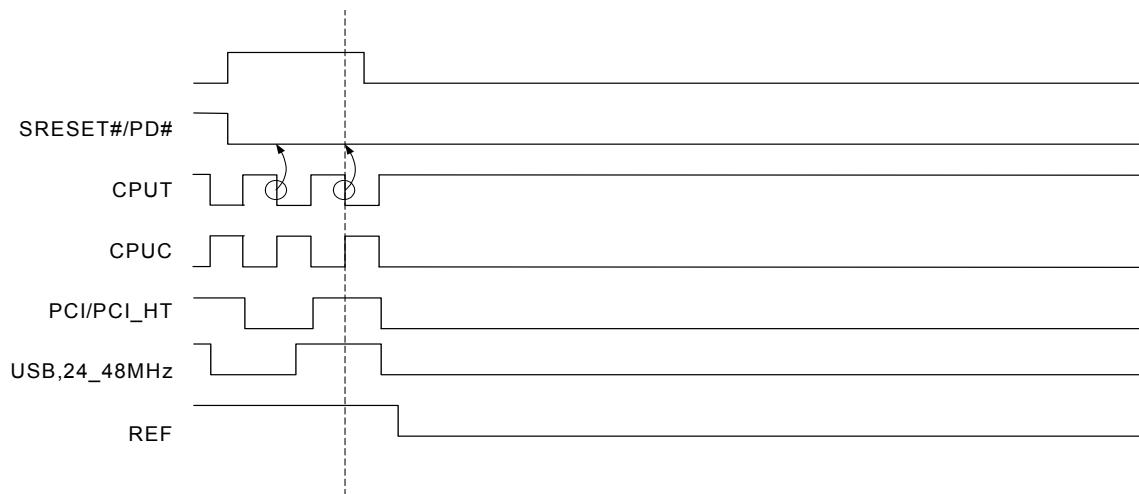
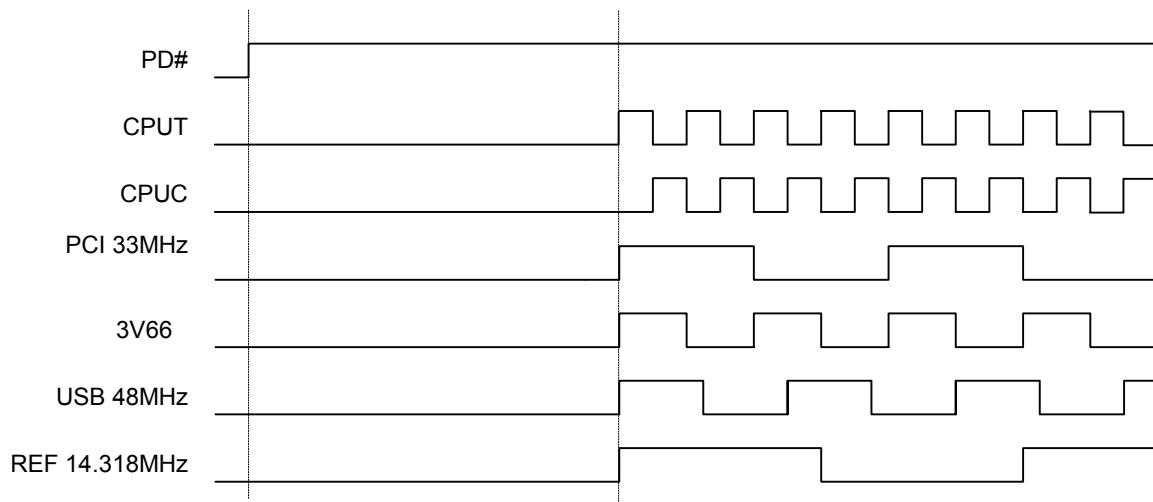
2. All skews in this skew budget are measured from the first referenced signal to the next. Therefore, this skew specifies the maximum SKEW WINDOW between these two signals to be 500 ps whether the CPU crossing leads or lags the PCI clock. This should NOT be interpreted to mean that the PCI33 edge could either be 500 ps before the CPU clock to 500 ps after the clock, thus defining a 1000ps window in which the PCI33 clock edge could fall.

**Table 7.**

| Clock Name                 | Max Load (in pF) <sup>[3]</sup> |
|----------------------------|---------------------------------|
| CPU, USB, 24_48MHz, REF    | 20                              |
| PCI33, PCI33_F, PCI33_HT66 | 30                              |


**Figure 2. PCISTOP# Assertion Waveform**

**Figure 3. PCISTOP# Deassertion Waveform**

**Figure 4. Test Load Configuration**
**Note:**

3. The above loads are positioned near each output pin when tested.

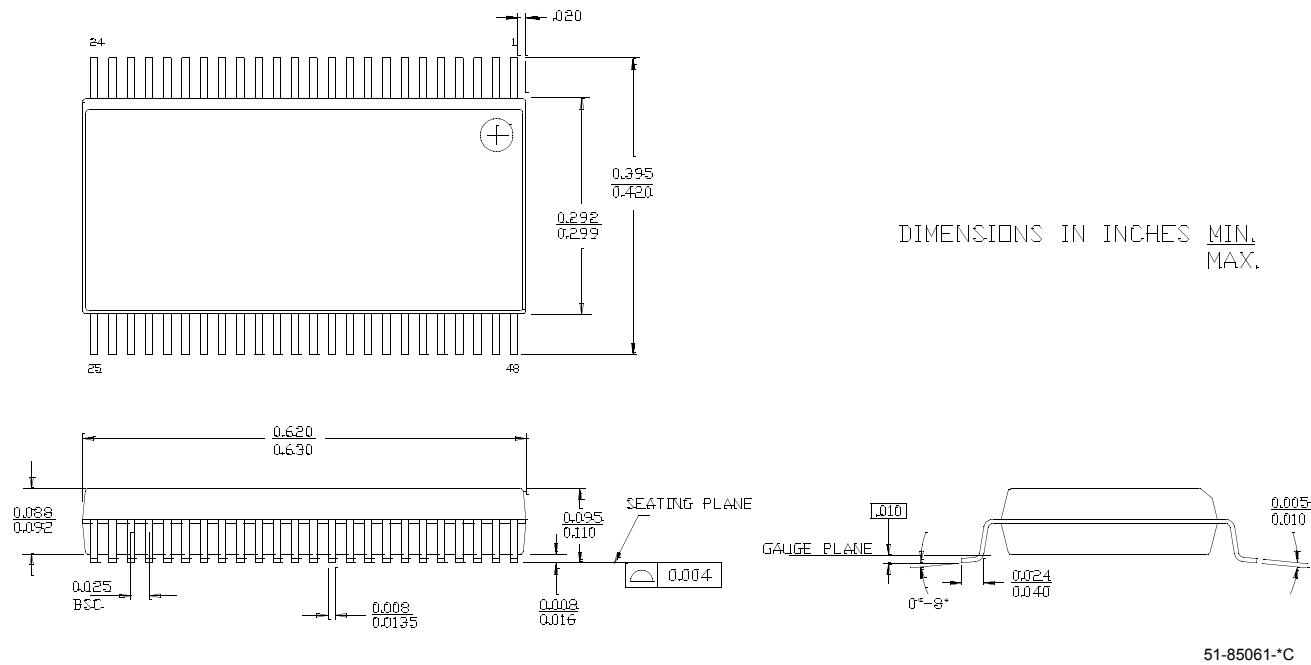

**Figure 5. PD# Assertion Waveform**

**Figure 6. PD# Deassertion Waveform**

## Ordering Information

| Part Number      | Package Type                | Product Flow           |
|------------------|-----------------------------|------------------------|
| CY28331OC        | 48-pin SSOP                 | Commercial, 0° to 70°C |
| CY28331OCT       | 48-pin SSOP – Tape and Reel | Commercial, 0° to 70°C |
| <b>Lead-free</b> |                             |                        |
| CY28331OXC       | 48-pin SSOP                 | Commercial, 0° to 70°C |
| CY28331OXCT      | 48-pin SSOP – Tape and Reel | Commercial, 0° to 70°C |

## Package Drawing and Dimensions

## 48-pin Shrunk Small Outline Package O48



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## Document History Page

| Document Title: CY28331 Clock Generator for AMD™ Hammer<br>Document Number: 38-07491 |         |            |                 |  |
|--|---------|------------|-----------------|--|
| REV.   | ECN NO. | Issue Date | Orig. of Change | Description of Change  |
| **   | 120617  | 11/11/02   | RGL             | New Data Sheet   |
| *A   | 121407  | 11/12/02   | CA              | Minor change corrected rev ** on date  |
| *B   | 125988  | 04/17/03   | RGL             | Changed the power up value of the Byte7 bit6 from 0 to 1   |
| *C   | 131420  | 12/05/03   | RGL/SDR         | Changed min. $T_R$ value for PCI/Hypertransport from 1 to 0.5 V/ns<br>Changed min. $T_F$ value for PCI/Hypertransport from 1 to 0.5 V/ns<br>Changed max. $T_{CCJ}$ value for PCI/Hypertransport from 250 to 400 ps |
| *D   | 237872  | See ECN    | RGL             | Minor Change: typo error in page one   |
| *E   | 353939  | See ECN    | RGL             | Added Lead-free devices  |