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# 2.5 V or 3.3 V, 200 MHz, 11 Output Zero Delay Buffer

## Features

- Output frequency range: 16.67 MHz to 200 MHz
- Input frequency range: 16.67 MHz to 200 MHz
- 2.5 V or 3.3 V operation
- Split 2.5 V and 3.3 V outputs
- $\pm 2\%$  maximum output duty cycle variation
- 11 clock outputs: drive up to 22 clock lines
- LVCMOS reference clock input
- 125 ps maximum output-output skew
- PLL bypass mode
- Spread Aware™
- Output enable and disable
- Pin compatible with MPC9352 and MPC952
- Industrial temperature range:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- 32-pin 1.4 mm TQFP package

## Description

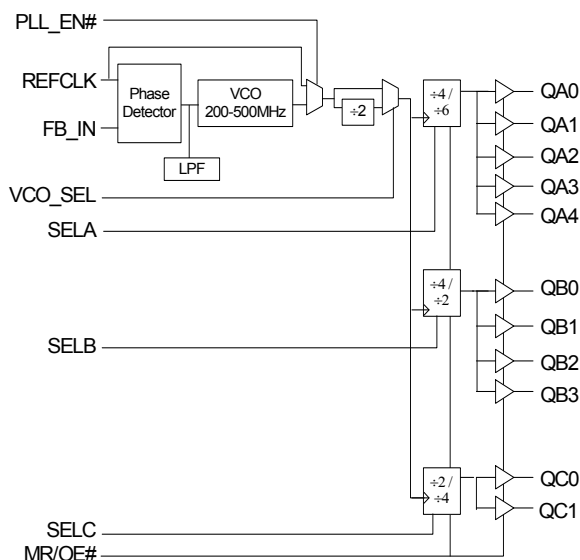
The CY29352 is a low voltage high performance 200 MHz PLL based zero delay buffer designed for high speed clock distribution applications.

The CY29352 features an LVCMOS reference clock input and provides 11 outputs partitioned in three banks of five, four, and two outputs. Bank A divides the VCO output by four and six while bank B divides by four and two, and bank C divides by two and four per SEL(A:C) settings, see [Function Table on page 4](#). These dividers allow output to input ratios of 3:1, 2:1, 3:2, 1:1, 2:3, 1:2, and 1:3. Each LVCMOS compatible output drives  $50\ \Omega$  series or parallel terminated transmission lines. For series terminated transmission lines, each output drives one or two traces, giving the device an effective fanout of 1:22.

The PLL is stable if the VCO is configured to run between 200 MHz to 500 MHz. This allows a wide range of output frequencies from 16.67 MHz to 200 MHz. For normal operation, the external feedback input, FB\_IN, is connected to one of the outputs. The internal VCO runs at multiples of the input reference clock set by the feedback divider, see [Frequency Table on page 4](#). When PLL\_EN# is HIGH, PLL is bypassed and the reference clock directly feeds the output dividers. This mode is fully static and the minimum input clock frequency specification does not apply.

For a complete list of related documentation, click [here](#).

## Block Diagram



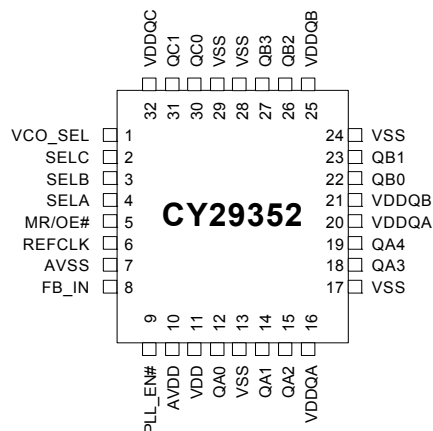
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## Pinouts

**Figure 1. 32-pin TQFP pinout**



## Pin Definitions

Pin	Name	I/O <sup>[1]</sup>	Type	Description
6	REFCLK	I, PD	LVC MOS	Reference clock input
12, 14, 15, 18, 19	QA(0:4)	O	LVC MOS	Clock output bank A
22, 23, 26, 27	QB(0:3)	O	LVC MOS	Clock output bank B
30, 31	QC(0,1)	O	LVC MOS	Clock output bank C
8	FB_IN	I, PD	LVC MOS	Feedback clock input. Connect to an output for normal operation. This input must be at the same voltage rail as input reference clock, see <a href="#">Frequency Table on page 4</a> .
1	VCO_SEL	I, PD	LVC MOS	VCO divider select input, see <a href="#">Function Table on page 4</a> .
5	MR/OE#	I, PD	LVC MOS	Master reset or output enable and disable input, see <a href="#">Function Table on page 4</a> .
9	PLL_EN#	I, PD	LVC MOS	PLL enable and disable input, see <a href="#">Function Table on page 4</a> .
2, 3, 4	SEL(A:C)	I, PD	LVC MOS	Frequency select input, bank (A:C), see <a href="#">Function Table on page 4</a> .
16, 20	V <sub>DDQA</sub>	Supply	V <sub>DD</sub>	2.5 V or 3.3 V power supply for bank A output clocks <sup>[2, 3]</sup>
21, 25	V <sub>DDQB</sub>	Supply	V <sub>DD</sub>	2.5 V or 3.3 V power supply for bank B output clocks <sup>[2, 3]</sup>
32	V <sub>DDQC</sub>	Supply	V <sub>DD</sub>	2.5 V or 3.3 V power supply for bank C output clocks <sup>[2, 3]</sup>
10	AV <sub>DD</sub>	Supply	V <sub>DD</sub>	2.5 V or 3.3 V power supply for PLL <sup>[2, 3]</sup>
11	V <sub>DD</sub>	Supply	V <sub>DD</sub>	2.5 V or 3.3 V power supply for core and inputs <sup>[2, 3]</sup>
7	AV <sub>SS</sub>	Supply	Ground	Analog ground
13, 17, 24, 28, 29	V <sub>SS</sub>	Supply	Ground	Common ground

### Notes

1. PD = Internal pull down.
2. A 0.1-μF bypass capacitor must be placed as close as possible to each positive power pin (< 0.2"). If these bypass capacitors are not close to the pins, the high frequency filtering characteristics are cancelled by the lead inductance of the traces.
3. AV<sub>DD</sub> and V<sub>DD</sub> pins must be connected to a power supply level that is at least equal or higher than that of V<sub>DDQA</sub>, V<sub>DDQB</sub>, and V<sub>DDQC</sub> power supply pins.

## Frequency Table

VCO_SEL	Feedback Output Divider	VCO	Input Frequency Range (AVDD = 3.3 V)	Input Frequency Range (AVDD = 2.5 V)
0	÷2	Input clock * 2	100 MHz to 200 MHz	100 MHz to 200 MHz
0	÷4	Input clock * 4	50 MHz to 125 MHz	50 MHz to 100 MHz
0	÷6	Input clock * 6	33.33 MHz to 83.33 MHz	33.33 MHz to 66.67 MHz
1	÷2	Input clock * 4	50 MHz to 125 MHz	50 MHz to 100 MHz
1	÷4	Input clock * 8	25 MHz to 62.5 MHz	25 MHz to 50 MHz
1	÷6	Input clock * 12	16.67 MHz to 41.67 MHz	16.67 MHz to 33.33 MHz

## Function Table

Control	Default	0	1
VCO_SEL	0	VCO	VCO ÷ 2
PLL_EN#	0	PLL enabled, the VCO output connects to the output dividers	Bypass mode, PLL disabled, the input clock connects to the output dividers
MR/OE#	0	Outputs enabled	Outputs disabled (three-state), VCO runs at its minimum frequency
SELA	0	QA = VCO ÷ 4	QA = VCO ÷ 6
SELB	0	QB = VCO ÷ 4	QB = VCO ÷ 2
SELC	0	QC = VCO ÷ 2	QC = VCO ÷ 4

## Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V <sub>DD</sub>	DC supply voltage		−0.3	5.5	V
V <sub>DD</sub>	DC operating voltage	Functional	2.375	3.465	V
V <sub>IN</sub>	DC input voltage	Relative to V <sub>SS</sub>	−0.3	V <sub>DD</sub> + 0.3	V
V <sub>OUT</sub>	DC output voltage	Relative to V <sub>SS</sub>	−0.3	V <sub>DD</sub> + 0.3	V
V <sub>TT</sub>	Output termination voltage		−	V <sub>DD</sub> ÷ 2	V
LU	Latch up immunity	Functional	200	−	mA
R <sub>PS</sub>	Power supply ripple	Ripple frequency < 100 kHz	−	150	mVp-p
T <sub>S</sub>	Temperature, storage	Non functional	−65	+150	°C
T <sub>A</sub>	Temperature, operating ambient	Functional	−40	+85	°C
T <sub>J</sub>	Temperature, junction	Functional	−	155	°C
Θ <sub>JC</sub>	Dissipation, junction to case	Functional	−	42	°C/W
Θ <sub>JA</sub>	Dissipation, junction to ambient	Functional	−	105	°C/W
ESD <sub>H</sub>	ESD protection (human body model)		2000	−	V
FIT	Failure in time	Manufacturing test	10		ppm

## DC Parameters

(V<sub>DD</sub> = 2.5 V ± 5%, T<sub>A</sub> = −40 °C to +85 °C)

Parameter	Description	Condition	Min	Typ	Max	Unit
V <sub>IL</sub>	Input voltage, low	LVC MOS	−	−	0.7	V
V <sub>IH</sub>	Input voltage, high	LVC MOS	1.7	−	V <sub>DD</sub> + 0.3	V
V <sub>OL</sub>	Output voltage, low <sup>[4]</sup>	I <sub>OL</sub> = 15 mA		−	0.6	V
V <sub>OH</sub>	Output voltage, high <sup>[4]</sup>	I <sub>OH</sub> = −15 mA	1.8	−		V
I <sub>IL</sub>	Input current, low	V <sub>IL</sub> = V <sub>SS</sub>	−	−	−10	μA
I <sub>IH</sub>	Input current, high <sup>[5]</sup>	V <sub>IL</sub> = V <sub>DD</sub>	−	−	100	μA
I <sub>DDA</sub>	PLL supply current	AV <sub>DD</sub> only	−	5	10	mA
I <sub>DDQ</sub>	Quiescent supply current	All V <sub>DD</sub> pins except AV <sub>DD</sub>	−	3	5	mA
I <sub>DD</sub>	Dynamic supply current		−	170		mA
C <sub>IN</sub>	Input pin capacitance		−	4		pF
Z <sub>OUT</sub>	Output impedance		−	17–20		Ω

### Notes

- Driving one 50 Ω parallel terminated transmission line to a termination voltage of V<sub>TT</sub>. Alternatively, each output drives up to two 50 Ω series terminated transmission lines.
- Inputs have pull down resistors that affect the input current.

## DC Parameters

( $V_{DD} = 3.3 \text{ V} \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Description	Condition	Min	Typ	Max	Unit
$V_{IL}$	Input voltage, low	LVC MOS	–	–	0.8	V
$V_{IH}$	Input voltage, high	LVC MOS	2.0	–	$V_{DD} + 0.3$	V
$V_{OL}$	Output voltage, low <sup>[6]</sup>	$I_{OL} = 24 \text{ mA}$	–	–	0.55	V
		$I_{OL} = 12 \text{ mA}$	–	–	0.30	
$V_{OH}$	Output voltage, high <sup>[6]</sup>	$I_{OH} = -24 \text{ mA}$	2.4	–	–	V
$I_{IL}$	Input current, low	$V_{IL} = V_{SS}$	–	–	–10	$\mu\text{A}$
$I_{IH}$	Input current, high <sup>[7]</sup>	$V_{IL} = V_{DD}$	–	–	100	$\mu\text{A}$
$I_{DDA}$	PLL supply current	$AV_{DD}$ only	–	5	10	mA
$V_{IL}$	Input voltage, low	LVC MOS	–	–	0.8	V
$V_{IH}$	Input voltage, high	LVC MOS	2.0	–	$V_{DD} + 0.3$	V
$V_{OL}$	Output voltage, low <sup>[6]</sup>	$I_{OL} = 24 \text{ mA}$	–	–	0.55	V
		$I_{OL} = 12 \text{ mA}$	–	–	0.30	
$V_{OH}$	Output voltage, high <sup>[6]</sup>	$I_{OH} = -24 \text{ mA}$	2.4	–	–	V
$I_{IL}$	Input current, low	$V_{IL} = V_{SS}$	–	–	–10	$\mu\text{A}$
$I_{IH}$	Input current, high <sup>[7]</sup>	$V_{IL} = V_{DD}$	–	–	100	$\mu\text{A}$
$I_{DDA}$	PLL supply current	$AV_{DD}$ only	–	5	10	mA
$I_{DDQ}$	Quiescent supply current	All $V_{DD}$ pins except $AV_{DD}$	–	3	5	mA
$I_{DD}$	Dynamic supply current		–	240	–	mA
$C_{IN}$	Input pin capacitance		–	4	–	pF
$Z_{OUT}$	Output impedance		–	14–17	–	$\Omega$

### Notes

- Driving one 50  $\Omega$  parallel terminated transmission line to a termination voltage of  $V_{TT}$ . Alternatively, each output drives up to two 50  $\Omega$  series terminated transmission lines.
- Inputs have pull down resistors that affect the input current.

## AC Parameters

( $V_{DD} = 2.5 \text{ V} \pm 5\%$ ,  $T_A = -40 \text{ }^{\circ}\text{C}$  to  $+85 \text{ }^{\circ}\text{C}$ )

Parameter <sup>[8]</sup>	Description	Condition	Min	Typ	Max	Unit
$f_{VCO}$	VCO frequency		200	—	400	MHz
$f_{in}$	Input frequency	$\div 2$ feedback	100	—	200	MHz
		$\div 4$ feedback	50	—	100	
		$\div 6$ feedback	33.33	—	66.67	
		$\div 8$ feedback	25	—	50	
		$\div 12$ feedback	16.67	—	33.33	
		Bypass mode (PLL_EN# = 1)	0	—	200	
$f_{refDC}$	Input duty cycle		25	—	75	%
$t_r, t_f$	TCLK input rise and fall time	0.7 V to 1.7 V	—	—	1.0	ns
$f_{MAX}$	Maximum output frequency	$\div 2$ output	100	—	200	MHz
		$\div 4$ output	50	—	100	
		$\div 6$ output	33.33	—	66.67	
		$\div 8$ output	25	—	50	
		$\div 12$ output	16.67	—	33.33	
DC	Output duty cycle	$f_{MAX} < 100 \text{ MHz}$	47	—	53	%
		$f_{MAX} > 100 \text{ MHz}$	44	—	56	
$t_r, t_f$	Output rise and fall times	0.6 V to 1.8 V	0.1	—	1.0	ns
$t_{(\phi)}$	Propagation delay (static phase offset)	TCLK to FB_IN, same $V_{DD}$ , does not include jitter	–100	—	100	ps
$t_{sk(O)}$	Output to output skew	Skew within bank	—	—	125	ps
$t_{sk(B)}$	Bank to bank skew	Banks at same voltage, same frequency	—	—	175	ps
		Banks at same voltage, different frequency	—	—	225	
$t_{PLZ, HZ}$	Output disable time		—	—	8	ns
$t_{PZL, ZH}$	Output enable time		—	—	10	ns
BW	PLL closed loop bandwidth (–3 dB)	$\div 2$ feedback	—	2	—	MHz
		$\div 4$ feedback	—	1–1.5	—	
		$\div 6$ feedback	—	0.6	—	
		$\div 8$ feedback	—	0.75	—	
		$\div 12$ feedback	—	0.5	—	
$t_{JIT(CC)}$	Cycle to cycle jitter	Same frequency	—	—	100	ps
		Multiple frequencies	—	—	300	
$t_{JIT(PER)}$	Period jitter	Same frequency	—	—	100	ps
		Multiple frequencies	—	—	150	
$t_{JIT(\phi)}$	IO phase jitter	VCO < 300 MHz	—	150	—	ps
		VCO > 300 MHz	—	100	—	
$t_{LOCK}$	Maximum PLL lock time		—	—	1	ms

### Note

8. AC characteristics apply for parallel output termination of  $50 \text{ } \Omega$  to  $V_{TT}$ . Outputs are at the same supply voltage unless otherwise stated. Parameters are guaranteed by characterization and are not 100% tested.



## AC Parameters

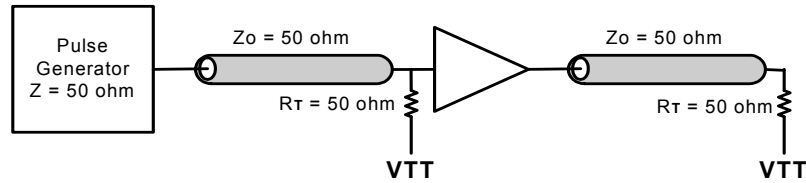
( $V_{DD} = 3.3 \text{ V} \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter <sup>[9]</sup>	Description	Condition	Min	Typ	Max	Unit
$f_{VCO}$	VCO frequency		200	—	500	MHz
$f_{in}$	Input frequency	$\div 2$ feedback	100	—	200	MHz
		$\div 4$ feedback	50	—	125	
		$\div 6$ feedback	33.33	—	83.33	
		$\div 8$ feedback	25	—	62.5	
		$\div 12$ feedback	16.67	—	41.67	
		Bypass mode (PLL_EN# = 1)	0	—	200	
$f_{refDC}$	Input duty cycle		25	—	75	%
$t_r, t_f$	TCLK input rise and fall time	0.8 V to 2.0 V	—	—	1.0	ns
$f_{MAX}$	Maximum output frequency	$\div 2$ output	100	—	200	MHz
		$\div 4$ output	50	—	125	
		$\div 6$ output	33.33	—	83.33	
		$\div 8$ output	25	—	62.5	
		$\div 12$ output	16.67	—	41.67	
DC	Output duty cycle	$f_{MAX} < 100 \text{ MHz}$	48	—	52	%
			—	—	—	
$t_{(\phi)}$	Propagation delay (static phase offset)	TCLK to FB_IN, same $V_{DD}$ , does not include jitter	–100	—	200	ps
$t_{sk(O)}$	Output to output skew	Skew within each Bank	—	—	125	ps
$t_{sk(B)}$	Bank to bank skew	Banks at same voltage, same frequency	—	—	175	ps
		Banks at same voltage, different frequency	—	—	235	
		Banks at different voltage	—	—	425	
$t_{PLZ, HZ}$	Output disable time		—	—	8	ns
$t_{PZL, ZH}$	Output enable time		—	—	10	ns
BW	PLL closed loop bandwidth (–3 dB)	$\div 2$ feedback	—	2	—	MHz
		$\div 4$ feedback	—	1–1.5	—	
		$\div 6$ feedback	—	0.6	—	
		$\div 8$ feedback	—	0.75	—	
		$\div 12$ feedback	—	0.5	—	
$t_{JIT(CC)}$	Cycle to cycle jitter	Same frequency	—	—	100	ps
		Multiple frequencies	—	—	275	
$t_{JIT(PER)}$	Period jitter	Same frequency	—	—	100	ps
		Multiple frequencies	—	—	150	
$t_{JIT(\phi)}$	IO phase jitter	VCO < 300 MHz	—	150	—	ps
		VCO > 300 MHz	—	100	—	
$t_{LOCK}$	Maximum PLL lock time		—	—	1	ms

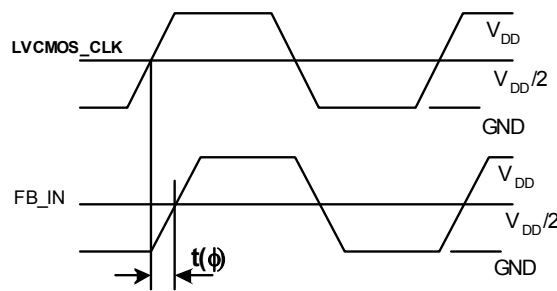
### Note

9. AC characteristics apply for parallel output termination of  $50 \Omega$  to  $V_{TT}$ . Outputs are at the same supply voltage unless otherwise stated. Parameters are guaranteed by characterization and are not 100% tested.

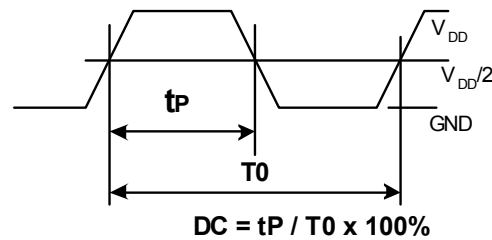
**Figure 2. AC Test Reference for  $V_{DD} = 3.3\text{ V} / 2.5\text{ V}$**



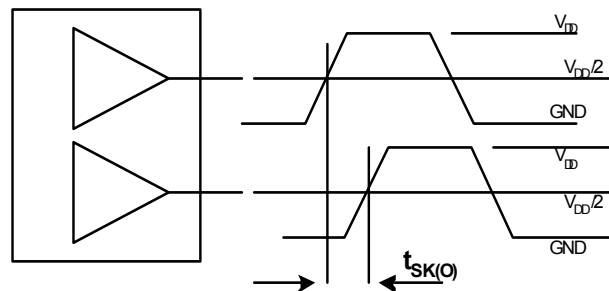
**Figure 3. Propagation Delay  $t(\phi)$ , Static Phase Offset**



**Figure 4. Output Duty Cycle (DC)**



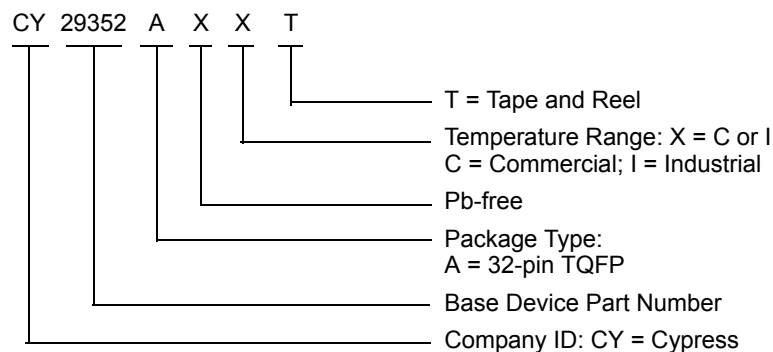
**Figure 5. Output to Output Skew,  $t_{sk(O)}$**



## Ordering Information

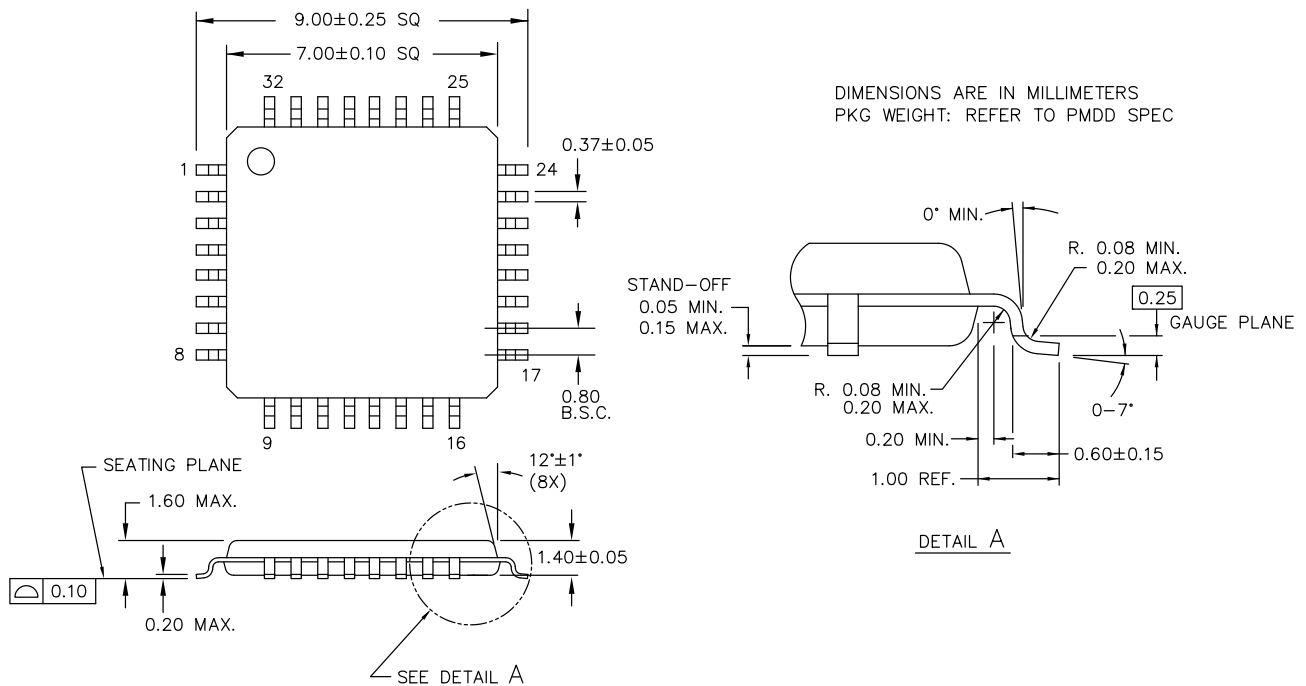
Part Number	Package Type	Product Flow
<b>Pb-free</b>		
CY29352AXI	32-pin TQFP	Industrial, -40 °C to +85 °C
CY29352AXIT	32-pin TQFP – Tape and Reel	Industrial, -40 °C to 85 °C

## Ordering Code Definitions



## Package Drawing and Dimension

**Figure 6. 32-pin TQFP (7 × 7 × 1.4 mm) Package Outline, 51-85088**



51-85088 \*E

## Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	electrostatic discharge
I/O	Input/Output
LVC MOS	Low Voltage Complementary Metal Oxide Semiconductor
LV TTL	Low Voltage Transistor-Transistor Logic
PLL	Phase Locked Loop
TQFP	Thin Quad Flat Pack
VCO	Voltage-Controlled Oscillator

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
kHz	kilohertz
kV	kilovolt
MHz	megahertz
μA	microampere
mA	milliampere
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
ppm	parts per million
%	percent
pF	picofarad
ps	picosecond
V	volt
W	watt



## Document History Page

Document Title: CY29352, 2.5 V or 3.3 V, 200 MHz, 11 Output Zero Delay Buffer Document Number: 38-07476				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	124654	03/21/03	RGL	New Data Sheet
*A	739798	See ECN	RGL	Removed the leaded parts and replaced by lead-free parts
*B	1923227	See ECN	PYG / KVM / AESA	Corrected package thickness from 1.0 mm to 1.4 mm in Features section on page 1 and in Figure 5.
*C	3163592	02/05/2011	CXQ	Added <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Drawing and Dimension</a> . Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Updated in new template.
*D	4311272	03/17/2014	CINM	Updated <a href="#">Package Drawing and Dimension</a> : spec 51-85088 – Changed revision from *C to *E.  Updated in new template.  Completing Sunset Review.
*E	4587350	12/05/2014	AJU	Added related documentation hyperlink in page 1.

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