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CY29430

High-Performance Clock Synthesizer

Features

- Low-noise PLL for high-performance clock applications
- Differential Clock Output: Four frequencies selectable, reconfigurable by I^2C
- Output frequency support from 15 MHz to 2.1 GHz
- Fractional N PLL with fully integrated VCO
- Works on third overtone (OT3) of a fixed frequency crystal, Low frequency fundamental (LFF), High frequency fundamental (HFF) mode crystal and Low Frequency Input
- LVPECL, CML, HCSL, LVDS or LVCMOS output standards available
- Compatible with 3.3 V, 2.5 V, and 1.8 V supply
- 150 fs typical integrated jitter performance (12 kHz to 20 MHz frequency offsets) for output greater than 150 MHz
- VCXO functionality provided with tunable Total Pull Range (TPR) from +/- 50 ppm to +/- 275 ppm
- 16 pin QFN package: 3 × 3 × 0.6 mm

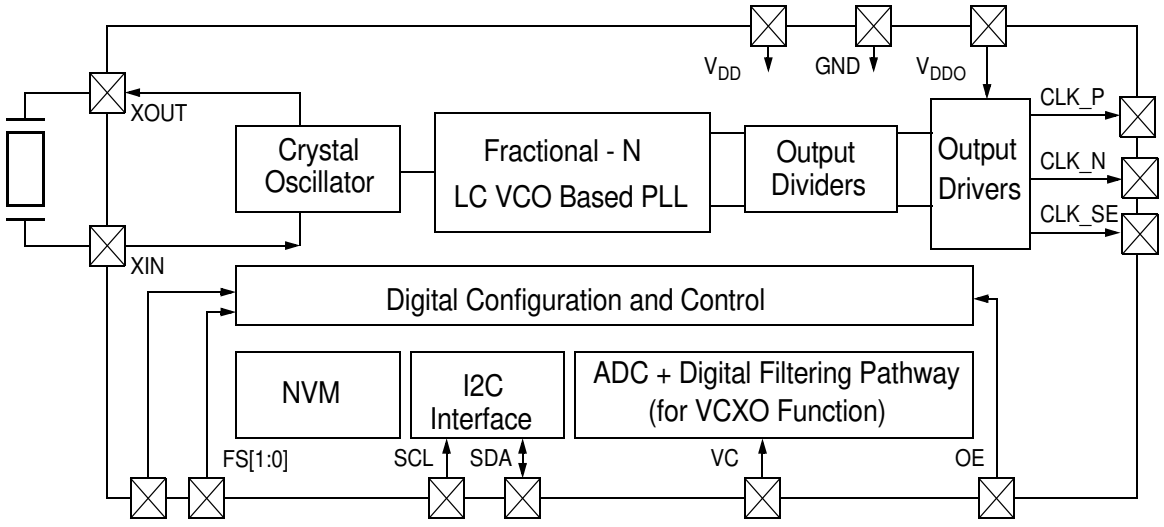
Functional Description

The CY29430 is a Programmable PLL based crystal oscillator solution with flexible output frequency options. It is field and factory programmable for any output frequency between 15 MHz and 2.1 GHz. Four frequencies are independently programmable on the differential output with the frequency select (FS) pins. Additionally, other frequency options can be configured with the I^2C interface. Using advanced design technology, it provides excellent jitter performance across the entire output frequency range working reliably at supply voltages from 1.8 V to 3.3 V for ambient temperatures from –40 °C to +105 °C. This makes it ideally suited for communications applications (for example, OTN, SONET/SDH, xDSL, GbE, Networking, Wireless Infrastructure), test and instrumentation applications, and high speed data converters. Additionally, the VCXO function enables the use of CY29430 in applications requiring a clock source with voltage control and in discrete clocking solutions for synchronous timing applications.

The CY29430 device configuration can be created using ClockWizard 2.1. For programming support, contact Cypress technical support or send an email to clocks@cypress.com.

For a complete list of related documentation, click here.

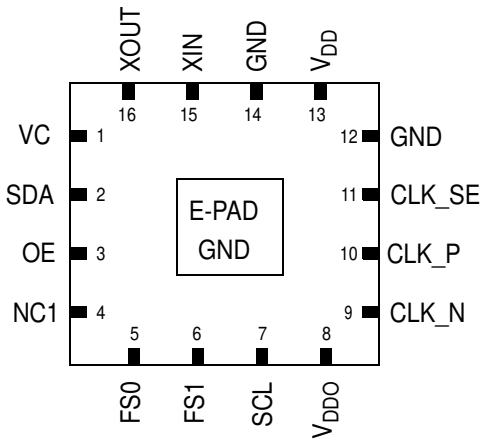
Logic Block Diagram



Contents

Pin Diagram

CY29430 PINOUT



Pin Description

Name	Pin Number	Description
VC[1]	1	Input Voltage for VCXO
SDA	2	Serial Data input/output for I^2C
OE	3	Output Enable input
NC1	4	No Connect
FS0	5	Frequency Select-0 (100 kΩ pull-down)
FS1	6	Frequency Select-1 (100 kΩ pull-down)
SCL	7	Serial Clock input for I^2C
V_{DDO}	8	Power supply for output Driver
CLK_N[2]	9	Complementary Clock Output
CLK_P[2]	10	True Clock Output
CLK_SE[2]	11	(Optional) LVCMOS clock output
GND	12	Supply Ground for Output Driver
V_{DD}	13	Power supply for core
GND	14	Supply ground
XIN	15	Crystal or Clock reference input
XOUT	16	Crystal reference output, leave floating in case clock input for XIN
E-PAD		Exposed Pad. Must be connected to ground

Note
1. If VC is unused, do not leave it floating; connect it to VDD or GND.
2. CLK_SE and (CLK_P, CLK_N) will not be available at the same time. VDD should be equal VDDO.

Functional Overview

Programmable Features

Table 1. Programmable Features

Feature	Description
Frequency Tuning	Frequency for the PLL
	Oscillator tuning (load capacitance values)
Function	OE Polarity
Power Supply	V_{DD} (1.8, 2.5 or 3.3 V)
VCXO	Enable/Disable VCXO
	Kv Polarity
	Total Pull Range
	Modulation Bandwidth
Output	Output Standard (LVPECL, LVDS, HCSL, CML or LVCMOS)
Function	I^2C address
	4 Frequency Configurations
Reference	Crystal (HFF, OT3, LFF) or Clock input

Architecture Overview

The CY29430 is a high-performance programmable PLL crystal oscillator supporting multiple functions and multiple output standards. The device has internal one-time programmable (OTP) nonvolatile memory (NVM) that can be partitioned into Common Device Configurations and Output frequency-related Information (see Figure 2). The Common Device Configurations do not change with output frequency and consist of chip power supply, OE polarity, I^2C device address, input reference, output standards, and VCXO. The device also contains volatile memory that stores an exact copy of the NVM at the release of reset on Power ON. The Chip settings depend on the contents of the volatile memory and the output frequency depends on the configurations, as explained in Figure 1. The volatile memory can be accessed through the I^2C bus and modified.

Figure 1. Conceptual Memory Structure

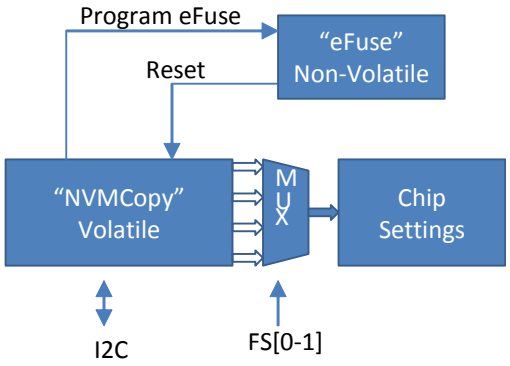
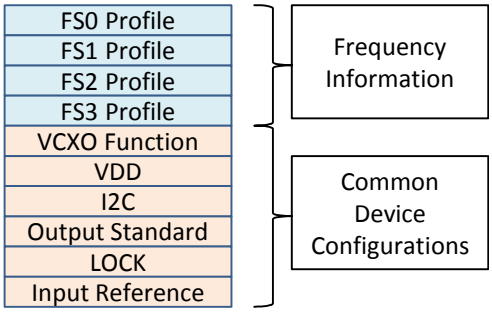


Figure 2. Memory structure for configurations



Description of Settings for the Memory Structure

- Profile[FS0-3]: Frequency information
- VCXO Function: VCXO enable/disable, TPR, modulation bandwidth and Kv (Slope for VC vs. Frequency) information
- V_{DD}: 1.8-/2.5-/3.3V range information
- I^2C: enable/disable, I^2C address information
- Output Standards: LVPECL, LVDS, CML, HCSL or LVCMOS
- LOCK pattern: 2-bit pattern to indicate eFuse lock
- Input Reference: Crystal (OT3, HFF, LFF) or Clock

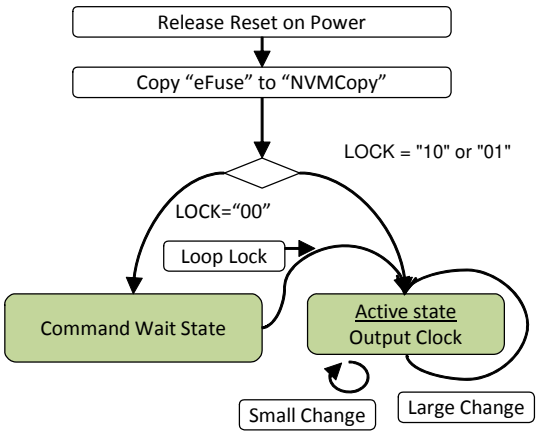
Internal State Diagram

The CY29430 contains a state machine which controls the device behavior. The state machine loads the “eFuse” contents to “NVMCopy” after reset as indicated in Figure 3. The state machine enters one of the following states: “Command Wait state” or “Active state” according to the value of LOCK. In the “Command Wait state” state, user may access all the registers and read/write the “NVMCopy” contents. The following commands can be used in the “Command Wait state”:

- Program eFuse
  - Selectively Program eFuse
- Copy eFuse to NVMCopy
- Copy NVMCopy to NVMRegister
- Loop Lock

User may test the device functionality by issuing “Loop Lock” command to enter the “Active state” without programming the LOCK. The device will function according to the settings.

Figure 3. State Diagrams



When the LOCK is programmed to "10" or "01" the device goes into the “Active state” and output clock is available after the completion of the power ON cycle.

In the “Active state”, user may change the output frequency by applying “Small Change” or “Large Change” commands.

Small/Large Changes

Small change refers to the case where the frequency is changing within ±500 ppm. The frequency information will be loaded through I^2C and the output frequency will change without any glitch from its original frequency to the new frequency. Note. the small change functionality is not supported in the Integer mode PLL. For more information, see AC Electrical Specifications for LVPECL, LVDS, CML Outputs.

Large change refers to the case where the frequency is changing more than ±500 ppm and is done through an I^2C or FS state change. The device will recalibrate and reconfigure the PLL and the output will be unstable until this process is completed.

Programming Support

The CY29430 is a software-configurable solution in which Cypress provides a Programming Specification that defines all necessary configuration bits. This information is used by the customer to develop programming software for use with their programmer hardware.

Frequency Configurations

The FS[0-3] setting is done based on the logic levels on the FS0 and FS1 pins as indicated in the Table 5 on page 6. The Frequency Configuration consists of the desired output frequency corresponding to each of the FS[0–3] setting. The Fractional-N PLL is loaded with values required to generate the frequency for each of these settings based on the input crystal frequency. The Frequency configuration for FS[0–3] is provided in Table 3.

Programmable OE Polarity

The CY29430 contains a bit for OE polarity setting (default is active-low). User can choose active-high or active-low polarity for the OE function. The output will be disabled when OE is deasserted

Programmable VCXO

The device incorporates a proprietary technique for modulating frequency by modifying VCO frequency according to the VC control voltage. The pull profile is linear and accurate comparing with pulling the OT3/HFF reference. Also, the VCXO characteristics are very stable and do not vary over temperature, supply voltage or process variations.

Kv (Slope for frequency vs. VC), TPR VC bandwidth and VCXO on/off are all programmable.Note. the VCXO functionality is not supported in the Integer mode PLL.

Power Supply Sequencing

The CY29430 does not require any specific sequencing for startup. Startup requires a monotonic V_{DD} ramp specified in the datasheet. After the ramp up, V_{DD} has to be maintained within the limits specified for it in the Recommended Operating Conditions. Brownout detection and protection has to be implemented elsewhere in the system.

Other input signals, VC, FS0 or FS1, can power up earlier or later than V_{DD}, there are no timing requirement for those input signals with reference to V_{DD}. The device will operate normally when all of the input signals are settled in the configured state.

If a TCXO or external clock is fed into the XIN/XOUT inputs, a stable input has to be present before start of the V_{DD} ramp up to the specified level. This is because the on-chip frequency calibration process starts at Power ON and requires a stable reference input to be available at the start of the process.

I^2C Interface

The CY29430 supports two-wire serial interface and I^2C in Fast Mode (400 kbits/s) and 7-bit addressing. The device address is programmable and is 55h by default. It supports single-byte access only. The first I^2C access to the device has to be 5 ms (minimum) after VDD reaches its minimum specified voltage.

Memory Map

Table 2. Common Configurations

Memory Address	Description
50h–57h	Device configurations

Table 3. FS[0-3]: Frequency Configurations

Memory Address	Description
10h, 20h, 30h, 40h	DIVO
11h, 21h, 31h, 41h	DIVO, DIVN_INT
12h, 22h, 32h, 42h	ICP,DIVN_INT, PLL_MODE
13h, 23h, 33h, 43h	DIVN_FRAC_L
14h, 24h, 34h, 44h	DIVN_FRAC_M
15h, 25h, 35h, 45h	DIVN_FRAC_H
1xh = FS0, 2xh = FS1, 3xh = FS2, 4xh = FS3	–

Table 4. Miscellaneous Information

Memory Address	Description
00h (Read only)	Device ID (= 51h)
D4h–D6h	User configurable information

The user must write all the contents created by the Configuration tool. Partial updates to the device is not allowed.

Access to locations other than those described here may cause fatal error in device operation.

Table 5. FS Setting

FS1	FS0	FS Setting
0	0	FS0
0	1	FS1
1	0	FS2
1	1	FS3

Absolute Maximum Ratings

Exceeding maximum ratings [3] may shorten the useful life of the device. User guidelines are not tested.

Supply voltage to ground potential .....–0.5 V to + 3.8 V
Input voltage .....–0.5 V to + 3.8 V
Storage temperature (non-condensing) ... –55 °C to +150 °C
Junction temperature ..... –40 °C to +125 °C
Programming temperature ..... 0 °C to +125 °C
Programming voltage .....2.5 V ± 0.1 V
Supply Current for eFuse Programming ..... 50 mA
Data retention at T_J = 125 °C .....> 10 years
Maximum programming cycles 1
ESD HBM (JEDEC JS-001-2012) ..... 2000 V
ESD MM (JEDEC JESD22-A115B) ..... 200 V
ESD CDM (JEDEC JESD22-C101E) 500V
Latch up current ..... ±140 mA

Recommended Operating Conditions

Parameter	Description	Min	Max	Unit
V_{DD}, V_{DDO}	Supply voltage, 1.8 V operating range, 1.8 V ± 5%	1.71	1.89	V
	Supply voltage, 2.5 V operating range, 2.5 V ± 10%	2.25	2.75	
	Supply voltage, 3.3 V operating range, 3.3 V ± 10%	2.97	3.63	
T_A	Ambient temperature	–40	+105	°C
f_{RES}	Frequency resolution	–	2	ppb
$T_{PLLHOLD}$	PLL Hold Temperature Range	–	125	°C

DC Electrical Specifications

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
I_{DD}[4]	Supply current, LVPECL	V_{DD} = 3.3 V/2.5 V, 50 Ω to V_{TT} (V_{DDO} – 2.0 V), with common mode current	–	93	106	mA
	Supply current, LVPECL	V_{DD} = 3.3 V/2.5 V, 50 Ω to V_{TT} (V_{DDO} – 2.0 V), without common mode current[5]	–	81	94	
	Supply current, LVDS	V_{DD} = 3.3 V/2.5 V/1.8 V, 100 Ω between CLKP and CLKN	–	69	81	
	Supply current, HCSL	V_{DD} = 3.3 V/2.5 V/1.8 V, 33 Ω and 49.9 Ω to GND	–	80	93	
	Supply current, CML	V_{DD} = 3.3 V/2.5 V/1.8 V, 50 Ω to V_{DDO}	–	73	86	
	Supply current, CMOS	V_{DD} = 3.3 V/2.5 V/1.8 V, 0-pF load, 33.33 MHz	–	58	70	
	Supply current, CMOS	V_{DD} = 3.3 V/2.5 V/1.8 V, 10-pF load, 33.33 MHz	–	66	78	
	Supply current, PLL only	V_{DD} = 3.3 V/2.5 V/1.8 V	–	59	70	
I_{IH}	Input high current	Logic input, Input = V_{DD}	–	30	50	µA
I_{IL}	Input low current	Logic input, Input = GND	–	30	50	µA
V_{IH}[6]	Input high voltage	OE, FS, SCL, SDA logic level = 1	0.7 × V_{DD}	–	–	V
V_{IL}[6]	Input low voltage	OE, FS, SCL, SDA logic level = 0	–	–	0.3 × V_{DD}	V
V_{IN}	Input voltage level	All input, relative to GND	–0.5	–	3.8	V
R_P	Internal pull-up resistance	OE, configured active High	–	200	–	kΩ
R_D	Internal pull-down resistance	OE, configured active Low	–	200	–	kΩ
		FS0, FS1 pins	–	100	–	kΩ

Notes
3. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or at any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability or cause permanent device damage.
4. I_{DD} is the total supply current and is measured with V_{DD} and V_{DDO} shorted together.
5. In ClockWizard 2.1, setting the output standard to LVPECL2 configures the output to "LVPECL without common mode current". Refer to AN210253 for LVPECL terminations for different use case configurations.
6. I^2C operation applicable for V_{DD} of 1.8 V and 2.5 V only.

DC Specifications for LVDS Output

(V_{DDO} = 1.8-V, 2.5-V, or 3.3-V range)

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OCM}[7]	Output common-mode voltage	V_{DDO} = 2.5-V or 3.3-V range	1.125	1.200	1.375	V
ΔV_{OCM}	Change in V_{OCM} between complementary output states	–	–	–	50	mV
I_{OZ}	Output leakage current	Output off, V_{OUT} = 0.75 V to 1.75 V	–20	–	20	µA

DC Specifications for LVPECL Output

(V_{DDO} = 2.5-V or 3.3-V range, with common mode current)

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OH}	Output high voltage	R-term = 50 Ω to V_{TT} (V_{DDO} – 2.0 V)	V_{DDO} – 1.165	–	V_{DDO} – 0.800	V
V_{OL}	Output low voltage	R-term = 50 Ω to V_{TT} (V_{DDO} – 2.0 V)	V_{DDO} – 2.0	–	V_{DDO} – 1.55	V

DC Specifications For CML Output

(V_{DDO} = 1.8-V, 2.5-V, or 3.3-V range)

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OH}	Output high voltage	R-term = 50 Ω to V_{DDO}	V_{DDO} – 0.085	V_{DDO} – 0.01	V_{DDO}	V
V_{OL}	Output low voltage	R-term = 50 Ω to V_{DDO}	V_{DDO} – 0.6	V_{DDO} – 0.4	V_{DDO} – 0.32	V

DC Specifications for HCSL Output

(V_{DDO} = 1.8-V, 2.5-V or 3.3-V range)

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{MAX}[8]	Max output high voltage	Measurement taken from single-ended waveform	–	–	1150	mV
V_{MIN}[8]	Min output low voltage	Measurement taken from single-ended waveform	–300	–	–	mV
V_{OHDIFF}	Differential output high voltage	Measurement taken from differential waveform	150	–	–	mV
V_{OLDIFF}	Differential output low voltage	Measurement taken from differential waveform	–	–	–150	mV
V_{CROSS}[8]	Absolute crossing point voltage	Measurement taken from single-ended waveform	250	–	600	mV
$V_{CROSSDELTA}$[8]	Variation of V_{CROSS} over all rising clock edges	Measurement taken from single-ended waveform	–	–	140	mV

Notes
7. Requires external AC coupling for V_{DDO} = 1.8-V range, as indicated in Figure 9. The common-mode voltage of 1.2V has to be generated and applied externally.
8. Parameters are guaranteed by design and characterization. Not 100% tested in production.

DC Specifications for LVCMOS Output

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OH}	Output high voltage	100 µA load	V_{DDO} – 0.2	–	–	V
		4 mA load, V_{DD} = 3.3 V	V_{DDO} – 0.3	–	–	
		4 mA load, V_{DD} = 1.8 V and 2.5 V	V_{DDO} – 0.4	–	–	
V_{OL}	Output low voltage	100 µA load	–	–	0.2	V
		4 mA load	–	–	0.3	

VCXO Specific Parameters

Parameter[9]	Description	Condition	Min	Typ	Max	Units
TPR	Total Pull Range	VC range 0.1 × V_{DD} to 0.9 × V_{DD}	±50	–	±275	ppm
K_{BSL}	Best-fit Straight Line (BSL) linearity	Deviation from BSL line	–5	–	5	%
K_{INC}	Incremental linearity	Kv slope deviation	–10	–	10	%
K_{BW}	Bandwidth of Kv modulation	Programmable	5	10	20	kHz
K_{RANGE}	voltage range on the control port permissible	–	0	–	V_{DD}	V
V_{CTYP}	Nominal center voltage	VC control voltage	–	0.5 × V_{DD}	–	V
R_{VCIN}[10]	Input resistance for VC	–	5	–	–	MΩ
V_{RANGE}	Input voltage range	range of input possible at control port	0.1 × V_{DD}	–	0.9 × V_{DD}	V

Notes
9. Parameters are guaranteed by design and characterization. Not 100% tested in production.
10. R_{VCIN} is 100% tested.

AC Electrical Specifications for LVPECL, LVDS, CML Outputs

(V_{DD} = 3.3 V and 2.5 V for LVPECL, with common mode current, and V_{DD} = 3.3 V, 2.5 V, and 1.8 V for LVDS and CML outputs)

Parameter[10]	Description	Details/Conditions	Min	Typ	Max	Unit
f_{OUT}	Clock Output Frequency	LVPECL, CML, LVDS output standards	15	–	2100	MHz
t_{RF}	LVPECL Output Rise/Fall Time	20% to 80% of AC levels. Measured at 156.25 MHz for PECL outputs.	–	–	350	ps
	CML Output Rise/Fall Time	20% to 80% of AC levels. Measured at 156.25 MHz for CML outputs.	–	–	350	ps
	LVDS Output Rise/Fall Time	20% to 80% of AC levels. Measured at 156.25 MHz for LVDS outputs.	–	–	350	ps
t_{ODC}	Output Duty Cycle	Measured at differential 50% level, 156.25 MHz.	45	50	55	%
V_P	LVDS output differential peak	15 MHz to 700 MHz	247	–	454	mV
V_P	LVDS output differential peak	700 MHz to 2100 MHz	150	–	454	mV
ΔV_P	Change in VP between complementary output states	–	–	–	50	mV
V_P	LVPECL output differential peak	f_{OUT} = 15 MHz to 325 MHz	450	–	–	mV
V_P		f_{OUT} = 325 MHz to 700 MHz	350	–	–	mV
V_P		f_{OUT} = 700 MHz to 2100 MHz	250	–	–	mv
V_P	CML output differential peak	f_{OUT} = 15 MHz to 700 MHz	250	–	600	mV
V_P	CML output differential peak	f_{OUT} = 700 MHz to 2100 MHz	200	–	600	mV
t_{CCJ}	Cycle to Cycle Jitter	pk, measured at differential signal, 156.25 MHz, over 10k cycles, 100 MHz–130 MHz crystal	–	–	50	ps
t_{PJ}	Period Jitter	pk-pk, measured at differential signal, 156.25 MHz, over 10k cycles, 100 MHz–130 MHz crystal	–	–	50	ps
J_{RMS}	RMS Phase Jitter	f_{OUT} = 156.25 MHz, 12 kHz–20 MHz offset, non-VCXO mode	–	150	250	fs
Non-VCXO Mode						
PN1k	Phase Noise, 1 kHz Offset	100 MHz–130 MHz crystal reference, f_{OUT} = 156.25 MHz	–	–	-113	dBc/Hz
PN10k	Phase Noise, 10 kHz Offset	100 MHz–130 MHz crystal reference, f_{OUT} = 156.25 MHz	–	–	-127	dBc/Hz
PN100k	Phase Noise, 100 kHz Offset	100 MHz–130 MHz crystal reference, f_{OUT} = 156.25 MHz	–	–	-135	dBc/Hz
PN1M	Phase Noise, 1MHz Offset	100 MHz–130 MHz crystal reference, f_{OUT} = 156.25 MHz	–	–	-144	dBc/Hz
PN10M	Phase Noise, 10 MHz Offset	100 MHz–130 MHz crystal reference, f_{OUT} = 156.25 MHz	–	–	–152	dBc/Hz
PN-SPUR	Spur	At frequency offsets equal to and greater than the update rate of the PLL	–	–	–65	dBc/Hz

Note
11. Parameters are guaranteed by design and characterization. Not 100% tested in production.

AC Electrical Specifications for HCSL Output

Parameter [12]	Description	Test Conditions	Min	Typ	Max	Units
f_{OUT}	Output frequency	HCSL	15	–	700	MHz
E_R	Rising edge rate	Measured taken from differential waveform, –150 mV to +150 mV	0.6	–	5.7 [13]	V/ns
E_F	Falling edge rate	Measured taken from differential waveform, –150 mV to +150 mV	0.6	–	5.7 [13]	V/ns
t_{STABLE}	Time before voltage ring back (VRB) is allowed	Measured taken from differential waveform, –150 mV to +150 mV	500	–	–	ps
$R\text{-}F_{\_MATCHING}$	Rise-Fall matching	Measured taken from single-ended waveform, rising edge rate to falling edge rate matching, 100 MHz	–100	–	100	ps
t_{DC}	Output duty cycle	Measured taken from differential waveform, f_{OUT} = 100 MHz	45	–	55	%
t_{CCJ}	Cycle to cycle Jitter	Measured taken from differential waveform, 100 MHz	–	–	50	ps
$J_{RMSPCIE}$	Random jitter, PCIE Specification 3.0	100 MHz–130 MHz crystal	–	–	1	ps (RMS)

AC Electrical Specifications for LVCMOS Output

(Load: 10 pF < 100 MHz, 7.5 pF < 150 MHz, 5 pF > 150 MHz)

Parameter[12]	Description	Test Conditions	Min	Typ	Max	Unit
f_{OUT}	Output frequency		15	–	250	MHz
t_{DC}	Output duty cycle	Measured at 1/2 V_{DDO}, loaded, f_{OUT} < 100 MHz	45	–	55	%
		Measured at 1/2 V_{DDO}, loaded, f_{OUT} > 100 MHz	40	–	60	%
t_{RFCMOS}	Rise/Fall time	V_{DDO} = 1.8 V, 20%–80%	–	–	2	ns
		V_{DDO} = 2.5 V, 20%–80%	–	–	1.5	ns
		V_{DDO} = 3.3 V, 20%–80%	–	–	1.2	ns
t_{CCJ}	Cycle to cycle Jitter	pk, Measured at 1/2V_{DDO} over 10k cycle, f_{OUT} = 156.25 MHz	–	–	50	ps
t_{PJ}	Period Jitter	pk, Measured at 1/2V_{DDO} over 10k cycle, f_{OUT} = 156.25 MHz	–	–	100	ps

Notes
12. Parameters are guaranteed by design and characterization. Not 100% tested in production.
13. Edge rates are higher than 4 V/ns due to jitter performance requirements.

HFF Crystal Specifications

Parameter[14]	Description	Test Conditions	Min	Typ	Max	Unit
f_{XTAL}	Crystal frequency range	–	100	–	130	MHz
C0	Crystal shunt capacitance	–	–	–	2	pF
CL	Crystal load capacitance	–	–	5	–	pF
ESR	Crystal equivalent series resistance	ESR = Rm (1 + C0/CL) ^ 2 Rm = Crystal motional resistance	–	20	–	Ω
DL	Drive level	–	–	–	200	µW

OT3 Crystal Specifications

Parameter[14]	Description	Test Conditions	Min	Typ	Max	Units
f_{XTAL}	Crystal frequency range	–	100	–	130	MHz
C0	Crystal shunt capacitance	–	–	–	2	pF
CL	Crystal load capacitance	–	–	5	–	pF
ESR	Crystal equivalent series resistance	ESR = Rm (1 + C0/CL) ^ 2 Rm = Crystal motional resistance	–	60	90	Ω
DL	Drive level	–	–	–	200	µW

LFF Crystal Specifications

Parameter[14]	Description	Test Conditions	Min	Typ	Max	Units
f_{XTAL}	Crystal frequency range	–	50	–	60	MHz
C0	Crystal shunt capacitance	–	–	–	2	pF
CL	Crystal load capacitance	–	–	–	8	pF
ESR	Crystal equivalent series resistance	ESR = Rm (1 + C0/CL) ^ 2 Rm = Crystal motional resistance	–	–	90	W
DL	Drive level	–	–	–	200	µW

Note
14. Parameters are guaranteed by design and characterization. Not 100% tested in production.

LF Low Frequency Reference

(TCXO reference input)

Parameter[15]	Description	Test Conditions	Min	Typ	Max	Units
f_{IN}	Input frequency	–	50	–	60	MHz
t_{DC}	Input duty cycle	Measured at 1/2 input swing	40	–	60	%
V_{PP}	pk-pk input swing	AC coupled input	0.8	–	1.2	V
V_{IL}	Input low voltage	DC coupled input	–	–	0.2	V
V_{IH}[16]	Input high voltage	DC coupled input	0.8	–	1.2	V
t_R	Input rise time	20%–80% of input	–	–	1.5	ns
t_F	Input fall time	20%–80% of input	–	–	1.5	ns
PN_{10K}	Input phase noise	10 kHz offset	–	–	–151	dBc/Hz
PN_{100K}	Input phase noise	100 kHz offset	–	–	–155	dBc/Hz
PN_{1M}	Input phase noise	1 MHz offset	–	–	–156	dBc/Hz

Timing Parameters

Parameter[15]	Description	Min	Max	Unit
t_{PU}	Supply ramp time (0.5 V to $V_{DD(min)}$).	0.01	3000	ms
t_{WAKEUP}[16]	Time from minimum specified power supply to <± 0.1 ppm accurate output frequency clock, programmable (Clock stable within 2.2 ms (max) from VDDX Level, refer to Input Clock Measurement Point)	–	10	ms
	Time from minimum specified power supply to <± 0.1 ppm accurate output frequency clock, programmable (Clock stable within 5.8 ms (max) from VDDX Level, refer to Input Clock Measurement Point)	–	15	
t_{OEEN}	Time from OE edge to output enable	–	2.5	ms
t_{OEDIS}	Time for OE edge to output disable	–	10	µs
t_{FS}	Time form FS change to new frequency	–	2.5	ms
t_{FSAMLL}	Frequency change time for small trigger (≤ ±500ppm)	–	400	µs
t_{FLARGE}	Frequency change time for large trigger (> ±500ppm)	–	2.5	ms
t_{CLOCK}	Clock stable time delay from VDD ramp (see Figure 5), normal configuration	–	2.2	ms
	Clock stable time delay from VDD ramp (see Figure 5), delay programmed	–	5.8	

Input Clock Measurement Point

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{DDX}[15, 17]	t_{CLOCK} Measurement Point	Supply voltage 1.8 V	1.4	–	–	V
		Supply voltage 2.5 V	1.8	–	–	
		Supply voltage 3.3 V	2.3	–	–	

Notes
15. Parameters are guaranteed by design and characterization. Not 100% tested in production.
16. V_{IH} should not to exceed 0.5V when VDD = 0V.
17. Applies to TCXO/External Clock Input.

Phase Jitter Characteristics

(12 kHz to 20 MHz Integration Bandwidth)

Parameter[18]	Description	Condition	Min	Typ	Max	Units
Non VCXO functionality						
J_{RMS}	RMS jitter	f_{OUT} = 644.53 MHz	–	110	–	fs
J_{RMS}	RMS jitter	f_{OUT} = 622.08 MHz	–	120	–	fs
J_{RMS}	RMS jitter	f_{OUT} = 156.25 MHz	–	145	–	fs
J_{RMS}	RMS jitter	f_{OUT} = 2.105 GHz	–	145	–	fs
Modulation bandwidth = 10 kHz, VDD = 3.3V, f_{OUT} = 622.08 MHz						
J_{RMS}	RMS jitter	TPR = 50 ppm, Kv = 37.9 ppm/V	–	151	–	fs
J_{RMS}	RMS jitter	TPR = 155 ppm, Kv = 117.4 ppm/V	–	158	–	fs
J_{RMS}	RMS jitter	TPR = 275 ppm, Kv = 208.3 ppm/V	–	170	–	fs
Modulation bandwidth = 10 kHz, VDD = 2.5V, f_{OUT} = 622.08 MHz						
J_{RMS}	RMS jitter	TPR = 50 ppm, Kv = 50 ppm/V	–	152	–	fs
J_{RMS}	RMS jitter	TPR = 155 ppm, Kv = 155 ppm/V	–	160	–	fs
J_{RMS}	RMS jitter	TPR = 275 ppm, Kv = 275 ppm/V	–	175	–	fs
Modulation bandwidth = 10 kHz, VDD = 1.8V, f_{OUT} = 622.08 MHz						
J_{RMS}	RMS jitter	TPR = 50 ppm, Kv = 69.4 ppm/V	–	153	–	fs
J_{RMS}	RMS jitter	TPR = 155 ppm, Kv = 215.3 ppm/V	–	166	–	fs
J_{RMS}	RMS jitter	TPR = 275 ppm, Kv = 381.9 ppm/V	–	190	–	fs

I^2C Bus Timing Specifications

Parameter [18, 19]	Description	Min	Typ	Max	Units
f_{SCL}	SCL clock frequency	–	–	400	kHz
$t_{HD:STA}$	Hold time START condition	0.6	–	–	µs
t_{LOW}	Low period of SCL	1.3	–	–	µs
t_{HIGH}	High period of SCL	0.6	–	–	µs
$t_{SU:STA}$	Setup time for a repeated START condition	0.6	–	–	µs
$t_{HD:DAT}$	Data hold time	0	–	–	µs
$t_{SU:DAT}$	Data setup time	100	–	–	ns
t_R	Rise time	–	–	300	ns
t_F	Fall time	–	–	300	ns
$t_{SU:STO}$	Setup time for STOP condition	0.6	–	–	µs
t_{BUF}	Bus-free time between STOP and START conditions	1.3	–	–	µs

Notes
18. Parameters are guaranteed by design and characterization. Not 100% tested in production.
19. I^2C operation applicable for V_{DD} of 1.8 V and 2.5 V only.

Voltage and Timing Definitions

Figure 4. Differential Output Definitions

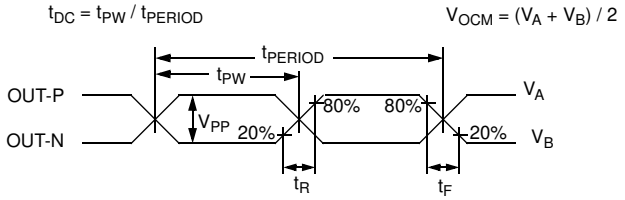


Figure 5. Input Clock Stable time

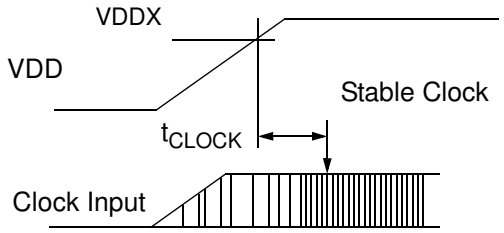


Figure 6. Output Enable/Disable/Frequency Select Timing

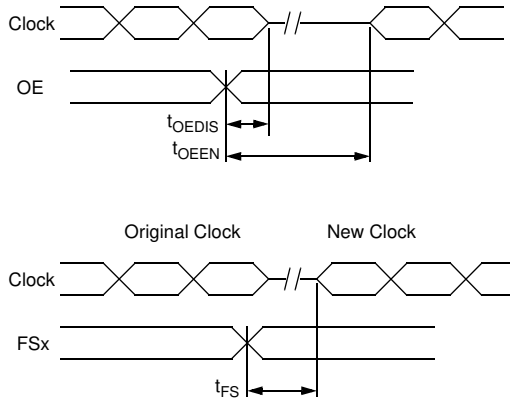


Figure 7. Power Ramp and PLL Lock Time

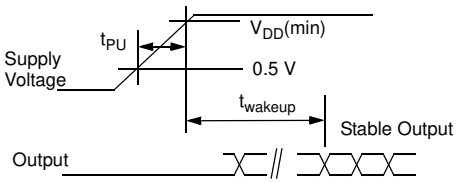


Figure 8. Output Termination Circuit

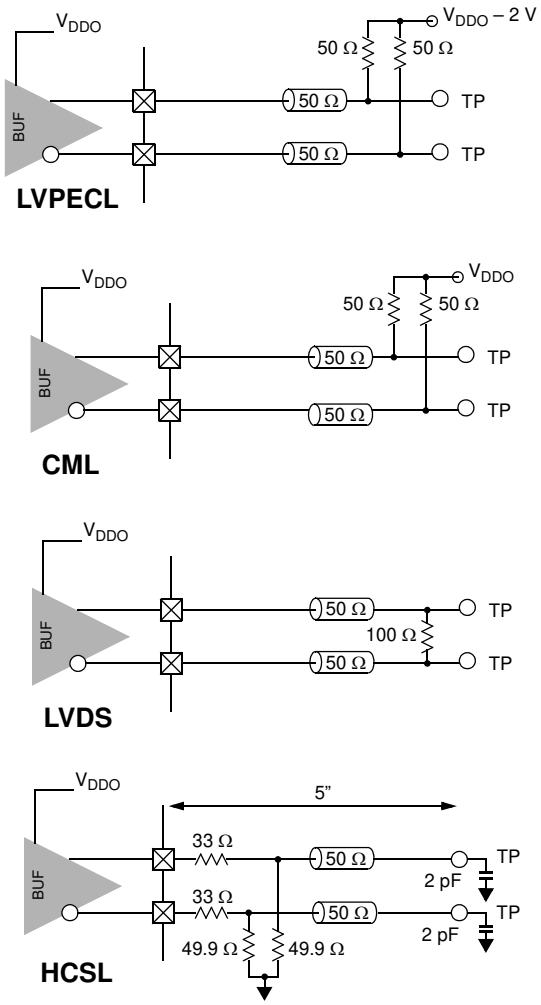
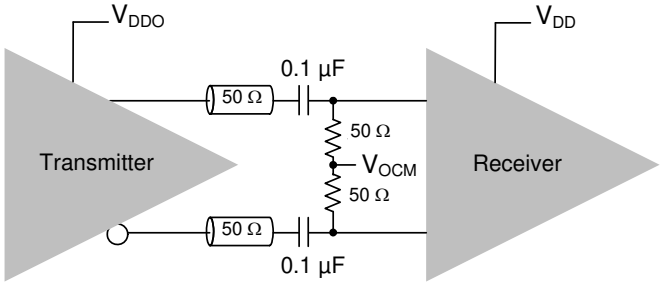


Figure 9. LVDS Termination for 1.8 V[20]



Note

20. The termination circuit shown in this figure is specific to the LVDS output standard for V_{DD} =1.8-V operation. This needs AC coupling (100-nF series capacitor). The 50-ohm termination resistors along with the bias voltage (V_{OCM}) is required to be set at the destination circuit as shown in the figure.

Figure 10. HCSL: Single-ended Measurement Points for Absolute Crossing Point

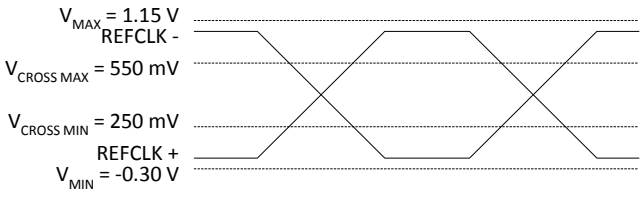


Figure 11. HCSL: Single-ended Measurement Points for Delta Crossing Point

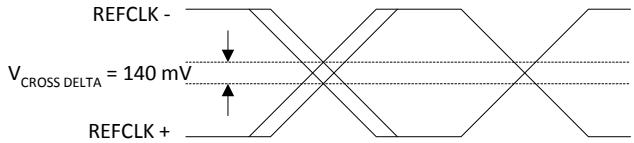


Figure 12. HCSL: Differential Measurement Points for Rise and Fall Time

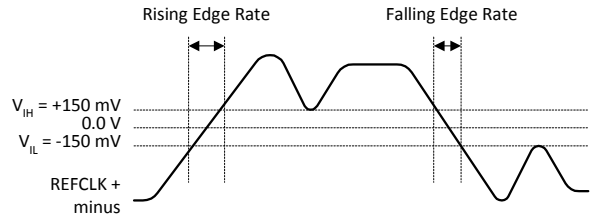


Figure 13. HCSL: Differential Measurement Points for Ringback

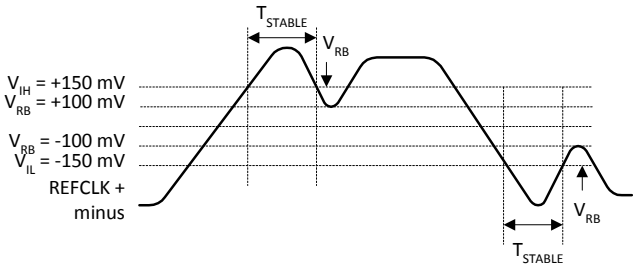
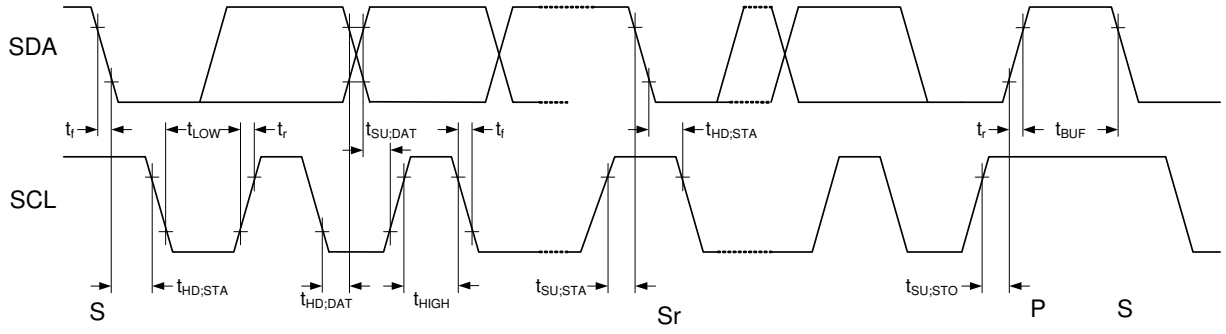


Figure 14. I^2C Bus Timing Specifications



Phase Noise Plots

Figure 15. Typical Phase Noise at 156.25 MHz (12 kHz–20 MHz)

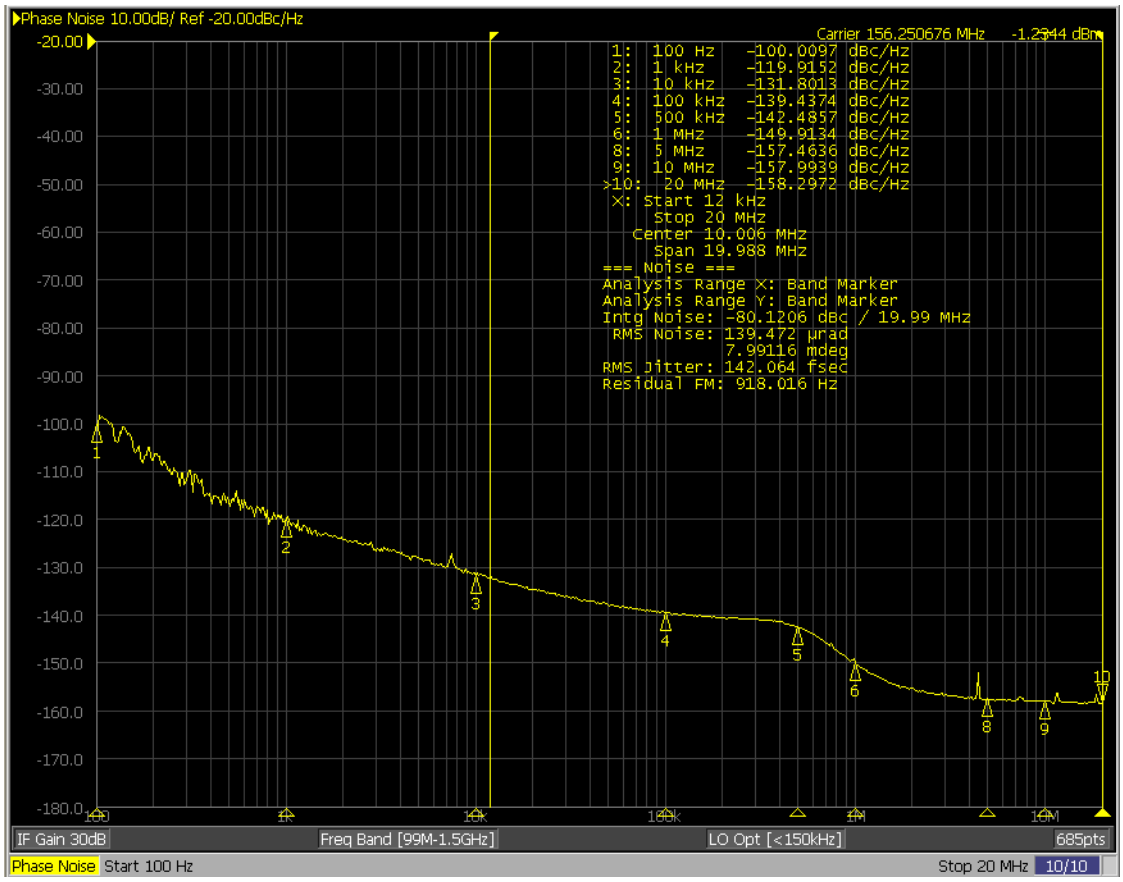


Figure 16. Typical Phase Noise at 622.08 MHz (12 kHz–20 MHz)

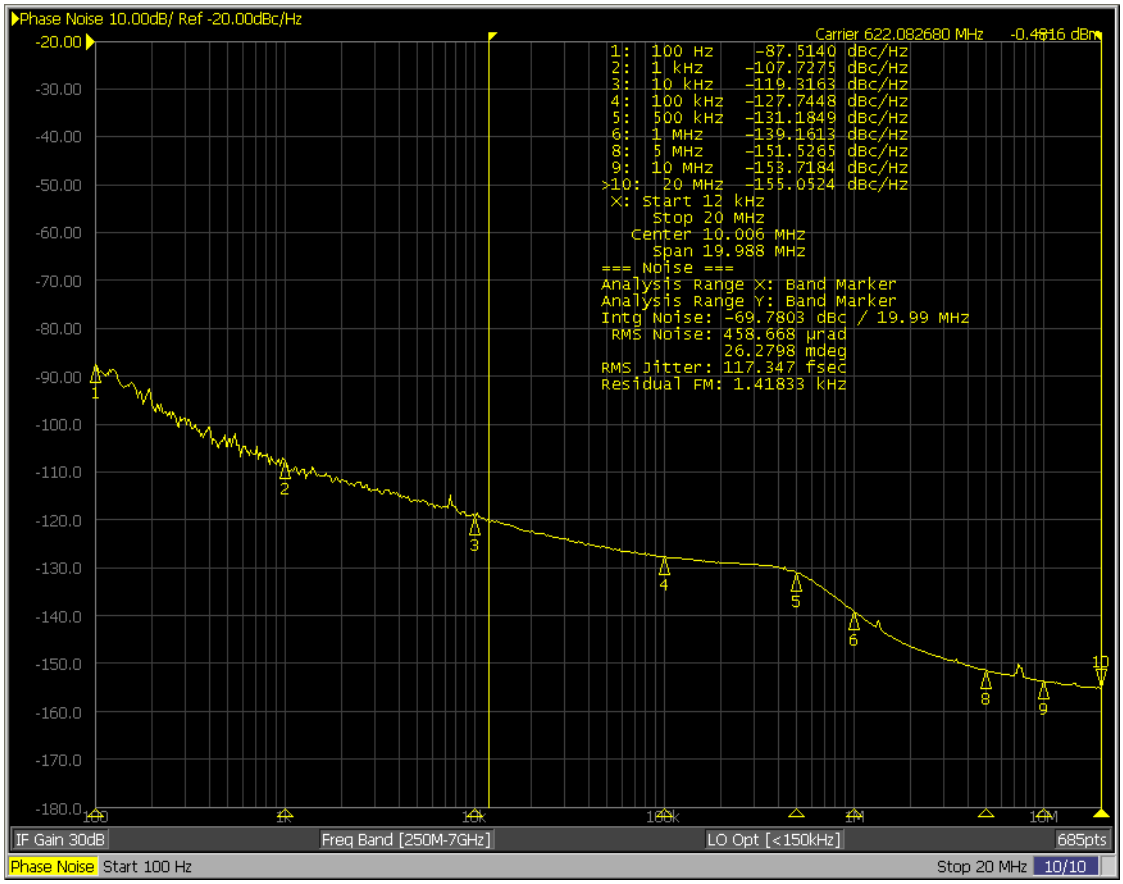
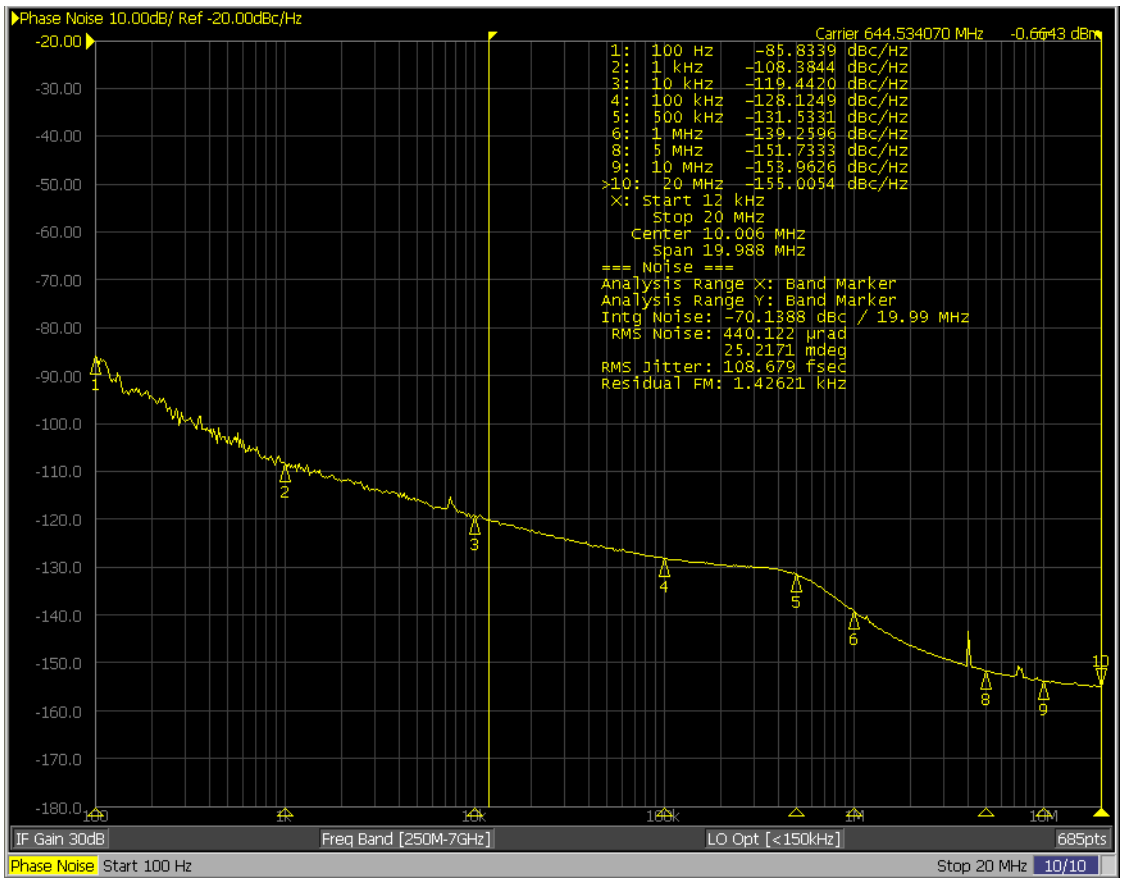


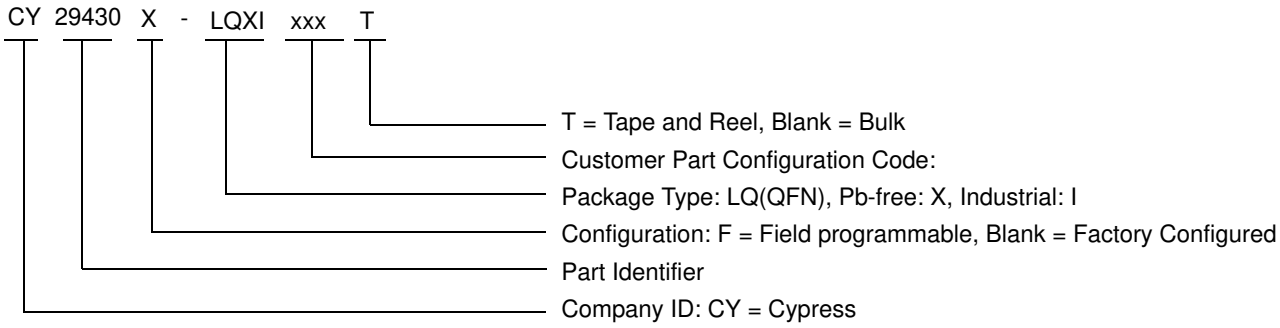
Figure 17. Typical Phase Noise at 644.53 MHz (12 kHz–20 MHz)



Ordering Information

Ordering Code	Configuration	Package Description	Product Flow
CY29430FLQXIT	Field-programmable	16-pin QFN – Tape and Reel	Industrial, –40 °C to +105 °C
CY29430LQXIxxxT	Factory-configured[21]	16-pin QFN – Tape and Reel	Industrial, –40 °C to +105 °C

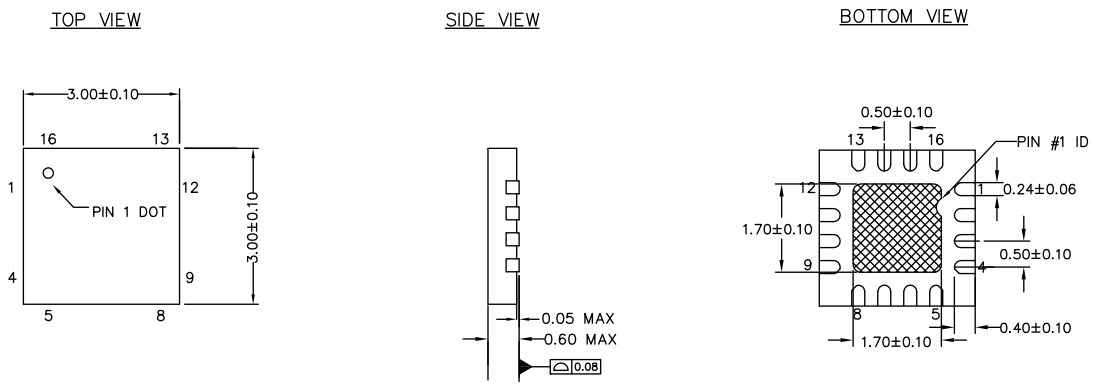
Ordering Code Definitions



Note
21. These are factory-programmed customer-specific part numbers. Contact your local Cypress FAE or sales representative for more information.

Package Diagram

Figure 18. 16-pin QFN (3 × 3 × 0.6 mm) LQ16A 1.7 × 1.7 E-Pad (Sawn) Package Outline, 001-87187



NOTES

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO−248
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web

001-87187 *A

Acronyms

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
BSL	best-fit straight line
CML	current mode logic
DC	direct current
ESD	electrostatic discharge
FS	frequency select
HCSL	high-speed current steering logic
I^2C	inter-integrated circuit
JEDEC	Joint Electron Device Engineering Council
LDO	low dropout (regulator)
LVCMOS	low voltage complementary metal oxide semiconductor
LVDS	low-voltage differential signals
LVPECL	low-voltage positive emitter-coupled logic
NV	non-volatile
OE	output enable
PLL	phase-locked loop
POR	power-on reset
PSoC®	Programmable Sytem-on-Chip
QFN	quad flat no-lead
RMS	root mean square
SCL	serial I^2C clock
SDA	serial I^2C data
VRB	voltage ring back
VCXO	voltage controlled crystal oscillator
XTAL	crystal

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	Degrees Celsius
fs	femtoseconds
GHz	gigahertz
kΩ	kilohms
kHz	kilohertz
MHz	megahertz
MΩ	megaohms
µA	microamperes
µm	micrometers
µs	microseconds
µW	microwatts
mA	milliamperes
mm	millimeters
mΩ	milliohms
ms	milliseconds
mV	millivolts
nH	nanohenrys
ns	nanoseconds
Ω	ohms
ppm	parts per million
ppb	parts per billion
%	percent
pF	picofarads
ps	picoseconds
V	volts

Document History Page

Document Title: CY29430, High-Performance Clock Synthesizer Document Number: 002-11000				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
*B	5320399	07/18/2016	MGPL	Changed status from Preliminary to Final.
*C	5429121	09/07/2016	MGPL	Updated Absolute Maximum Ratings: Added “Supply Current for eFuse Programming”. Replaced “≥ 2000 V” with “2000 V” in value corresponding to “ESD HBM”. Replaced “> 200 V” with “200 V” in value corresponding to “ESD MM”. Added “ESD CDM (JEDEC JESD22-C101E)”. Updated to new template.
*D	5518357	11/15/2016	MGPL/ PSR	Added Table 5 and reference to Table 5 in Frequency Configurations. Added Figure 9.
*E	5613574	02/03/2017	PSR	Added links to ClockWizard 2.1 and technical support, and added reference to related documentation in Functional Description. Updated LVPECL specs in DC Electrical Specifications. Added note clarifying voltage range in AC Electrical Specifications for LVPECL, LVDS, CML Outputs. Added a note for factory-configured parts in Ordering Information.
*F	5682054	04/03/2017	PSR	Updated the template. Added Clock Tree Services link to Sales, Solutions, and Legal Information. Updated Table 1.

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