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CY2CC810

1:10 Clock Fanout Buffer

Features

- Low-voltage operation
- V_{DD} range from 2.5V to 3.3V
- 1:10 fanout
- Over voltage tolerant input hot swappable
- Drives either a 50-Ohm or 75-Ohm transmission line
- Low-input capacitance
- 250 ps typical output-to-output skew
- 19 ps typical DJ jitter
- Typical propagation delay < 3.5 ns
- High-speed operation > 500 MHz
- Industrial versions available
- Available packages include: SOIC, SSOP

Description

The Cypress series of network circuits are produced using advanced 0.35-micron CMOS technology, achieving the industry's fastest logic and buffers.

The Cypress CY2CC810 fanout buffer features one input and ten outputs. Designed for data communications clock management applications, the large fanout from a single input reduces loading on the input clock.

AVCMOS-type outputs dynamically adjust for variable impedance matching and reduce noise overall.

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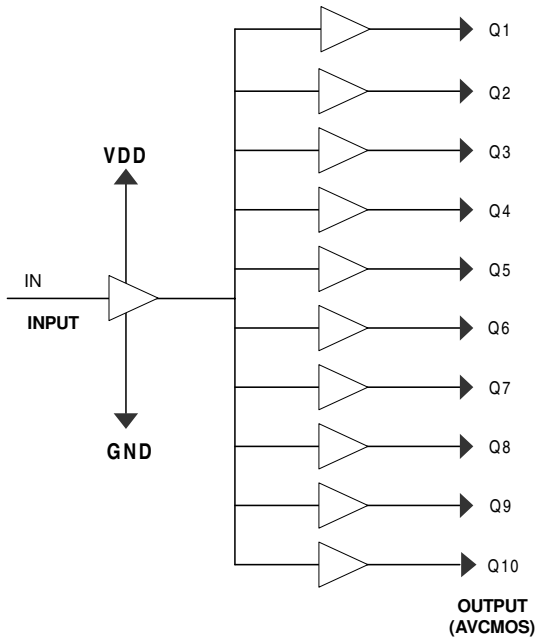
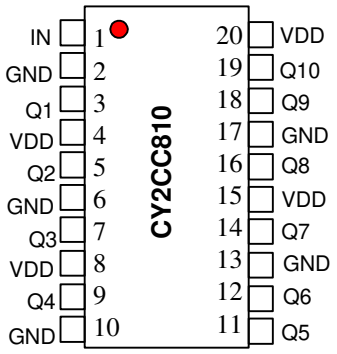
Block Diagram



Pin Configuration



20 pin SOIC/SSOP

Pin Description

Pin Number	Pin Name	Description	
1	IN	Input	LVCMOS
2, 6, 10, 13, 17	GND	Ground	Power
4, 8, 15, 20	V_{DD}	Power Supply	Power
3, 5, 7, 9, 11, 12, 14, 16, 18, 19	Q1... Q10	Output	AVCMOS

Absolute Maximum Conditions[1, 2]

Parameter	Description	Min.	Max.	Unit
V_{DD}	V_{DD} Ground Supply voltage	–0.5	4.6	V
V_{IN}	Input Supply Voltage to Ground Potential	–0.5	5.8	V
V_{OUT}	Output Supply Voltage to Ground Potential	–0.5	V_{DD} +1	V
T_S	Temperature, Storage	–65	150	°C
T_A	Temperature, Operating Ambient	–40	85	°C
	Power Dissipation	0.75		W

DC Electrical Characteristics @ 3.3V (see *Figure 5*)

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
V_{OH}	Output High Voltage	V_{DD} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12 mA	2.3	3.3		V
V_{OL}	Output Low Voltage	V_{DD} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12 mA		0.2	0.5	V
V_{IH}	Input High Voltage	Guaranteed Logic High Level		2		5.8	V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level				0.8	V
I_{IH}	Input High Current	V_{DD} = Max.	V_{IN} = 2.7V			1	µA
I_{IL}	Input Low Current	V_{DD} = Max.	V_{IN} = 0.5V			–1	µA
I_I	Input High Current	V_{DD} = Max., V_{IN} = V_{DD}(Max.)				20	µA
V_{IK}	Clamp Diode Voltage	V_{DD} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
I_{OK}	Continuous Clamp Current	V_{DD} = Max., V_{OUT} = GND				–50	mA
O_{OFF}	Power down Disable	V_{DD} = GND, V_{OUT} = < 4.5V				100	µA
V_H	Input Hysteresis	V_{DD} = Min., V_{IN} = V_{IH} or V_{IL}			80		mV

DC Electrical Characteristics @ 2.5V (see *Figure 1*)

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
V_{OH}	Output High Voltage	V_{DD} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –7 mA	1.8			V
			I_{OH} = 12 mA	1.6			V
V_{OL}	Output Low Voltage	V_{DD} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12 mA			0.65	V
V_{IH}	Input High Voltage	Guaranteed Logic High Level		1.6		5.0	V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level				0.8	V
I_{IH}	Input High Current	V_{DD} = Max.	V_{IN} = 2.4V			1	µA
I_{IL}	Input Low Current	V_{DD} = Max.	V_{IN} = 0.5V			–1	µA
I_I	Input High Current	V_{DD} = Max., V_{IN} = V_{DD}(Max.)				20	µA
V_{IK}	Clamp Diode Voltage	V_{DD} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
I_{OK}	Continuous Clamp Current	V_{DD} = Max., V_{OUT} = GND				–50	mA
O_{OFF}	Power-down Disable	V_{DD} = GND, V_{OUT} = < 4.5V				100	µA
V_H	Input Hysteresis				80		mV

Capacitance

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
Cin	Input Capacitance	V_{IN} = 0V		2.5		pF
Cout	Output Capacitance	V_{OUT} = 0V		6.5		pF

Note

1. Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

Power Supply Characteristics (see *Figure 5*)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
Δ_{ICC}	Delta I_{CC} Quiescent Power Supply Current	(I_{DD} @ V_{DD} = Max. and V_{IN} = V_{DD}) – (I_{DD} @ V_{DD} = Max. and V_{IN} = V_{DD} – 0.6V)			50	µA
I_{CCD}	Dynamic Power Supply Current	V_{DD} = Max. Input toggling 50% Duty Cycle, Outputs Open			0.63	mA/ MHz
I_C	Total Power Supply Current	V_{DD} = Max. Input toggling 50% Duty Cycle, Outputs Open fL = 40 MHZ			25	mA
t_{PU}	Power-up time for all V_{DD}s	Power-up to reach minimum specified voltage (power ramp must be monotonic)	0.05		500	ms

High-frequency Parametrics

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
D_J	Jitter, Deterministic	50% duty cycle t_W(50–50) The “point to point load circuit” Output Jitter – Input Jitter	2.5V		23	35	ps
			3.3V		19	30	ps
$F_{max(3.3V)}$	Maximum frequency V_{DD} = 3.3V	50% duty cycle t_W(50–50) Standard Load Circuit.	See *Figure 5*			160	MHz
		50% duty cycle t_W(50–50) The “point to point load circuit”	See *Figure 7*			650	
$F_{max(2.5V}$	Maximum frequency V_{DD} = 2.5 V	The “point to point load circuit” V_{IN} = 2.4V/0.0V V_{OUT} = 1.7V/0.7V	See *Figure 7*			200	MHz
$F_{max(20)}$	Maximum frequency V_{DD} = 3.3 V	20% duty cycle t_W(20–80) The “point to point load circuit” V_{IN} = 3.0V/0.0V V_{OUT} = 2.3V/0.4V	See *Figure 7*			250	MHz
	Maximum frequency V_{DD} = 2.5 V	The “point to point load circuit” V_{IN} = 2.4V/0.0V V_{OUT} = 1.7V/0.7V	See *Figure 3*			200	MHz
t_W	Minimum pulse V_{DD} = 3.3 V	The “point to point load circuit” V_{IN} = 3.0V/0.0V F = 100 MHz V_{OUT} = 2.0V/0.8V	See *Figure 7*	1			ns
	Minimum pulse V_{DD} = 2.5 V	The “point to point load circuit” V_{IN} = 2.4V/0.0V F = 100 MHz V_{OUT} = 1.7V/0.7V	See *Figure 3*	1			

AC Switching Characteristics @ 3.3V, V_{DD} = 3.3V ±5%, Temperature = –40°C to +85°C

Parameter	Description		Min.	Typ.	Max.	Unit
t_{PLH}	Propagation Delay – Low to High	See *Figure 4*	1.5	2.7	3.5	ns
t_{PHL}	Propagation Delay – High to Low		1.5	2.7	3.5	ns
t_R	Output Rise Time			0.8		V/ns
t_F	Output Fall Time			0.8		V/ns
$t_{SK(0)}$	Output Skew: Skew between outputs of the same package (in phase)	See *Figure 10*		0.25	0.38	ns
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output (t_{PHL} – t_{PLH}).	See *Figure 9*			0.2	ns
$t_{SK(t)}$	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type.	See *Figure 11*			0.42	ns

AC Switching Characteristics @ 2.5V, V_{DD} = 2.5V ±5%, Temperature = –40°C to +85°C

Parameter	Description		Min.	Typ.	Max.	Unit
t_{PLH}	Propagation Delay – Low to High	See *Figure 4*	1.5	2.0	3.5	ns
t_{PHL}	Propagation Delay – High to Low		1.5	2.0	3.5	ns
t_R	Output Rise Time			0.8		V/ns
t_F	Output Fall Time			0.8		V/ns
$t_{SK(0)}$	Output Skew: Skew between outputs of the same package (in phase)	See *Figure 10*		0.25	0.38	ns
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output ($t_{PHL} – t_{PLH}$).	See *Figure 9*			0.4	ns
$t_{SK(t)}$	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type.	See *Figure 11*			0.65	ns

Parameter Measurement Information: V_{DD} @ 2.5V

Figure 1. Load Circuit [3,4,5]

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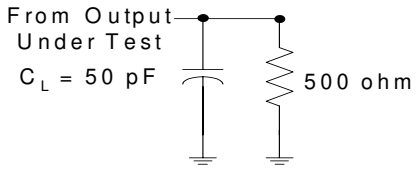


Figure 2. Voltage Waveforms Pulse Duration[6]

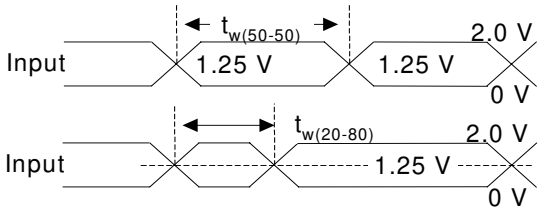
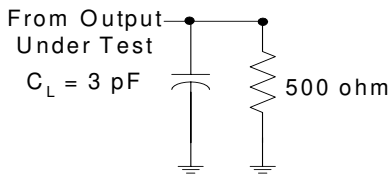
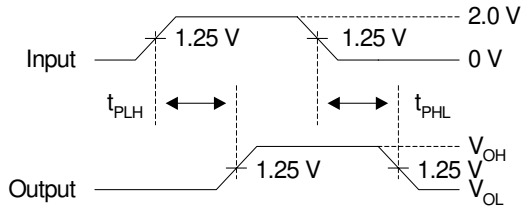


Figure 3. Point to Point Load Circuit[3,4,5]



Notes
3. C_L includes probe and jig capacitance.
4. All input pulses are supplied by generators having the following characteristics: PRR < 100 MHz, Z_0 = 50W, t_R < 2.5 nS, t_F < 2.5 nS.
5. The outputs are measured one at a time with one transition per measurement.
6. T_{PLH} and T_{PHL} are the same as t_{pd}..

Figure 4. Voltage WaveformsPropagation Delay Times[4]



Parameter Measurement Information: V_{DD} @ 3.3V

Figure 5. Load Circuit [3,4,5]

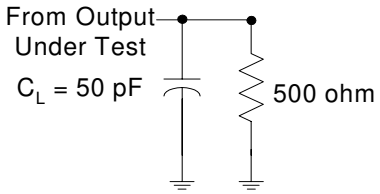


Figure 6. Voltage Waveforms–Pulse Duration[6]

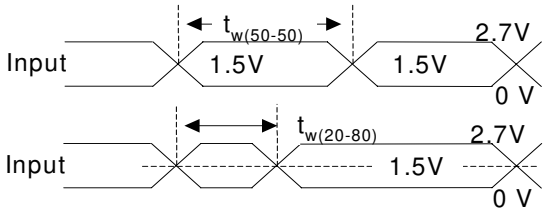


Figure 7. Point to Point Load Circuit[3,4,5]

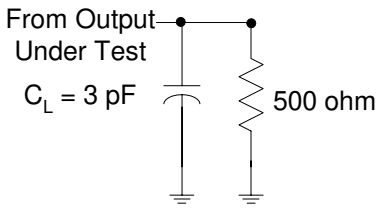


Figure 8. Voltage Waveforms Propagation Delay Times[4]

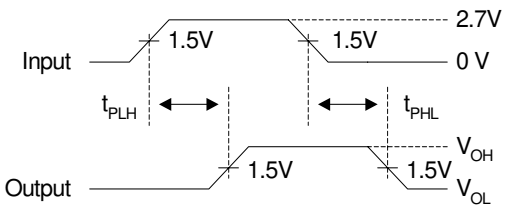
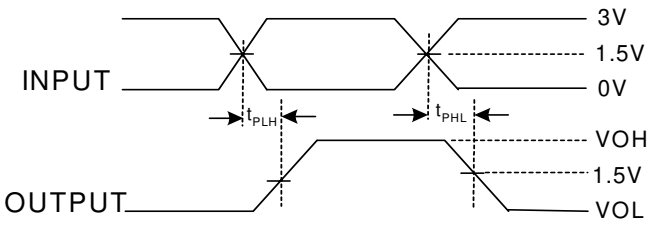
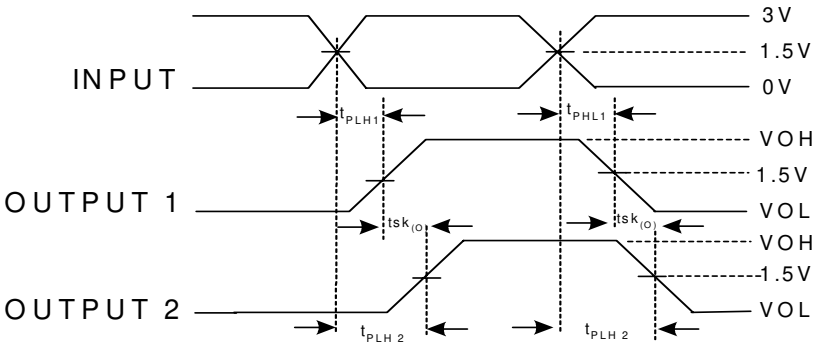


Figure 9. Pulse Skew–$tsk_{(p)}$



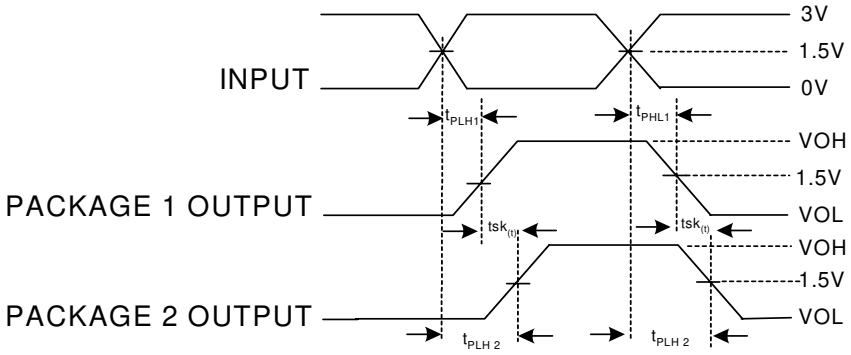
$$tsk_{(P)} = | t_{PHL} - t_{PLH} |$$

Figure 10. Output Skew–$tsk_{(0)}$



$$tsk_{(P)} = | t_{PLH2} - t_{PLH1} | \text{ or } t_{PHL2} - t_{PHL1} |$$

Figure 11. Package Skew–$tsk_{(t)}$



$$tsk_{(t)} = | t_{PLH2} - t_{PLH1} | \text{ or } t_{PHL2} - t_{PHL1} |$$

Ordering Information

Part Number	Package Type	Product Flow
CY2CC810OI	20-pin SSOP	Industrial, –40°C to 85°C
CY2CC810OIT	20-pin SSOP–Tape and Reel	Industrial, –40°C to 85°C
CY2CC810OC	20-pin SSOP	Commercial, 0°C to 70°C
CY2CC810OCT	20-pin SSOP–Tape and Reel	Commercial, 0°C to 70°C
Lead-free		
CY2CC810OXC	20-pin SSOP	Commercial, 0°C to 70°C
CY2CC810OXCT	20-pin SSOP–Tape and Reel	Commercial, 0°C to 70°C
CY2CC810OXI	20-pin SSOP	Industrial, –40°C to 85°C
CY2CC810OXIT	20-pin SSOP–Tape and Reel	Industrial, –40°C to 85°C

Package Drawing and Dimensions

Figure 12. 20-Lead (300-Mil) SOIC S20.3/SZ20.3

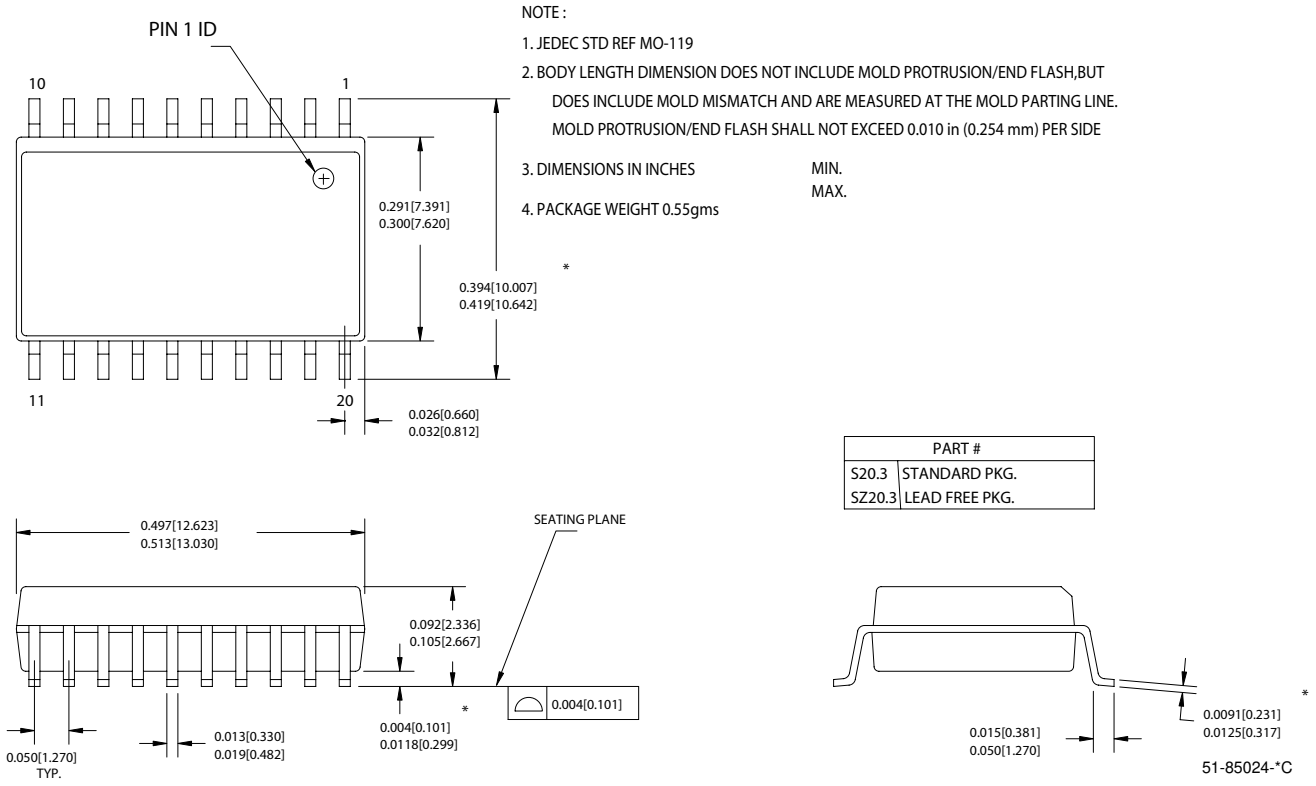
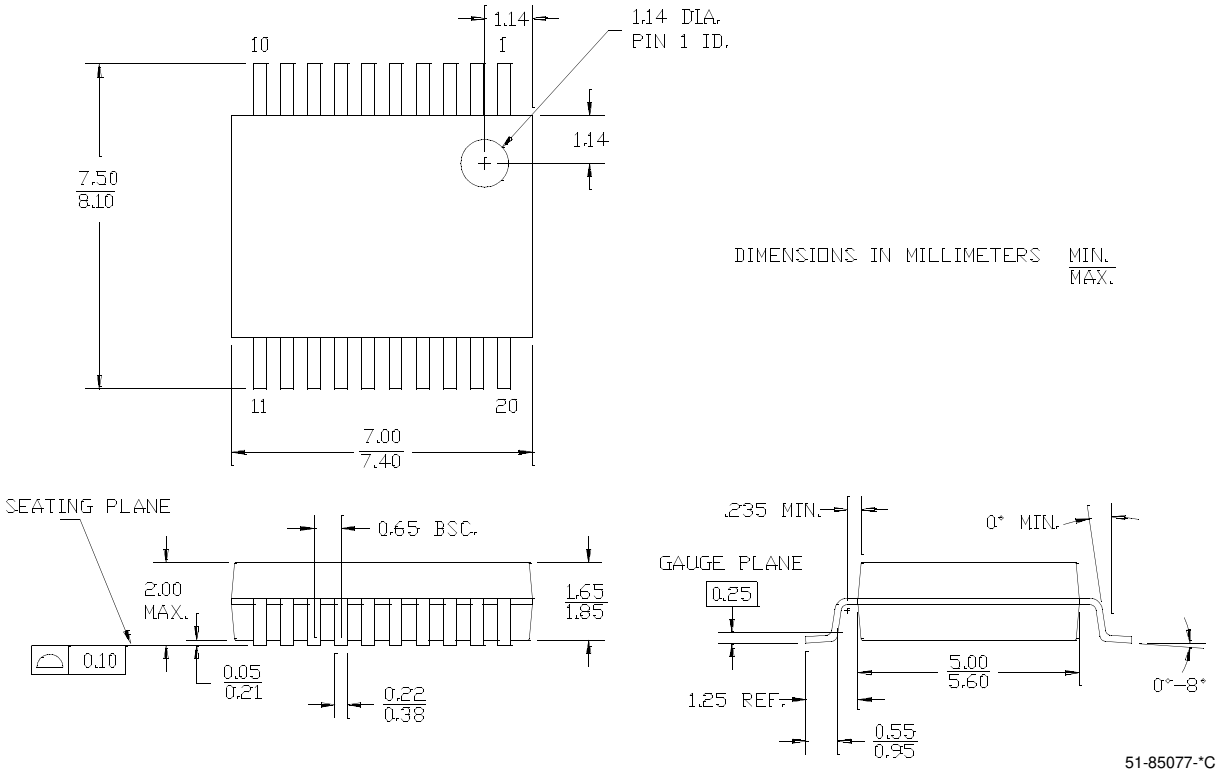


Figure 13. 20-lead (5.3-mm) Shrunk Small Outline Package O20



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Document History Page

Document Title: CY2CC810 1:10 Clock Fanout Buffer Document #: 38-07056				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107081	06/07/01	IKA	Convert from IMI to Cypress
*A	114315	05/09/02	TSM	ΔI_{DD} Validation
*B	119117	10/07/02	RGL	Added 5.8 as the Max. value of V_{IH} in the DC Electrical Characteristics @3.3V table. Changed the Max. value of V_{IH} from 1.8 to 5.0 in the DC Electrical Characteristics @2.5V table.
*C	122743	12/14/02	RBI	Added power up requirements to maximum ratings information.
*D	387761	See ECN	RGL	Added typical values Updated jitter and skew specs. Removed devices with SOIC package Added Lead-free SSOP package
*E	499991	See ECN	RGL	Added tpu parameter in the Power Supply Characteristics table