Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

CY2CC810

1:10 Clock Fanout Buffer

Features

- Low-voltage operation
- V_{DD} range from 2.5 V to 3.3 V
- 1:10 fanout
- Over voltage tolerant input hot swappable
- Drives either a 50-Ohm or 75-Ohm transmission line
- Low-input capacitance
- 250 ps typical output-to-output skew
- 19 ps typical DJ jitter
- Typical propagation delay < 3.5 ns
- High-speed operation > 500 MHz
- Industrial temperature range
- Available packages include: SSOP

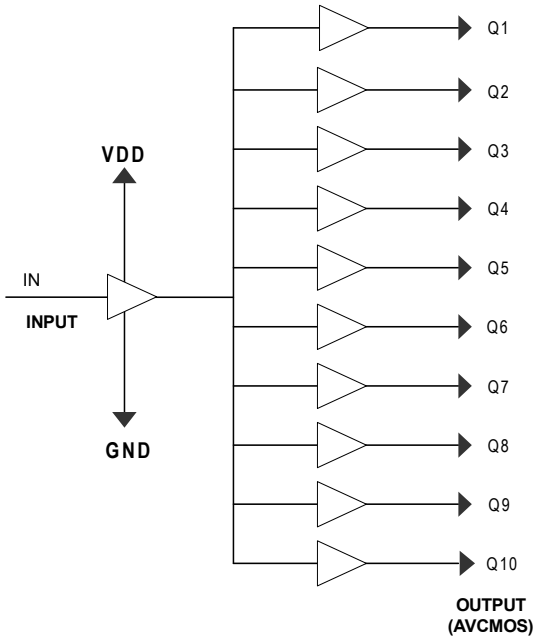
Functional Description

The Cypress series of network circuits are produced using advanced 0.35-micron CMOS technology, achieving the industry's fastest logic and buffers.

The Cypress CY2CC810 fanout buffer features one input and ten outputs. Designed for data communications clock management applications, the large fanout from a single input reduces loading on the input clock.

For a complete list of related documentation, click here.

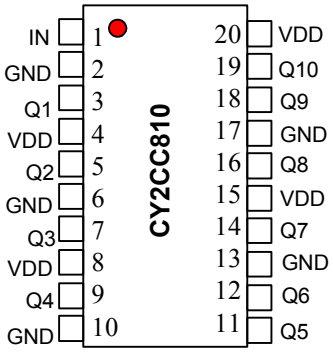
Logic Block Diagram



Contents

Pin Configuration

Figure 1. 20-pin SSOP pinout



20 pin SOIC/SSOP

Pin Description

Pin Number	Pin Name	Description	
1	IN	Input	LVCMOS
2, 6, 10, 13, 17	GND	Ground	Power
4, 8, 15, 20	V_{DD}	Power Supply	Power
3, 5, 7, 9, 11, 12, 14, 16, 18, 19	Q1... Q10	Output	AVCMOS

Absolute Maximum Conditions

Parameter [1, 2]	Description	Min	Max	Unit
V_{DD}	V_{DD} ground supply voltage	–0.5	4.6	V
V_{IN}	Input supply voltage to ground potential	–0.5	5.8	V
V_{OUT}	Output supply voltage to ground potential	–0.5	V_{DD} + 1	V
T_S	Temperature, storage	–65	150	°C
T_A	Temperature, operating ambient	–40	85	°C
	Power dissipation	0.75		W

DC Electrical Characteristics

@ 3.3 V (see Figure 6)

Parameter	Description	Conditions		Min	Typ	Max	Unit
V_{OH}	Output high voltage	V_{DD} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12 mA	2.3	3.3	–	V
V_{OL}	Output low voltage	V_{DD} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12 mA	–	0.2	0.5	V
V_{IH}	Input high voltage	Guaranteed Logic High Level	–	2	–	5.8	V
V_{IL}	Input low voltage	Guaranteed Logic Low Level	–	–	–	0.8	V
I_{IH}	Input high current	V_{DD} = Max	V_{IN} = 2.7 V	–	–	1	µA
I_{IL}	Input low current	V_{DD} = Max	V_{IN} = 0.5 V	–	–	–1	µA
I_I	Input high current	V_{DD} = Max, V_{IN} = V_{DD}(Max)	–	–	–	20	µA
V_{IK}	Clamp diode voltage	V_{DD} = Min, I_{IN} = –18 mA	–	–	–0.7	–1.2	V
I_{OK}	Continuous clamp current	V_{DD} = Max, V_{OUT} = GND	–	–	–	–50	mA
O_{OFF}	Power down disable	V_{DD} = GND, V_{OUT} ≤ 4.5 V	–	–	–	100	µA
V_H	Input hysteresis	V_{DD} = Min, V_{IN} = V_{IH} or V_{IL}	–	–	80		mV

Notes
1. Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Electrical Characteristics

@ 2.5 V (see Figure 2)

Parameter	Description	Conditions		Min	Typ	Max	Unit
V_{OH}	Output high voltage	V_{DD} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = –7 mA	1.8	–	–	V
			I_{OH} = 12 mA	1.6	–	–	V
V_{OL}	Output low voltage	V_{DD} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12 mA		–	0.65	V
V_{IH}	Input high voltage	Guaranteed Logic High Level	–	1.6	–	5.0	V
V_{IL}	Input low voltage	Guaranteed Logic Low Level	–	–	–	0.8	V
I_{IH}	Input high current	V_{DD} = Max	V_{IN} = 2.4 V	–	–	1	µA
I_{IL}	Input low current	V_{DD} = Max	V_{IN} = 0.5 V	–	–	–1	µA
I_I	Input high current	V_{DD} = Max, V_{IN} = V_{DD}(Max)	–	–	–	20	µA
V_{IK}	Clamp diode voltage	V_{DD} = Min, I_{IN} = –18 mA	–	–	–0.7	–1.2	V
I_{OK}	Continuous clamp current	V_{DD} = Max, V_{OUT} = GND	–	–	–	–50	mA
O_{OFF}	Power-down disable	V_{DD} = GND, V_{OUT} ≤ 4.5 V	–	–	–	100	µA
V_H	Input hysteresis	–	–	–	80	–	mV

Capacitance

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
Cin	Input capacitance	V_{IN} = 0 V	–	2.5	–	pF
Cout	Output capacitance	V_{OUT} = 0 V	–	6.5	–	pF

Thermal Resistance

Parameter [3]	Description	Test Conditions	20-pin SSOP	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	79	°C/W
θ_{JC}	Thermal resistance (junction to case)		35	°C/W

Note
3. These parameters are guaranteed by design and are not tested.

Power Supply Characteristics

(see Figure 6)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
Δ_{ICC}	Delta I_{CC} quiescent power supply current	(I_{DD} @ V_{DD} = Max and V_{IN} = V_{DD}) – (I_{DD} @ V_{DD} = Max and V_{IN} = V_{DD} – 0.6 V)	–	–	50	µA
I_{CCD}	Dynamic power supply current	V_{DD} = Max Input toggling 50% Duty Cycle, Outputs Open	–		0.63	mA/ MHz
I_C	Total power supply current	V_{DD} = Max Input toggling 50% Duty Cycle, Outputs Open fL = 40 MHz	–	–	25	mA
t_{PU}	Power-up time for all V_{DD}s	Power-up to reach minimum specified voltage (power ramp must be monotonic)	0.05	–	500	ms

High-frequency Parametrics

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
D_J	Jitter, Deterministic	50% duty cycle t_W(50–50) The “point to point load circuit” Output Jitter – Input Jitter	2.5 V	–	23	35	ps
			3.3 V	–	19	30	ps
$F_{max(3.3\ V)}$	Maximum frequency V_{DD} = 3.3 V	50% duty cycle t_W(50–50) Standard Load Circuit.	See Figure 6	–	–	160	MHz
		50% duty cycle t_W(50–50) The “point to point load circuit”	See Figure 8	–	–	650	
$F_{max(2.5\ V}$	Maximum frequency V_{DD} = 2.5 V	The “point to point load circuit” V_{IN} = 2.4 V/0.0 V V_{OUT} = 1.7 V/0.7 V	See Figure 8	–	–	200	MHz
$F_{max(20)}$	Maximum frequency V_{DD} = 3.3 V	20% duty cycle t_W(20–80) The “point to point load circuit” V_{IN} = 3.0 V/0.0 V V_{OUT} = 2.3 V/0.4 V	See Figure 8	–	–	250	MHz
	Maximum frequency V_{DD} = 2.5 V	The “point to point load circuit” V_{IN} = 2.4 V/0.0 V V_{OUT} = 1.7 V/0.7 V	See Figure 4	–	–	200	MHz
t_W	Minimum pulse V_{DD} = 3.3 V	The “point to point load circuit” V_{IN} = 3.0 V/0.0 V F = 100 MHz V_{OUT} = 2.0 V/0.8 V	See Figure 8	1	–	–	ns
	Minimum pulse V_{DD} = 2.5 V	The “point to point load circuit” V_{IN} = 2.4 V/0.0 V F = 100 MHz V_{OUT} = 1.7 V/0.7 V	See Figure 4	1	–	–	

AC Switching Characteristics

@ 3.3 V, V_{DD} = 3.3 V ± 5%, Temperature = –40 °C to +85 °C

Parameter	Description		Min	Typ	Max	Unit
t_{PLH}	Propagation delay – Low to High	See Figure 5	1.5	2.7	3.5	ns
t_{PHL}	Propagation delay – High to Low		1.5	2.7	3.5	ns
t_R	Output rise time	–	–	0.8	–	V/ns
t_F	Output fall time	–	–	0.8	–	V/ns
$t_{SK(0)}$	Output Skew: Skew between outputs of the same package (in phase)	See Figure 11	–	0.25	0.38	ns
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output ($t_{PHL} – t_{PLH}$).	See Figure 10	–	–	0.2	ns
$t_{SK(t)}$	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type.	See Figure 12	–	–	0.42	ns

AC Switching Characteristics

@ 2.5 V, V_{DD} = 2.5 V ± 5%, Temperature = –40 °C to +85 °C

Parameter	Description		Min	Typ	Max	Unit
t_{PLH}	Propagation delay – Low to High	See Figure 5	1.5	2.0	3.5	ns
t_{PHL}	Propagation delay – High to Low		1.5	2.0	3.5	ns
t_R	Output rise time	–	–	0.8	–	V/ns
t_F	Output fall time	–	–	0.8	–	V/ns
$t_{SK(0)}$	Output Skew: Skew between outputs of the same package (in phase)	See Figure 11	–	0.25	0.38	ns
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output ($t_{PHL} – t_{PLH}$).	See Figure 10	–	–	0.4	ns
$t_{SK(t)}$	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type.	See Figure 12	–		0.65	ns

Parameter Measurement Information

V_{DD} @ 2.5 V

Figure 2. Load Circuit [4, 5, 6]

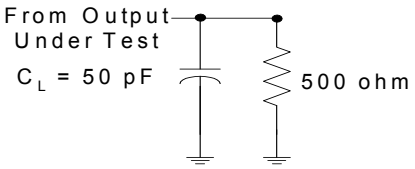


Figure 3. Voltage Waveforms Pulse Duration [7]

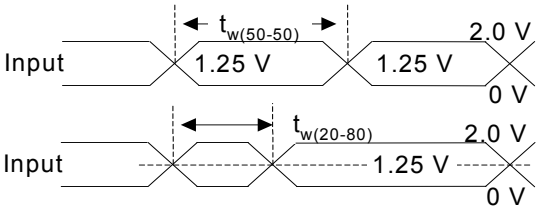


Figure 4. Point to Point Load Circuit [4, 5, 6]

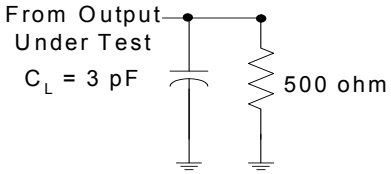
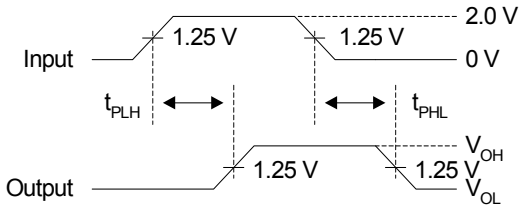


Figure 5. Voltage Waveforms Propagation Delay Times [5]



Notes
4. C_L includes probe and jig capacitance.
5. All input pulses are supplied by generators having the following characteristics: PRR < 100 MHz, Z_0 = 50W, t_R < 2.5 nS, t_F < 2.5 nS.
6. The outputs are measured one at a time with one transition per measurement.
7. T_{PLH} and T_{PHL} are the same as t_{pd}..

Parameter Measurement Information

V_{DD} @ 3.3 V

Figure 6. Load Circuit [8, 9, 10]

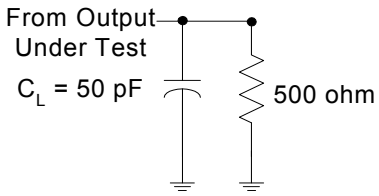


Figure 7. Voltage Waveforms – Pulse Duration [11]

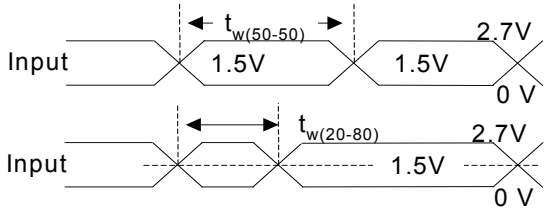


Figure 8. Point to Point Load Circuit [8, 9, 10]

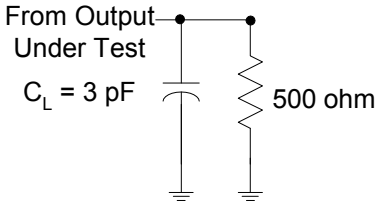
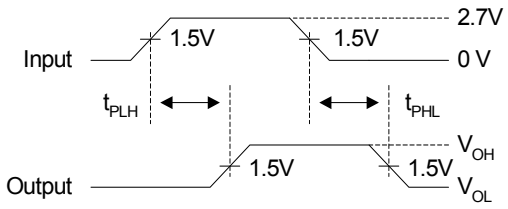


Figure 9. Voltage Waveforms Propagation Delay Times [9]

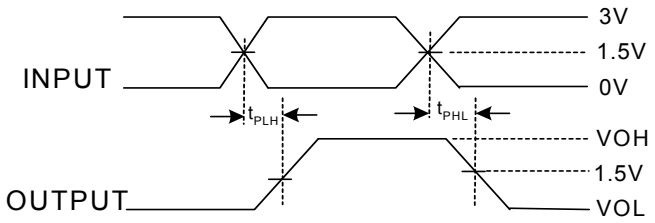


Notes
8. C_L includes probe and jig capacitance.
9. All input pulses are supplied by generators having the following characteristics: PRR < 100 MHz, Z_0 = 50W, t_R < 2.5 nS, t_F < 2.5 nS.
10. The outputs are measured one at a time with one transition per measurement.
11. T_{PLH} and T_{PHL} are the same as t_{pd}.

Parameter Measurement Information (Continued)

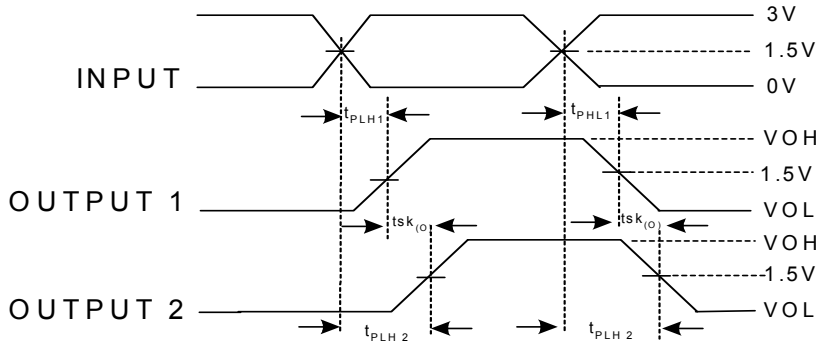
V_{DD} @ 3.3 V

Figure 10. Pulse Skew – $tsk_{(p)}$



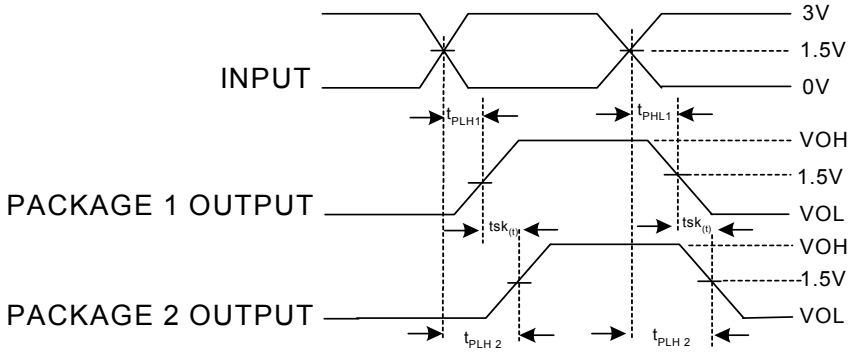
$$tsk_{(P)} = | t_{PHL} - t_{PLH} |$$

Figure 11. Output Skew – $tsk_{(0)}$



$$tsk_{(P)} = | t_{PLH2} - t_{PLH1} | \text{ or } | t_{PHL2} - t_{PHL1} |$$

Figure 12. Package Skew – $tsk_{(t)}$

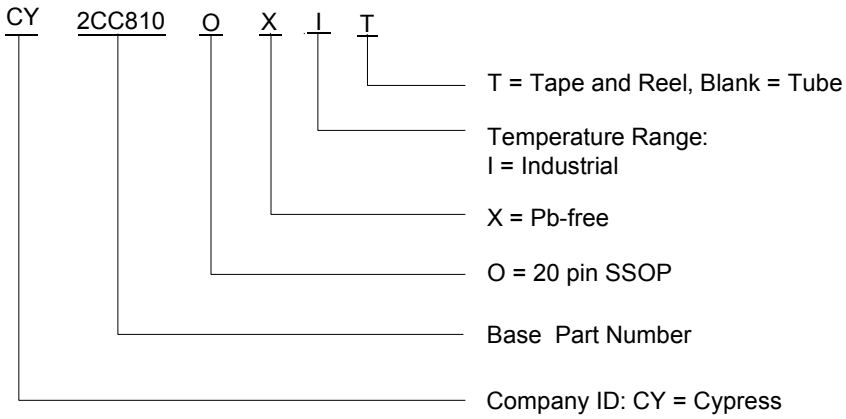


$$tsk_{(t)} = | t_{PLH2} - t_{PLH1} | \text{ or } | t_{PHL2} - t_{PHL1} |$$

Ordering Information

Part Number [12]	Package Type	Product Flow
Pb-free		
CY2CC810OXI	20-pin SSOP	Industrial, –40 °C to 85 °C
CY2CC810OXIT	20-pin SSOP–Tape and Reel	Industrial, –40 °C to 85 °C
CY2CC810OXI-1	20-pin SSOP	Industrial, –40 °C to 85 °C
CY2CC810OXI-1T	20-pin SSOP–Tape and Reel	Industrial, –40 °C to 85 °C

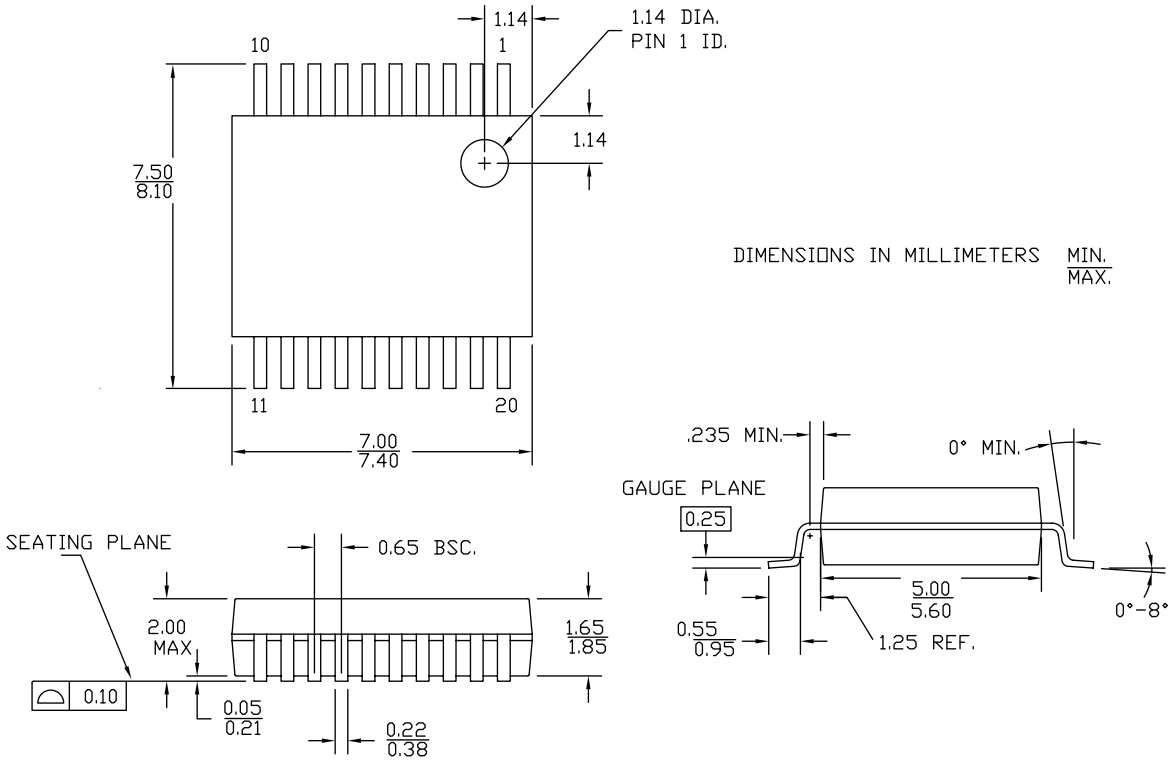
Ordering Code Definitions



Note
12. Devices with part numbers ending with -1 are identical to devices without the -1 suffix. There are no differences in specification.

Package Drawing and Dimensions

Figure 13. 20-pin SSOP (210 Mils) O20.21 Package Outline, 51-85077



51-85077 *F

Acronym

Acronym	Description
CMOS	complementary metal oxide semiconductor
DJ	Deterministic Jitter
SSOP	shrunk small outline package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHZ	megahertz
uA	microampere
mA	milliampere
ms	millisecond
ns	nanosecond
%	percent
pF	picofarad
ps	picosecond
V	volt

Document History Page

Document Title: CY2CC810, 1:10 Clock Fanout Buffer Document Number: 38-07056				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	107081	06/07/01	IKA	Convert from IMI to Cypress
*A	114315	05/09/02	TSM	ΔI_{DD} Validation
*B	119117	10/07/02	RGL	Updated DC Electrical Characteristics (@ 3.3 V): Added 5.8 V as the maximum value of V_{IH} parameter. Updated DC Electrical Characteristics (@ 2.5 V): Changed maximum value of V_{IH} parameter from 1.8 V to 5.0 V.
*C	122743	12/14/02	RBI	Updated Absolute Maximum Conditions: Added Note 2 (power-up requirements) and referred the same note in “Parameter” column.
*D	387761	See ECN	RGL	Updated High-frequency Parametrics: Updated details in “Test Conditions” column corresponding to D_J parameter. Updated values of D_J parameter. Updated AC Switching Characteristics: Updated values of $t_{SK(0)}$, $t_{SK(p)}$, $t_{SK(t)}$ parameters. Updated AC Switching Characteristics: Updated values of $t_{SK(0)}$, $t_{SK(p)}$, $t_{SK(t)}$ parameters. Updated Ordering Information: Removed devices with SOIC package. Added devices Lead-free SSOP package.
*E	499991	See ECN	RGL	Updated Power Supply Characteristics: Added t_{PU} parameter and its details.
*F	2896073	03/19/10	CXQ	Removed SOIC package related information in all instances across the document. Updated Ordering Information: Removed obsolete parts. Added CY2CC810OXI-1, CY2CC810OXI-1T parts. Updated Package Drawing and Dimensions.
*G	3056154	10/08/2010	CXQ	Updated Ordering Information: Removed CY2CC810OXC and CY2CC810OXCT parts.
*H	3396159	10/10/2011	PURU	Updated Functional Description: Removed “AVCMOS-type outputs dynamically adjust for variable impedance matching and reduce noise overall”. Added Ordering Code Definitions under Ordering Information. Updated Package Drawing and Dimensions. Added Acronym, and Units of Measure.
*I	4559526	11/07/2014	PURU	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*J	5272946	05/16/2016	PSR	Added Thermal Resistance. Updated Package Drawing and Dimensions: spec 51-85077 – Changed revision from *E to *F. Updated to new template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Lighting & Power Control	cypress.com/powerpsoc
Memory	cypress.com/memory
PSoC	cypress.com/psoc
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless/RF	cypress.com/wireless

PSoC®Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support