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CY2DP1504

1:4 LVPECL Fanout Buffer with Selectable Clock Input

Features

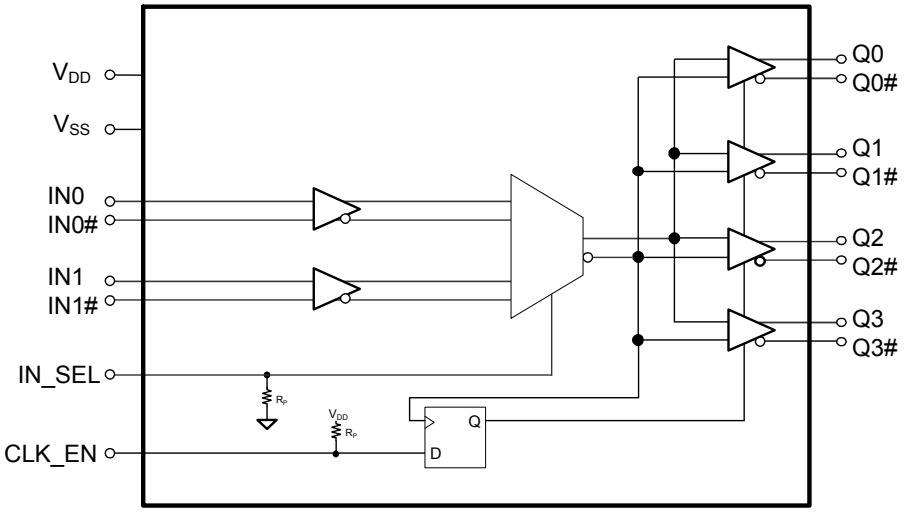
- Select one of two differential (LVPECL, LVDS, HCSL, or CML) input pairs to distribute to four LVPECL output pairs
- Translates any single-ended input signal to 3.3 V LVPECL levels with resistor bias on INx# input
- 30 ps maximum output-to-output skew
- 480 ps maximum propagation delay
- 0.15 ps maximum additive RMS phase jitter at 156.25 MHz (12 kHz to 20 MHz offset)
- Up to 1.5 GHz operation
- Synchronous clock enable function
- 20-pin TSSOP
- 2.5 V or 3.3 V operating voltage [1]
- Commercial and industrial operating temperature range

Functional Description

The CY2DP1504 is an ultra-low noise, low-skew, low-propagation delay, 1:4 LVPECL fanout buffer targeted to meet the requirements of high-speed clock distribution applications. The CY2DP1504 can select between separate differential (LVPECL, LVDS, HCSL, or CML) input clock pairs using the IN_SEL pin. The synchronous clock enable function ensures glitch-free output transitions during enable and disable periods. The device has a fully differential internal architecture that is optimized to achieve low additive jitter and low skew at operating frequencies of up to 1.5 GHz.

For a complete list of related documentation, click here.

Logic Block Diagram

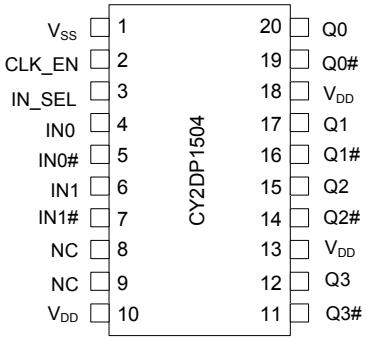


Note
1. Input AC-coupling capacitors are required for voltage-translation applications.

Contents

Pinouts

Figure 1. 20-pin TSSOP pinout



Pin Definitions

Pin No.	Pin Name	Pin Type	Description
1	V_{SS}	Power	Ground
2	CLK_EN	Input	Synchronous clock enable. LVCMOS/LVTTL. When CLK_EN = Low, Q(0:3) outputs are held Low and Q(0:3)# outputs are held High
3	IN_SEL	Input	Input clock select pin. LVCMOS/LVTTL; When IN_SEL = Low, the IN0/IN0# differential input pair is active When IN_SEL = High, the IN1/IN1# differential input pair is active
4	IN0	Input	Differential (LVPECL, HCSL, LVDS, or CML) input clock. Active when IN_SEL = Low
5	IN0#	Input	Differential (LVPECL, HCSL, LVDS, or CML) complementary input clock. Active when IN_SEL = Low
6	IN1	Input	Differential (LVPECL, HCSL, LVDS, or CML) input clock. Active when IN_SEL = High
7	IN1#	Input	Differential (LVPECL, HCSL, LVDS, or CML) complementary input clock. Active when IN_SEL = High
8, 9	NC		No connection
10, 13, 18	V_{DD}	Power	Power supply
11, 14, 16, 19	Q(0:3)#	Output	LVPECL complementary output clocks
12, 15, 17, 20	Q(0:3)	Output	LVPECL output clocks

Absolute Maximum Ratings

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage	Non functional	–0.5	4.6	V
V_{IN}[2]	Input voltage, relative to V_{SS}	Non functional	–0.5	Lesser of 4.0 or V_{DD} + 0.4	V
V_{OUT}[2]	DC output or I/O voltage, relative to V_{SS}	Non functional	–0.5	Lesser of 4.0 or V_{DD} + 0.4	V
T_S	Storage temperature	Non functional	–55	150	°C
ESD_{HBM}	Electrostatic discharge (ESD) protection (Human body model)	JEDEC STD 22-A114-B	2000	–	V
L_U	Latch up		Meets or exceeds JEDEC Spec JESD78B IC Latch up Test		
UL–94	Flammability rating	At 1/8 in	V-0		
MSL	Moisture sensitivity level		3		

Operating Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage	2.5-V supply	2.375	2.625	V
		3.3-V supply	3.135	3.465	V
T_A	Ambient operating temperature	Commercial	0	70	°C
		Industrial	–40	85	°C
t_{PU}	Power ramp time	Power-up time for V_{DD} to reach minimum specified voltage (power ramp must be monotonic).	0.05	500	ms

Note
2. The voltage on any I/O pin cannot exceed the power pin during power up. Power supply sequencing is not required.

DC Electrical Specifications

(V_{DD} = 3.3 V ± 5% or 2.5 V ± 5%; T_A = 0 °C to 70 °C (Commercial) or –40 °C to 85 °C (Industrial))

Parameter	Description	Condition	Min	Max	Unit
I_{DD}	Operating supply current	All LVPECL outputs floating (internal I_{DD})	–	61	mA
V_{IH1}	Input high voltage, differential input clocks IN0 and IN0#, IN1 and IN1#		–	V_{DD} + 0.3	V
V_{IL1}	Input low voltage, differential input clocks IN0 and IN0#, IN1 and IN1#		–0.3	–	V
V_{IH2}	Input high voltage, CLK_EN, IN_SEL	V_{DD} = 3.3 V	2.0	V_{DD} + 0.3	V
V_{IL2}	Input low voltage, CLK_EN, IN_SEL	V_{DD} = 3.3 V	–0.3	0.8	V
V_{IH3}	Input high voltage, CLK_EN, IN_SEL	V_{DD} = 2.5 V	1.7	V_{DD} + 0.3	V
V_{IL3}	Input low voltage, CLK_EN, IN_SEL	V_{DD} = 2.5 V	–0.3	0.7	V
V_{ID_LDVS} [3]	LVDS input differential amplitude	See Figure 2 on page 8	0.4	0.8	V
V_{ID_LVPECL} [3]	LVPECL/CML/HSCL input differential amplitude	See Figure 2 on page 8	0.4	1.0	V
V_{ICM}	Input common mode voltage	See Figure 2 on page 8	0.2	V_{DD} – 0.2	V
I_{IH}	Input high current, all inputs	Input = V_{DD} [4]	–	150	µA
I_{IL}	Input low current, all inputs	Input = V_{SS} [4]	–150	–	µA
V_{OH}	LVPECL output high voltage	Terminated with 50 Ω to V_{DD} – 2.0 [5]	V_{DD} – 1.20	V_{DD} – 0.70	V
V_{OL}	LVPECL output low voltage	Terminated with 50 Ω to V_{DD} – 2.0 [5]	V_{DD} – 2.0	V_{DD} – 1.63	V
R_P	Internal pull-up/pull-down resistance, LVCMOS logic inputs	CLK_EN has pull-up only IN_SEL has pull-down only	60	165	kΩ
C_{IN}	Input capacitance	Measured at 10 MHz; per pin	–	3	pF

Thermal Resistance

Parameter [6]	Description	Test Conditions	20-pin TSSOP	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	80	°C/W
θ_{JC}	Thermal resistance (junction to case)		16	°C/W

Notes
3. V_{ID} minimum of 400 mV is required to meet all output AC Electrical Specifications. The device is functional with V_{ID} minimum of greater than 200 mV.
4. Positive current flows into the input pin, negative current flows out of the input pin.
5. Refer to Figure 3 on page 8.
6. These parameters are guaranteed by design and are not tested.

AC Electrical Specifications

(V_{DD} = 3.3 V ± 5% or 2.5 V ± 5%; T_A = 0 °C to 70 °C (Commercial) or –40 °C to 85 °C (Industrial))

Parameter	Description	Condition	Min	Typ	Max	Unit
F_{IN}	Input frequency	Differential Input	DC	–	1.5	GHz
		Single-ended CMOS Input [7]	DC		250	MHz
F_{OUT}	Output frequency	F_{OUT} = F_{IN}, Differential Input	DC	–	1.5	GHz
		F_{OUT} = F_{IN}, Single-ended CMOS Input [7]	DC	–	250	MHz
V_{PP}	LVPECL differential output voltage peak to peak, single-ended. Terminated with 50 Ω to V_{DD} – 2.0 [8]	Fout = DC to 150 MHz	600	–	–	mV
		Fout = >150 MHz to 1.5 GHz	400	–	–	mV
t_{PD}[9]	Propagation delay differential input pair to differential output pair	Input rise/fall time < 1.5 ns (20% to 80%)	–	–	480	ps
t_{ODC}[10]	Output duty cycle	50% duty cycle at input, Frequency range up to 1 GHz, Differential input	48	–	52	%
		50% duty cycle at input, Frequency range up to 250 MHz, Single-ended CMOS input [7]	45	–	55	%
t_{SK1}[11]	Output-to-output skew	Any output to any output, with same load conditions at DUT	–	–	30	ps
$t_{SK1\ D}$[11]	Device-to-device output skew	Any output to any output between two or more devices. Devices must have the same input and have the same output load.	–	–	150	ps
PN_{ADD}	Additive RMS phase noise, 156.25-MHz input, Rise/fall time < 150 ps (20% to 80%), V_{ID} > 400 mV or Input Swing = 3.0 V [7]	Offset = 1 kHz	–	–	–120	dBc/Hz
		Offset = 10 kHz	–	–	–130	dBc/Hz
		Offset = 100 kHz	–	–	–135	dBc/Hz
		Offset = 1 MHz	–	–	–145	dBc/Hz
		Offset = 10 MHz	–	–	–153	dBc/Hz
		Offset = 20 MHz	–	–	–155	dBc/Hz

Notes
7. Refer to Application Information on page 10.
8. Refer to Figure 3 on page 8.
9. Refer to Figure 4 on page 8.
10. Refer to Figure 5 on page 8.
11. Refer to Figure 6 on page 9.

AC Electrical Specifications (continued)

(V_{DD} = 3.3 V ± 5% or 2.5 V ± 5%; T_A = 0 °C to 70 °C (Commercial) or –40 °C to 85 °C (Industrial))

Parameter	Description	Condition	Min	Typ	Max	Unit
t_{JIT}[12]	Additive RMS phase jitter (random)	156.25 MHz, 12 kHz to 20 MHz offset; input rise/fall time < 150 ps (20% to 80%), V_{ID} > 400 mV	–	–	0.15	ps
		156.25 MHz Sinewave, 12 kHz to 20 MHz offset, input rise/fall time < 150 ps (20% to 80%), Input Swing = 3.0 V [13]	–	–	0.15	ps
t_R, t_F[14]	Output rise/fall time	50% duty cycle at input, 20% to 80% of full swing (V_{OL} to V_{OH}) Input rise/fall time < 1.5 ns (20% to 80%)	–	–	300	ps
t_{SOD}	Time from clock edge to outputs disabled	Synchronous clock enable (CLK_EN) switched Low	–	–	700	ps
t_{SOE}	Time from clock edge to outputs enabled	Synchronous clock enable (CLK_EN) switched High	–	–	700	ps

Notes
12. Refer to Figure 7 on page 9.
13. Refer to Application Information on page 10.
14. Refer to Figure 8 on page 9.

Switching Waveforms

Figure 2. Input Differential and Common Mode Voltages

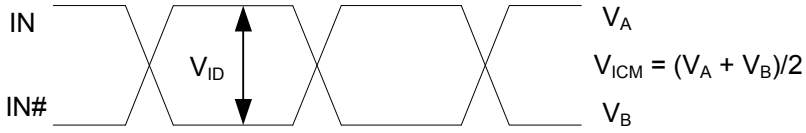


Figure 3. Output Differential Voltage

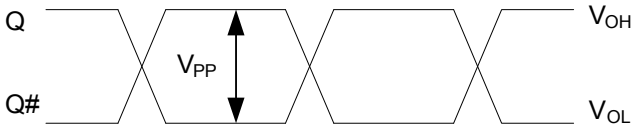


Figure 4. Input to Any Output Pair Propagation Delay

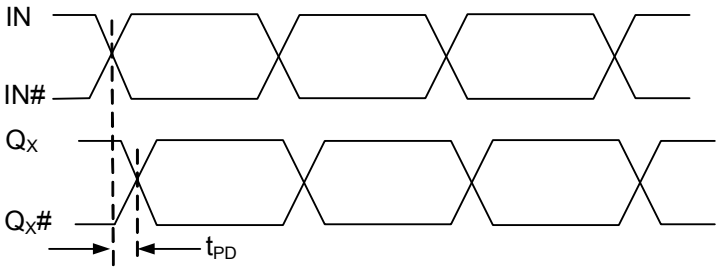
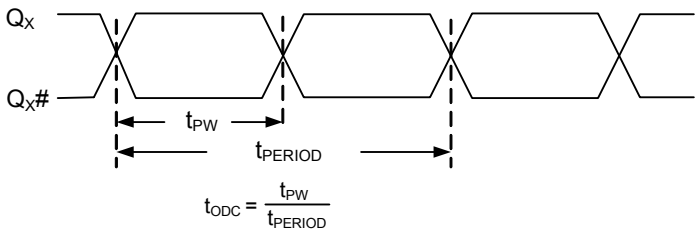


Figure 5. Output Duty Cycle



Switching Waveforms (continued)

Figure 6. Output-to-Output and Device-to-Device Skew

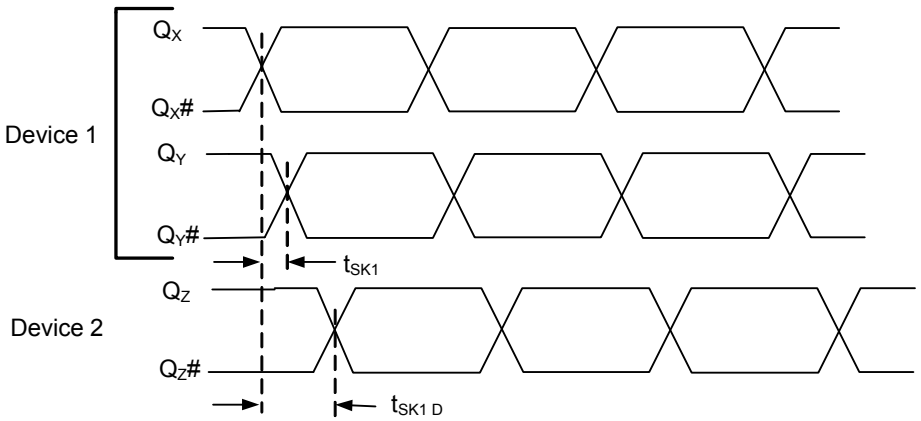


Figure 7. RMS Phase Jitter

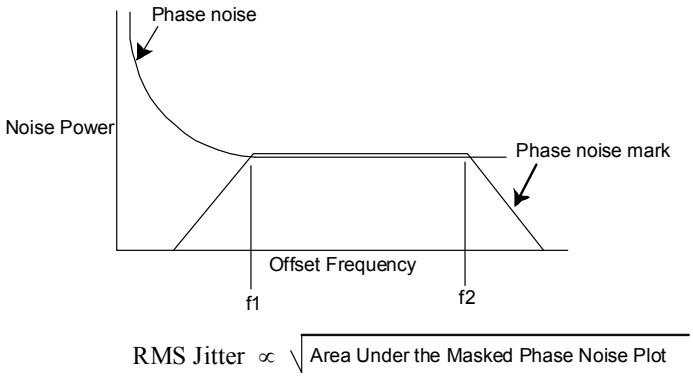


Figure 8. Output Rise/Fall Time

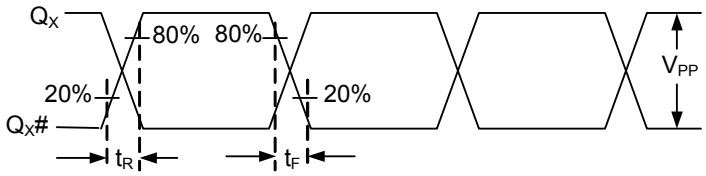
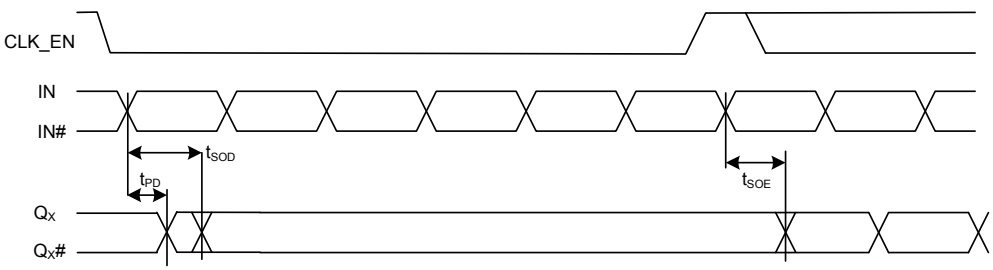


Figure 9. Synchronous Clock Enable Timing



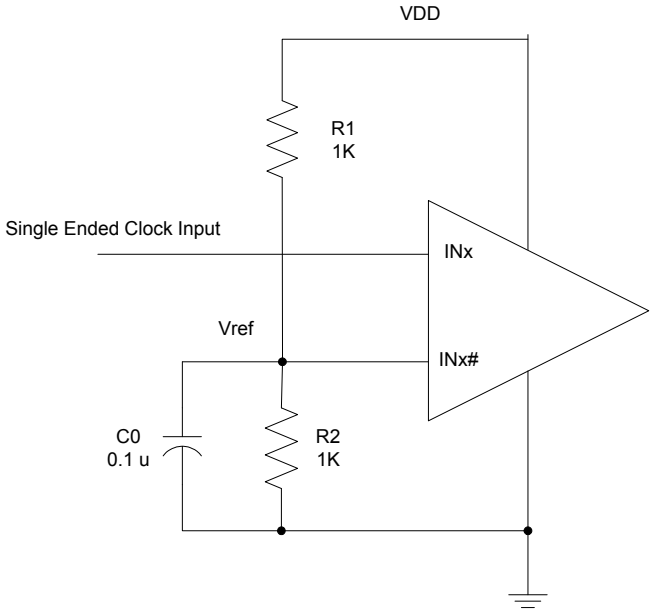
Application Information

CY2DP1504 can be used with a single-ended CMOS input by biasing the Complementary Input Clock (INx#). “True” input pins (INx) of differential input pair can be fed with a single-ended CMOS input signal. The “complementary” input pin (INx#) of the same differential input pair can be biased with Vref.

Figure 10 shows the schematic which can be used to give single-ended CMOS input to the CY2DP1504.

The reference voltage Vref = VDD/2 is generated by the bias resistors R1, R2 and capacitor C0. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the Vref in the center of the input voltage swing. For example, if the input clock swing is 2.5 V and VDD = 3.3 V, Vref should be 1.25 V and R2/R1 = 0.609.

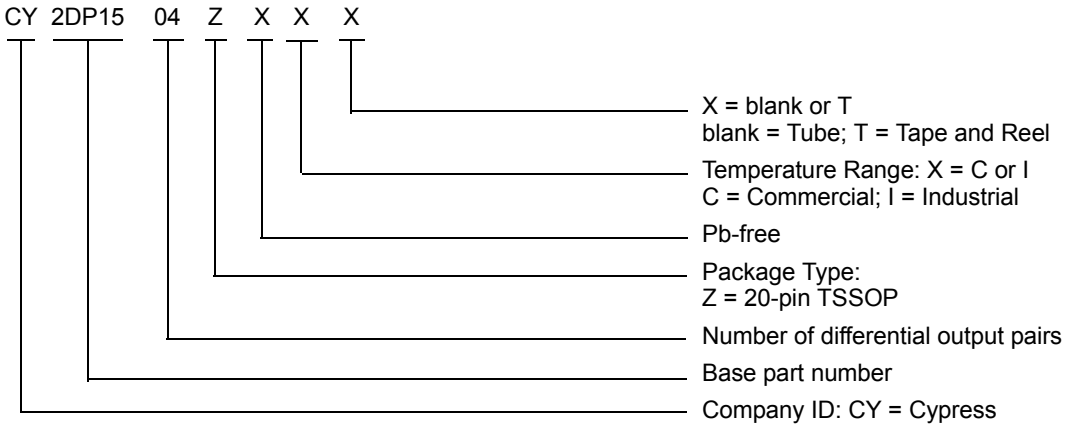
Figure 10. Application Example



Ordering Information

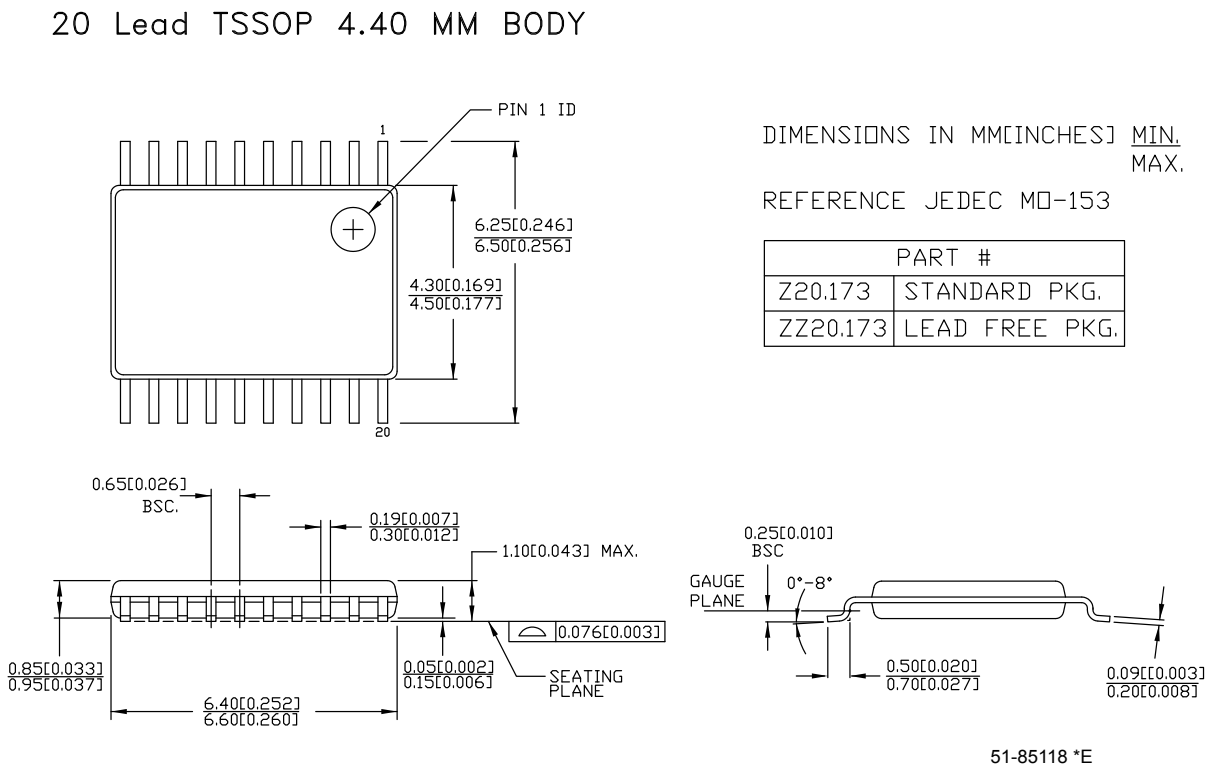
Part Number	Type	Production Flow
Pb-free		
CY2DP1504ZXC	20-pin TSSOP	Commercial, 0 °C to 70 °C
CY2DP1504ZXCT	20-pin TSSOP – Tape and Reel	Commercial, 0 °C to 70 °C
CY2DP1504ZXI	20-pin TSSOP	Industrial, –40 °C to 85 °C
CY2DP1504ZXIT	20-pin TSSOP – Tape and Reel	Industrial, –40 °C to 85 °C

Ordering Code Definitions



Package Diagram

Figure 11. 20-pin TSSOP 4.40 mm Body Z20.173/ZZ20.173 Package Outline, 51-85118



Acronyms

Acronym	Description
ESD	electrostatic discharge
HBM	human body model
HCSL	high-speed current steering logic
JEDEC	joint electron devices engineering council
LVCMOS	low-voltage complementary metal oxide semiconductor
LVPECL	low-voltage positive emitter-coupled logic
LVTTL	low-voltage transistor-transistor logic
RMS	root mean square
TSSOP	thin shrunk small outline package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dBc	decibels relative to the carrier
GHz	gigahertz
Hz	hertz
kΩ	kilohm
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
ms	millisecond
mV	millivolt
MHz	megahertz
ns	nanosecond
Ω	ohm
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY2DP1504, 1:4 LVPECL Fanout Buffer with Selectable Clock Input Document Number: 001-56215				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2782891	CXQ	10/09/09	New data sheet.
*A	2838916	CXQ	01/05/2010	Changed status from “ADVANCE” to “PRELIMINARY”. Changed from 0.34 ps to 0.25 ps maximum additive jitter in “Features” on page 1 and in t_{JIT} in the AC Electrical Specs table on page 5. Added t_{PU} spec to the Operating Conditions table on page 3. Changed max I_{DD} spec in the DC Electrical Specs table on page 4 from 60 mA to 61 mA. Change V_{OH} in the DC Electrical Specs table on page 4: minimum from V_{DD} - 1.15V to V_{DD} - 1.20V; maximum from V_{DD} - 0.75V to V_{DD} - 0.70V. Removed V_{OD} spec from the DC Electrical Specs table on page 4. Added R_P spec in the DC Electrical Specs table on page 4. Min = 60 kΩ, Max = 140 kΩ. Added a measurement definition for C_{IN} in the DC Electrical Specs table on page 4. Added V_{PP} spec to the AC Electrical Specs table on page 5. V_{PP} min = 600 mV for DC - 150 MHz and min = 400 mV for 150 MHz to 1.5 GHz. Changed letter case and some names of all the timing parameters in the AC Electrical Specs table on page 5 to be consistent with EROS. Lowered all additive phase noise mask specs by 3 dB in the AC Electrical Specs table on page 5. Added condition to t_R and t_F specs in the AC Electrical specs table on page 5 that input rise/fall time must be less than 1.5 ns (20% to 80%). Changed letter case and some names of all the timing parameters in Figures 3, 4, 5, 6 and 8, to be consistent with EROS.
*B	3011766	CXQ	08/20/2010	Changed maximum additive jitter from 0.25 ps to 0.11 ps in “Features” on page 1 and in t_{JIT} in the AC Electrical Specs table. Added note 3 to describe I_{IH} and I_{IL} specs. Removed reference to data distribution from “Functional Description”. Changed R_P for differential inputs from 100 kΩ to 150 kΩ in the Logic Block Diagram and from 60 kΩ min / 140 kΩ max to 90 kΩ min / 210 kΩ max in the DC Electrical Specs table. Added max V_{ID} of 1.0V in DC Electrical Specs table. Updated phase noise specs for 1 k/10 k/100 k/1 M/10 M/20 MHz offset to -120/-130/-135/-150/-150/-150dBc/Hz, respectively, in the AC Electrical Specs table. Added “Frequency range up to 1 GHz” condition to t_{ODC} spec. Added Ordering Code Definition. Updated package diagram. Added Acronyms.
*C	3017258	CXQ	08/27/2010	Corrected Output Rise/Fall time diagram.
*D	3100234	CXQ	11/18/2010	Updated Phase jitter to 0.15ps max from 0.11ps max. Changed V_{IN} and V_{OUT} specs from 4.0V to “lesser of 4.0 or V_{DD} + 0.4” Removed 200mA min LU spec, replaced with “Meets or exceeds JEDEC Spec JESD78B IC Latchup Test” Removed R_P spec for differential input clock pins IN_X and IN_X#. Changed C_{IN} condition to “Measured at 10 MHz”. Changed PN_{ADD} specs for 1MHz, 10MHz, and 20MHz offsets. Removed t_S and t_H specs from AC specs table.
*E	3135201	CXQ	01/12/2011	Removed “Preliminary” status heading. Removed resistors from IN_x/IN_x# in Logic Block Diagram. Added Figure 9 to describe T_{SOE} and T_{SOD}.
*F	3090938	CXQ	02/25/2011	Post to external web.

Document History Page (continued)

Document Title: CY2DP1504, 1:4 LVPECL Fanout Buffer with Selectable Clock Input Document Number: 001-56215				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*G	3208968	CXQ	03/29/2011	Changed R_P max from 140 kΩ to 165 kΩ and updated R_P in Logic Block Diagram.
*H	3308039	CXQ	07/11/2011	Updated supported differential input clock types to include LVPECL/LVDS/CML in Features, Functional Description, Pin Definitions, and DC specs table sections. Broke out V_{ID} spec into V_{ID_LVDS} and V_{ID_LVPECL} specs.
*I	3395868	PURU	10/05/11	Updated supported differential input clock types to include HCSL in Features, Pinouts, and DC Electrical Specifications table. Changed Min value of V_{ICM}.
*J	3740406	CINM	09/11/2012	Minor text edits.
*K	3799048	PURU	12/05/2012	Updated Features: Added “Translates any single-ended input signal to 3.3 V LVPECL levels with resistor bias on INx# input”. Updated AC Electrical Specifications: Added Note 7 and Note 13. Added F_{IN} parameter values for “Single Ended CMOS Input” condition (Minimum value = DC, Maximum value = 250 MHz). Added F_{OUT} parameter values for “Single Ended CMOS Input” condition (Minimum value = DC, Maximum value = 250 MHz). Updated t_{PD} parameter (Changed description from “Propagation delay input pair to output pair” to “Propagation delay differential input pair to differential output pair”). Added t_{ODC} parameter values for “Single Ended CMOS Input” condition (Minimum value = 45%, Maximum value = 55%). Updated description of PN_{ADD} parameter (Replaced “Additive RMS phase noise, 156.25-MHz input, Rise/fall time < 150 ps (20% to 80%), V_{ID} > 400 mV” with “Additive RMS phase noise, 156.25-MHz input, Rise/fall time < 150 ps (20% to 80%), V_{ID} > 400 mV or Input Swing = 3.0 V[7]”). Added t_{JIT} parameter values for the Condition “156.25 MHz Sinewave, 12 kHz to 20 MHz offset, input rise/fall time < 150 ps (20% to 80%), Input Swing = 3.0 V [13]” (Maximum value = 0.15 ps). Added Application Information. Updated to new template.
*L	4586288	PURU	12/04/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Package Diagram: spec 51-85118 – Changed revision from *D to *E.
*M	4959240	TAVA	10/12/2015	Updated to new template. Completing Sunset Review.
*N	5267558	PSR	05/13/2016	Added Thermal Resistance. Updated to new template.

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