



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



High Performance LVPECL Oscillator with Frequency Margining – Pin Control

Features

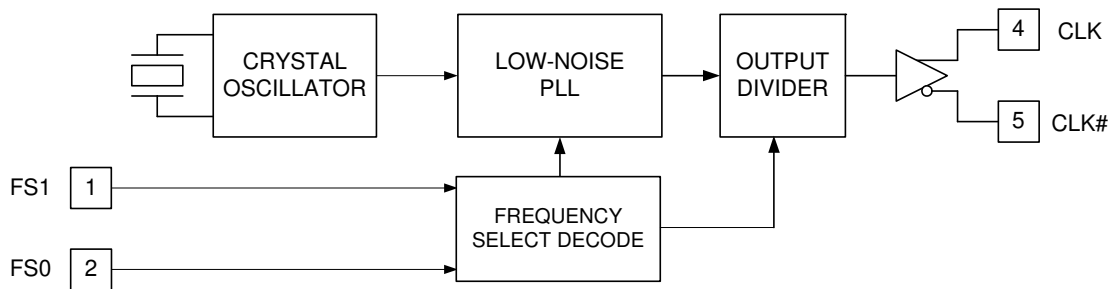
- Low Jitter Crystal Oscillator (XO)
- Less than 1 ps Typical RMS Phase Jitter
- Differential LVPECL Output
- Output Frequency from 50 MHz to 690 MHz
- Two Frequency Margining Control Pins (FS0, FS1)
- Factory Configured or Field Programmable
- Integrated Phase-Locked Loop (PLL)
- Supply Voltage: 3.3 V or 2.5 V
- Pb-Free Package: 5.0 × 3.2 mm LCC
- Commercial and Industrial Temperature Ranges

Functional Description

The CY2XF34 is a high performance and high frequency Crystal Oscillator (XO). It uses a Cypress proprietary low noise PLL to synthesize the frequency from an integrated crystal. The output frequency can be changed through two select pins, allowing easy frequency margin testing in applications.

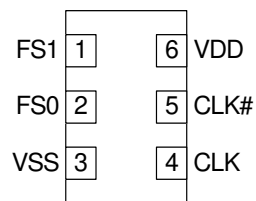
The CY2XF34 is available as a factory configured device or as a field programmable device.

Logic Block Diagram



Pinouts

Figure 1. Pin Diagram - 6-pin Ceramic LCC



Pin Definitions

Pin	Name	I/O Type	Description
1, 2	FS1, FS0	CMOS input	Frequency select
4, 5	CLK, CLK#	LVPECL output	Differential output clock
6	VDD	Power	Supply voltage: 2.5 V or 3.3 V
3	VSS	Power	Ground

Contents

Logic Block Diagram	1	Switching Waveforms	7
Pinouts	1	Termination Circuits	7
Pin Definitions	1	Ordering Information	8
Functional Description	3	Possible Configuration	8
Programming Description	3	Ordering Code Definitions	8
Field Programmable CY2XF34F	3	Package Drawings and Dimensions	9
Factory Configured CY2XF34	3	Acronyms	10
Programming Variables	3	Document Conventions	10
Output Frequencies	3	Units of Measure	10
Industrial Versus Commercial Device Performance	3	Document History Page	11
Phase Noise Versus Jitter Performance	3	Sales, Solutions, and Legal Information	12
Absolute Maximum Conditions	4	Worldwide Sales and Design Support	12
Operating Conditions	4	Products	12
DC Electrical Characteristics	4	PSoC Solutions	12
AC Electrical Characteristics	5		
Typical Output Characteristics	5		

Functional Description

The FS0 and FS1 pins select between four different output frequencies, as shown in [Table 1](#). Frequency margining is a common application for this feature. One frequency is used for the standard operating mode of the device, while the other frequencies are available for margin testing, either during product development or in system manufacturing test.

Table 1. Frequency Select

FS1	FS0	Output Frequency
0	0	Frequency 0
0	1	Frequency 1
1	0	Frequency 2
1	1	Frequency 3

When changing the output frequency, the frequency transition is not guaranteed to be smooth. There can be frequency excursions beyond the start frequency and the new frequency. Glitches and runt pulses are possible, and time must be allowed for the PLL to relock.

Programming Description

The CY2XF34 is a programmable device. Before being used in an application, it must be programmed with the output frequencies and other variables described in a later section. Two different device types are available, each with its own programming flow. They are described in the following sections.

Field Programmable CY2XF34F

Field programmable devices are shipped unprogrammed and must be programmed before being installed on a printed circuit board (PCB). Customers use CyberClocks™ Online Software to specify the device configuration and generate a JEDEC (extension .jed) programming file. Programming of samples and prototype quantities is available using a Cypress programmer. Third party vendors manufacture programmers for small to large volume applications. Cypress's value added distribution partners also provide programming services. Field programmable devices are designated with an "F" in the part number. They are intended for quick prototyping and inventory reduction. The CY2XF34 is One Time Programmable (OTP).

The software is located at [CyberClocks\(TM\) Online Software](#)

Factory Configured CY2XF34

For customers wanting ready-to-use devices, the CY2XF34 is available with no field programming required. All requests are submitted to the local Cypress Field Application Engineer (FAE) or sales representative. After the request is processed, you receive a new part number, samples, and datasheet with the programmed values. This part number is used for additional sample requests and production orders.

Programming Variables

Output Frequencies

The CY2XF34 is programmed with up to four independent output frequencies, which are then selected using the FS0 and FS1 pins. The device can synthesize frequencies to a resolution of 1 part per million (ppm), but the actual accuracy of the output frequency is limited by the accuracy of the integrated reference crystal.

The CY2XF34 has an output frequency range of 50 MHz to 690 MHz, but the range is not continuous. The CY2XF34 cannot generate frequencies in the ranges of 521 MHz to 529 MHz, and 596 MHz to 617 MHz.

Industrial Versus Commercial Device Performance

Industrial and Commercial devices have different internal crystals. This has a potentially significant impact on performance levels for applications requiring the lowest possible phase noise. CyberClocks Online Software displays expected performance for both options.

Phase Noise Versus Jitter Performance

In most cases, the device configuration for optimal phase noise performance is different from the device configuration for optimal cycle to cycle or period jitter. CyberClocks Online Software includes algorithms to optimize performance for either parameter.

Table 2. Device Programming Variables

Variable
Output Frequency 0 (Power on default)
Output Frequency 1
Output Frequency 2
Output Frequency 3
Optimization (phase noise or jitter)
Temperature range (Commercial or Industrial)

Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V _{DD}	Supply voltage		-0.5	4.4	V
V _{IN} ^[1]	Input voltage, DC	Relative to V _{SS}	-0.5	V _{DD} + 0.5	V
T _S	Temperature, storage	Non operating	-55	135	°C
T _J	Temperature, Junction		-40	135	°C
ESD _{HBM}	ESD Protection (Human Body Model)	JEDEC STD 22-A114-B	2000	-	V
Θ _{JA} ^[2]	Thermal resistance, Junction to Ambient	0 m/s airflow		64	°C/W

Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V _{DD}	3.3 V Supply voltage range	3.135	3.3	3.465	V
	2.5 V Supply voltage range	2.375	2.5	2.625	V
T _{PU}	Power Up Time for V _{DD} to Reach Minimum Specified Voltage (Power Ramp is Monotonic)	0.05	-	500	ms
T _A	Ambient temperature (Commercial)	0	-	70	°C
	Ambient temperature (Industrial)	-40	-	85	°C

DC Electrical Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
I _{DD} ^[3]	Operating supply current	V _{DD} = 3.465 V, CLK = 150 MHz, output terminated	-	-	150	mA
		V _{DD} = 2.625 V, CLK = 150 MHz, output terminated	-	-	145	mA
V _{OH}	LVPECL high output voltage	V _{DD} = 3.3 V or 2.5 V, R _{TERM} = 50 Ω to V _{DD} - 2.0 V	V _{DD} - 1.15	-	V _{DD} - 0.75	V
V _{OL}	LVPECL low output voltage	V _{DD} = 3.3 V or 2.5 V, R _{TERM} = 50 Ω to V _{DD} - 2.0 V	V _{DD} - 2.0	-	V _{DD} - 1.625	V
V _{OD1}	LVPECL output voltage swing (V _{OH} - V _{OL})	V _{DD} = 3.3 V or 2.5 V, R _{TERM} = 50 Ω to V _{DD} - 2.0 V	600	-	1000	mV
V _{OD2}	LVPECL output voltage swing (V _{OH} - V _{OL})	V _{DD} = 2.5 V, R _{TERM} = 50 Ω to V _{DD} - 1.5 V	500	-	1000	mV
V _{OCM}	LVPECL output common mode Voltage ((V _{OH} + V _{OL})/2)	V _{DD} = 2.5 V, R _{TERM} = 50 Ω to V _{DD} - 1.5 V	1.2	-	-	V
V _{IH}	Input high voltage		0.7 × V _{DD}	-	-	V
V _{IL}	Input low voltage		-	-	0.3 × V _{DD}	V
I _{IH0}	Input high current, FS0 pin	Input = V _{DD}	-	-	115	μA
I _{IH1}	Input high current, FS1 pin	Input = V _{DD}	-	-	10	μA
I _{IL0}	Input low current, FS0 pin	Input = V _{SS}	-50	-	-	μA
I _{IL1}	Input low current, FS1 pin	Input = V _{SS}	-20	-	-	μA

Notes

- The voltage on any input or IO pin cannot exceed the power pin during power up.
- Simulated. The board is derived from the JEDEC multilayer standard. It measures 76 × 114 × 1.6 mm and has 4-layers of copper (2/1/1/2 oz.). The internal layers are 100% copper planes, while the top and bottom layers have 50% metalization. No vias are included in the model.
- I_{DD} includes ~24 mA of current that is dissipated externally in the output termination resistors.

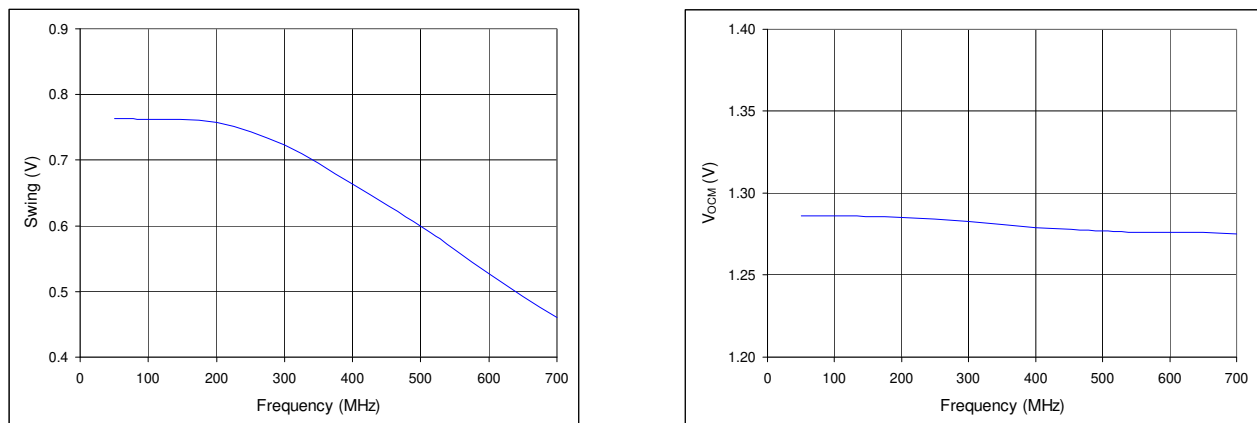
DC Electrical Characteristics (continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
$C_{IN0}^{[4]}$	Input Capacitance, FS0 pin		–	15	–	pF
$C_{IN1}^{[4]}$	Input Capacitance, FS1 pin		–	4	–	pF

AC Electrical Characteristics

 The AC Electrical Characteristics for part CY2XF34 are as follows ^[4]

Parameter	Description	Condition	Min	Typ	Max	Unit
F_{OUT}	Output Frequency ^[5]		50	–	690	MHz
FSC	Frequency Stability, commercial devices ^[6]	$T_A = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$	–	–	± 35	ppm
FSI	Frequency Stability, industrial devices ^[6]	$T_A = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$	–	–	± 55	ppm
AG	Aging, 10 years		–	–	± 15	ppm
T_{DC}	Output Duty Cycle	$F \leq 450\text{ MHz}$, measured at zero crossing	45	50	55	%
		$F > 450\text{ MHz}$, measured at zero crossing	40	50	60	%
T_R, T_F	Output Rise and Fall Time	20% and 80% of full output swing	0.2	0.4	1.0	ns
T_{LOCK}	Startup Time	Time for CLK to reach valid frequency measured from the time $V_{DD} = V_{DD(min)}$	–	–	10	ms
T_{LFS}	Re-lock Time	Time for CLK to reach valid frequency from FS0 or FS1 pin change	–	–	10	ms
$T_{Jitter(\phi)}$	RMS Phase Jitter (Random)	$f_{OUT} = 106.25\text{ MHz}$ (12 kHz–20 MHz)	–	1	–	ps

Typical Output Characteristics
Figure 2. 2.5V Supply and Termination to $V_{DD} = 1.5\text{ V}$, minimum V_{DD} and maximum T_A

Notes

4. Not 100% tested, guaranteed by design and characterization.
5. This parameter is specified in CyberClocks Online software.
6. Frequency stability is the maximum variation in frequency from F_0 . It includes initial accuracy, plus variation from temperature and supply voltage.

Figure 3. 2.5 V Supply and Termination to $V_{DD}-2$ V, minimum V_{DD} and maximum T_A

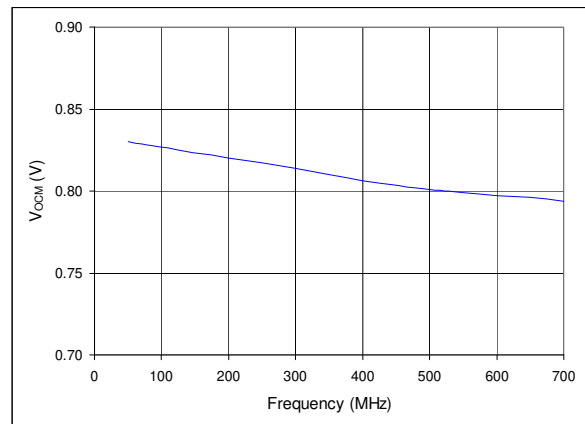
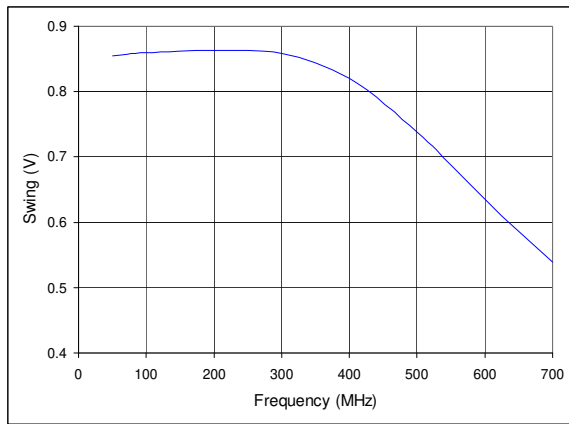
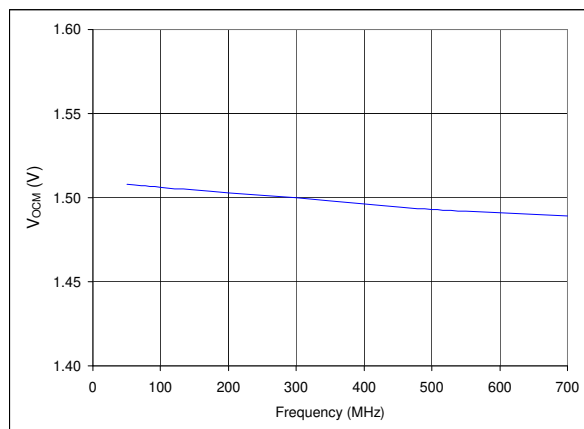
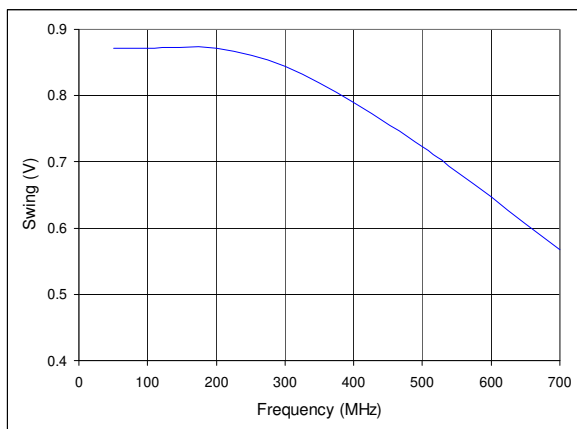


Figure 4. 3.3 V Supply and Termination to $V_{DD}-2$ V, minimum V_{DD} and maximum T_A



Switching Waveforms

Figure 5. Output DC Parameters

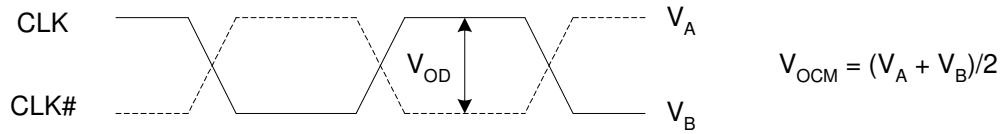


Figure 6. Duty Cycle Timing

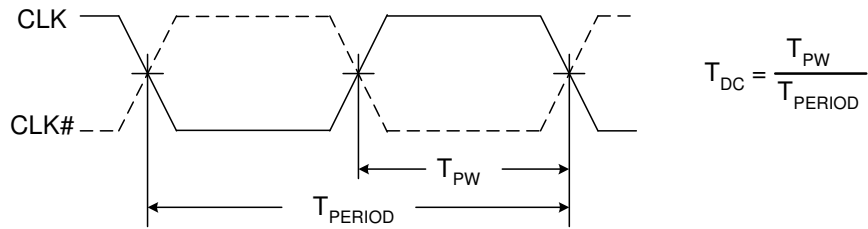
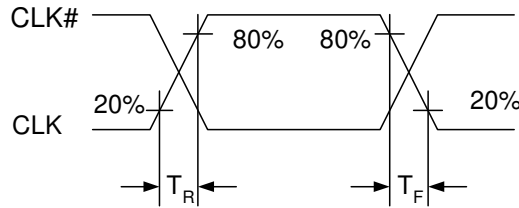
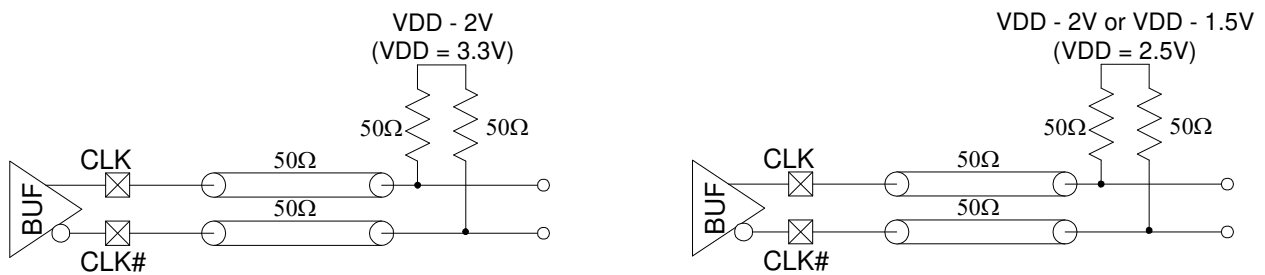


Figure 7. Output Rise and Fall Time



Termination Circuits

Figure 8. LVPECL Termination



Ordering Information

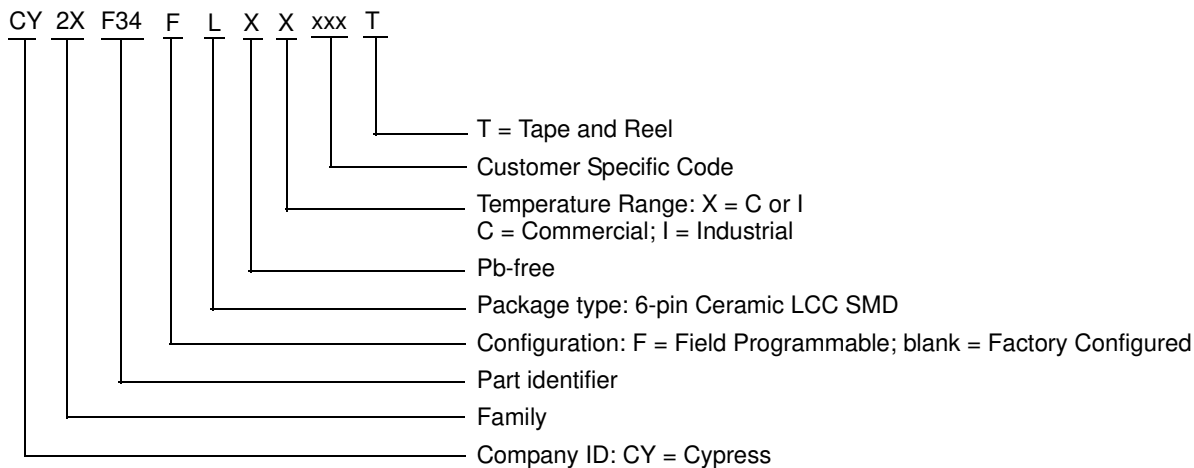
Part Number	Configuration	Package Description	Product Flow
Pb-Free			
CY2XF34FLXCT	Field programmable	6-pin ceramic LCC SMD - Tape and Reel	Commercial, 0 °C to 70 °C
CY2XF34FLXIT	Field programmable	6-pin ceramic LCC SMD - Tape and Reel	Industrial, -40 °C to 85 °C

Possible Configuration

Some product offerings are factory programmed customer specific devices with customized part numbers. The Possible Configurations table shows the available device types, but not complete part numbers. Contact your local Cypress FAE or Sales Representative for more information.

Part Number ^[7]	Configuration	Package Description	Product Flow
Pb-Free			
CY2XF34LXCxxxT	Factory configured	6-pin ceramic LCC SMD - Tape and Reel	Commercial, 0 °C to 70 °C
CY2XF34LXIxxxT	Factory configured	6-pin ceramic LCC SMD - Tape and Reel	Industrial, -40 °C to 85 °C

Ordering Code Definitions

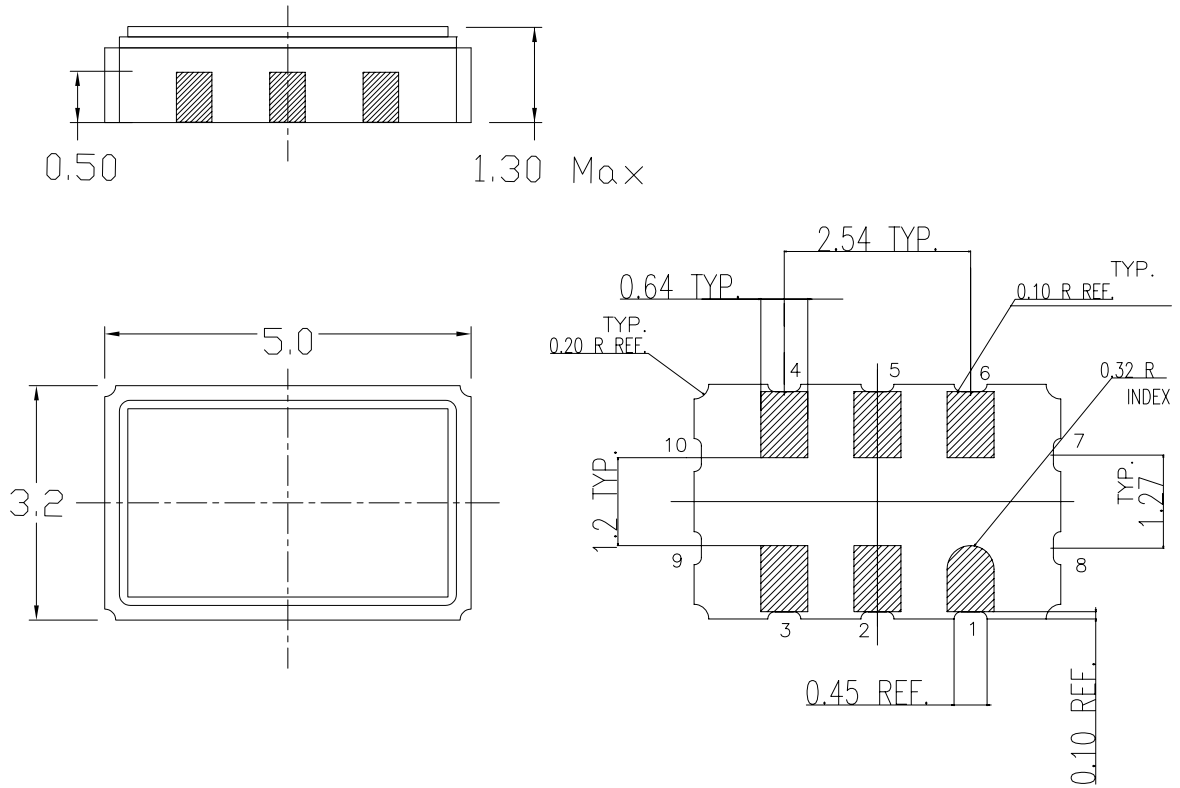


Note

7. "xxx" is a factory assigned code that identifies the programming option. For more details, contact your local Cypress FAE or Sales Representative.

Package Drawings and Dimensions

Figure 9. 6-pin 3.2 x 5.0 mm Ceramic LCC LZ06A



Dimensions in mm
 General Tolerance: ± 0.15MM
 Kyocera dwg ref KD-VA6432-A
 Package Weight ~ 0.12 grams

001-10044 *A

Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
ESD	electrostatic discharge
FAE	field application engineer
I/O	input/output
OTP	one time programmable
PCB	printed circuit board
PLL	phase-locked loop
SMD	surface mounted devices

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree celsius
μA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
MHz	megahertz
ns	nanosecond
pF	picofarad
ps	picosecond
ppm	parts per million
V	volts
W	watts
%	percent
Ω	ohms

Document History Page

Document Title: CY2XF34 High Performance LVPECL Oscillator with Frequency Margining – Pin Control Document Number: 001-53149				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2704379	KVM/PYRS	05/11/09	New datasheet
*A	2734005	WWZ	07/09/09	Post to external web
*B	2761926	KVM	09/10/09	Revised maximum output rise and fall times Added Absolute Maximum Conditions table
*C	2898472	KVM	03/24/2010	Moved 'xxx' parts to Possible Configurations table. Updated package diagram.
*D	3199911	BASH	03/18/2011	Changed status from Preliminary to Final. Added Ordering Code Definitions . Added Acronyms and Units of Measure . Updated in new template.
*E	3281222	BASH	06/13/2011	Swapped FS0 and FS1 in Logic Block Diagram, Pinouts and Pin Definition on page 1.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc
	cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions
PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2009-2011. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.