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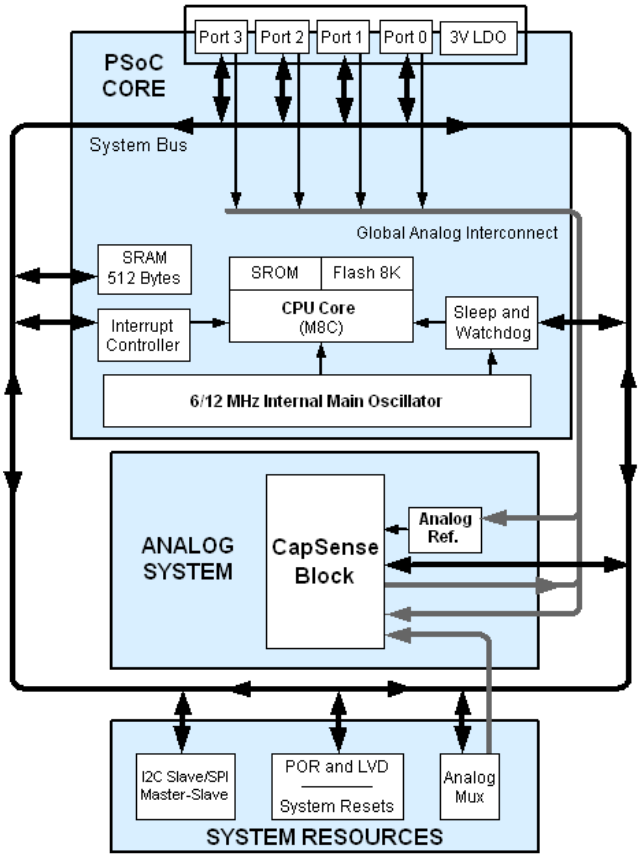
CY8C20234
CY8C20334 and CY8C20434

Features

- **Low Power CapSense Block**
  - Configurable Capacitive Sensing Elements
  - Supports Combination of CapSense Buttons, Sliders, Touchpads and Proximity Sensors
- **Powerful Harvard Architecture Processor**
  - M8C Processor Speeds Running up to 12 MHz
  - Low Power at High Speed
  - 2.4V to 5.25V Operating Voltage
  - Industrial Temperature Range: -40°C to +85°C
- **Flexible On-Chip Memory**
  - 8K Flash Program Storage 50,000 Erase/Write Cycles
  - 512 Bytes SRAM Data Storage
  - Partial Flash Updates
  - Flexible Protection Modes
  - Interrupt Controller
  - In-System Serial Programming (ISSP)
- **Complete Development Tools**
  - Free Development Tool (PSoC Designer™)
  - Full-Featured, In-Circuit Emulator and Programmer
  - Full Speed Emulation
  - Complex Breakpoint Structure
  - 128K Trace Memory
- **Precision, Programmable Clocking**
  - Internal ±5.0% 6/12 MHz Main Oscillator
  - Internal Low Speed Oscillator at 32 kHz for Watchdog and Sleep
- **Programmable Pin Configurations**
  - Pull Up, High Z, Open Drain, CMOS Drive Modes on All GPIO
  - Up to 28 Analog Inputs on GPIO
  - Configurable Inputs on All GPIO
  - Selectable, Regulated Digital IO on Port 1
    - -- 3.0V, 20 mA Total Port 1 Source Current
    - -- 5 mA Strong Drive Mode on Port 1
- **Versatile Analog Mux**
  - Common Internal Analog Bus
  - Simultaneous Connection of IO Combinations
  - Comparator Noise Immunity
  - Low-Dropout Voltage Regulator for the Analog Array
- **Additional System Resources**
  - Configurable Communication Speeds
    - -- I2C: Selectable to 50 kHz, 100 kHz or 400 kHz
    - -- SPI : Configurable between 46.9 kHz and 3 MHz
  - I^2C™ Slave
  - SPI Master and SPI Slave
  - Watchdog and Sleep Timers
  - Internal Voltage Reference
  - Integrated Supervisory Circuit



PSoC® Functional Overview

The PSoC family consists of many *Mixed-Signal Array with On-Chip Controller* devices. These devices are designed to replace multiple traditional MCU-based system components with one, low cost single-chip programmable component. A PSoC device includes configurable analog and digital blocks, as well as programmable interconnect. This architecture allows the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable IO are included in a range of convenient pinouts.

The PSoC architecture for this device family, as illustrated on the left, is comprised of three main areas: the Core, the System Resources, and the CapSense Analog System. A common, versatile bus allows connection between IO and the analog system. Each CY8C20x34 PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 28 general purpose IO (GPIO) are also included. The GPIO provide access to the MCU and analog mux.

The PSoC Core

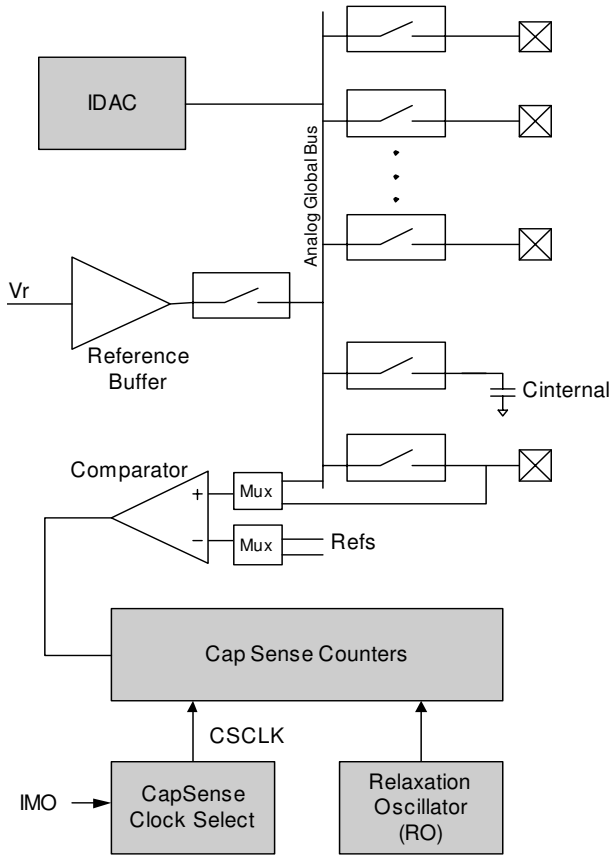
The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO (internal main oscillator) and ILO (internal low speed oscillator). The CPU core, called the M8C, is a powerful processor with speeds up to 12 MHz. The M8C is a two-MIPS, 8-bit Harvard architecture microprocessor.

System Resources provide additional capability, such as a configurable I2C slave/SPI master-slave communication interface and various system resets supported by the M8C.

The Analog System is composed of the CapSense PSoC block and an internal 1.8V analog reference, which together support capacitive sensing of up to 28 inputs.

The CapSense Analog System

The Analog System contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins can be completed quickly and easily across multiple ports.



Analog System Block Diagram

The Analog Multiplexer System

The Analog Mux Bus can connect to every GPIO pin. Pins can be connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Complex capacitive sensing interfaces, such as sliders and touchpads.
- Chip-wide mux that allows analog input from any IO pin.
- Crosspoint connection between any IO pin combinations.

Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. Brief statements describing the merits of each system resource are presented below.

- The I2C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over 3 or 4 wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.8V reference provides an absolute reference for capacitive sensing.
- The 5V maximum input, 3V fixed output, low-dropout regulator (LDO) provides regulation for IOs. A register-controlled bypass mode allows the user to disable the LDO.

Getting Started

The quickest path to understanding the PSoC silicon is by reading this data sheet and using the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications. For in-depth information, along with detailed programming information, reference the *PSoC Mixed-Signal Array Technical Reference Manual*, which can be found on http://www.cypress.com/psoc.

For up-to-date Ordering, Packaging, and Electrical Specification information, reference the latest PSoC device data sheets on the web at http://www.cypress.com.

Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store contains development kits, **C** compilers, and all accessories for PSoC development. Go to the Cypress Online Store web site at http://www.cypress.com, click the Online Store shopping cart icon at the bottom of the web page, and click *PSoC (Programmable System-on-Chip)* to view a current list of available items.

Technical Training

Free PSoC technical training is available for beginners and is taught by a marketing or application engineer over the phone. PSoC training classes cover designing, debugging, advanced analog, as well as application-specific classes covering topics such as PSoC and the LIN bus. Go to http://www.cypress.com, click on Design Support located on the left side of the web page, and select Technical Training for more details.

Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to http://www.cypress.com, click on Design Support located on the left side of the web page, and select CYPros Consultants.

Technical Support

PSoC application engineers take pride in fast and accurate response. They can be reached with a 4-hour guaranteed response at http://www.cypress.com/support/login.cfm.

Application Notes

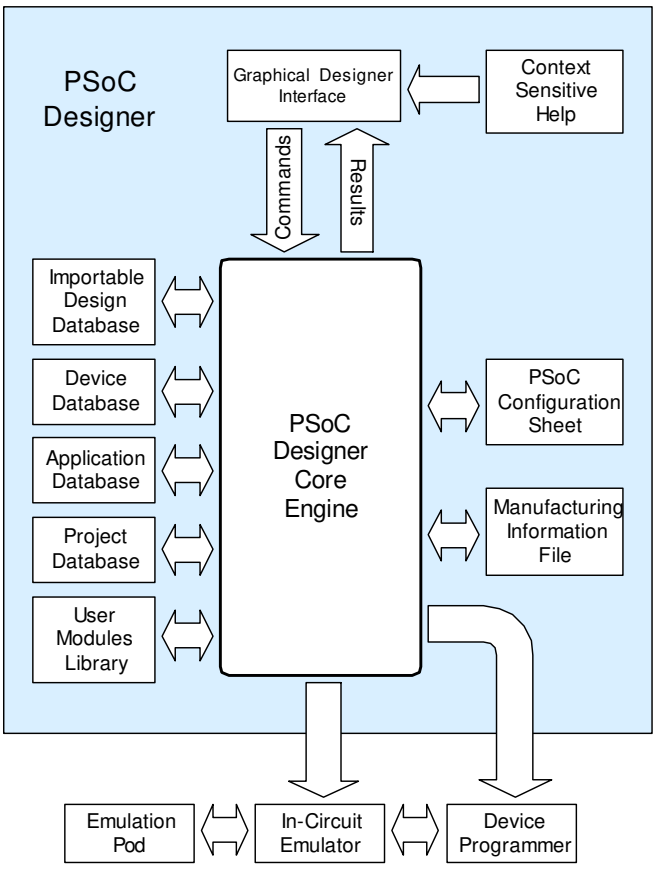
A long list of application notes will assist you in every aspect of your design effort. To view the PSoC application notes, go to the http://www.cypress.com web site and select Application Notes under the Design Resources list located in the center of the web page. Application notes are sorted by date by default.

Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE and application runs on Windows NT 4.0, Windows 2000, Windows Millennium (Me), or Windows XP. (Reference the PSoC Designer Functional Flow diagram below.)

PSoC Designer helps the customer to select an operating configuration for the PSoC, write application code that uses the PSoC, and debug the application. This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and the CYASM macro assembler for the CPUs.

PSoC Designer also supports a high-level C language compiler developed specifically for the devices in the family.



PSoC Designer Subsystems

PSoC Designer Software Subsystems

Device Editor

The device editor subsystem allows the user to select different onboard analog and digital components called user modules using the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration allows for changing configurations at run time.

PSoC Designer sets up power-on initialization tables for selected PSoC block configurations and creates source code for an application framework. The framework contains software to operate the selected components and, if the project uses more than one operating configuration, contains routines to switch between different sets of PSoC block configurations at run time. PSoC Designer can print out a configuration sheet for a given project configuration for use during application programming in conjunction with the Device Data Sheet. Once the framework is generated, the user can add application-specific code to flesh out the framework. It's also possible to change the selected components and regenerate the framework.

Application Editor

In the Application Editor you can edit your C language and Assembly language source code. You can also assemble, compile, link, and build.

Assembler. The macro assembler allows the assembly code to be merged seamlessly with C code. The link libraries automatically use absolute addressing or can be compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compiler. A C language compiler is available that supports the PSoC family of devices. Even if you have never worked in the C language before, the product quickly allows you to create complete C programs for the PSoC family devices.

The embedded, optimizing C compiler provides all the features of C tailored to the PSoC architecture. It comes complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing the designer to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read the program and read and write data memory, read and write IO registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

Hardware Tools

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and will operate with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

Designing with User Modules

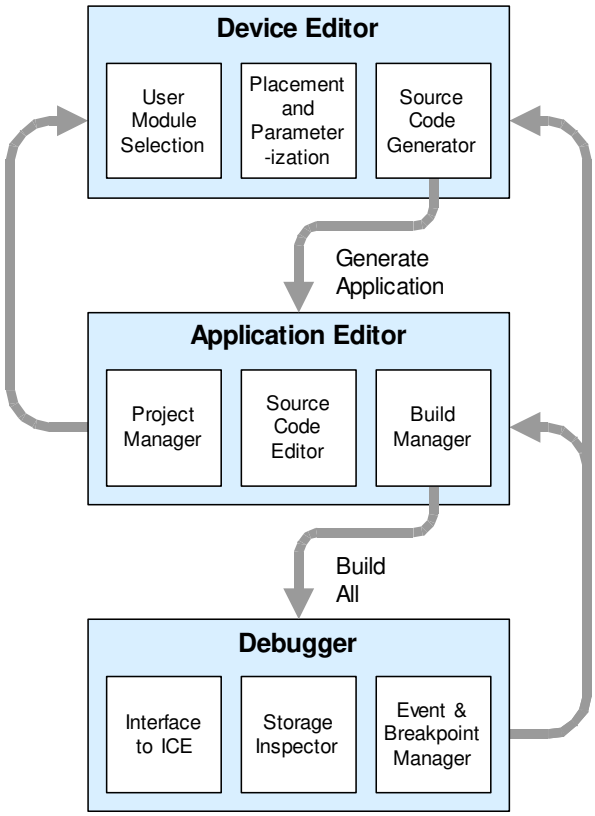
The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. Each block has several registers that determine its function and connectivity to other blocks, multiplexers, buses and to the IO pins. Iterative development cycles permit you to adapt the hardware as well as the software. This substantially lowers the risk of having to select a different part to meet the final design requirements.

To speed the development process, the PSoC Designer Integrated Development Environment (IDE) provides a library of pre-built, pre-tested hardware peripheral functions, called “User Modules.” User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and mixed signal varieties.

Each user module establishes the basic register settings that implement the selected function. It also provides parameters that allow you to tailor its precise configuration to your particular application. For example, a Pulse Width Modulator User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. User modules also provide tested software to cut your development time. The user module application programming interface (API) provides high-level functions to control and respond to hardware events at run time. The API also provides optional interrupt service routines that you can adapt as needed.

The API functions are documented in user module data sheets that are viewed directly in the PSoC Designer IDE. These data sheets explain the internal operation of the user module and provide performance specifications. Each data sheet describes the use of each user module parameter and documents the setting of each register controlled by the user module.

The development process starts when you open a new project and bring up the Device Editor, a graphical user interface (GUI) for configuring the hardware. You pick the user modules you need for your project and map them onto the PSoC blocks with point-and-click simplicity. Next, you build signal chains by interconnecting user modules to each other and the IO pins. At this stage, you also configure the clock source connections and enter parameter values directly or by selecting values from drop-down menus. When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Application” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the high-level user module API functions.



User Module and Source Code Development Flows

The next step is to write your main program, and any sub-routines using PSoC Designer’s Application Editor subsystem. The Application Editor includes a Project Manager that allows you to open the project source code files (including all generated code files) from a hierarchal view. The source code editor provides syntax coloring and advanced edit features for both C and assembly language. File search capabilities include simple string searches and recursive “grep-style” patterns. A single mouse click invokes the Build Manager. It employs a professional-strength “makefile” system to automatically analyze all file dependencies and run the compiler and assembler as necessary. Project-level options control optimization strategies used by the compiler and linker. Syntax errors are displayed in a console window. Double clicking the error message takes you directly to the offending line of source code. When all is correct, the linker builds a HEX file image suitable for programming.

The last step in the development process takes place inside the PSoC Designer’s Debugger subsystem. The Debugger downloads the HEX image to the In-Circuit Emulator (ICE) where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Acronym	Description
AC	alternating current
API	application programming interface
CPU	central processing unit
DC	direct current
GPIO	general purpose IO
GUI	graphical user interface
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
IO	input/output
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip™
SLIMO	slow IMO
SRAM	static random access memory

Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 2-1 on page 11 lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexidecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexidecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (e.g., 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or 0x are decimal.

Table of Contents

For an in depth discussion and more information on your PSoC device, obtain the *PSoC Mixed-Signal Array Technical Reference Manual* on http://www.cypress.com. This document is organized into the following chapters and sections.

1. Pin Information

This chapter describes, lists, and illustrates the CY8C20234, CY8C20334 and CY8C20434 PSoC device pins and pinout configurations.

1.1 Pinouts

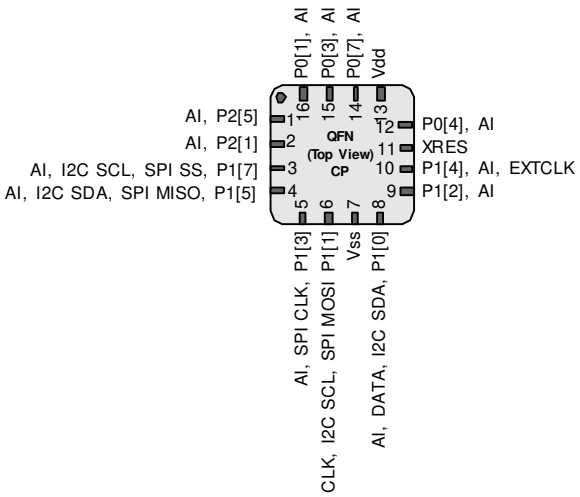
The CY8C20x34 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital IO and connection to the common analog bus. However, Vss, Vdd, and XRES are not capable of Digital IO.

1.1.1 16-Pin Part Pinout

Table 1-1. 16-Pin Part Pinout (QFN)**

Pin No.	Type		Name	Description
	Digital	Analog		
1	IO	I	P2[5]	
2	IO	I	P2[1]	
3	IOH	I	P1[7]	I2C SCL, SPI SS.
4	IOH	I	P1[5]	I2C SDA, SPI MISO.
5	IOH	I	P1[3]	SPI CLK.
6	IOH	I	P1[1]	CLK*, I2C SCL, SPI MOSI.
7	Power		Vss	Ground connection.
8	IOH	I	P1[0]	DATA*, I2C SDA.
9	IOH	I	P1[2]	
10	IOH	I	P1[4]	Optional external clock input (EXTCLK).
11	Input		XRES	Active high external reset with internal pull down.
12	IO	I	P0[4]	
13	Power		Vdd	Supply voltage.
14	IO	I	P0[7]	
15	IO	I	P0[3]	Integrating input.
16	IO	I	P0[1]	
CP	Power		Vss	Center pad must be connected to ground.

CY8C20234 16-Pin PSoC Device



LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive.

* These are the ISSP pins, which are not High Z at POR (Power On Reset).

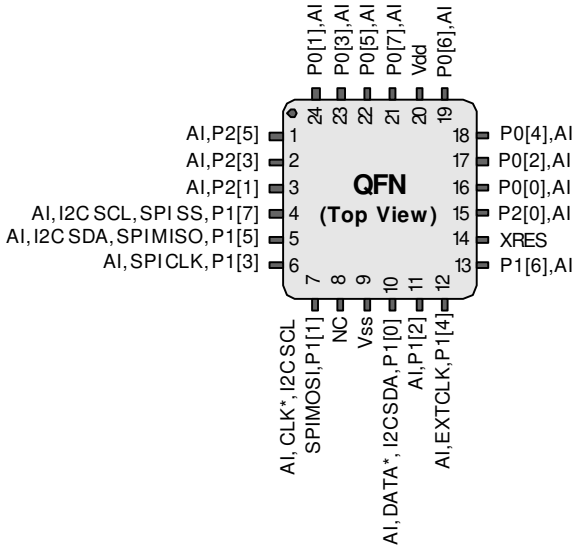
** The center pad (CP) on the QFN package should be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

1.1.2 24-Pin Part Pinout

Table 1-2. 24-Pin Part Pinout (QFN)**

Pin No.	Type		Name	Description
	Digital	Analog		
1	IO	I	P2[5]	
2	IO	I	P2[3]	
3	IO	I	P2[1]	
4	IOH	I	P1[7]	I2C SCL, SPI SS.
5	IOH	I	P1[5]	I2C SDA, SPI MISO.
6	IOH	I	P1[3]	SPI CLK.
7	IOH	I	P1[1]	CLK*, I2C SCL, SPI MOSI.
8			NC	No connection.
9	Power		Vss	Ground connection.
10	IOH	I	P1[0]	DATA*, I2C SDA.
11	IOH	I	P1[2]	
12	IOH	I	P1[4]	Optional external clock input (EXTCLK).
13	IOH	I	P1[6]	
14	Input		XRES	Active high external reset with internal pull down.
15	IO	I	P2[0]	
16	IO	I	P0[0]	
17	IO	I	P0[2]	
18	IO	I	P0[4]	
19	IO	I	P0[6]	Analog bypass.
20	Power		Vdd	Supply voltage.
21	IO	I	P0[7]	
22	IO	I	P0[5]	
23	IO	I	P0[3]	Integrating input.
24	IO	I	P0[1]	
CP	Power		Vss	Center pad must be connected to ground.

CY8C20334 24-Pin PSoC Device



LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive.

* These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Mixed-Signal Array Technical Reference Manual* for details.

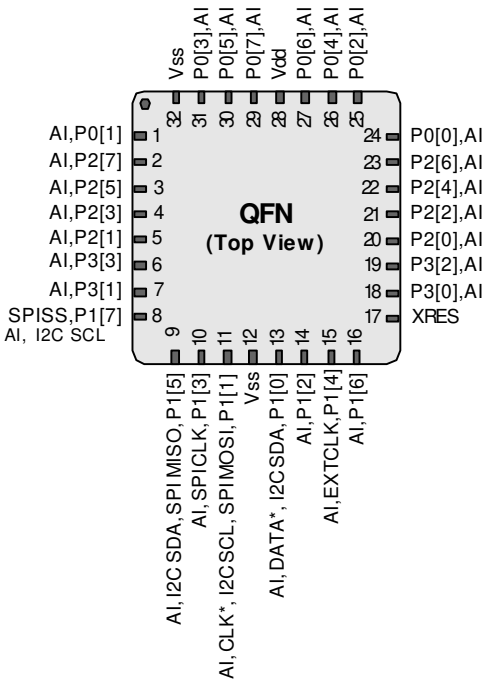
** The center pad on the QFN package should be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

1.1.3 32-Pin Part Pinout

Table 1-3. 32-Pin Part Pinout (QFN)**

Pin No.	Type		Name	Description
	Digital	Analog		
1	IO	I	P0[1]	
2	IO	I	P2[7]	
3	IO	I	P2[5]	
4	IO	I	P2[3]	
5	IO	I	P2[1]	
6	IO	I	P3[3]	
7	IO	I	P3[1]	
8	IOH	I	P1[7]	I2C SCL, SPI SS.
9	IOH	I	P1[5]	I2C SDA, SPI MISO.
10	IOH	I	P1[3]	SPI CLK.
11	IOH	I	P1[1]	CLK*, I2C SCL, SPI MOSI.
12	Power		Vss	Ground connection.
13	IOH	I	P1[0]	DATA*, I2C SDA.
14	IOH	I	P1[2]	
15	IOH	I	P1[4]	Optional external clock input (EXTCLK).
16	IOH	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull down.
18	IO	I	P3[0]	
19	IO	I	P3[2]	
20	IO	I	P2[0]	
21	IO	I	P2[2]	
22	IO	I	P2[4]	
23	IO	I	P2[6]	
24	IO	I	P0[0]	
25	IO	I	P0[2]	
26	IO	I	P0[4]	
27	IO	I	P0[6]	Analog bypass.
28	Power		Vdd	Supply voltage.
29	IO	I	P0[7]	
30	IO	I	P0[5]	
31	IO	I	P0[3]	Integrating input.
32	Power		Vss	Ground connection.
CP	Power		Vss	Center pad must be connected to ground.

CY8C20434 32-Pin PSoC Device



LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive.

* These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Mixed-Signal Array Technical Reference Manual* for details.

** The center pad on the QFN package should be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

1.1.4 48-Pin OCD Part Pinout

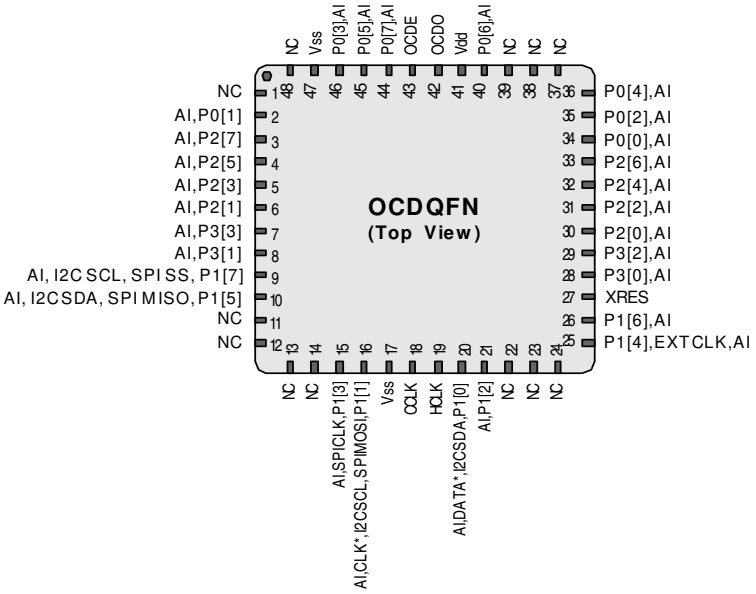
The 48-pin QFN part table and drawing below is for the CY8C20000 On-Chip Debug (OCD) PSoC device.

Note This part is only used for in-circuit debugging. It is NOT available for production

Table 1-4. 48-Pin OCD Part Pinout (QFN)**

Pin No.	Digital	Analog	Name	Description
1			NC	No connection.
2	IO	I	P0[1]	
3	IO	I	P2[7]	
4	IO	I	P2[5]	
5	IO	I	P2[3]	
6	IO	I	P2[1]	
7	IO	I	P3[3]	
8	IO	I	P3[1]	
9	IOH	I	P1[7]	I2C SCL, SPI SS.
10	IOH	I	P1[5]	I2C SDA, SPI MISO.
11			NC	No connection.
12			NC	No connection.
13			NC	No connection.
14			NC	No connection.
15	IOH	I	P1[3]	SPI CLK.
16	IOH	I	P1[1]	CLK*, I2C SCL, SPI MOSI.
17	Power		Vss	Ground connection.
18			CCLK	OCD CPU clock output.
19			HCLK	OCD high speed clock output.
20	IOH	I	P1[0]	DATA*, I2C SDA.
21	IOH	I	P1[2]	
22			NC	No connection.
23			NC	No connection.
24			NC	No connection.
25	IOH	I	P1[4]	Optional external clock input (EXTCLK).
26	IOH	I	P1[6]	
27	Input		XRES	Active high external reset with internal pull down.
28	IO	I	P3[0]	
29	IO	I	P3[2]	
30	IO	I	P2[0]	
31	IO	I	P2[2]	
32	IO	I	P2[4]	
33	IO	I	P2[6]	
34	IO	I	P0[0]	
35	IO	I	P0[2]	
36	IO	I	P0[4]	
37			NC	No connection.
38			NC	No connection.
39			NC	No connection.
40	IO	I	P0[6]	Analog bypass.

CY8C20000 OCD PSoC Device



Not for Production

Pin No.	Digital	Analog	Name	Description
41	Power		Vdd	Supply voltage.
42			OCDO	OCD even data IO.
43			OCDE	OCD odd data output.
44	IO	I	P0[7]	
45	IO	I	P0[5]	
46	IO	I	P0[3]	Integrating input.
47	Power		Vss	Ground connection.
48			NC	No connection.
CP	Power		Vss	Center pad must be connected to ground.

LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive.

* ISSP pin which is not HighZ at POR. See the *PSoC Mixed-Signal Array Technical Reference Manual* for details.

** The center pad on the QFN package should be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

2. Electrical Specifications

This chapter presents the DC and AC electrical specifications of the CY8C20234, CY8C20334 and CY8C20434 PSoC devices. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com/psoc.

Specifications are valid for -40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C as specified, except where noted.

Refer to Table 2-10 for the electrical specifications on the internal main oscillator (IMO) using SLIMO mode.

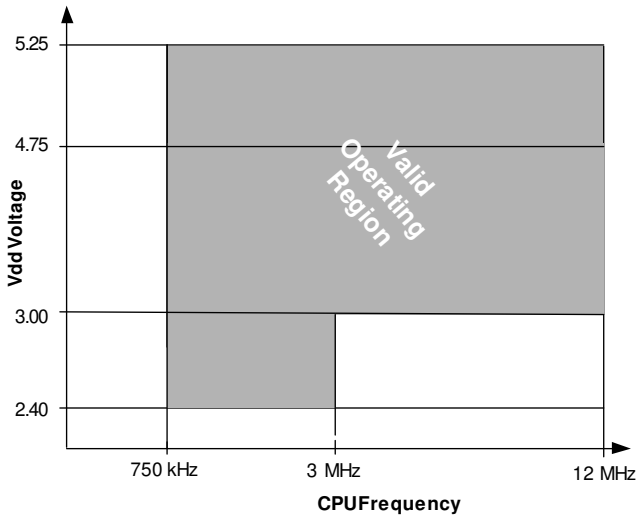


Figure 2-1a. Voltage versus CPU Frequency

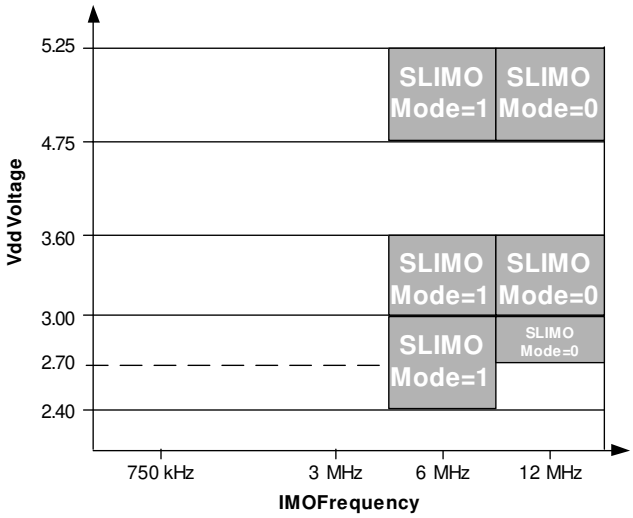


Figure 2-1b. IMO Frequency Trim Options

The following table lists the units of measure that are used in this chapter.

Table 2-1: Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	µW	microwatts
dB	decibels	mA	milli-ampere
fF	femto farad	ms	milli-second
Hz	hertz	mV	milli-volts
KB	1024 bytes	nA	nanoampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
kΩ	kilohm	Ω	ohm
MHz	megahertz	pA	picoampere
MΩ	megaohm	pF	picofarad
µA	microampere	pp	peak-to-peak
µF	microfarad	ppm	parts per million
µH	microhenry	ps	picosecond
µs	microsecond	sps	samples per second
µV	microvolts	σ	sigma: one standard deviation
µVrms	microvolts root-mean-square	V	volts

2.1 Absolute Maximum Ratings

Table 2-2. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	25	+100	oC	Higher storage temperatures will reduce data retention time. Recommended storage temperature is +25oC ± 25oC. Extended duration storage temperatures above 65oC will degrade reliability.
T_A	Ambient Temperature with Power Applied	-40	–	+85	oC	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss - 0.5	–	Vdd + 0.5	V	
V_{IOZ}	DC Voltage Applied to Tri-state	Vss - 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	–	+50	mA	
ESD	Electro Static Discharge Voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch-up Current	–	–	200	mA	

2.2 Operating Temperature

Table 2-3. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature	-40	–	+85	oC	
T_J	Junction Temperature	-40	–	+100	oC	The temperature rise from ambient to junction is package specific. See "Thermal Impedances" on page 27. The user must limit the power consumption to comply with this requirement.

2.3 DC Electrical Characteristics

2.3.1 DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 2-4. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd	Supply Voltage	2.40	–	5.25	V	See table titled "DC POR and LVD Specifications" on page 14.
I_{DD12}	Supply Current, IMO = 12 MHz	–	1.5	2.5	mA	Conditions are Vdd = 3.0V, T_A = 25oC, CPU = 12 MHz.
I_{DD6}	Supply Current, IMO = 6 MHz	–	1	1.5	mA	Conditions are Vdd = 3.0V, T_A = 25oC, CPU = 6 MHz.
I_{SB27}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active. Mid temperature range.	–	2.6	4.	µA	Vdd = 2.55V, 0oC ≤ T_A ≤ 40oC.
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active.	–	2.8	5	µA	Vdd = 3.3V, -40oC ≤ T_A ≤ 85oC.

2.3.2 DC General Purpose IO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

Table 2-5. 5V and 3.3V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up Resistor	4	5.6	8	kΩ	
V_{OH1}	High Output Voltage Port 0, 2, or 3 Pins	Vdd - 0.2	–	–	V	IOH ≤ 10 μA, Vdd ≥ 3.0V, maximum of 10 mA source current in all IOs.
V_{OH2}	High Output Voltage Port 0, 2, or 3 Pins	Vdd - 0.9	–	–	V	IOH = 1 mA, Vdd > 3.0V, maximum of 20 mA source current in all IOs.
V_{OH3}	High Output Voltage Port 1 Pins with LDO Regulator Disabled	Vdd - 0.2	–	–	V	IOH < 10 μA, Vdd > 3.0V, maximum of 10 mA source current in all IOs.
V_{OH4}	High Output Voltage Port 1 Pins with LDO Regulator Disabled	Vdd - 0.9	–	–	V	IOH = 5 mA, Vdd > 3.0V, maximum of 20 mA source current in all IOs.
V_{OH5}	High Output Voltage Port 1 Pins with LDO Regulator Enabled	2.75	3.0	3.2	V	IOH < 10 μA, Vdd > 3.1V, maximum of 4 IOs all sourcing 5 mA.
V_{OH6}	High Output Voltage Port 1 Pins with LDO Regulator Enabled	2.2	–	–	V	IOH = 5 mA, Vdd > 3.1V, maximum of 20 mA source current in all IOs.
V_{OL}	Low Output Voltage	–	–	0.75	V	IOL = 20 mA, Vdd > 3V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]).
V_{IL}	Input Low Voltage	–	–	0.8	V	Vdd = 3.0 to 5.25.
V_{IH}	Input High Voltage	2.0	–		V	Vdd = 3.0 to 5.25.
V_H	Input Hysteresis Voltage	–	140	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive Load on Pins as Input	0.5	1.7	5	pF	Package and pin dependent. Temp = 25ºC.
C_{OUT}	Capacitive Load on Pins as Output	0.5	1.7	5	pF	Package and pin dependent. Temp = 25ºC.

Table 2-6. 2.7V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up Resistor	4	5.6	8	kΩ	
V_{OH1}	High Output Voltage Port 0, 2, or 3 Pins	Vdd - 0.2	–	–	V	IOH < 10 μA, maximum of 10 mA source current in all IOs.
V_{OH2}	High Output Voltage Port 0, 2, or 3 Pins	Vdd - 0.5	–	–	V	IOH = 0.2 mA, maximum of 10 mA source current in all IOs.
V_{OH3}	High Output Voltage Port 1 Pins with LDO Regulator Disabled	Vdd - 0.2	–	–	V	IOH < 10 μA, maximum of 10 mA source current in all IOs.
V_{OH4}	High Output Voltage Port 1 Pins with LDO Regulator Disabled	Vdd - 0.5	–	–	V	IOH = 2 mA, maximum of 10 mA source current in all IOs.
V_{OL}	Low Output Voltage	–	–	0.75	V	IOL = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]).
V_{IL}	Input Low Voltage	–	–	0.8	V	Vdd = 2.4 to 3.0V.
V_{IH}	Input High Voltage	2.0	–		V	Vdd = 2.4 to 3.0V.
V_H	Input Hysteresis Voltage	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive Load on Pins as Input	0.5	1.7	5	pF	Package and pin dependent. Temp = 25ºC.
C_{OUT}	Capacitive Load on Pins as Output	0.5	1.7	5	pF	Package and pin dependent. Temp = 25ºC.

2.3.3 DC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 2-7. DC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{SW}	Switch Resistance to Common Analog Bus	–	–	400 800	Ω Ω	Vdd ≥ 2.7V 2.4V ≤ Vdd ≤ 2.7V

2.3.4 DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 2-8. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	Vdd Value for PPOR Trip					Vdd must be greater than or equal to 2.5V during startup, reset from the XRES pin, or reset from Watchdog.
V_{PPOR0}	PORLEV[1:0] = 00b		2.36	2.40	V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	2.60	2.65	V	
V_{PPOR2}	PORLEV[1:0] = 10b		2.82	2.95	V	
	Vdd Value for LVD Trip					
V_{LVD0}	VM[2:0] = 000b	2.39	2.45	2.51[a]	V	
V_{LVD1}	VM[2:0] = 001b	2.54	2.71	2.78[b]	V	
V_{LVD2}	VM[2:0] = 010b	2.75	2.92	2.99[c]	V	
V_{LVD3}	VM[2:0] = 011b	2.85	3.02	3.09	V	
V_{LVD4}	VM[2:0] = 100b	2.96	3.13	3.20	V	
V_{LVD5}	VM[2:0] = 101b	–	–	–	V	
V_{LVD6}	VM[2:0] = 110b	–	–	–	V	
V_{LVD7}	VM[2:0] = 111b	4.52	4.73	4.83	V	

a. Always greater than 50 mV above V_{PPOR} (PORLEV = 00) for falling supply.
b. Always greater than 50 mV above V_{PPOR} (PORLEV = 01) for falling supply.
c. Always greater than 50 mV above V_{PPOR} (PORLEV = 10) for falling supply.

2.3.5 DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 2-9. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd_{IWRITE}	Supply Voltage for Flash Write Operations	2.70	–	–	V	
I_{DDP}	Supply Current During Programming or Verify	–	5	25	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd - 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[a]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

a. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).

2.4 AC Electrical Characteristics

2.4.1 AC Chip-Level Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 2-10. 5V and 3.3V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{CPU1}	CPU Frequency (3.3V Nominal)	0.75	–	12.6	MHz	12 MHz only for SLIMO Mode = 0.
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
F_{IMO12}	Internal Main Oscillator Stability for 12 MHz (Commercial Temperature)[a]	11.4	12	12.6	MHz	Trimmed for 3.3V operation using factory trim values. See Figure 2-1b, SLIMO Mode = 0.
F_{IMO6}	Internal Main Oscillator Stability for 6 MHz (Commercial Temperature)	5.70	6.0	6.30	MHz	Trimmed for 3.3V operation using factory trim values. See Figure 2-1b, SLIMO Mode = 1.
DC_{IMO}	Duty Cycle of IMO	40	50	60	%	
T_{RAMP}	Supply Ramp Time	0	–	–	µs	

a. 0 to 70 °C ambient, Vdd = 3.3 V.

Table 2-11. 2.7V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{CPU1}	CPU Frequency (2.7V Nominal)	0.75	–	3.25	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	8	32	96	kHz	
F_{IMO12}	Internal Main Oscillator Stability for 12 MHz (Commercial Temperature)[a]	11.0	12	12.9	MHz	Trimmed for 2.7V operation using factory trim values. See Figure 2-1b, SLIMO Mode = 0.
F_{IMO6}	Internal Main Oscillator Stability for 6 MHz (Commercial Temperature)	5.60	6.0	6.40	MHz	Trimmed for 2.7V operation using factory trim values. See Figure 2-1b, SLIMO Mode = 1.
DC_{IMO}	Duty Cycle of IMO	40	50	60	%	
T_{RAMP}	Supply Ramp Time	0	–	–	µs	

a. 0 to 70 °C ambient, Vdd = 3.3 V.

2.4.2 AC General Purpose IO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 2-12. 5V and 3.3V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	6	MHz	Normal Strong Mode, Port 1.
TRise023	Rise Time, Strong Mode, Cload = 50 pF Ports 0, 2, 3	15	–	80	ns	Vdd = 3.0 to 3.6V and 4.75V to 5.25V, 10% - 90%
TRise1	Rise Time, Strong Mode, Cload = 50 pF Port 1	10	–	50	ns	Vdd = 3.0 to 3.6V, 10% - 90%
TFall	Fall Time, Strong Mode, Cload = 50 pF All Ports	10	–	50	ns	Vdd = 3.0 to 3.6V and 4.75V to 5.25V, 10% - 90%

Table 2-13. 2.7V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	1.5	MHz	Normal Strong Mode, Port 1.
TRise023	Rise Time, Strong Mode, Cload = 50 pF Ports 0, 2, 3	15	–	100	ns	Vdd = 2.4 to 3.0V, 10% - 90%
TRise1	Rise Time, Strong Mode, Cload = 50 pF Port 1	10	–	70	ns	Vdd = 2.4 to 3.0V, 10% - 90%
TFall	Fall Time, Strong Mode, Cload = 50 pF All Ports	10	–	70	ns	Vdd = 2.4 to 3.0V, 10% - 90%

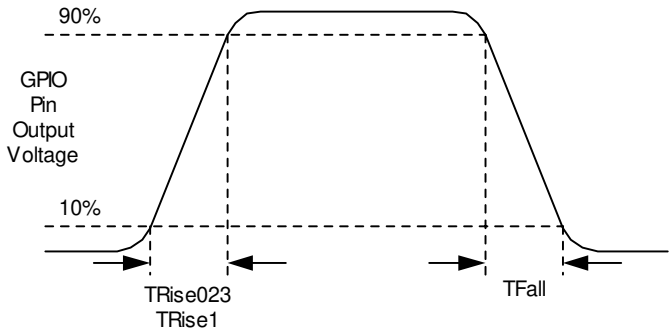


Figure 2-2. GPIO Timing Diagram

2.4.3 AC Comparator Amplifier Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 2-14. AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{COMP}	Comparator Response Time, 50 mV Overdrive			100 200	ns ns	Vdd ≥ 3.0V. 2.4V < Vcc < 3.0V.

2.4.4 AC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 2-15. AC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{SW}	Switch Rate	–	–	3.17	MHz	

2.4.5 AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 2-16. 5V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.750	–	12.6	MHz	
–	High Period	38	–	5300	ns	
–	Low Period	38	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

Table 2-17. 3.3V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU Clock divide by 1	0.750	–	12.6	MHz	Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
–	High Period with CPU Clock divide by 1	41.7	–	5300	ns	
–	Low Period with CPU Clock divide by 1	41.7	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

Table 2-18. 2.7V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU Clock divide by 1	0.750	–	3.08	MHz	Maximum CPU frequency is 3 MHz at 2.7V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU Clock divide by 2 or greater	0.15	–	6.35	MHz	If the frequency of the external clock is greater than 3 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider will ensure that the fifty percent duty cycle requirement is met.
–	High Period with CPU Clock divide by 1	160	–	5300	ns	
–	Low Period with CPU Clock divide by 1	160	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

2.4.6 AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 2-19. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash Erase Time (Block)	–	15	–	ms	
T_{WRITE}	Flash Block Write Time	–	30	–	ms	
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	45	ns	3.6 < Vdd
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	50	ns	3.0 ≤ Vdd ≤ 3.6
T_{DSCLK2}	Data Out Delay from Falling Edge of SCLK	–	–	70	ns	2.4 ≤ Vdd ≤ 3.0

2.4.7 AC SPI Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 2-20. 5V and 3.3V AC SPI Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{SPIM}	Maximum Input Clock Frequency Selection, Master	–	–	6.3	MHz	Output clock frequency is half of input clock rate.
F_{SPIS}	Maximum Input Clock Frequency Selection, Slave	–	–	2.05	MHz	
T_{SS}	Width of SS_ Negated Between Transmissions	50	–	–	ns	

Table 2-21. 2.7V AC SPI Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{SPIM}	Maximum Input Clock Frequency Selection, Master	–	–	3.15	MHz	Output clock frequency is half of input clock rate.
F_{SPIS}	Maximum Input Clock Frequency Selection, Slave	–	–	1.025	MHz	
T_{SS}	Width of SS_ Negated Between Transmissions	50	–	–	ns	

2.4.8 AC I²C Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 2-22. AC Characteristics of the I²C SDA and SCL Pins for Vdd ≥ 3.0V

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz	
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs	
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs	
$T_{SUSTAI2C}$	Set-up Time for a Repeated START Condition	4.7	–	0.6	–	µs	
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs	
$T_{SUDATI2C}$	Data Set-up Time	250	–	100[a]	–	ns	
$T_{SUSTOI2C}$	Set-up Time for STOP Condition	4.0	–	0.6	–	µs	
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs	
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns	

a. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Table 2-23. 2.7V AC Characteristics of the I²C SDA and SCL Pins (Fast Mode not Supported)

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL Clock Frequency	0	100	–	–	kHz	
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	–	–	µs	
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	–	–	µs	
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	–	–	µs	
$T_{SUSTAI2C}$	Set-up Time for a Repeated START Condition	4.7	–	–	–	µs	
$T_{HDDATI2C}$	Data Hold Time	0	–	–	–	µs	
$T_{SUDATI2C}$	Data Set-up Time	250	–	–	–	ns	
$T_{SUSTOI2C}$	Set-up Time for STOP Condition	4.0	–	–	–	µs	
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	–	–	µs	
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	–	–	–	–	ns	

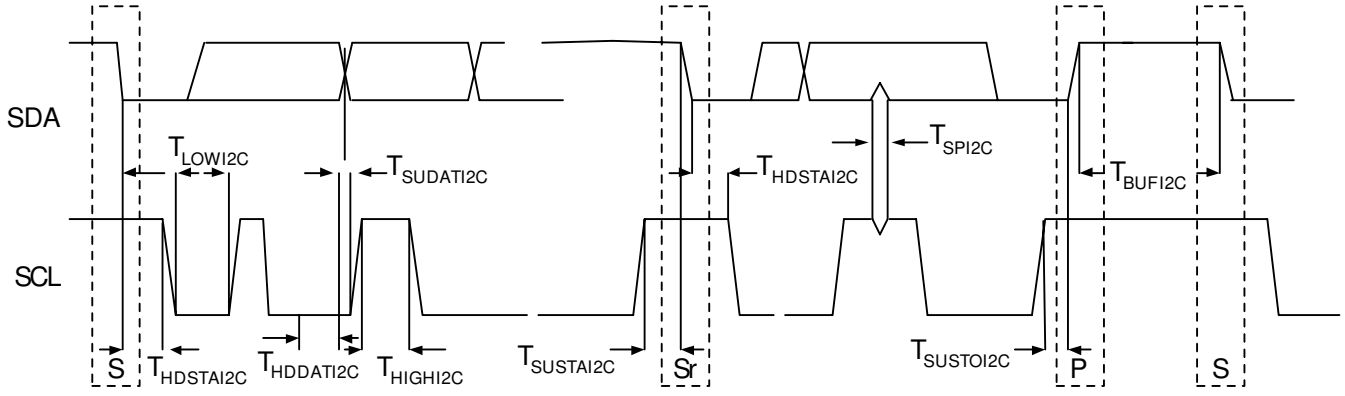


Figure 2-3. Definition for Timing for Fast/Standard Mode on the I²C Bus

3. Packaging Information

This chapter illustrates the packaging specifications for the CY8C20x34 PSoC device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/design/MR10161.

3.1 Packaging Dimensions

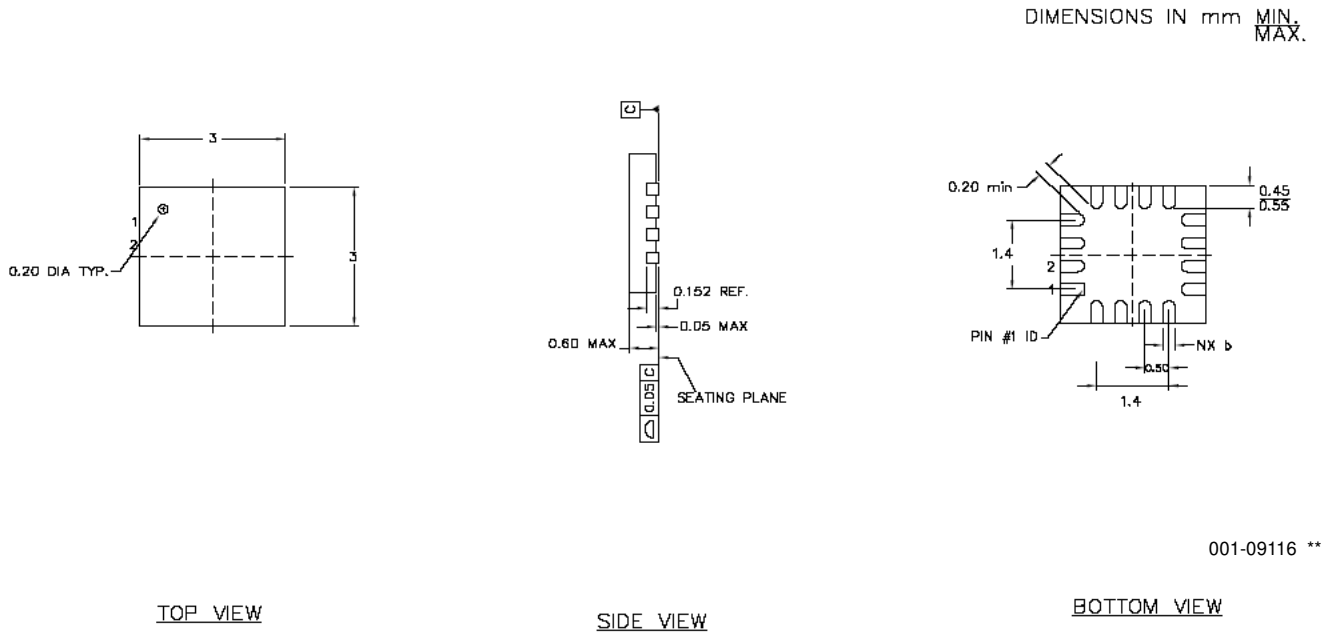


Figure 3-1. 16-Lead (3x3 mm x 0.6 MAX) QFN -- Preliminary

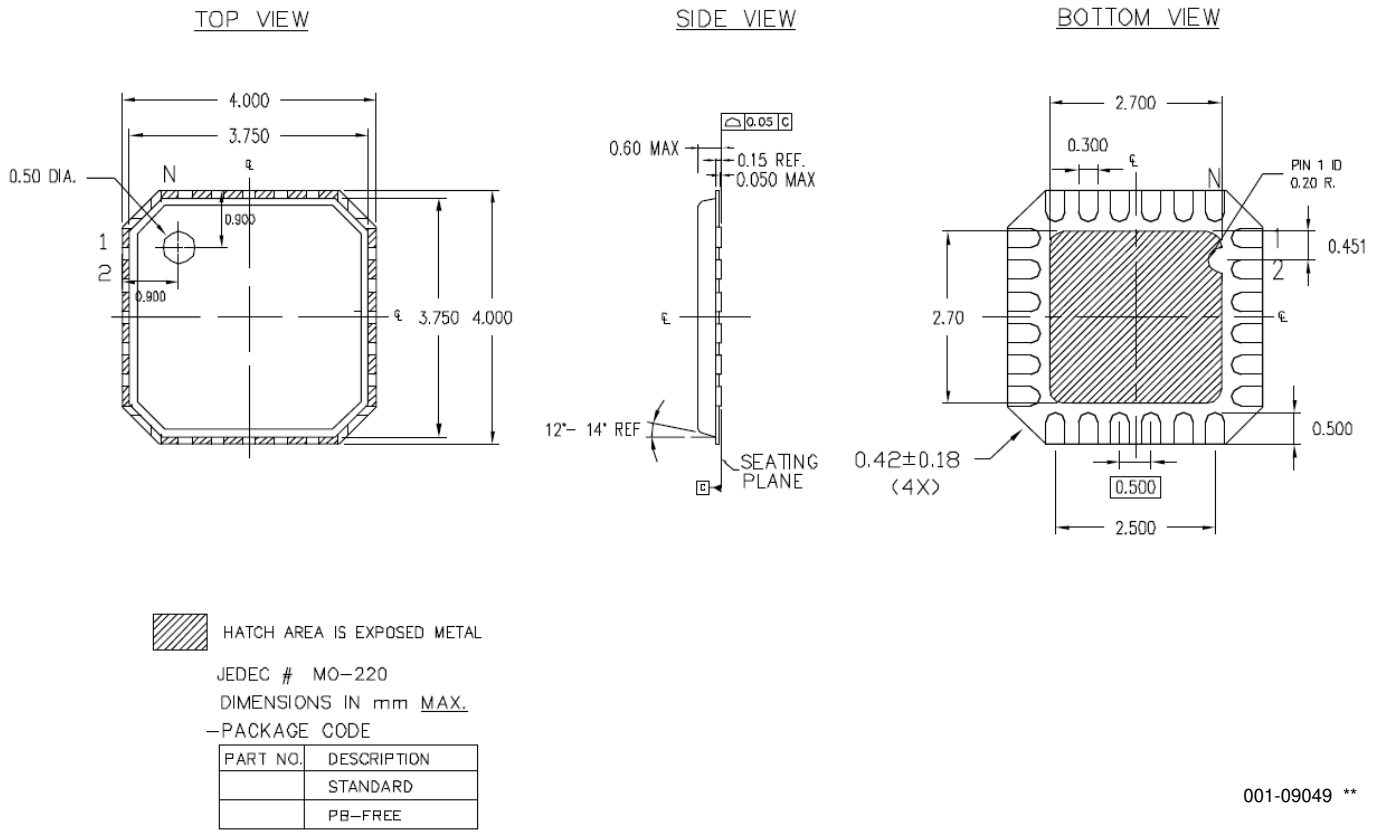


Figure 3-2. 24-Lead (4x4 x 0.6 mm) QFN -- Preliminary

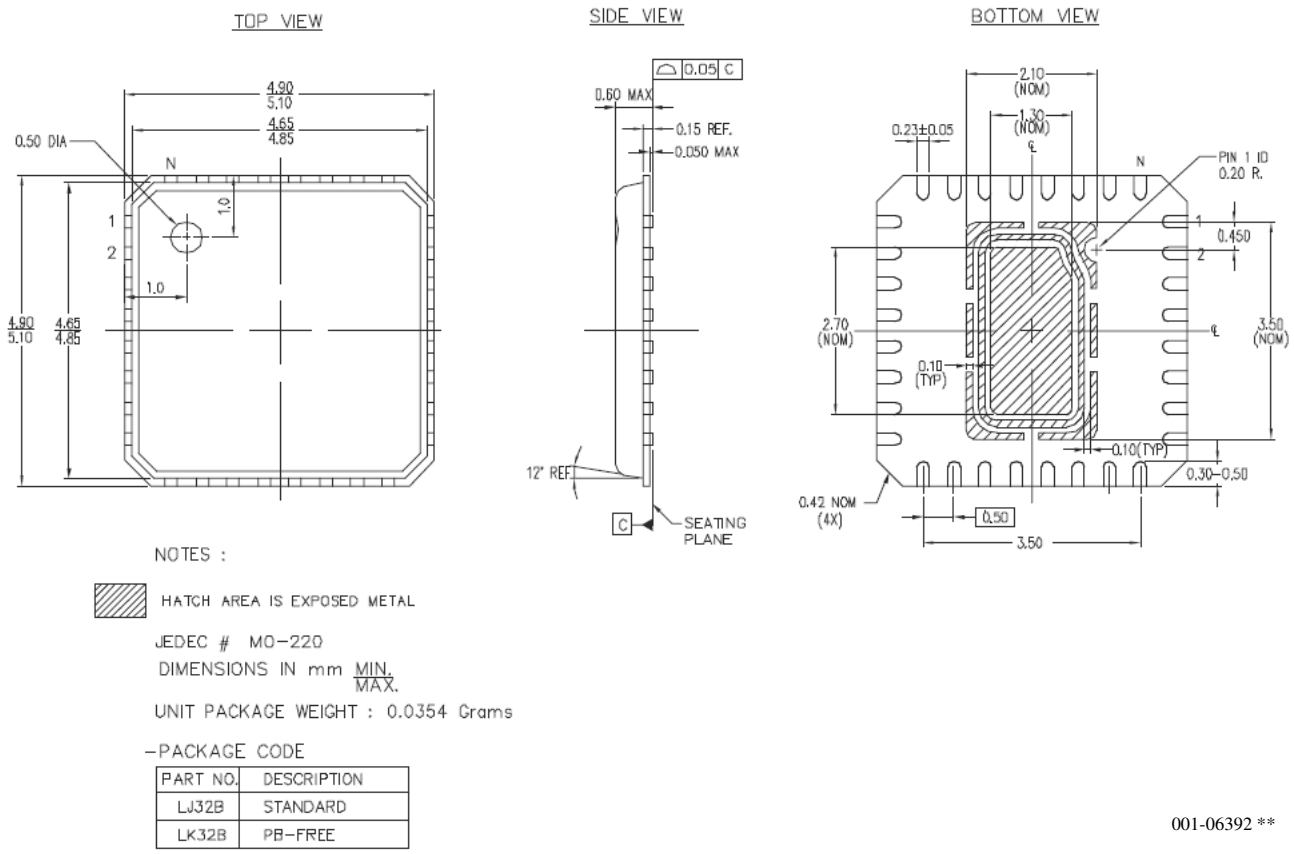


Figure 3-3. 32-Lead (5x5 mm 0.60 MAX) QFN