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CY3677

Evaluation Kit User Guide

Doc. No. 002-12185 Rev. *D

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Safety Information



The CY3677 Evaluation Kit is intended for use as an evaluation platform for hardware or software in a laboratory environment. The board is an open system design, which does not include a shielded enclosure, so the board may cause interference to other electrical or electronic devices in close proximity. In a domestic environment, this product may cause radio interference. In such cases, the user may be required to take adequate preventive measures. Also, this board should not be used near any medical equipment or RF devices.

Attaching additional wiring to this product or modifying the product operation from the factory default may affect its performance and cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.



The CY3677 Evaluation Kit contains electrostatic discharge (ESD)-sensitive devices. Electrostatic charges readily accumulate on the human body and any equipment, and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused CY3677 Evaluation Kit boards in the protective shipping package.

General Safety Instructions

ESD Protection

ESD can damage boards and associated components. Cypress recommends that the user perform procedures only at an ESD workstation. If an ESD workstation is not available, use appropriate ESD protection by wearing an antistatic wrist strap attached to the chassis ground (any unpainted metal surface) on the board when handling parts.

Handling Boards

The CY3677 Evaluation Kit is sensitive to ESD. Hold the board only by its edges. After removing the board from its box, place it on a grounded, static-free surface. Use a conductive foam pad if available. Do not slide the board over any surface.

Certification Disclaimer

This kit is intended for demonstration, evaluation, or development purposes only and is not considered by Cypress Semiconductor to be a finished end-product fit for general consumer use. It generates and can radiate radio frequency energy and has not been specifically tested for CE certification compliance. Operation of this equipment in other environments may cause interference with radio communications, in which case users at their own expense will be required to take whatever measures may be required to correct this interference.

1 Introduction



Thank you for your interest in the CY3677 Evaluation Kit (EVK). The CY3677 EVK is designed to enable you to evaluate the programmable clock device CY29430, the latest addition to the Cypress timing product portfolio. The clock device CY29430 is a high-performance programmable oscillator with one fractional PLL that generates any frequency up to 2.1 GHz with jitter as low as 110 fs. The device offers one differential output and one single-ended output. The device can be configured to generate either a single-ended output or a differential output but not both simultaneously. The device comes in a 16-pin QFN package for industrial applications. The differential I/O standards supported are LVDS, LVPECL, High-Speed Current Steering Logic (HCSL), and Current Mode Logic (CML). The single-ended signal supported is LVCMOS. The device also supports features such as a Voltage-Controlled Crystal Oscillator (VCXO), and provides the user with an I²C programming interface. The device supports four frequency profiles, which can be switched dynamically using external Frequency Select (FS0 and FS1) signals. There are two jumpers provided on the EVK to perform frequency selection on the board.

The CY3677 EVK allows you to evaluate output clock signals by making required on-board termination settings.

The CY3677 EVK is available through the Cypress Online Store or through our distributors.

1.1 CY3677 EVK Contents

The CY3677 EVK includes the following:

- CY3677 Evaluation Board
- USB Standard-A to Mini-B cable
- Quick Start Guide







Inspect the contents of the kit. If you find any part missing, contact your nearest Cypress sales office for assistance: www.cypress.com/support.

1.2 Getting Started

To learn the solution quickly and apply it to your design, refer to the CY3677 Quick Start Guide inside the kit box or in the installation directory. The default location for the kit documents is:

<Install Directory>\CY3677 Evaluation Kit\<version>\Documentation

This guide will help you get acquainted with the CY3677 EVK:

The Software Installation chapter describes the installation of the kit software.

The Kit Operation chapter describes the major features of the CY3677 Evaluation Kit.

The Hardware chapter describes the hardware content of the CY3677 Evaluation Kit and the hardware operation.

The Example Projects chapter describes the multiple projects that will help you understand how to evaluate different supported output standards on this kit.

The Appendix captures DC/AC Measurements of Clock Outputs, Schematics, Fab Drawing, and the bill of materials (BOM).

1.3 Additional Learning Resources

Visit www.cypress.com/CY3677 and www.cypress.com/HPO for additional learning resources including datasheets and application notes.

1.4 Technical Support

For assistance, go to_www.cypress.com/support, or contact our customer support at +1(800) 541-4736 Ext. 2 (in the USA), or +1 (408) 943-2600 Ext. 2 (International).



1.5 Document Conventions

Table 1-1	Document	Conventions	for	Guides
	. Document	COnventions	101	QUIGES

Convention	Usage
Courier New	Displays file locations, user entered text, and source code: C:\cd\icc\
Italics	Displays file names and reference documentation.
[Bracketed, Bold]	Displays keyboard commands in procedures: [Enter] or [Ctrl] [C]
File > Open	Represents menu paths: File > Open > New Project
Bold	Displays commands, menu paths and icon names in procedures: Click the File icon and then click Open .
Times New Roman	Displays an equation: 2 + 2 = 4
Text in gray boxes	Describes Cautions or unique functionality of the product.

1.6 Acronyms

Acronym	Definition
BOM	Bill of Materials
CML	Current Mode Logic
DNP, DNM	Do Not Populate, Do Not Mount
FS	Frequency Select
HCSL	High-Speed Current Steering Logic
l ² C	Inter-Integrated Circuit
JEDEC	Joint Electron Device Engineering Council
LDO	Low-Dropout
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVPECL2	Low Voltage Positive Emitter Coupled Logic with zero Common-mode current
LVDS	Low Voltage Differential Signaling
OE	Output Enable
OT3	Third Overtone Crystal
SMA	Subminiature Version A
VCXO	Voltage-Controlled Crystal Oscillator
тсхо	Temperature Compensated Crystal Oscillator
OTP	One-Time Programmable

2 Software Installation



This chapter describes the steps to install the software tools and packages on a PC for using the CY3677 Evaluation Kit.

2.1 Before You Begin

All Cypress software installations require administrator privileges. Ensure that you have the required privileges on the system for successful installation. Before you install the kit software, close any other Cypress software that is currently running.

2.2 Install Software

Follow these steps to install the CY3677 Evaluation Kit software:

- 1. Download the CY3677 Evaluation Kit software from www.cypress.com/CY3677. The software is available in the following formats:
 - a. CY3677 Evaluation Kit Complete Setup: This installation package contains the files related to the CY3677 Evaluation Kit. However, it does not include the Windows Installer or Microsoft .NET Framework packages. If these packages are not available on your computer, the installer directs you to download and install them from the Internet.
 - b. CY3677 Evaluation Kit Only: This executable file installs only the CY3677 EVK contents, which include example projects, hardware files, and user documents. This package can be used if all the software prerequisites are installed on your PC.
 - c. **CY3677 Evaluation Kit ISO:** This file is a complete package, stored in a CD/DVD-ROM image format that you can use to create a CD/DVD or extract using an ISO extraction program such as WinZip or WinRAR. The file can also be mounted similar to a virtual CD/DVD using virtual drive programs such as Virtual CloneDrive and MagicISO. This file includes all the required software, utilities, drivers, hardware files, and user documents.
- 2. If you have downloaded the ISO file, mount it on a virtual drive. If you do not have a virtual drive to mount, extract the ISO contents using the appropriate ISO extractor (such as MagicISO or PowerISO). Double-click *cyautorun.exe* in the root directory of the extracted content or the mounted ISO if the "Autorun from CD/DVD" option is not enabled on the PC. The installation window will appear automatically.

Note: If you are using the "Kit Complete Setup" or "Kit Only" file, then go to step 4 for installation.

3. Click Install CY3677 EVK to start the installation as shown in Figure 2-1.



Figure 2-1. Installer Screen



4. Click **Change...** if you want to install the CY3677 EVK in a location other than the default, and then click **Next** as shown in Figure 2-2.

Note: When you click **Next**, the CY3677 EVK installer automatically installs the required software, if it is not present on your computer. The pre-requisites are ClockWizard 2.1 and PSoC Programmer 3.25.0 or later.

CY3677 Evaluation Kit - InstallSI	nield Wizard	×
	Welcome to the InstallShield Wizard for Evaluation Kit	CY3677
Manual Innormal	The InstallShield Wizard will install CY3677 Evalu on your computer. To continue, click Next. Select folder where setup will install files.	uation Kit
	C:\\Cypress	Change
	< Back Next >	Cancel

Figure 2-2. InstallShield Wizard



Select the Installation Type (see Figure 2-3). The drop-down menu contains three options: Typical (installs all the required features), Custom (lets you choose the features to be installed), and Complete (installs all the contents). Click Next after you select the Installation Type.

Note: It is recommended that you choose the Typical Installation Type.

Figure 2-3. Product Installation Overview

CyInstaller for CY3677 Evaluation Kit Troduct Installation Overview Choose the install type that best suits your needs	3
Choose the type of installation Product: CY3677 Evaluation Kit Installation Type: Typical Installs the most common features of CY3677 Evaluation Kit.	
Contact Us	Next > Cancel

6. Read and accept the End-User License Agreement, and then click Next.

When the installation begins, a list of packages appears on the Installation page. A green check mark appears next to each package after successful installation.

- 7. Enter your contact information or select the Continue Without Contact Information check box.
- 8. Click Finish to complete the CY3677 Evaluation Kit installation.

After the installation is complete, the kit contents are available at:

<Install_Directory>\CY3677 Evaluation Kit\<version>. Default location: Windows 7 (64-bit): C:\Program Files (x86)\Cypress\CY3677 Evaluation Kit Windows 7 (32-bit): C:\Program Files\Cypress\CY3677 Evaluation Kit



2.3 Install Hardware

No additional hardware installation is required for this kit.

2.4 Uninstall Software

You can uninstall the software using one of the following methods:

- Go to Start > All Programs > Cypress > Cypress Update Manager > Cypress Update Manager, and select the specific software package. Click the Uninstall button.
- Go to Start > Control Panel > Programs and Features, and select the specific software package. Click the Uninstall/Change button.

3 Kit Operation



The CY3677 EVK can be used to evaluate the CY29430, a high performance programmable oscillator. Connect the CY3677 kit through USB to a PC running Cypress's ClockWizard 2.1 software. The clock device CY29430 can be configured and programmed to generate frequencies with best-in-class performance.

3.1 Theory of Operation

The CY3677 EVK offers one differential clock output and one single-ended clock output (only one operates at a time) for evaluation. The CY29430 device uses an on-board crystal or Temperature Compensated Crystal Oscillator (TCXO) reference input.

The kit is capable of generating fixed 3.3 V, 2.5 V, and 1.8 V voltages from a 5-V USB port. The on-board PSoC 5LP (U7) performs the USB-to-I²C conversion. There is one power LED (LED2) driven from the on-board LDO supply and one status LED (LED1) controlled by PSoC 5LP. The output of LDO regulator (U8) is configurable (3.3 V, 2.5 V, or 1.8 V) through jumper J13.

Note: An additional on-board LDO (U9 – not shown in Figure 3-1) generates a fixed 3.3-V supply for the PSoC 5LP in the **CY3677 Rev** ** EVK. This feature has been changed in **CY3677 Rev** ***A** EVK where the PSoC 5LP is directly powered by a 5-V USB supply. The CY3677 kit revision is printed on the label at the back of the kit box.

Figure 3-1 illustrates the block diagram of the CY3677 EVK.







3.2 Functional Description

The differential clock outputs (J7, J8) and single-ended output (J10) are driven out on to SMA connectors. The EVK is populated with $50-\Omega$ resistors (R30 and R31) for output termination. The termination options of the differential outputs on the evaluation board are listed in the Hardware chapter. These termination circuits are designed to terminate the output clocks in LVPECL, LVDS, HCSL, LVPECL2, and CML signal types by populating, or by not populating the J5 jumper shunt. The single-ended (LVCMOS) clock does not need any on-board termination settings.

Figure 3-2 illustrates the top view and bottom view of the CY3677 EVK.



CY3677 EVK Top View

CY3677 EVK Bottom View

3.3 CY3677 EVK USB Connection

The CY29430 clock device on the kit is loaded with a default configuration. To view and evaluate other configurations on an oscilloscope (or other standard instruments), the clock device must be programmed with the desired configuration. The ClockWizard 2.1 application is required for programming any configuration. Therefore, the kit should be connected (see Figure 3-3) to a PC through a USB port for programming.







The kit enumerates as a USB Composite Device as part of the Driver Software installation on Windows.

Figure 3-4. USB Driver Installation

Installing device driver soft	ware	
USB Composite Device	🖌 Ready to use	
KitProg USBUART	Searching Windows Update	
KitBridge	Searching Windows Update	
KitProg Programmer	Searching Windows Update	
Obtaining device driver software fro	m Windows Update might take a while.	
Skip obtaining driver software from	Windows Update	

After the driver installation is complete, the device is ready to use.



3.4 Programming the CY29430

The CY29430 device has an internal one-time programmable (OTP) nonvolatile memory called eFuse. The device also contains volatile memory that stores an exact copy of the eFuse at the release of reset at power-up. The output frequency depends on the configurations in the volatile memory. Writing the entire device configuration in the volatile memory section of a blank device after power-up, is called Functional Programming. The CY3677 kit is shipped with a programmed CY29430 device. This program is written to a specific internal memory location of the device. This kit can be used to check both the Functional and eFuse Programming of the device using ClockWizard 2.1. See Functional Programming of the CY29430 and eFuse Programming of the CY29430 for details.



Kit Operation

3.5 Functional Programming of the CY29430

ClockWizard 2.1 is used for functional programming of the CY29430. A configuration created in ClockWizard 2.1 can be downloaded to the volatile memory section of the device.

The example ClockWizard 2.1 projects can be found at the following location:

<Install_Directory>\CY3677 Evaluation Kit\<version>\Firmware\Example Projects

Configuration profiles generated from these projects can be used to evaluate the CY29430 device on the CY3677 EVK. Refer to Functional Programming for the kit's hardware settings prior to programming. It is recommended that you copy the example projects to another location if you want to make any modifications to the settings so that the default project is retained in the installation directory.

CAUTION Before programming the CY3677 EVK through ClockWizard 2.1, it is recommended to go through CAUTION ClockWizard 2.1 configuration may cause potential damage of the EVK. Specifically, the voltage setting on the kit selected with J13 must match the voltage setting within the configuration to be programmed.

3.5.1 Generating and Programming the Device Configuration Profile

The ClockWizard 2.1 is used to generate profiles and to perform functional programming of the device.

- 1. Verify that the power supply voltage jumper (J13) is set for the voltage used in the project that you intend to program. See the Hardware section for details.
- 2. Connect the CY3677 EVK to your PC through the supplied USB cable.
- 3. To launch the ClockWizard 2.1 application, go to Start > All Programs > Cypress > ClockWizard 2.1.

The workspace files are located in the Workspace folders. The four workspaces available are:

- CY3677_LVPECL_3p3.cpj
- CY3677_LVDS_2p5.cpj
- CY3677_HCSL_2p5.cpj
- CY3677_LVCMOS_1p8.cpj
- 4. Select the **File** menu in ClockWizard 2.1, select **Open workspace**, browse the required workspace file with a *.cpj* extension, and then click **Open**. Each Workspace file can contain multiple projects.
- 5. Click **Configure**, as shown in Figure 3-6. The various configuration parameters appear on the right panel of the block diagram in the tabbed interface. For more information on configuration parameters, refer to the ClockWizard 2.1 User Guide located in **Help** > **User guide** of the ClockWizard 2.1 software.
- 6. Click the **Generate** button (see Figure 3-6). This will generate the JEDEC file for the configuration selected. On completion of generation, the Results are displayed as shown in Figure 3-7.





Figure 3-6. Generating a Configuration Profile using ClockWizard 2.1

7. Click **Results** in the navigation pane to view the results at any time after a JEDEC file has been generated for a configuration, as shown in Figure 3-7.

ome	Input and outp	ut					JEDEC file:	Project_	00.jed		
ojects roject_00 - CY29430	Output Frequ	ency	Target Frequency (MHz)	Calcul (MHz)	lated Frequency	PPM Error	Created on 10/2 Register progra	4/2016 2:00 mming det	B PM ails		
Results	Profile 0		33.333	33.332	999970867	-0.000874	Device slave add	lress: 0x5	5		
ogram	Profile 1		50	49.999	9999532	-0.000936	Register name	Address	Value		
gram	Profile 2		100	99.999	9999193	-0.000807	DIVO_FS0	0x10	0xCD		
	Profile 3		156.25	156.24	9999863906	-0.000871	DIVN_FS0	0x11	0x3C		
	L						DIVO_MISC	0x12	0x0A		
	Common Settings	Catego	ory		Settings		DIVN_FRAC0 DIVN_FRAC1	0x13 0x14	0xF8 0x9B		
	Input	Ref Clo	ck Type		OT3 XTAL		DIVN_FRAC2	0x15	0xCA		
		Referen	nce Input (MHz)		114.285		DIVO_FS1	0x20	0x89		
		XO_Do	ubler		Disable		DIVO_MISC	0x27	0x0A		
	Common	Output	Standard		LVPECL		DIVN FRACO	0x23	0x8C		
		OE Pola	OE Polarity Active Low DIVN_FR/		DIVN_FRAC1	0x24	0x18				
		I2C Add	ress (decimal)		85		DIVN_FRAC2	0x25	0xF0		
		VDD			3.3 V		DIVO_FS2	0x30	0x45		
		VCXO			Disable		DIVN_FS2	0x31	0x3C		
		VCXO E	landwidth		10 KHz		DIVN_ERACO	0x32	0xBA		
		Total Pu	ill Range		150 ppm		DIVN FRAC1	0x34	0x18		
		VCXO C	ain Polarity		Positive		DIVN_FRAC2	0x35	0x60		
	Option	USER_	DATA_1 (0xD4)		0		DIVO_FS3	0x40	0x2C		
		USER_	DATA_2 (0xD5)		0		DIVN_FS3	0x41	0x3C		
		USER_	DATA_3 (0xD6)		0		DIVO_MISC	0x42	A0x0		
							DIVIN_FRACO	0x43	0.43		
							*	m			

Figure 3-7. View Results Generated from the Configuration Profile using ClockWizard 2.1



8. To program the CY29430 device, select **Program** in the left navigation pane, as shown in Figure 3-8. Choose the appropriate device in the **Select Device (I2C Master)** drop-down list prior to programming, and then click the **Functional Program** button. This will program the device directly from ClockWizard. LED1 blinks to indicate that the device is being programmed. The required output will appear on the oscilloscope.

For more information, refer to the ClockWizard 2.1 User Guide located in **Help** > **User guide** of the ClockWizard 2.1 software.

Program - F	Project_00						
Device selectio	n	JEDEC programming					
Select Device (I2C Master):	KitProg/100F0D28010D5400	 Select JEDEC: 		Project_00		
					eFuse Program Fund	tional Program	
-Large change	programming				Small change program	nming	
Profile 0 (MHz)	33.333	VCXO:	Enable	*	Select FS profile:	00 -	
Profile 1 (MHz)	50	Gain polarity.	Positive	-	Small change (ppm):		
Profile 2 (MHz)	100	Total pull range (ppm)	50		Sm	all change update	
Profile 3 (MHz)	156.25	VCXO BW (KHz):	5				
			Large change update				
- Frequency set	ect signal						
FS1:FS0:	0	- Apply					

Figure 3-8. Programming Configuration Profile using ClockWizard 2.1

9. The CY29430 supports the selections of four frequency profiles for a single configuration. The Frequency Select inputs of the CY29430 device (FS0 and FS1) can either be controlled by ClockWizard 2.1 or they can be hard-coded using jumpers on the board. To allow selection of a frequency profile in ClockWizard 2.1, jumpers J14 and J15 must be set to positions 2 and 3. With the jumpers in those positions, you can select any of the four available profiles in ClockWizard 2.1 and click **Apply** (see Figure 3-9). Refer to the section Frequency Select (FS) for details on the hardware settings.

Figure 3-9. Frequency Select (FS) Operation of the CY29430 device through ClockWizard 2.1

ClockWizard 2.1 - CY3677	_LVPECL_3p3.cpj				
File Tools Help					
Configure Results Program	Program - Project Device selection Select Device (I2C Maste	_00 er): KilProg/100F0D28010D5400	JEDEC programming	Project_00 v	
	Large change program Profile 0 (MHz): 333. Profile 1 (MHz): 50 Profile 2 (MHz): 100 Profile 3 (MHz): 156 Frequency select signal FS1 FS0: 00	ming 333 VCXO: Gain polarity: D Total pull range (ppm): 325 VCXO BW (kHz): I Apply	Disable * Positive * 150 * 10 * Large change update	Small change programming Select FS profile: 00 • Small change (ppm): Small change update	
Messages Info: Device is not eFused Info: Programming started fo Info: Programming operation	r Project_00 at 12/13/2016 1:00 completed successfully	132 PM			



After functional programming, the frequency values of the current .*cpj* are displayed in the following fields (see Figure 3-10): Profile 0 (MHz), Profile 1 (MHz), Profile 2 (MHz), and Profile 3 (MHz). You can change any of the frequencies in these fields. To make the changes effective, click Large change update. The expected output frequency will appear on the oscilloscope.

Note: Large change programming refers to the case where the frequency is changing more than ± 500 ppm.

.KW12dru 2.1 * C150//_L	VPECL_3p3.cpj				
fools Help					
e ects	Program - Pro	ject_00			
ject_00 - CY29430	Device selection			JEDEC programming	
ifigure	Select Device (I2C	Master):	KitProg/100F0D28010D5400	 Select JEDEC: 	Project_00 👻
am					eFuse Program Functional Program
	Large change pro	gramming			Small change programming
	Profile 0 (MHz):	33.333	VCXO:	Disable	✓ Select FS profile: 00 ✓
	Profile 1 (MHz):	50	Gain polarity:	Positive	 Small change (ppm):
	Profile 2 (MHz):	100	Total pull range (ppm):	150	* Small change undate
	Profile 3 (MHz):	156.25	VCXO BW (KHz):	10	*
				Large change update	
	Frequency select s	signal			
	FS1:FS0: 00		Apply		

11. If you want to change the frequency to less than ±500 ppm, fill in the desired ppm in the **Small change (ppm)** field, Select FS profile and click on **Small change update**. The settings are shown in Figure 3-11.

Figure 3-11. Evaluation of Other Frequencies through Small Change Update

File Tools Help					
Home Projects Project_00 - CY29430 Configure Results Program	Program - Pro Device selection Select Device (I2C I	ject_00 Master):	KilProg/100F0D28010D5400	JEDEC programm	Projed_00 Functional Program
	Profile 0 (MHz): Profile 1 (MHz): Profile 2 (MHz): Profile 3 (MHz):	33.333 50 100 156.25	VCXO: Gain polarity: Total pull range (ppm): VCXO BW (KHz):	Disable Positive 150 10 Large change update	Select FS profile: 00 Small change (ppm): 100 Small change update e
	Frequency select s	ignal	 Apply 		
Messages 🔀	_			_	
Info: Device is not eFused Info: Programming started for F Info: Programming operation co	roject_00 at 12/13/2016 mpleted successfully	1:00:32 PM			

Info: Programming started for Project_00 at 12/13/2016 1:00:32 PM Info: Programming operation completed successfully



3.6 eFuse Programming of the CY29430

After functional programming and evaluation of different clock configurations, you may choose to write the configuration to the nonvolatile memory section of the device. The nonvolatile memory of the CY29430 is a one-time programmable (OTP) eFuse. Any configuration after functional evaluation can permanently be written to the eFuse of the device. See Figure 3-12 for the programming procedure.

Configure the device supply to 2.5 V before starting the eFuse programming. Table 4-2 provides the hardware configuration (J13 settings) of CY3677 for setting the device supply to 2.5 V.

ElockWizard 2.1 - CY3677_LV	VPECL_3p3.cpj
File Tools Help	
😂 🚓 🕂 🖬	
Home	Program - Project 00
Projects	
Configure	Device selection JEDEC programming
Results	Select Device (I2C Master): KitProg/100F0D28010D5400 Select JEDEC: Project_00
Program	eFuse Program Functional Program
	Large change programming Small change programming
	Profile 0 (MHz) 33.333 eFuse programming Profile: 00 +
	Profile 1 (MHz): 50 thange (opm): 100
	Profile 2 (MHzr) 100 2 You are about to permanently program the device. Do you want to
	Small change update
	Yes
	Frequency select signal
	FS1:F80: 00 v Apply
Messages	
×	
Info: Device is not eFused	
Info: Programming started for P Info: Programming operation co	rojeđ, 00 at 12/13/2016 1:0:032 PM mpleto successfully
Info: Device is not eFused	
	v

Figure 3-12. eFuse Programming using ClockWizard 2.1

CAUTION CAUTION For Configuration cannot be modified or erased once it is written to the eFuse. The CY29430 supply must be set to 2.5 V for eFuse programming. Setting the CY29430 supply to any other voltage during eFuse programming will cause potential damage to the device.

After the device is eFuse-programmed, you can only change the output frequency through the following ways. Note that these changes will revert after a power cycle.

- Large change programming: This refers to the case where the frequency is changing more than ±500 ppm. Enter the desired frequencies in the Profile 0 (MHz), Profile 1 (MHz), Profile 2 (MHz), and Profile 3 (MHz) fields, and click on Large change update. The device will recalibrate and reconfigure the internal circuit and the output will change to the desired frequencies.
- Small change programming: This refers to the case where the frequency is changing less than ±500 ppm. Select FS profile, enter the desired ppm in the small change (ppm), and click on Small change update. The device will recalibrate and reconfigure the internal circuit and the output will change to the desired frequencies.

3.7 Custom Profile Generation

ClockWizard 2.1 should be used to generate custom configuration profiles. For details on how to create custom profiles, refer to the ClockWizard 2.1 User Guide located in **Help** > **User guide** of the ClockWizard 2.1 software.

To understand the output termination settings of different output standards (for example, LVPECL, HCSL, or LVDS), refer to the B.1. Termination Settings of Differential Clock Outputs section.

4 Hardware



4.1 Board Overview

The CY3677 EVK is used for evaluating the CY29430 device.

Following are the key features of the CY3677 EVK:

- Powered from a USB port
- Jumper to configure on-board LDO output
- Jumper to short or isolate external connection for termination settings

Figure 4-1 illustrates the CY3677 EVK board with a markup of the on-board components.

Figure 4-1. CY3677 EVK On-board Components





Label Name	Description
CY29430FLQXI	CY29430FLQXI is the Cypress clock chip that is evaluated with the CY3677 EVK.
Main Power Supply Jumper (J1)	Short pin 1 and 2 of jumper J1 to power up the CY29430. The core supply and I/O supply are shorted on the board, and hence are the same for the device.
LDO Sottings lumpor (112)	Set the J13 jumper per Table 4-2 to set the LDO output voltage.
LDO Settings Jumper (J15)	Note: The brightness of LED2 will vary depending on the voltage selection. It will be brightest at 3.3 V and dimmest at 1.8 V.
USB Mini-B Connector	Connect the kit to a PC using the USB Standard-A to Mini-B cable.
Differential Clock Output	Connect SMA cables to the SMA connectors (J7 and J8) on one end and to an oscilloscope on the other end.
Single-Ended Clock Output (LVCMOS)	Connect the SMA cable to the SMA connector (J10) on one end and to an oscilloscope on the other end.
External Clock Reference (TCXO)	Connect the SMA cable to the SMA connector (J11) on one end and to an external clock reference (TCXO) on the other end.
Termination Jumper (J5)	The board has an on-board jumper (J5) to connect and disconnect output termination.
Status LED	This LED (LED1) turns ON after the USB enumeration is completed. This LED blinks during programming of the CY29430 device from a PC.
Power LED	This LED (LED2) turns ON when the CY29430 device is powered.
OE Control (J16)	Jumper to set the OE input of the CY29430 to enable or disable the clock output.
Frequency Select Jumpers (J14, J15)	J14 and J15 are used to set the frequency select bits of CY29430.
Crystal	On-board 114.285 MHz OT3 crystal for the reference input of the CY29430 device. This crystal has frequency tolerance of ± 20 ppm.
PSoC 5LP (CY8C5868LTI-LP039)	On-board PSoC 5LP device that converts the USB data-stream to I^2C format to program the CY29430 device.
VCXO Input (J2)	This jumper can be used to evaluate the VCXO operation of the CY29430 device. Vc (voltage at J2.1 pin) is by default set to 0 V via a jumper shunt. You can remove the shunt and instead apply an external power supply voltage (DC) to pin J2.1 to evaluate the VCXO operation.
	Cypress recommends that you contact our Technical Support team at www.cypress.com/support before connecting any external power supply to this jumper.

Table 4-1: CY3677 EVK Onboard Components Description

J13 Settings	LDO Output Voltage (Supply of CY29430)
Short pin 1 and 2	2.5 V
Short pin 2 and 3 (default)	3.3 V
Open	1.8 V

CAUTION	The kit should strictly be operated from a USB supply by connecting to a PC.
	The PCB should not be powered by any external source. Application of an external power source to any of the jumper pins or test points may cause potential damage of the PCB.
	To configure the device to a clock standard other than those specified in the example projects, or to apply custom termination voltage, go to our support web page at www.cypress.com/support, or e-mail at: clocks@cypress.com.
	Incorrect application of supply or termination voltage will cause performance degradation of the clock output. Prolonged incorrect operation may permanently damage the kit.



4.2 Board Details

4.2.1 Default Jumper Settings

The CY3677 EVK comes with default jumper settings that set the I/O and core supply voltages as 3.3 V. Table 4-3 lists the default jumper settings.

Jumper	Default Settings	Description
J1	Pin 1 and 2 are shorted	Power on CY29430.
J2	Pin 1 and 2 are shorted	VCXO input set to 0 V.
J5	Pin 1 and 2 are shorted	CY29430 output termination voltage set to 0 V through the 50- Ω termination resistors.
J13	Pin 2 and 3 are shorted	3.3 V selected for CY29430.
J14	Pin 1 and 2 are shorted	FS1 set to VDD_DUT (logic '1').
J15	Pin 1 and 2 are shorted	FS0 set to VDD_DUT (logic '1').
J16	Pin 2 and 3 are shorted	OE pin set to 0 V (logic '0').

Table 4-3: Default Jumper Settings on the k	≺it
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4.2.2 Power Settings

The only power option of this EVK is 5 V that comes from a USB port. The device has the same core and I/O supply voltage. The supply voltage of the device can be selected from on-board generated supplies of 1.8 V, 2.5 V, or 3.3 V.

Table 4-2 lists the hardware settings required for power selection.

CAUTION The J13 selection must match with the software configuration of the supply voltage during functional programming and must be set to 2.5 V during eFuse programming. Mismatch between the J13 setting and ClockWizard 2.1 setting may cause incorrect output or reliability problems with the device.

4.2.3 Functional Programming

The board should be connected to a PC through a USB connector to configure and program the device. Refer to the CY3677 EVK USB Connection section to learn how to connect the kit to a PC. Figure 4-2 illustrates the programming section of the kit.



Figure 4-2. Programming the CY29430 Device

The USB interface provides a 5-V power supply. The PSoC 5LP converts the JEDEC profiles into an I²C-compatible format, which is then loaded into the CY29430 clock device.

Note: During functional programming, keep the power supply of the CY29430 device (hardware settings) the same as in the ClockWizard 2.1 configuration (software settings). Table 4-2 provides the supply settings for the CY29430. During eFuse programming, set the power supply of the CY29430 to 2.5 V.

The Example Projects section provides the example projects (.cpj files) created in ClockWizard 2.1.



4.2.4 LED Indicators

Table 4-4: LED Indicators

LED	Label	Indicator	Description
LED1	USB_PWR_LED	USB Power and Status	This LED turns ON when the kit is connected to the USB port on a PC using the cable provided.
			If this LED does not turn ON, it indicates that the USB enumeration of the kit did not happen with the host PC. This LED blinks continuously when the device is being programmed through the PSoC 5LP device.
			Note:
			This LED may glow with low intensity under the following condition:
			The CY29430 supply is disconnected through the jumper (J1). This low-intensity LED glow may be misleading to the user on the status of the USB connection to the board. It is, therefore, recommended to avoid this condition during use of the kit.
LED2	POWER_LED	Clock Device Power	This LED turns ON when the core of the CY29430 device is powered. Ensure that a jumper shunt is populated or not populated on J13 per Table 4-2 for proper supply of CY29430.
			The intensity of this LED for 1.8 V is lower compared to 2.5 V and 3.3 V.

4.2.5 On-Board Crystal

This EVK is populated with a Third Overtone Crystal (OT3) of 114.285 MHz. This crystal has a frequency tolerance of ± 20 ppm. It serves as a clock source for the CY29430 device.

4.2.6 TCXO Input Reference

The CY29430 device can also be evaluated with external TCXO reference. The external reference clock source must be connected to the SMA connector J11. To activate the TCXO reference clock effective to the CY29430 device, desolder the resistor R40, and populate the $0-\Omega$ resistor R42. R40 and R42 are located on the secondary side near the Y1 crystal.

4.2.7 Frequency Select (FS)

The volatile and the nonvolatile memory of the CY29430 device stores four frequency profiles. The Frequency Select inputs of the device (FS0 and FS1) can be controlled by the on-board jumpers J14 and J15. FS0 and FS1 can also be configured using ClockWizard 2.1. Refer to Table 4-5 for the Frequency Select operation.

Jumper Settings for Hardware Control of FS Bits		Jumper Settings for ClockWizard 2.1 Control of FS Bits			FS Input (logic) to CY29430		Frequency Profile
J14 Settings	J15 Settings	J14 Settings	J15 Settings	ClockWizard 2.1 Settings	FS1_DUT	FS0_DUT	Selected
Open	Open	Short pin 2 and 3	Short pin 2 and 3	Select FS1:FS0: as 00 and click Apply	0	0	0
Open	Short pin 1 and 2			Select FS1:FS0: as 01 and click Apply	0	1	1
Short pin 1 and 2	Open			Select FS1:FS0: as 10 and click Apply	1	0	2
Short pin 1 and 2	Short pin 1 and 2			Select FS1:FS0: as 11 and click Apply	1	1	3

Table 4-5: Jumper Settings for Frequency Select

Note: The Hardware and ClockWizard 2.1 control are mutually exclusive and only one works at a time



and CLK_N.

Hardware

4.3 Evaluating Different I/O Standards Using the CY3677 EVK

The CY29430 device has one differential clock output pair (*CLK_P* and *CLK_N*) and one single-ended clock output (*CLK_SE*). The onboard components of the CY3677 can be configured to different settings for evaluating different clock standards.

Figure 4-3 and Table 4-6 illustrate the on-board components related to the CY29430 output clocks.

Figure 4-3. CY3677 Output Termination Settings



1.00

Table 4-6: CY29430 Clock Outputs

CLK P and CLK N.

Clock Output	CY29430 Pin	SMA Connector on CY3677	Resistor to Set Termination (50 Ω)
CLK_P	10	J8	R30
CLK_N	9	J7	R31

 CLK_SE
 11
 J10
 NA

 The CY29430 device supports LVPECL, LVDS, HCSL, LVPECL2, and CML differential output types. R30 and R31 are the on-board output termination resistors. The termination settings are controlled by the J5 jumper shunt. The typical laboratory setup for the evaluation of this kit is shown in Figure 4-4. See Table 4-7 to set correct on-board termination option of CLK_P

Table 4-7: J5 Jumper Settings to	Terminate Differential Clock Outputs
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IO Standard	J5 Jumper Position	Description
LVPECL, HCSL	Short	CLK_P and CLK_N termination voltage set to 0 V through the 50- Ω termination resistors.
LVDS	Open	100 Ω differential impedance between the <i>CLK_P</i> and <i>CLK_N</i> .
CAUTION If you want to configure this kit to any other mode, or any other termination setup, it is recommended to contact our support through the www.cypress.com/support web page, or e at clocks@cypress.com. J5 should not be powered by any external source. Connection of external power source damage the EVK.		