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CY3679 EVK

CY3679 Evaluation Kit User Guide

Doc. # 001-95978 Rev. *B

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Contents

Safety Information

The CY3679 Evaluation Kit is intended for use as a development platform for hardware or software in a laboratory environment. The board is an open system design, which does not include a shielded enclosure, so the board may cause interference to other electrical or electronic devices in close proximity. In a domestic environment, this product may cause radio interference. In such cases, the user may be required to take adequate preventive measures. Also, this board should not be used near any medical equipment or RF devices.

Attaching additional wiring to this product or modifying the product operation from the factory default may affect its performance and cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.

	The CY3679 Evaluation Kit contains electrostatic discharge (ESD)-sensitive devices. Electrostatic charges readily accumulate on the human body and any equipment, and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused CY3679 Evaluation Kit boards in the protective shipping package.

General Safety Instructions

ESD Protection

ESD can damage boards and associated components. Cypress recommends that the user perform procedures only at an ESD workstation. If ESD workstation is not available, use appropriate ESD protection by wearing an antistatic wrist strap attached to the chassis ground (any unpainted metal surface) on the board when handling parts.

Handling Boards

CY3679 Evaluation Kit is sensitive to ESD. Hold the board only by its edges. After removing the board from its box, place it on a grounded, static free surface. Use a conductive foam pad if available. Do not slide board over any surface.

Certification Disclaimer

This kit is intended for demonstration, evaluation or development purposes only and is not considered by Cypress Semiconductor to be a finished end-product fit for general consumer use. It generates and can radiate radio frequency energy and has not been specifically tested for CE certification compliance. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at their own expense will be required to take whatever measures may be required to correct this interference.

1 Introduction

Thank you for your interest in CY3679 Evaluation Kit (EVK). CY3679 EVK is designed to enable you to evaluate the programmable clock device CY27410, the latest addition to programmable devices in Cypress's timing product portfolio. The clock device CY27410 is a high-performance programmable clock generator with four independent fractional PLLs that generates any frequency with a zero-ppm synthesis error. The device offers eight differential and four single-ended outputs and comes in a 48-pin QFN package for industrial applications. The differential outputs can also be configured as single-ended. The differential I/O standards supported are LVDS (Low Voltage Differential Signaling), LVPECL (Low-Voltage Positive Emitter-Coupled Logic), HCSL (High-Speed Current steering logic) and CML (Current Mode Logic). The single–ended I/O standard supported is LVCMOS (Low Voltage Complementary Metal Oxide Semiconductor). The device also supports features like voltage-controlled crystal oscillator (VCXO), I^2C, and Frequency Select (FS) options.

This kit allows you to evaluate both AC and DC parameters of the output signals by making required on-board termination settings.

This kit is available through the Cypress Online Store or through our distributors.

1.1 CY3679 EVK Contents

The CY3679 EVK includes the following:

- CY3679 Evaluation Board
- Power cables (banana to 2-pin housing cables) for external supply
- Jumper shunts
- USB Standard-A to Mini-B cable
- Quick Start Guide

Figure 1-1. Kit Contents

Inspect the contents of the kit. If you find any part missing, contact your nearest Cypress sales office for help: www.cypress.com/go/support

1.2 Getting Started

To learn the solution quickly and apply it to your design, see the Quick Start Guide inside the kit box or in the installation directory. The default location for the kit documents is:

```
<Install_Directory>\CY3679 EVALUATION KIT\<version>\Documentation
```

This guide will help you get acquainted with the CY3679 Evaluation Kit:

- The Software Installation chapter describes the installation of the kit software.
- The Kit Operation chapter describes the major feature of CY3679 Evaluation kit such as evaluating the clock device.
- The Hardware chapter describes the hardware content of the CY3679 Evaluation Kit and the hardware operation.
- The Sample Projects chapter describes the multiple profiles that will help you understand how to evaluate different supported output standards on this kit. These profiles can be evaluated with the default termination settings on the board.
- The Appendix captures DC/AC Measurements of Clock Outputs, Schematics, Fab Drawing, and the bill of materials (BOM).

1.3 Additional Learning Resources

Visit www.cypress.com/go/CY3679 and www.cypress.com/go/CY27410 for additional learning resources including datasheets and application notes.

1.4 Technical Support

For assistance, go to our support: www.cypress.com/support web page, or contact our customer support at +1(800) 541-4736 Ext. 2 (in the USA), or +1 (408) 943-2600 Ext. 2 (International).

1.5 Document Conventions

Table 1-1. Document Conventions for Guides

Convention	Usage
Courier New	Displays file locations, user entered text, and source code: C:\ ...cd\icc\
Italics	Displays file names and reference documentation.
[**Bracketed, Bold**]	Displays keyboard commands in procedures: [**Enter**] or [**Ctrl**] [**C**]
File > Open	Represents menu paths: File > Open > New Project
Bold	Displays commands, menu paths and icon names in procedures: Click the **File** icon and then click **Open**.
Times New Roman	Displays an equation: 2 + 2 = 4
Text in gray boxes	Describes Cautions or unique functionality of the product.

1.6 Acronyms

Table 1-2. List of Acronyms used in this document

Acronym	Definition
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVDS	Low Voltage Differential Signaling
HCSL	High speed Current Steering Logic
CML	Current Mirror Logic
SMA	Subminiature version A
DNP, DNM	Do Not Populate, Do Not Mount
SS	Spread Spectrum
ZDB	Zero Delay Buffer
NZDB	Non-Zero Delay Buffer
PCIe	PCI Express
I^2C	Inter-Integrated Circuit
LDO	Low-Dropout
VCXO	Voltage Controlled Crystal Oscillator
BOM	Bill of Materials
FS	Frequency Select
JEDEC	Joint Electron Device Engineering Council

2 Software Installation

This chapter describes the steps to install the software tools and packages on a PC for using the CY3679 Evaluation Kit.

2.1 Before You Begin

All Cypress software installations require administrator privileges. Ensure that you have the required privileges on the system for successful installation. Before you install the kit software, close any other Cypress software that is currently running.

2.2 Install Software

Follow these steps to install the CY3679 Evaluation Kit software:

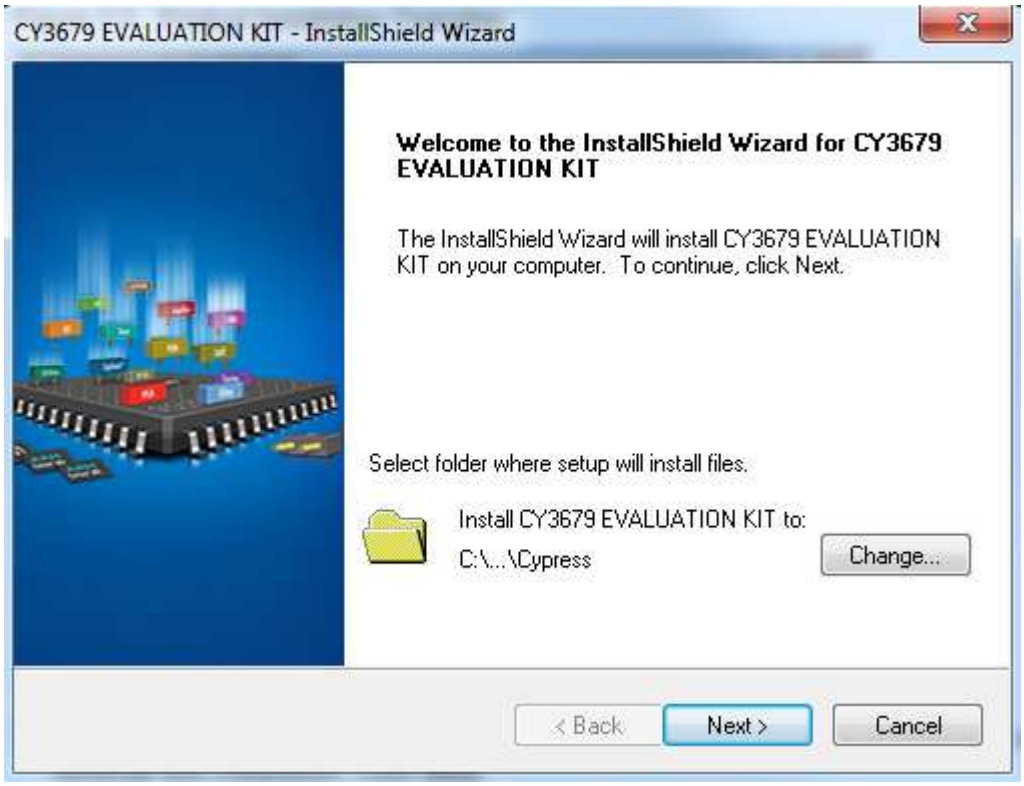
1. Download the CY3679 Evaluation Kit software from www.cypress.com/go/CY3679. The software is available in the following formats:
   a. **CY3679 Evaluation Kit Complete Setup:** This installation package contains the files related to the CY3679 Evaluation Kit. However, it does not include the Windows Installer or Microsoft .NET framework packages. If these packages are not available on your computer, the installer directs you to download and install them from the Internet.
   b. **CY3679 Evaluation Kit Only Package:** This executable file installs only the CY3679 Evaluation Kit contents, which include sample projects, hardware files, and user documents. This package can be used if all the software prerequisites (listed in **step 5**) are installed on your PC.
   c. **CY3679 Evaluation Kit CD/DVD ISO:** This file is a complete package, stored in a CD/DVD-ROM image format that you can use to create a CD/DVD or extract using an ISO extraction program such as WinZip or WinRAR. The file can also be mounted similar to a virtual CD/DVD using virtual drive programs such as Virtual CloneDrive and MagicISO. This file includes all the required software, utilities, drivers, hardware files, and user documents.
2. If you have downloaded the ISO file, mount it on a virtual drive. If you do not have a virtual drive to mount, extract the ISO contents using the appropriate ISO extractor (such as MagicISO or PowerISO). Double-click *cyautorun.exe* in the root directory of the extracted content or the mounted ISO if the “Autorun from CD/DVD” option is not enabled on the PC. The installation window will appear automatically.

   Note: If you are using the “Kit Complete Setup” or “Kit Only Package” file, then go to step 4 for installation
3. Click **Install CY3679 EVALUATION KIT** to start the installation, as shown in Figure 2-1.

Figure 2-1. Installer Screen

4. Select the folder in which you want to install the files related to CY3679 Evaluation Kit. Choose the directory and click **Next** as shown in Figure 2-2.

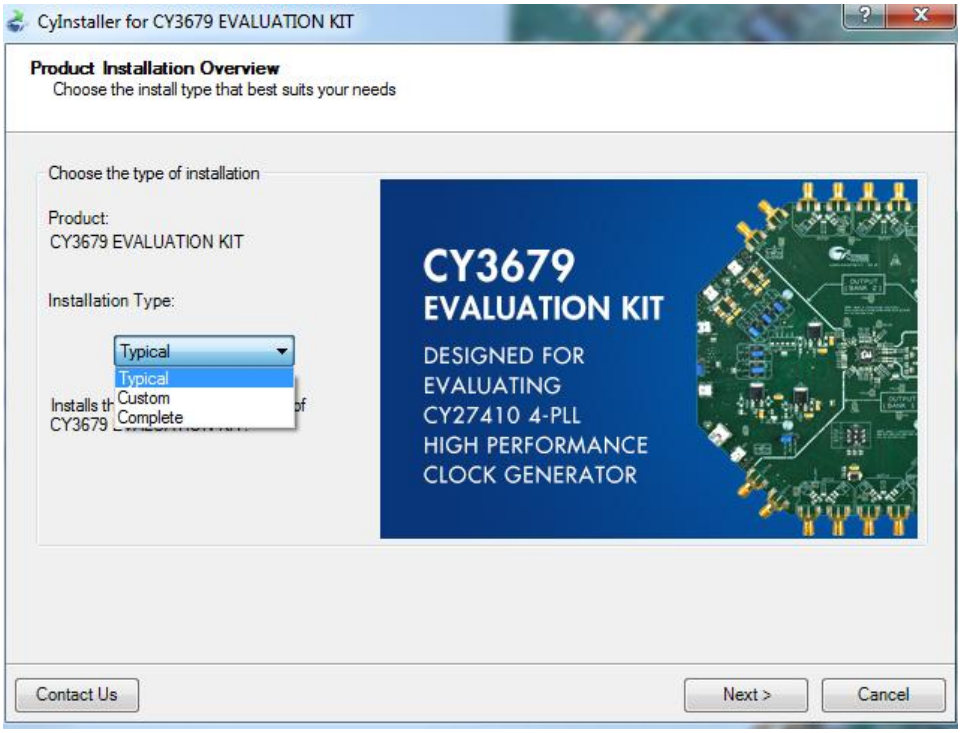
Figure 2-2. InstallShield Wizard



5. When you click **Next,** the CY3679 Evaluation Kit installer automatically installs the required software, if it is not present on your computer. The pre-requisites are Clock Wizard 2.0 and PSoC Programmer 3.23.0 or later.

6. Choose the installation type in the Product Installation Overview window, as shown in Figure 2-3. Click **Next** after you select the installation type.

Figure 2-3. Product Installation Overview



7. Read the license agreement and select **I accept the terms in the license agreement** to continue with installation. Click **Next**.

   When the installation begins, a list of packages appears on the installation page. A green check mark appears next to each package after successful installation.

8. Click **Finish** to complete the CY3679 Evaluation Kit installation.
9. Enter your contact information or select the **Continue Without Contact Information** check box.
10. Click **Finish** to complete the CY3679 Evaluation Kit installation.

    After the installation is complete, the kit contents are available at:

    `<Install_Directory>\CY3679 EVALUATION KIT\<version>.`

    Default location:

    Windows 7 (64-bit): `C:\Program Files (x86)\Cypress\CY3679 EVALUATION KIT`

    Windows 7 (32-bit): `C:\Program Files\Cypress\CY3679 EVALUATION KIT`

2.3 Install Hardware

There is no additional hardware installation required for this kit.

2.4 Uninstall Software

The software can be uninstalled using one of the following methods:

- Go to **Start** > **All Programs** > **Cypress** > **Cypress Update Manager** > **Cypress Update Manager**, and then click the **Uninstall** button for the appropriate software package.
- Go to **Start** > **Control Panel** > **Programs and Features**, and then click the **Uninstall/Change** button for the appropriate software package.

3 Kit Operation

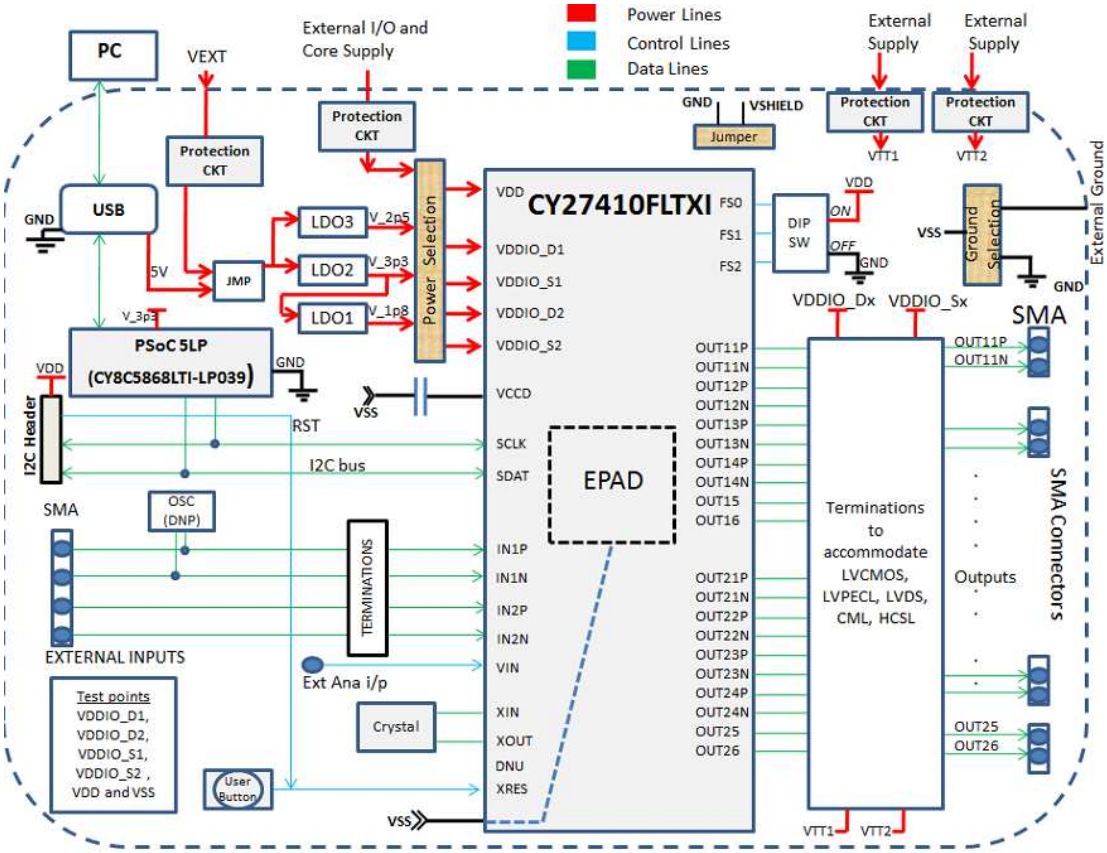
CY3679 EVK can be used to evaluate CY27410, a new-generation high-performance clock generator device. Connect CY3679 kit through USB to a PC running Cypress's Clock Wizard 2.0 software. The clock device CY27410 can be configured and programmed to generate frequencies with best-in-class performances.

3.1 Theory of Operation

The CY3679 EVK offers twelve outputs: eight differential and four single-ended. The outputs are distributed among two banks, Bank1 and Bank2. Each bank has four differential and two single-ended outputs. Differential outputs can be configured as single-ended outputs also. The inputs to the CY27410 device on this kit can be provided either with an on-board crystal or with external clock references.

The kit is capable of generating fixed 3.3 V, 2.5 V, and 1.8 V voltages from a 5 V input (either USB or external power supply).The on-board PSoC 5LP (U7) performs the USB-to-I^{2}C conversion and controls one power LED and one status LED. The LDOs (U2, U3, and U4) generate fixed supply voltages of 3.3 V, 2.5 V, and 1.8 V. The block diagram of the kit is shown in Figure 3-1.

Figure 3-1. Block Diagram



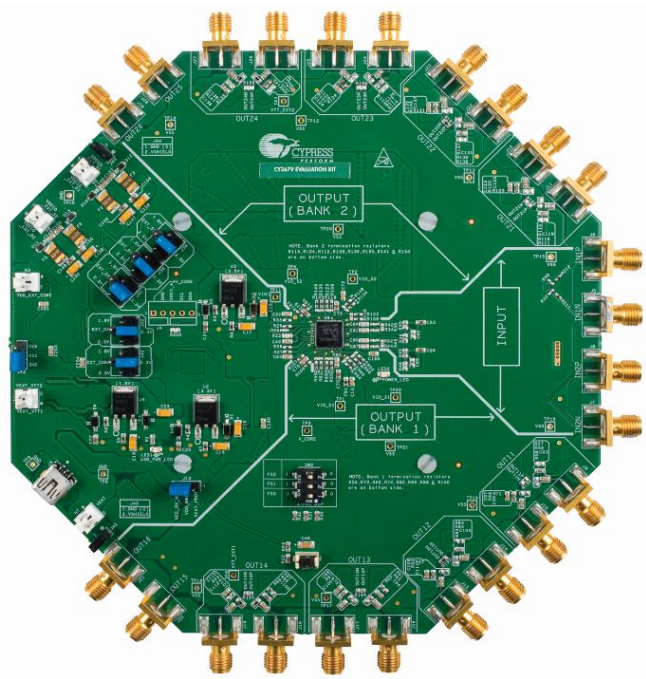
3.2 Functional Description

Each of the eight differential output drivers is AC-coupled to the SMA connectors, so the output signal will have no DC bias. If a signal with a DC bias is required or measurement is done using an active probe, the series AC-coupling capacitors can be replaced with a 0-Ω resistor. The EVK provides footprints for optional output terminations.

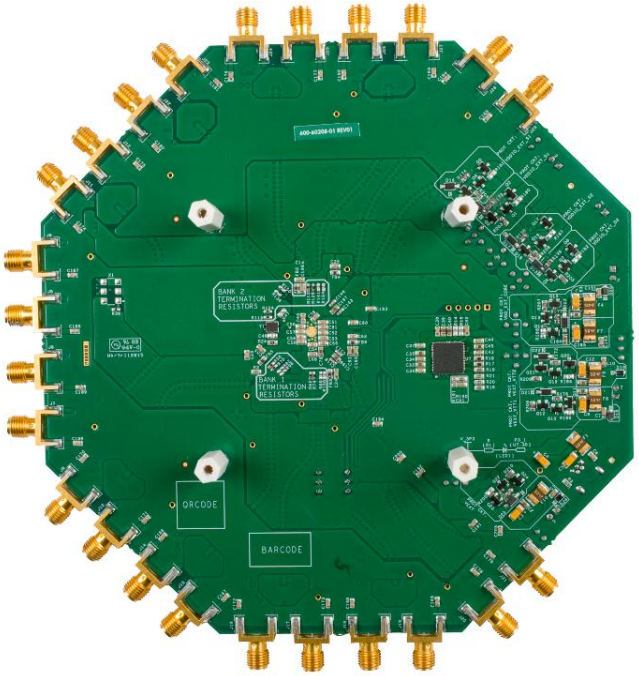
The termination options for differential outputs OUT11 to OUT14 and OUT21 to OUT24 in the evaluation board are listed in Evaluating Different I/O Standards Using CY3679 EVK. These termination circuits are designed to terminate the output clocks in LVPECL, LVDS, HCSL, CML, and LVCMOS signal types by populating (or by not populating) some resistors. DC or AC coupling of these outputs is also supported.

The top and bottom views of the kit are shown in Figure 3-2.

Figure 3-2. Top and Bottom Views of CY3679 Kit



TOP View

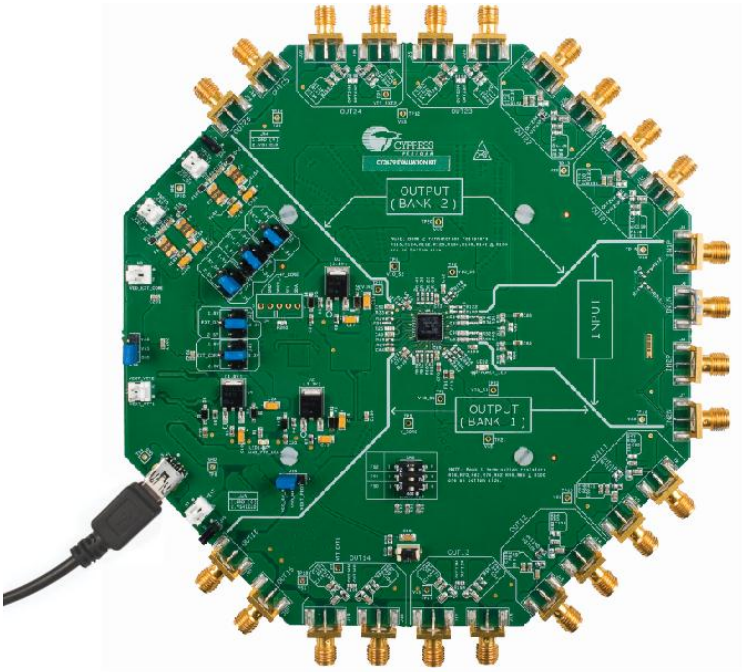


BOTTOM View

3.3 CY3679 Kit USB Connection

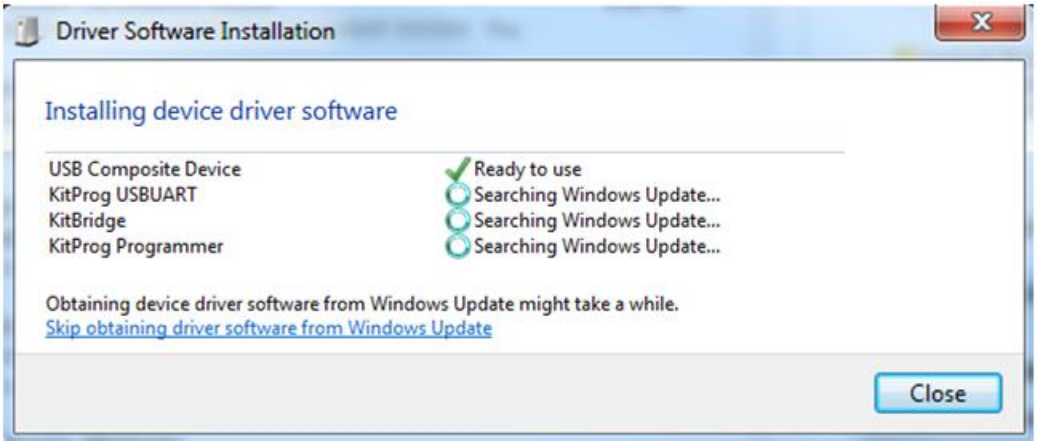
The clock device (CY27410) on the kit is loaded with a set of default configurations. For device configurations other than the default configurations, the clock device needs to be programmed with the desired configuration. The Clock Wizard 2.0 application is required for programming any configuration. Therefore, the kit should be connected (as shown in Figure 3-3) to the PC through the USB for programming.

Figure 3-3. Kit Connected through USB



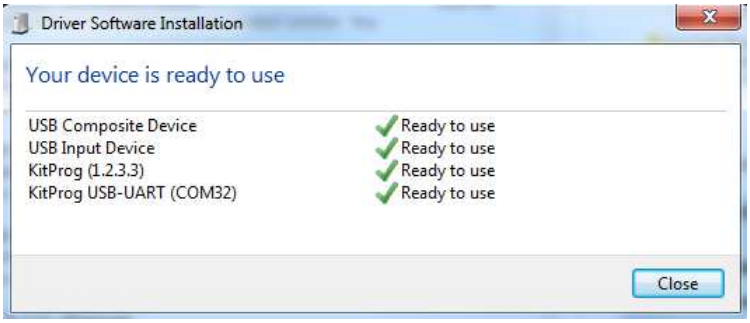
The kit enumerates as a USB Composite Device as part of the Driver Software Installation in Windows.

Figure 3-4. USB driver Installation



Once all the required drivers are installed, it shows that the device is ready to use.

Figure 3-5. USB Driver Installation Complete



3.4 Programming the Device CY27410

Clock Wizard 2.0 is used to program the device CY27410. The sample Clock Wizard 2.0 projects can be found at the following location:

`<Install_Directory>\CY3679 EVALUATION KIT\<version>\Firmware\Sample Projects`

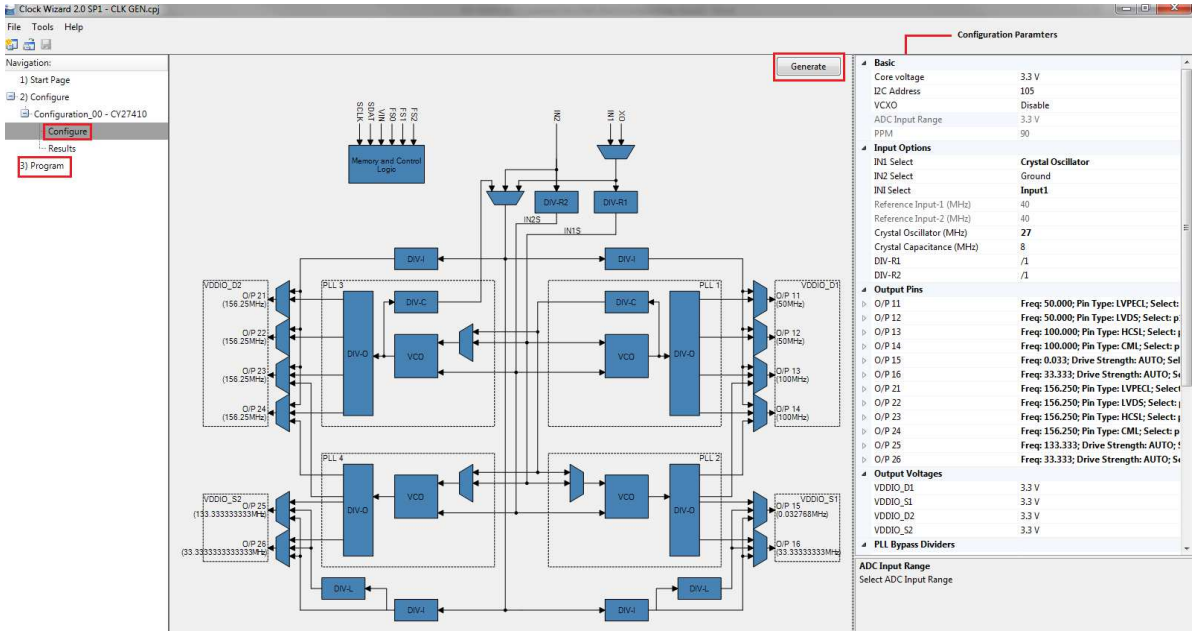
Configuration profiles generated from these projects can be used to evaluate CY27410 device. Refer Section 4.2.5 for hardware settings of the kit before programming.

3.4.1 Generating and Programming the Device Configuration Profile

Clock Wizard 2.0 tool is used to generate profiles and program the device. Clock Wizard 2.0 executable can be located in installation folder at `<Install_Directory>\CyClockWizard\2.0\bin\clockwizard.exe`.

1. Connect CY3679 EVK to your machine through USB cable.
2. To Launch Clock Wizard 2.0 application, go to **Start>All Programs>Cypress>ClockWizard 2.0**.
3. Project files are located in Project folders. For example, CLK GEN folder contains *CLK GEN.cpj* project file.
4. Select **File** menu in Clock Wizard 2.0 GUI, select **Open project**, browse the required project file with *.cpj* extension, and then click **Open**.
5. Click on **Configure** as shown in Figure 3-6.

Figure 3-6. Generating and Programming Configuration Profile using Clock Wizard 2.0



6. Click the **Generate** button. This will generate the JEDEC file for the configuration selected. The various configuration parameters can be seen on the right side of the block diagram. For further details on configuration parameters, refer to Clock Wizard 2.0 User Guide.
7. The results generated from this configuration can be viewed by clicking on **Results**. The results are split across 8 different profiles (**Profile 1** to **Profile 8**). You can expand the required Profile to see the configuration.
8. To program CY27410, select **Program**, under Navigation. Select appropriate **Ports** and **Configuration** before programming. Set the **I2C Address** to **105**, and then click the **Program** button. This will program the device directly from Clock Wizard. Refer to Clock Wizard User Guide for details.
9. The device will be programmed. LED1 blinks to indicate that the device is being programmed.

   The sample projects provided with this kit are configured to work with the default termination settings on different outputs. You can configure any output type, for example LVPECL, HCSL, or LVDS, on any output. See Section A.1. DC/AC Measurements of Clock Outputs for required termination settings for different I/O types.

3.5 Custom Profile Generation

Clock Wizard 2.0 should be used to generate custom configuration profiles. For details on how to create custom profiles using Clock Wizard 2.0, refer User Guide of Clock Wizard. To view this document, go to **Help** menu of Clock Wizard 2.0 software and click on **User guide**.

4 Hardware

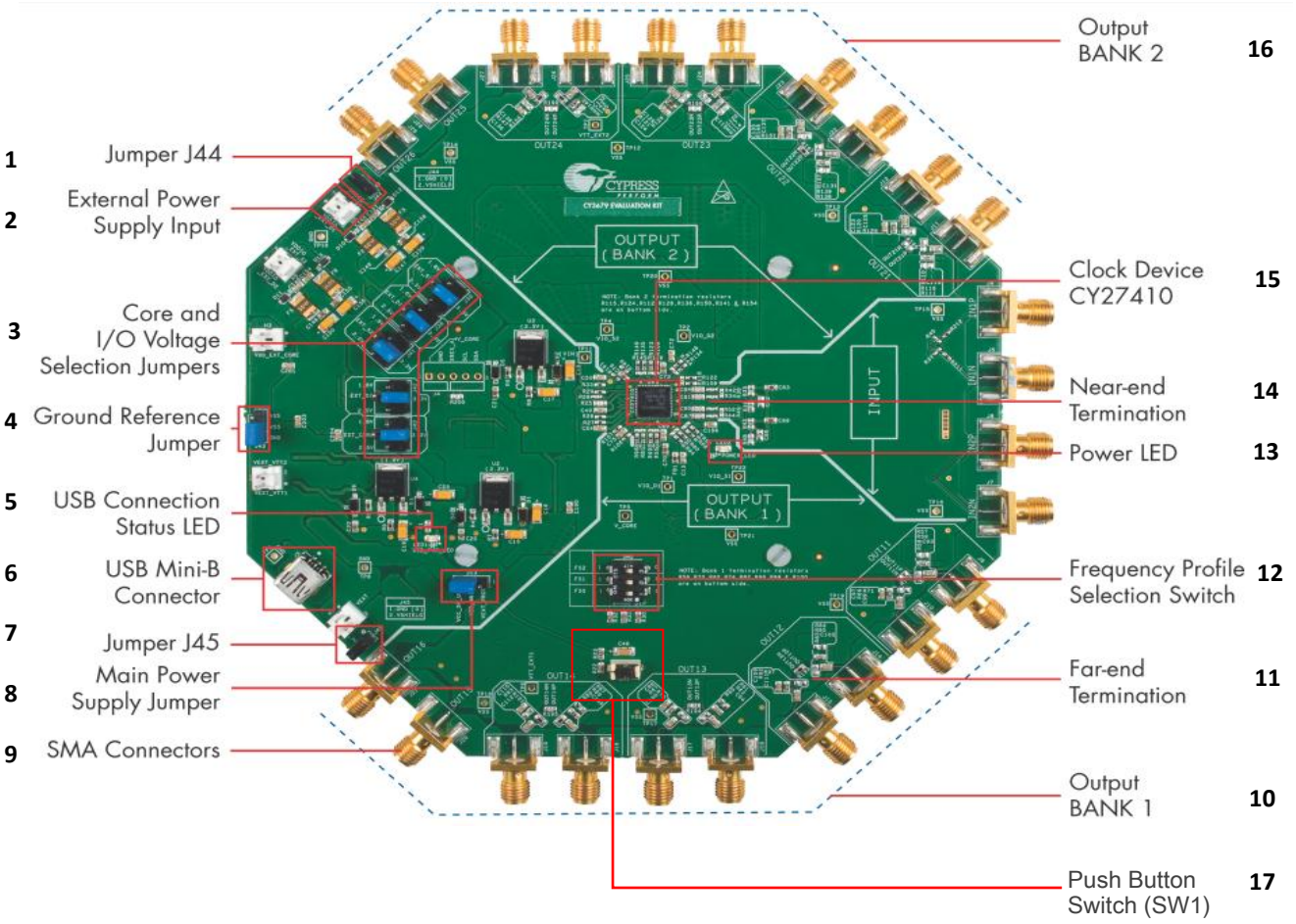
4.1 Board Overview

The CY3679 EVK is used for evaluating the CY27410 device. The following is a list of key features of the CY3679 Kit:

- Powered from either an USB port or external supply
- On-board 27-MHz crystal allows standalone operation
- Wide voltage range operation – both core (VDD) and I/O supplies (VDDIO_D1, VDDIO_D2, VDDIO_S1, and VDDIO_S2) can be independently set at 1.8 V, 2.5 V, 3.3 V, or external.
- Adjustable VDD and VSS provide flexibility to users for DC and AC measurements of signals using SMA connectors
- Jumper to short or isolate GND and VSS

Figure 4-1 shows the CY3679 board with a markup of the onboard components.

Figure 4-1. CY3679 Board with Onboard Components Labeled



1: Jumper J44

Jumper J44 is used to short GND (earth ground) and VSHIELD (SMA Ground). Refer to Grounding Scheme for more details on grounding scheme.

2: External Power Supply Input

The mark-up shows one of the five headers as shown in Figure 4-2 on the board (H1, H3, H5, H6, and H7) to which an external power supply can be connected.

3: Core and I/O Voltage Selection Jumpers

Use these to select the appropriate supply voltage from the on-board generated 3.3 V, 2.5 V, or 1.8 V, or direct external supply for Core and I/O supply voltages.

Figure 4-2. Power Select Jumpers Showing Default Selection of 3.3 V for Core and I/O Supply

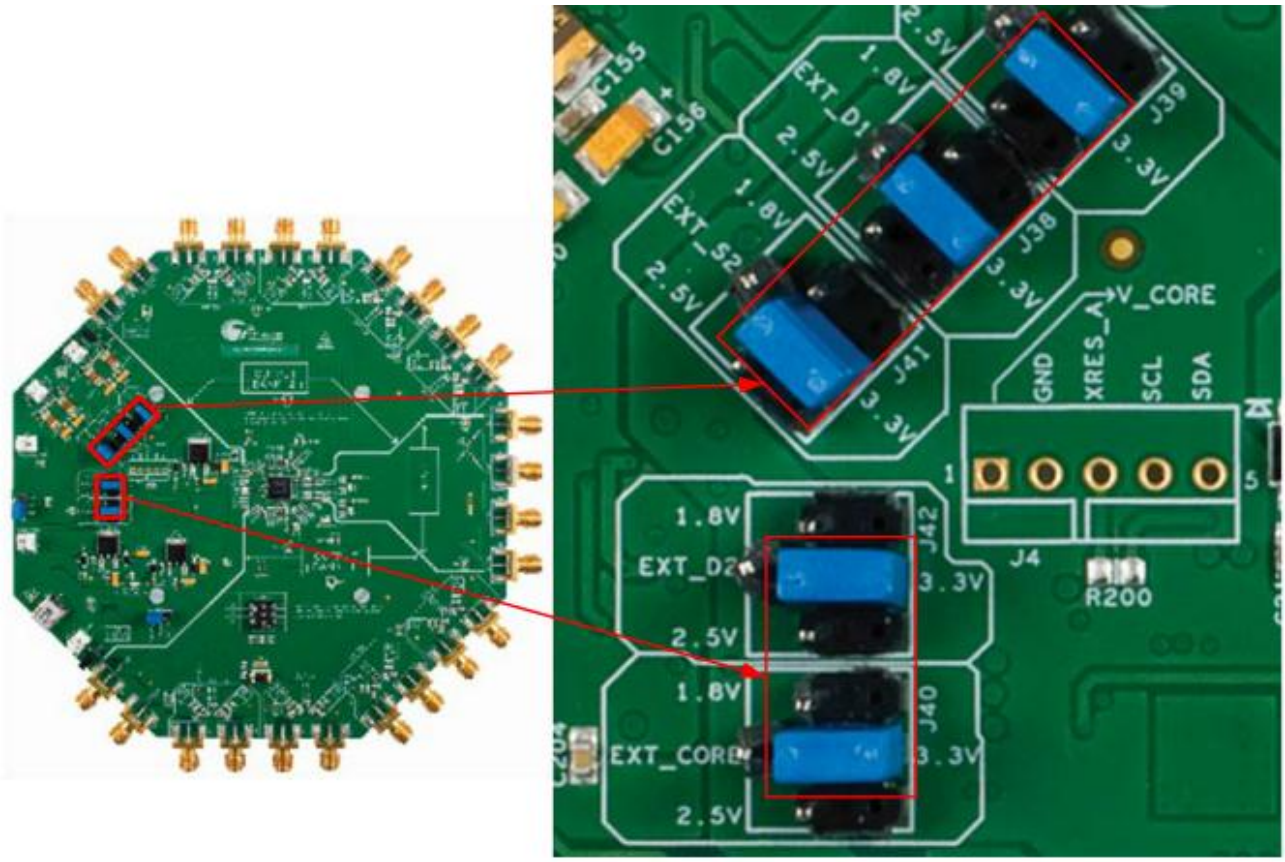
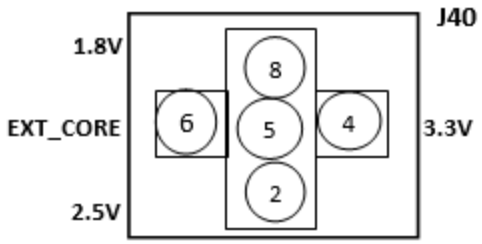


Figure 4-3 shows the pin numbering of these Core and I/O voltage jumpers.

Figure 4-3. Pin Numbering of Core and I/O Voltage Jumpers



See Figure 4-4 through Figure 4-7 to check how the core power supply (VDD) is selected using jumper J40. See Power Section for more details.

Figure 4-4. J40 Setting to Select 1.8 V (Short Pins 5 and 8)

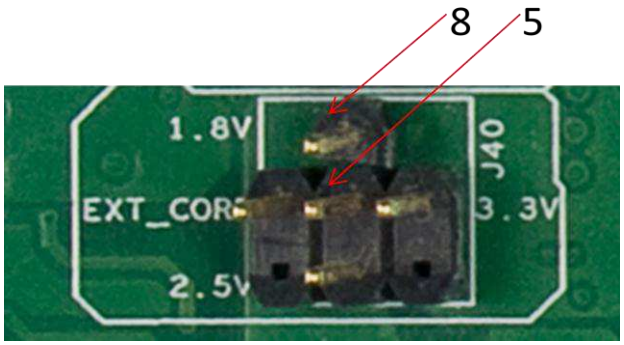


Figure 4-5. J40 Setting to Select 2.5 V (Short Pins 2 and 5)

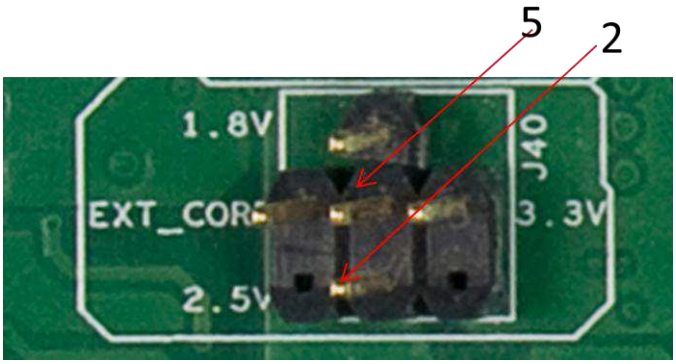


Figure 4-6. J40 Setting to Select 3.3 V (Short Pins 4 and 5)

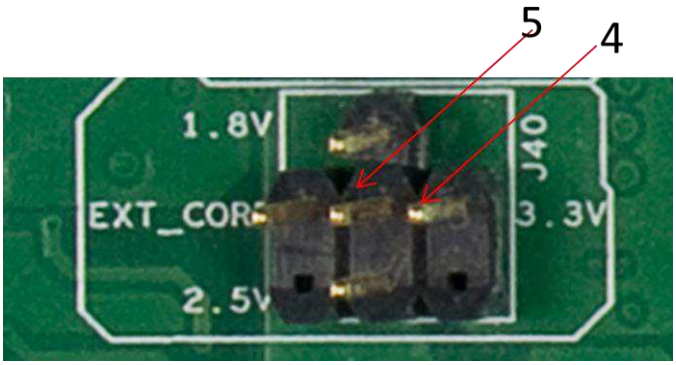
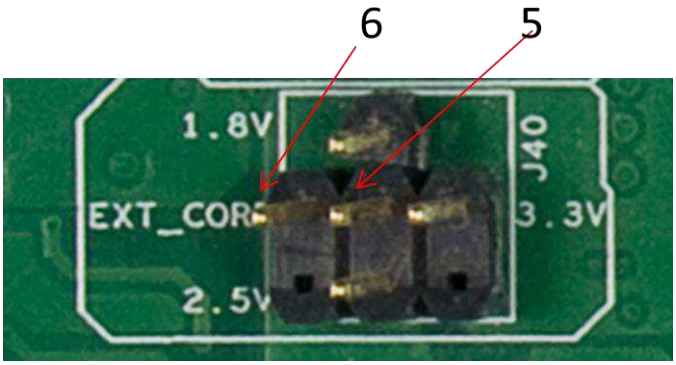


Figure 4-7. J40 Setting to Select External Supply (Short Pins 5 and 6)



Similarly, you can select the power for the I/O supplies VDDIO_D1 (on J38), VDDIO_S1 (on J39), VDDIO_D2 (on J42), and VDDIO_S2 (on J41).

4: Ground Reference Jumper

Proper jumper setting for J43 is important as it provides a ground reference to the device and the rest of the board (see Figure 4-8). See Grounding Scheme for more details.

Figure 4-8. Jumper Setting for Ground Reference

5: USB Connection Status LED

LED1 turns ON when the kit is connected to a PC through USB and blinks continuously when the device is being programmed.

6: USB Mini-B Connector

Connect the kit to a PC using the USB Standard-A to Mini-B cable.

7: Jumper J45

Jumper J45 is used to short GND (earth ground) and VSHIELD (SMA Ground). Refer to Section 4.2.4 for more details on grounding scheme.

8: Main Power Supply Jumper

Short pins **2** and **3** of jumper J13 to use the USB supply input to the kit. This is the default option. Otherwise, short pins **1** and **2** of J13 for external supply input to the kit through VEXT (header H7).

9: SMA Connectors

Connect SMA cables to the SMA connectors on one end and to an oscilloscope on the other end.

10: Output Bank 1

Bank1 consists of four differential and two single-ended outputs. OUT11P-OUT11N, OUT12P-OUT12N, OUT13P-OUT13N and OUT14P-OUT14N are differential output pairs. Differential outputs can be configured as single ended outputs also. OUT15 and OUT16 are dedicated single-ended outputs.

11: Far-End Termination Options

Soldering or desoldering of resistors of an appropriate value may be required for proper terminations. See Appendix A.1 for details.

12: Frequency Profile Selection Switch

Up to eight profiles are stored by programming the flash inside the clock device CY27410. Use the Profile Selection switch to select the active profile. The profile selection can be done while the kit is in operation.

13: Power LED

This LED (LED2) stays ON when the CY27410 device is powered (that is, when the CY27410 core supply is connected by proper selection on jumper J40).

14: Near-End Termination Options

Soldering or desoldering of resistors of an appropriate value may be required for proper terminations. See Evaluating Different I/O Standards Using CY3679 for details.

15: Cypress's Clock Device CY27410

CY27410 is the Cypress clock chip that is evaluated with the CY3679 kit.

16: Output Bank 2

Bank2 consists of four differential and two single-ended outputs. OUT21P-OUT21N, OUT22P-OUT22N, OUT23P-OUT23N, and OUT24P-OUT24N are differential output pairs. Differential outputs can be configured as single-ended outputs also. OUT25 and OUT26 are dedicated single-ended outputs.

17: Push Button Switch (SW1)

This is the push-button switch for Reset operation (XRES) of CY27410. Press this Switch to Reset CY27410.

4.2 Board Details

4.2.1 Default Jumper Settings

The CY3679 EVK comes with default jumper settings that select all I/O and core supply voltages as 3.3 V. Table 4-1 lists the default jumper settings.

Table 4-1. Default Jumper Settings on the Kit

Jumper	Default Settings	Selection
J13	Pin 2 and 3 are shorted	USB supply selected
J38	Pin 4 and 5 are shorted	3.3 V selected for VDDIO_D1
J39	Pin 4 and 5 are shorted	3.3 V selected for VDDIO_S1
J40	Pin 4 and 5 are shorted	3.3 V selected for VDD (core)
J41	Pin 4 and 5 are shorted	3.3 V selected for VDDIO_S2
J42	Pin 4 and 5 are shorted	3.3 V selected for VDDIO_D2
J43	Pin 1 and 2 are shorted	GND and VSS are shorted
J44	Pin 1 and 2 are shorted	GND and VSHIELD* are shorted
J45	Pin 1 and 2 are shorted	GND and VSHIELD* are shorted

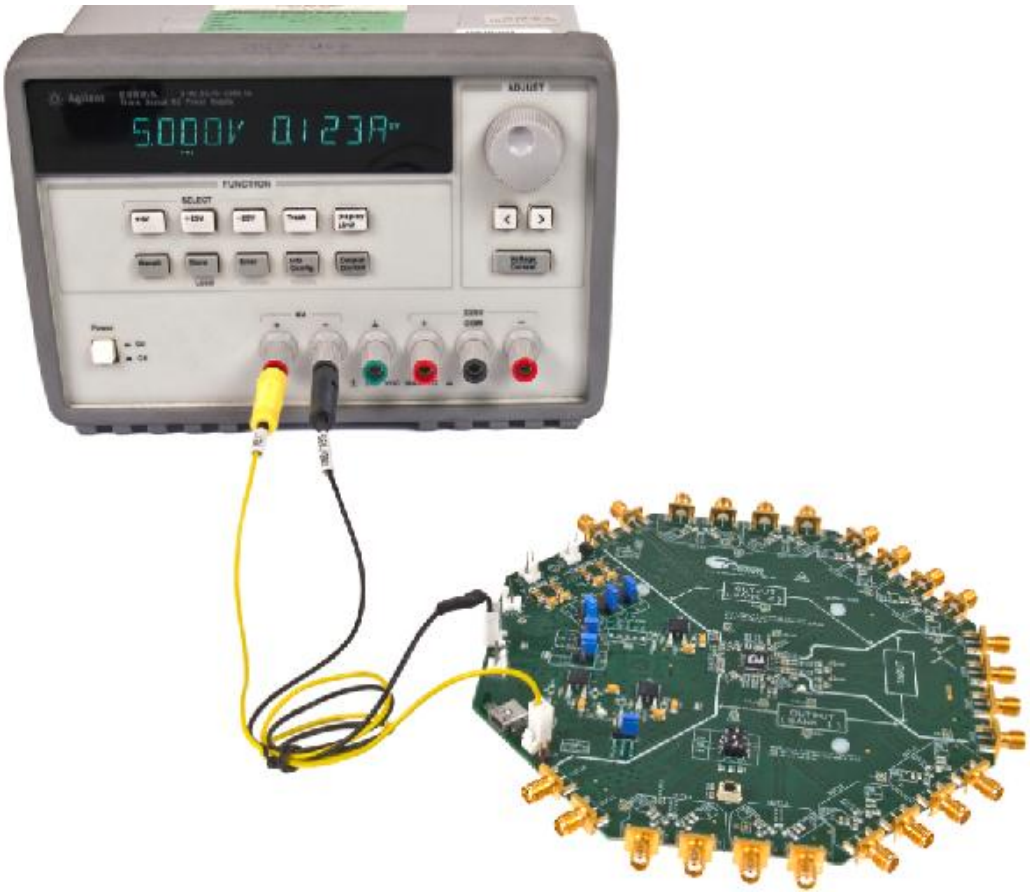
* Refer to Grounding Scheme for more details on grounding scheme

4.2.2 Power Section

You can choose either USB power supply or single external supply (VEXT) to power the kit by setting jumper J13. For using the USB supply option, short pins 2 and 3 of jumper J13.

If the external supply option is used, short pins 1 and 2 of jumper J13. Connect the external 5 V supply to header H7 (VEXT) and ground to VSS pin of J43. Use yellow and black colored wires to connect external supply as shown in Figure 4-9.

Figure 4-9. External 5 V Supply Connection



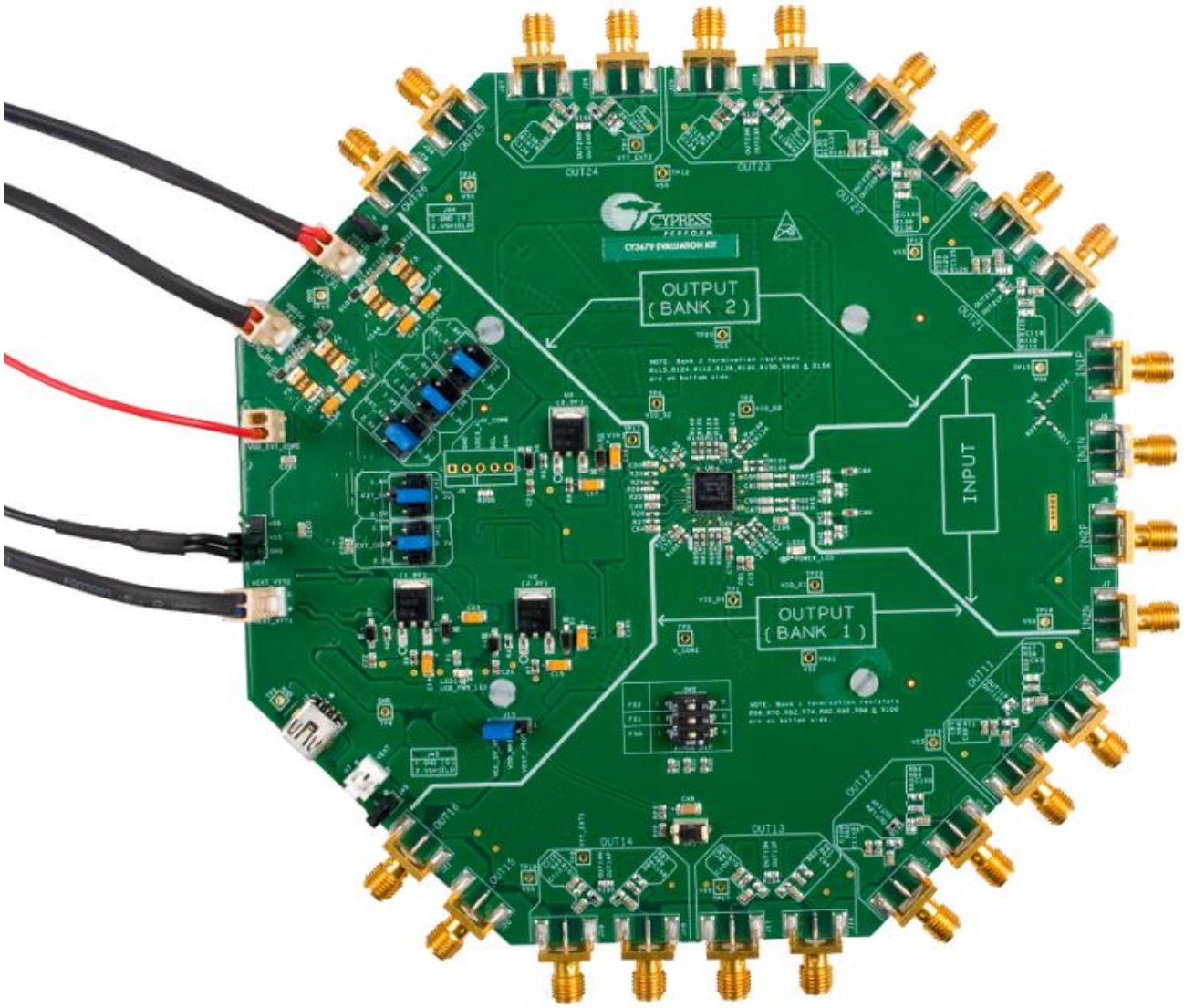
The device requires core and I/O supply voltages. The device has two banks of outputs, with each bank requiring a separate power supply for single-ended and differential outputs. The correct voltage must be selected for core and I/O supply for proper operation. Both core and I/O supplies can be independently selected from on-board generated supplies 1.8 V, 2.5 V, or 3.3 V or direct external supply on respective headers. Table 4-2 lists the hardware settings required for power selection. Figure 4-10 shows the different external supplies connected.

Table 4-2. Power Selection Guide

CY27410 Device Supply	Functionality	Jumper	Jumper Setting				Voltage Selected
			Short Pins 5 and 2	Short Pins 5 and 4	Short Pins 5 and 8	Short Pins 5 and 6	
VDD	Core supply	J40	Yes	No	No	No	2.5 V
			No	Yes	No	No	3.3 V
			No	No	Yes	No	1.8 V
			No	No	No	Yes	EXT (H3.1)
VDDIO_D1	Supply for differential outputs in Bank1	J38	Yes	No	No	No	2.5 V
			No	Yes	No	No	3.3 V

CY27410 Device Supply	Functionality	Jumper	Jumper Setting				Voltage Selected
			Short Pins 5 and 2	Short Pins 5 and 4	Short Pins 5 and 8	Short Pins 5 and 6	
			No	No	Yes	No	1.8 V
			No	No	No	Yes	EXT (H5.1)
VDDIO_S1	Supply for single ended outputs in Bank1	J39	Yes	No	No	No	2.5 V
			No	Yes	No	No	3.3 V
			No	No	Yes	No	1.8 V
			No	No	No	Yes	EXT (H5.2)
VDDIO_D2	Supply for differential outputs in Bank2	J42	Yes	No	No	No	2.5 V
			No	Yes	No	No	3.3 V
			No	No	Yes	No	1.8 V
			No	No	No	Yes	EXT (H6.1)
VDDIO_S2	Supply for single ended outputs in Bank 2	J41	Yes	No	No	No	2.5 V
			No	Yes	No	No	3.3 V
			No	No	Yes	No	1.8 V
			No	No	No	Yes	EXT (H6.2)

Figure 4-10. External Supply Connected to VDDIOs, Core, and Termination Voltages



4.2.3 Caution for 1.8-V Operation

If the profile is generated to configure the device for 1.8 V operation, before loading the profile into the clock device, ensure that the core and I/O jumpers are set properly to select 1.8 V as the supply voltage. See Table 4-2 for correct 1.8 V jumper settings.

4.2.4 Grounding Scheme

The board contains three ground references: earth ground (GND), CY27410 device ground (VSS), and SMA ground (VSHIELD). These three ground references have been isolated in this kit to provide the advanced feature of enabling DC measurement of the different output standards supported by the device using SMA connectors.

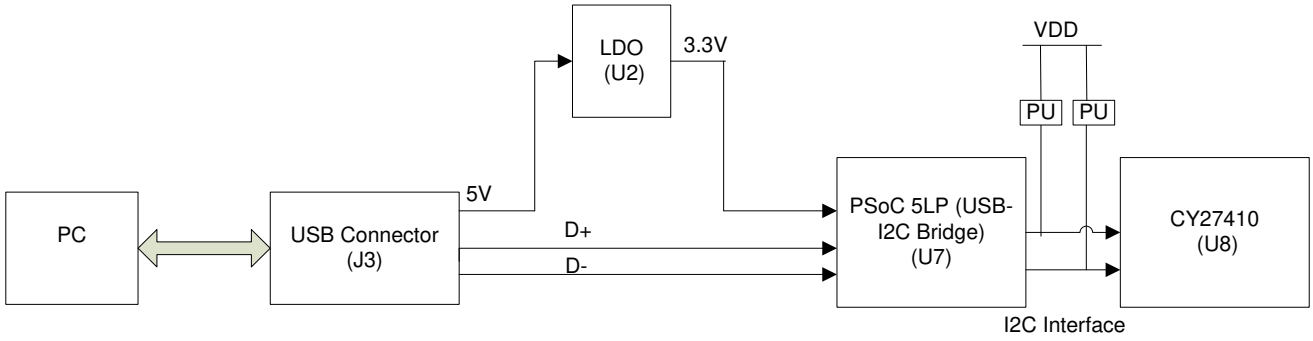
The device ground (VSS) is measured with respect to the earth ground (GND). You can use jumper J43 to short or isolate these two grounds on the board. When the board is powered using USB, GND is provided from the USB ground connection. Ensure that the jumper is placed to short pins 1 and 2 so that GND and VSS are shorted on the board.

The ground references of all SMA connectors are shorted on the board, designated as VSHIELD. When the board is connected to any instrument (such as an oscilloscope or a Modulation Domain Analyzer) through an SMA cable, the ground reference of the instrument is shorted to VSHIELD. This is enabled by default, wherein VSHIELD and GND are shorted (pins 1 and 2 of jumpers J44 and J45 are shorted). However, for advanced measurement of clock parameters, the jumper settings of J43, J44, and J45 should be set as listed in Table A-1, Table A-2, and Table A-3.

4.2.5 Programming Section

The board should be connected to a PC through a USB connector to configure and program the device. See CY3679 Kit USB Connection to learn how to connect the kit to a PC. Figure 4-11 illustrates the programming section of the kit.

Figure 4-11. Programming the CY27410 Device



The USB interface can generate a 5 V power supply. The on-board LDO generates a 3.3 V supply to power the on-board PSoC 5LP device. The PSoC 5LP converts the JEDEC profiles into an I^2C-compatible format, which is then loaded into the CY27410 clock device. Up to eight profiles can be programmed and saved in the CY27410 device memory at one time. The active profile selection can be made when the kit is in operation using the switch SW2.

During programming, you must keep the core power supply of CY27410 device same as that in Clock Wizard 2.0 software configuration. See Table 4-3 for details. Other I/O supplies can be left floating or powered to the voltages same as in software configuration.

Table 4-3. Hardware Setting for Programming

Board Component	Hardware Setting
J3 (USB Connector)	Connect J3 to the PC that has the required software installed
J13	Short Pin 2 and 3 to use USB power
J43	Short GND and VSS
J40	Short Pin 5 with pin 8 to power the device core with on-board 1.8V power supply option, Short Pin 5 with pin 2 to power the device core with on-board 2.5V power supply option, Short Pin 5 with pin 4 to power the device core with on-board 3.3V power supply option,

The sample projects are Clock Wizard 2.0 project files (.cpj) that contain the configuration data. See Sample Projects.

Table 4-4. Sample Projects

Projects	Project Name	Configuration	Hardware Settings
1	CLK GEN.cpj	All output types with different frequencies	Default. See Sample Project #1 for more details.
2	PCIE.cpj	HCSL – 2 outputs; OUT13 and OUT23	See Sample Project #2 for more details.
3	NZDB.cpj	All output types with different frequencies. External input required for reference clock.	See Sample Project #3 for more details.
4	ZDB.cpj	All differential outputs of Bank2 show a 50-MHz output	See Sample Project #4 for more details.