CY3687

MoBL-USB® FX2LP18 Development Kit User Guide

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Contents

1. Introduction

1.1 Introduction

The CY3687 MoBL-USB™ FX2LP18 Development Kit (DVK) is the best starting point for developing a MoBL-USB based product. The DVK includes a development board, code example, a generic device driver, documentation, and assorted tools. This guide provides a general overview and installation help for the DVK. The software installation of the kit includes additional help files and documentation more specific to the various components in the kit.

1.2 Kit Contents

The following list shows the components supplied in the CY3687 MoBL-USB FX2LP18 Development Kit. They represent most of the development tools required to build a USB system.

1.2.1 Hardware

- MoBL-USB FX2LP18 development board
- Prototyping board ('breadboard'). This board is compatible with the EZ-USB (FX1/FX2LP) developments kits as well.
- USB cable
- RS-232 cable
- Software Installation CD-ROM
- Quick start Guide Booklet
- 3 sample MOBL-USB FX2LP18 IC(CY7C68053-56BAXI)

1.2.2 Software on CD-ROM

- Firmware library and firmware frameworks
- Firmware sample code
- Microsoft certified Signed Cypress generic USB driver (3.4.5.000) for Windows XP, Vista and 7 OS platforms.
- Cypress USB C++ library (CyApi.lib)
- SuiteUSB 3.4.7 Development tools for Visual Studio
- Cypress GPIF Designer
- Cypress firmware and Keil monitor download driver sample
- MOBL-USB FX2LP18 documentation
- Keil uVision2 trail version IDE with 4k code limit

1.2.3 Required Tools Not Included

- Full retail Keil Development System (Keil uVision2)
- Microsoft Visual C++ (all PC sample codes are developed on this platform)
- USB capable PC running Windows XP or 2000

1.2.4 Other Suggested Tools

- CATC USB Protocol Analyzer.

1.3 Document Revision History

Table 1-1. Revision History

Revision	PDF Creation Date	Origin of Change	Description of Change
**	02/07/2011	ROSM	Initial version of user guide
*A	06/21/2012	NMMA	The document has to be updated with the OOB review comments.
*B	06/28/2012	NMMA	Minor text edits as per IC samples listed in UG

1.4 Documentation Conventions

Table 1-2. Document Conventions for Guides

Convention	Usage
`Courier New`	Displays file locations, user entered text, and source code: `C:\ ...cd\icc\`
Italics	Displays file names and reference documentation: Read about the *sourcefile.hex* file in the *PSoC Designer User Guide*.
[**Bracketed, Bold**]	Displays keyboard commands in procedures: [**Enter**] or [**Ctrl**] [**C**]
File > Open	Represents menu paths: File > Open > New Project
Bold	Displays commands, menu paths, and icon names in procedures: Click the **File** icon and then click **Open**.
Times New Roman	Displays an equation: $2 + 2 = 4$
Text in gray boxes	Describes Cautions or unique functionality of the product.

2. Getting Started

This chapter describes the installation of the CY3687 MoBL-USB FX2LP18 development Kit CD/DVD Software.

2.1 Kit Installation

To install the kit software, follow these steps:

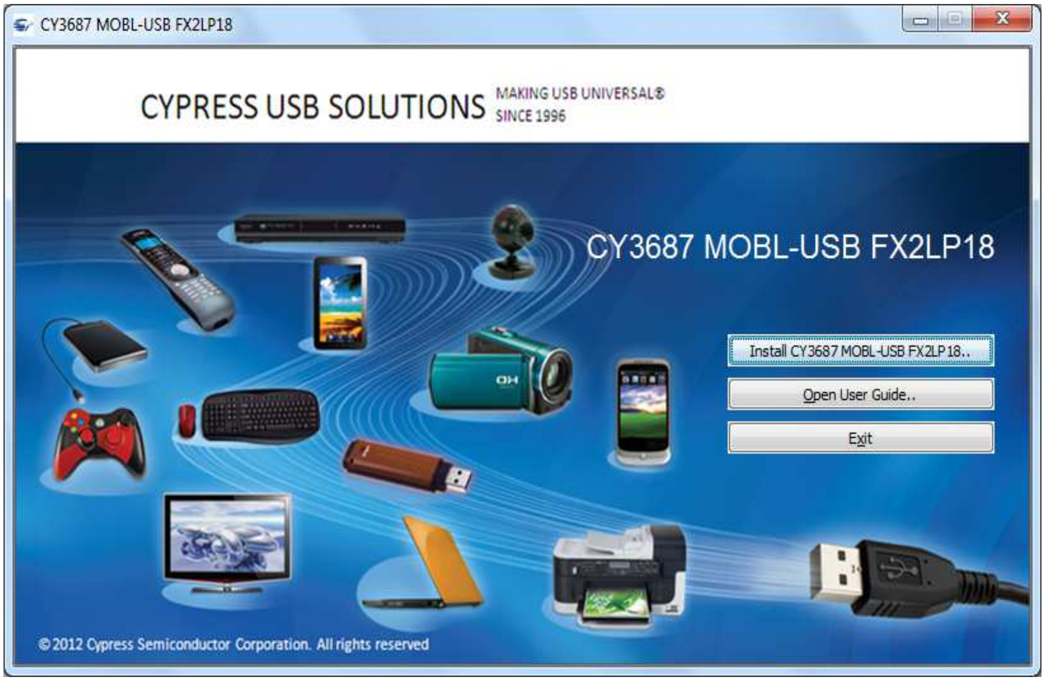
1. Insert the kit CD/DVD into the CD/DVD drive of your PC. The CD/DVD is designed to auto-run and the kit installer startup screen appears.

   You can also download the latest kit installer ISO file for CY3687

   Create an installer CD/DVD or extract the ISO using WinRar and install the executables.

2. Click **Install CY3687 MoBL-USB™ FX2LP18 DVK** to start the installation, as shown in Figure 2-1.

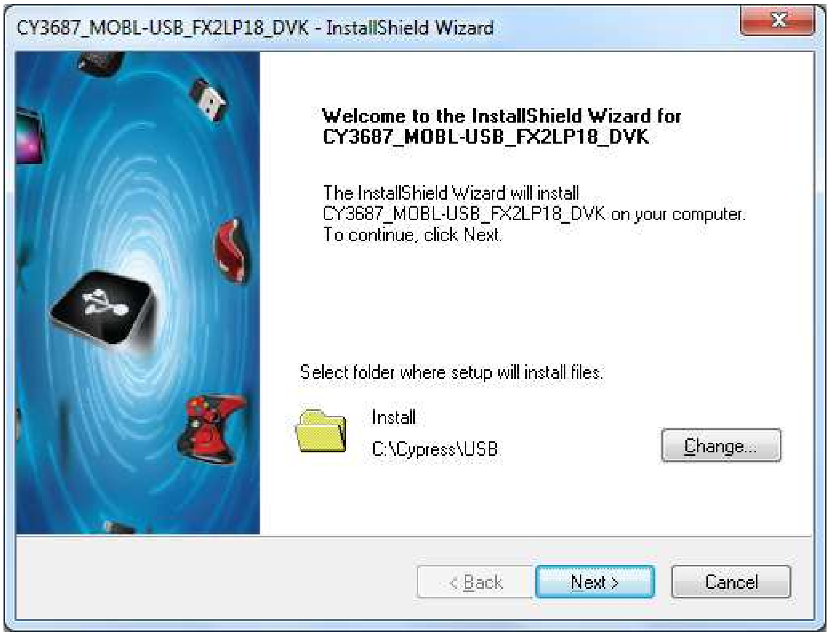
   Figure 2-1. Kit Installer Startup Screen



Note: If auto-run does not execute, double-click on the cyautorun.exe file in the root directory of the CD.

3. The InstallShield Wizard screen appears. The default location for setup is shown on the InstallShield Wizard screen. You can change the location for setup using **Change**, as shown in Figure 2-2. Click **Next** to launch the kit installer.

Figure 2-2. InstallShield Wizard



CY3687_MOBL-USB_FX2LP18_DVK - InstallShield Wizard

Welcome to the InstallShield Wizard for CY3687_MOBL-USB_FX2LP18_DVK

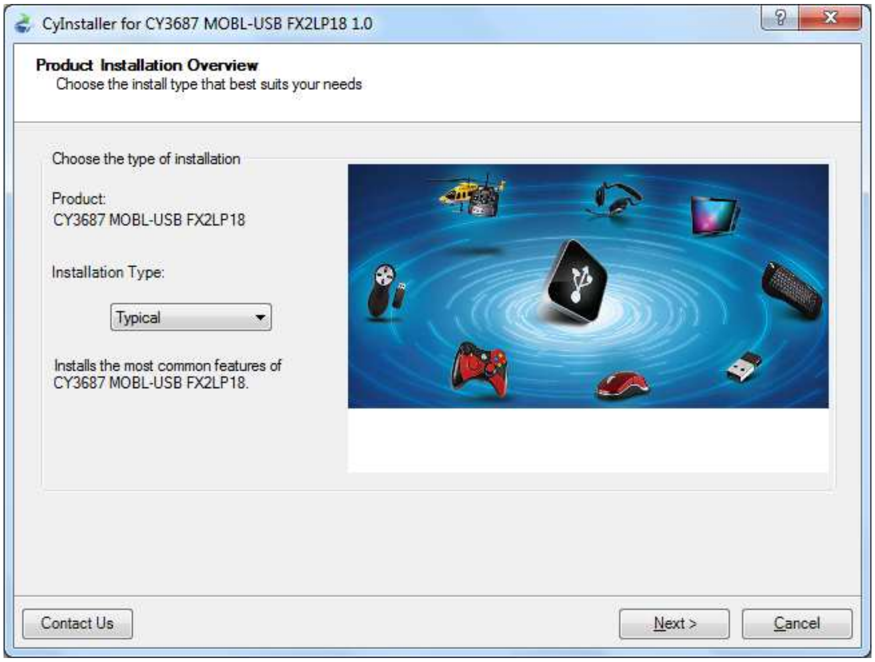
The InstallShield Wizard will install CY3687_MOBL-USB_FX2LP18_DVK on your computer. To continue, click Next.

Select folder where setup will install files.

Install
C:\Cypress\USB

4. On the Product Installation Overview screen, select the installation type that best suits your requirement. The drop-down menu has three options - **Typical**, **Complete**, and **Custom**, as shown in Figure 2-3. In the current installer all 3 installation types would result in same set of softwares getting installed.Select the default **Typical** installation and click **Next**.

Figure 2-3. Installation Type Options



CyInstaller for CY3687 MOBL-USB FX2LP18 1.0

Product Installation Overview
Choose the install type that best suits your needs

Choose the type of installation

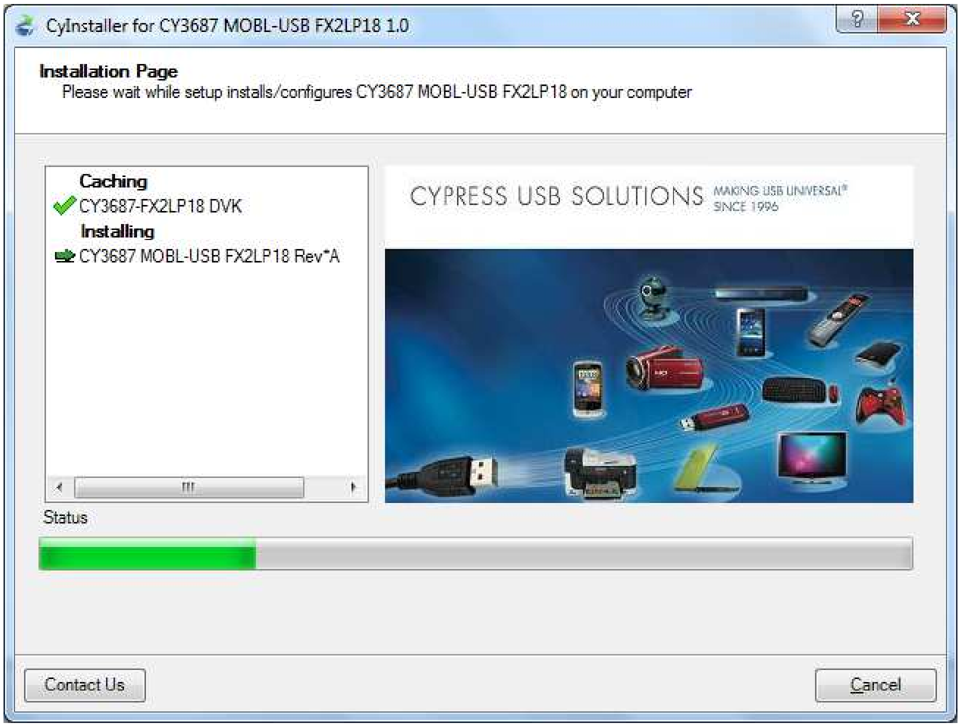
Product:
CY3687 MOBL-USB FX2LP18

Installation Type:
Typical

Installs the most common features of CY3687 MOBL-USB FX2LP18.

5. When the installation begins, all packages are listed on the Installation page. A green check mark appears adjacent to every package that is downloaded and installed, as shown in Figure 2-4. Wait until all the packages are downloaded and installed successfully.

Figure 2-4. Installation Page



CyInstaller for CY3687 MOBL-USB FX2LP18 1.0

Installation Page

Please wait while setup installs/configures CY3687 MOBL-USB FX2LP18 on your computer

Caching

✓ CY3687-FX2LP18 DVK

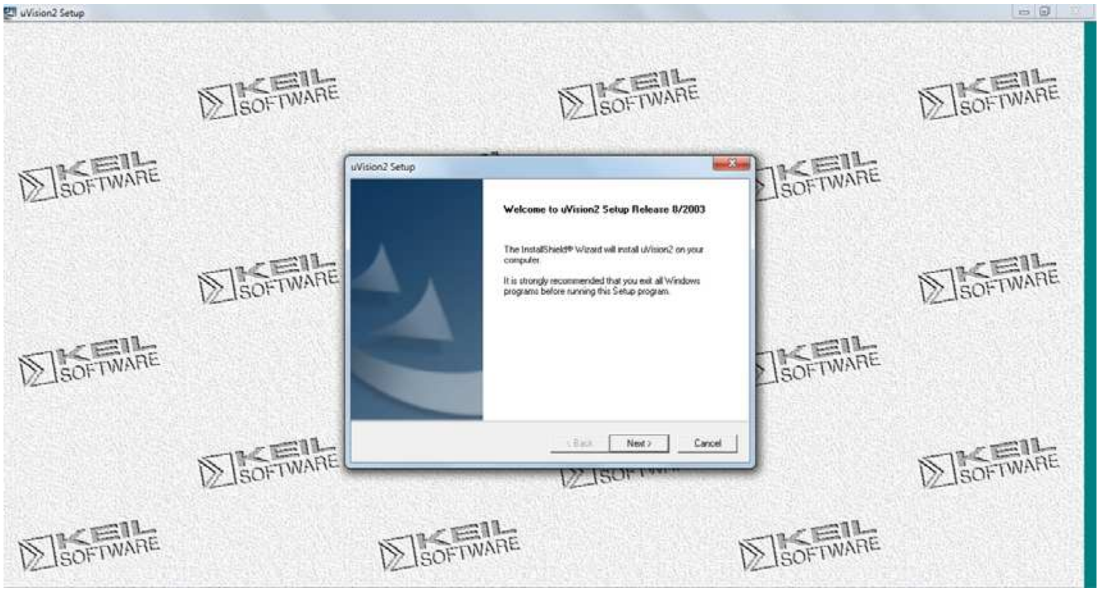
Installing

CY3687 MOBL-USB FX2LP18 Rev*A

Status

6. Keil uVision2 trial version IDE triggers at this stage. If the PC already has the software installed then the installer will not trigger the installation. If the PC does not contain the software then keil welcome screen appears as shown in Figure 2-5.Click **Next**.

Figure 2-5. Keil Welcome screen



uVision2 Setup

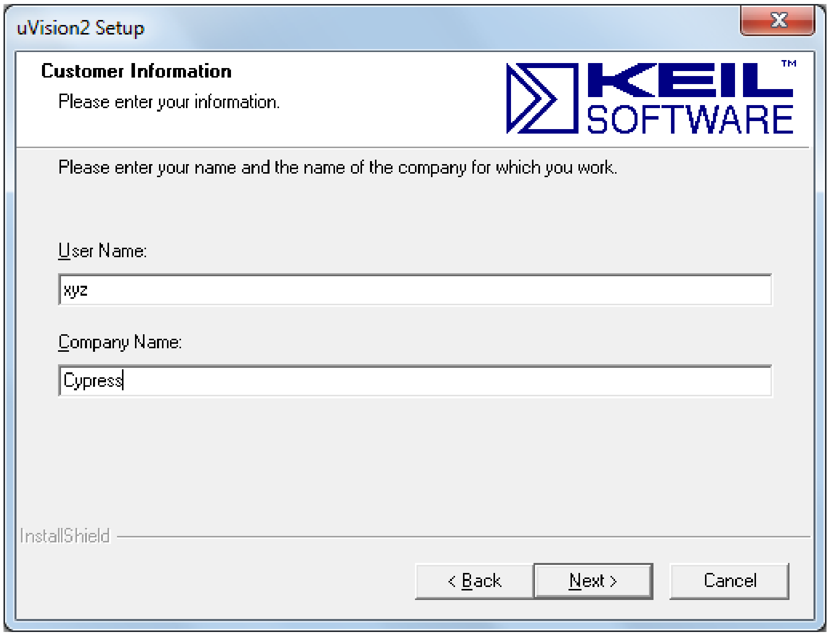
Welcome to uVision2 Setup Release 8/2003

The InstallShield® Wizard will install uVision2 on your computer.

It is strongly recommended that you exit all Windows programs before running this Setup program.

7. Enter the User name and company Name credentials as shown in Figure 2-6 to proceed further with the installation.

Figure 2-6. Keil User Information Input Window



uVision2 Setup

Customer Information

Please enter your information.

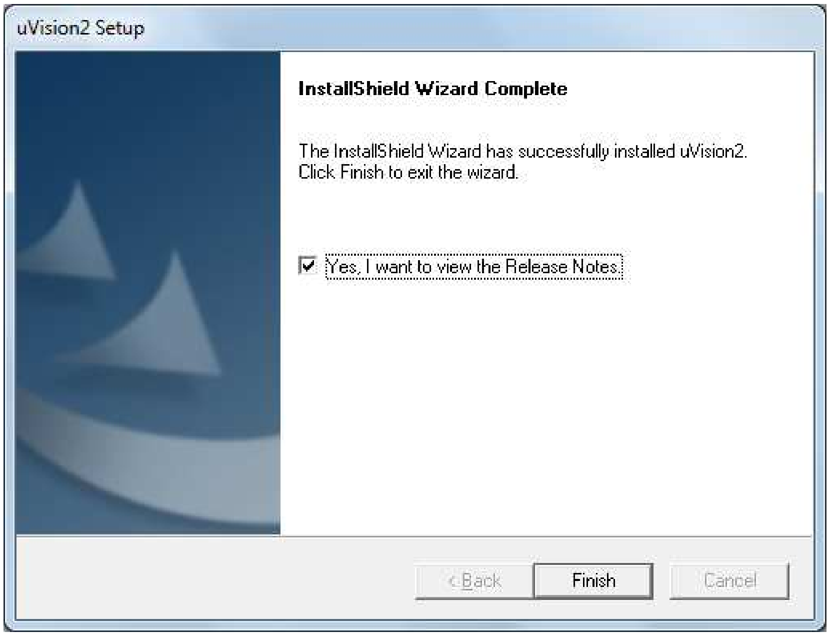
Please enter your name and the name of the company for which you work.

User Name: xyz

Company Name: Cypress

8. The keil software proceeds with the installation and copies necessary packages at default directory **C:\Keil**. After completion click on **Finish** as shown in Figure 2-7.

Figure 2-7. Keil User Information Input Window



uVision2 Setup

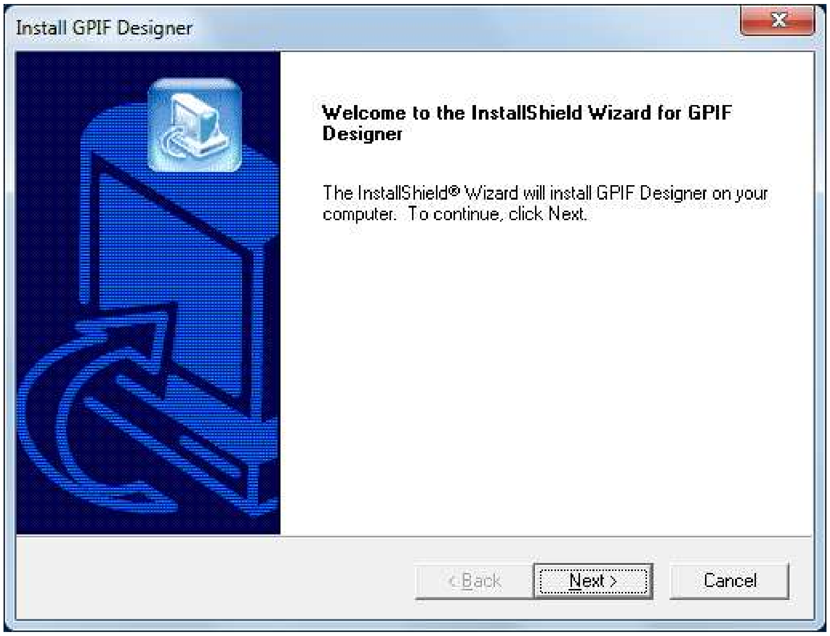
InstallShield Wizard Complete

The InstallShield Wizard has successfully installed uVision2. Click Finish to exit the wizard.

☑ Yes, I want to view the Release Notes.

9. GPIF designer software is triggered after keil installation.This software is used to create State machine waveforms to communicate between MoBL-USB FX2LP device and devices such as FPGA, Image sensors, FIFO, and so on. If the PC already has the software installed then the installer will not trigger the installation. If the PC does not contain the software then GPIF designer welcome screen appears as shown in Figure 2-8. Click **Next**.

Figure 2-8. GPIF Designer Welcome Window



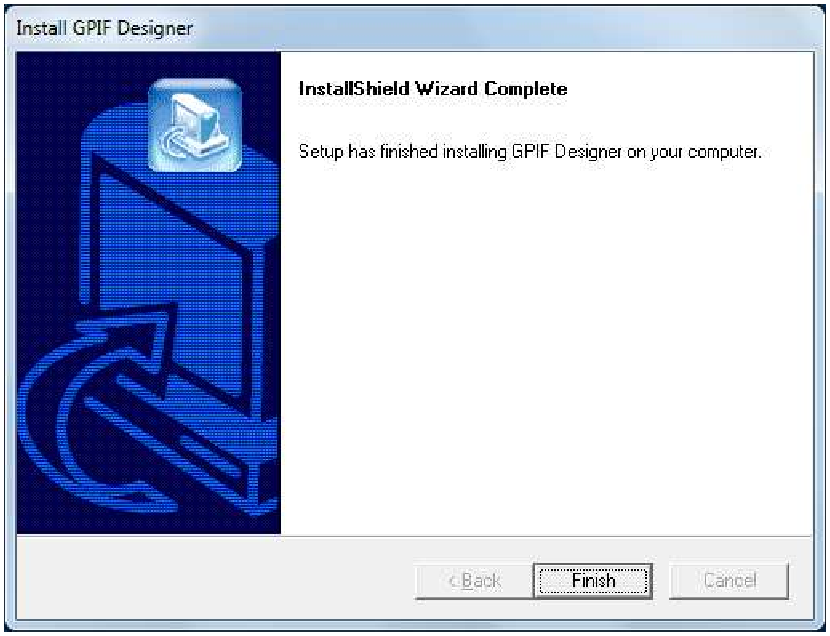
Install GPIF Designer

Welcome to the InstallShield Wizard for GPIF Designer

The InstallShield® Wizard will install GPIF Designer on your computer. To continue, click Next.

10. Click **Next** in the subsequent windows and Finish window appears as shown in Figure 2-9.

Figure 2-9. GPIF Designer Welcome Window



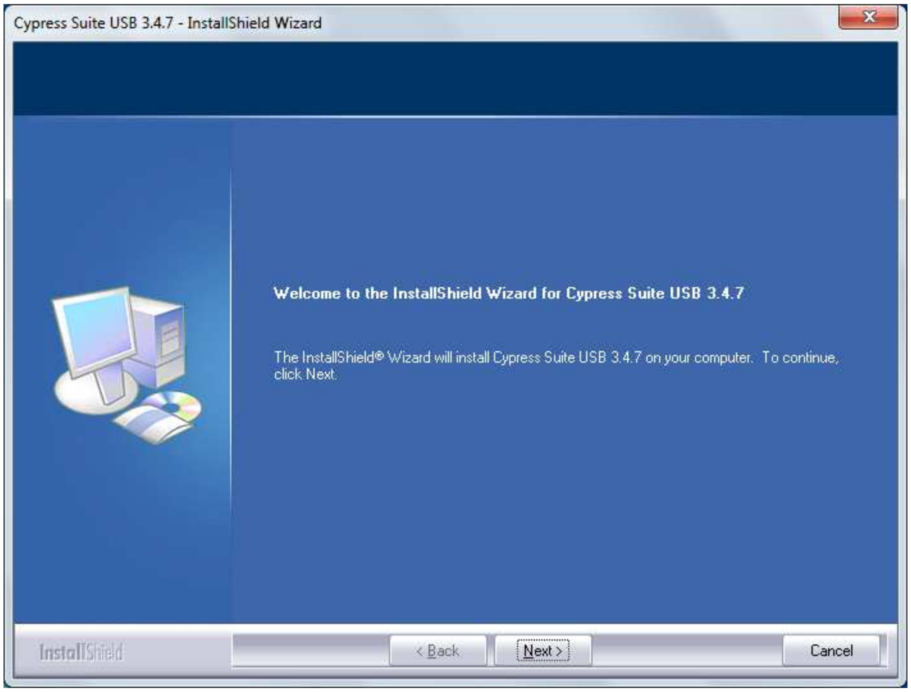
Install GPIF Designer

InstallShield Wizard Complete

Setup has finished installing GPIF Designer on your computer.

11. SuiteUSB 3.4.7 package install shield gets triggered after GPIF designer software installation. If the PC already has the software installed then the installer will not trigger the installation. If the PC does not contain the software then SuiteUSB welcome screen appears as shown in Figure 2-10. Click **Next** and accept Cypress Software license agreement as shown in Figure 2-11.

Figure 2-10. SuiteUSB Welcome Window

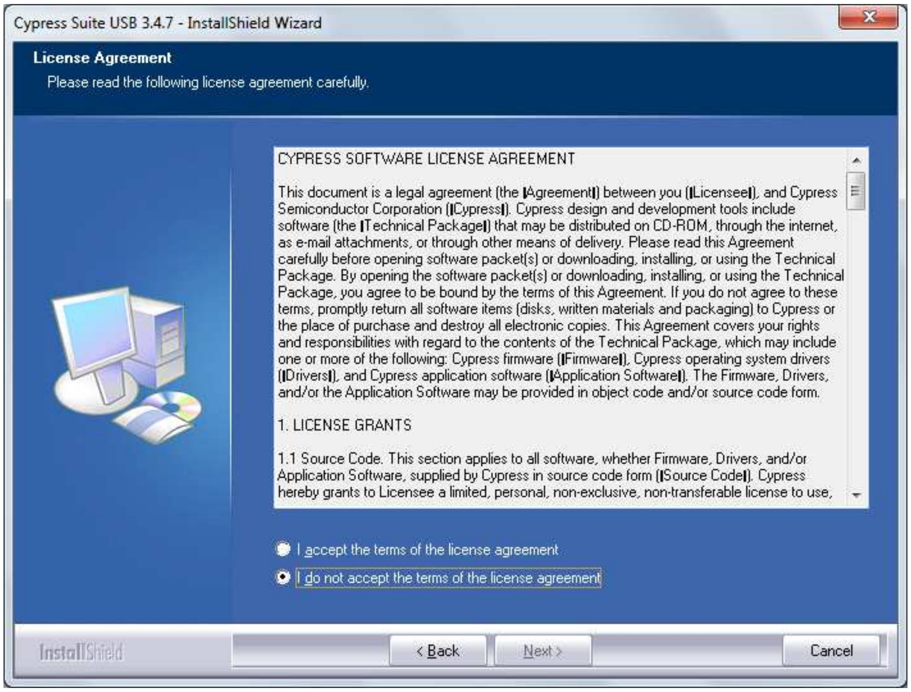


Cypress Suite USB 3.4.7 - InstallShield Wizard

Welcome to the InstallShield Wizard for Cypress Suite USB 3.4.7

The InstallShield® Wizard will install Cypress Suite USB 3.4.7 on your computer. To continue, click Next.

Figure 2-11. SuiteUSB License Agreement Window



Cypress Suite USB 3.4.7 - InstallShield Wizard

License Agreement

Please read the following license agreement carefully.

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1. LICENSE GRANTS

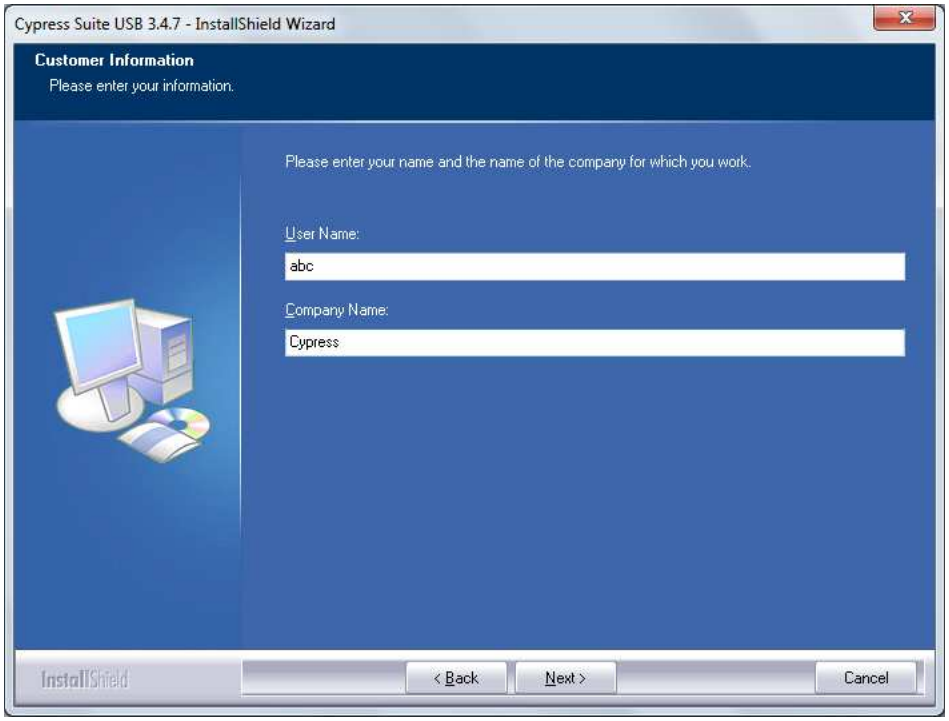
1.1 Source Code. This section applies to all software, whether Firmware, Drivers, and/or Application Software, supplied by Cypress in source code form (|Source Code|). Cypress hereby grants to Licensee a limited, personal, non-exclusive, non-transferable license to use,

○ I accept the terms of the license agreement

● I do not accept the terms of the license agreement

12. Enter User credentials in the SuiteUSB window as shown in Figure 2-12. Click **Next**. The default directory of the SuiteUSB is **C:\Cypress\Cypress Suite USB 3.4.7**. The default directory can be changed at this stage. Click **Next** after selecting the directory. Click **Install** button in the subsequent window. The SuiteUSB package installation progress is shown in the next window. Finally the SuiteUSB **Finish** window appears. Click **Finish** button to complete the installation process of SuiteUSB.

Figure 2-12. SuiteUSB User Login Window



Cypress Suite USB 3.4.7 - InstallShield Wizard

Customer Information

Please enter your information.

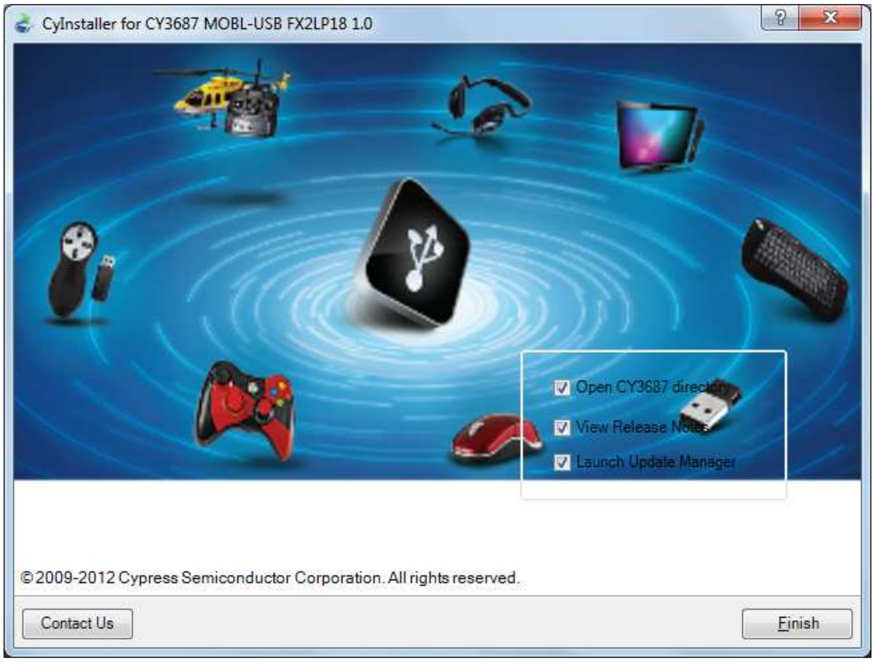
Please enter your name and the name of the company for which you work.

User Name: abc

Company Name: Cypress

13. The CY3687 MoBL-USB FX2LP18 development Kit. CY3687 **Finish** window appears after installing Kit content, Keil software, GPIF designer and SuiteUSB 3.4.7 package.

Figure 2-13. CY3687 Finish Window



CyInstaller for CY3687 MOBL-USB FX2LP18 1.0
☑ Open CY3687 directory
☑ View Release Notes
☑ Launch Update Manager
©2009-2012 Cypress Semiconductor Corporation. All rights reserved.
Contact Us
Finish

2.2 Install Hardware

Refer to section Binding Cypress USB Driver to MoBL-USB Development Board on page 43 for hardware installation for this kit.

3. Development Board

3.1 Introduction

The Cypress Semiconductor MoBL-USB Development Board provides expansion and interface signals on six 20-pin headers. A mating prototype board allows quick construction and testing of USB designs. The board may be powered from the USB connector or an external power supply. Note that some of the signals driven by the MoBL-USB FX2LP18 device on the Advanced Development board have been replaced by VCC-IO and 1.8 V supplies.

The MoBL-USB Development Board is supplied as part of the Cypress Semiconductor MoBL-USB Development Kit, which includes an evaluation version of Cypress-customized software development tools from Keil Software Inc. The Keil 8051 assembler, C Compiler, and debugger work in concert with the development board to provide a complete code development environment. The evaluation version of the Keil tools that ships with the DVK has several restrictions that make it inappropriate for real-world development. Most significantly, it limits the compiled object size to 4 KB. The full retail version allows code of any size.

3.2 Schematic Summary

This description should be read while referring to the MoBL-USB Development Board schematic and the MoBL-USB Development Board Assembly drawing. Both drawings are attached to the end of this document and are available in PDF format in the DVK hardware directory.

U3 is the MoBL-USB 56-pin device. Although there is a large (100-pin) FX2LP on the board (U11), this chip is only used for I^2C to serial translation, it is not available as a USB device.

Power to the MoBL-USB device comes from two or three different supplies. The AVCC pins draw 3.3 V through jumper JP4. The VCCCore supply requires 1.8 V, which it receives from JP2. The I/O pins (VCCIO) can run on voltages ranging from 1.8 V to 3.3 V. JP10 provides the ability to select the input voltage to VCCIO from the 1.8 V, 3.3 V or 2.5 V (adjustable) regulator.

U6, U9, and U10 provide power to the board. All of these devices can provide up to 500 mA, so there is plenty of spare power on all of the supplies to handle any devices on the prototype board. The output voltage of U9 can be varied by changing the ratio of R29 and R34. See the LT1763 data sheet for more information.

U7 and U8 are socketed EEPROMS, used for MoBL-USB FX2LP18 initialization and 8051 general purpose access. U5 is another EEPROM, used for factory initialization. This part is required because the MoBL-USB chip starts up disconnected from USB and it requires an EEPROM load to connect to USB. JP6 prevents this part from accidental programming.

U2 and U4 are Philips PCF8574 IO expanders, which attach to the MoBL-USB FX2LP18 I2C bus and provide eight GPIO pins. U2 reads the four push-button switches S2-S5, and U11 drives the seven-segment readout U1.

U11 is used only for converting the I^2C signals to RS-232 for running the Keil debugger. It is not used for USB access. U12 converts the 3.3 V 8051 serial port signals to bipolar RS-232 levels. U13 contains the I^2C to RS-232 conversion program. U13 is not intended to be user-programmable.

Six 20-pin headers, P1-P6, provide interface signals to the plug-in prototyping board supplied in this kit, as well as serving as connection points for HP(Agilent) logic analyzer pods. P8 contains a subset of signals from P1-P6 on a connector that is pinned out for connection to a 'straight- through' ATA cable. Two slide switches, SW1 and SW2, control the connection and selection of the three socketed EEPROMS at U5, U7, and U8.

3.3 Jumpers

Table 3-1. Jumper Settings

Jumper	Function	Default	Notes
JP1	Current measurement point for VCCIO	IN (1-2)	This jumper may be removed and replaced with ammeter probes in series to measure current for this supply.
JP2	Current measurement point for VCCORE	IN (1-2)	This jumper may be removed and replaced with ammeter probes in series to measure current for this supply.
JP3	Removed		This jumper has been removed from the schematic
JP4	Current measurement point for AVCC	IN (1-2)	This jumper may be removed and replaced with ammeter probes in series to measure current for this supply.
JP5	Board power source	IN (1-2)	If this jumper is in place, the board is bus-powered from the USB connector (J2). If this jumper is removed, the board must be powered via JP5.1 or another 5v jumper.
JP6	SAFE_WP	IN (1-2)	Removing this jumper allows the SAFE EEPROM to be reprogrammed. Reprogramming the SAFE EEPROM is not recommended. If the SAFE EEPROM contents are lost, the EEPROMs cannot be reprogrammed via USB.
JP7	EEPROM WP	PA7 (1-2)	This jumper selects the WP input for the 'normal' EEPROMs. Position 1-2 ties WP to PA7. In this position, PA7 must be driven low to reprogram the EEPROM. The Cypress programming tools will drive PA7 low during programming. If PA7 is used by your application, you can remove this jumper during normal use and move it to position (2-3) during EEPROM programming.
JP8	Current measurement point or alter-nate power input for 3.3 V supply	IN (1-2)	This jumper may be removed and replaced with ammeter probes in series to measure current for this supply. This point may be used to provide an external source for the 3.3 V supply.

Table 3-1. Jumper Settings

Jumper	Function	Default	Notes
JP9	Current measurement point or alter-nate power input for 2.5V supply	IN (1-2)	This jumper may be removed and replaced with ammeter probes in series to measure current for this supply. This point may be used to provide an external source for the 2.5 V supply.
JP10	Voltage selection for VCCIO	1.8V (5-6)	Selects the input voltage for VCCIO.
JP11	Current measurement point or alter-nate power input for 1.8V supply	IN (1-2)	This jumper may be removed and replaced with ammeter probes in series to measure current for this supply. This point may be used to provide an external source for the 1.8 V supply.
JP12	WP for debug FX2LP	IN (1-2)	When this jumper is in place, the debug firmware in the 100-pin FX2LP is protected from accidental writes. Removing this jumper allows the debug firmware to be overwritten.

3.4 EEPROM Select and Enable Switches SW1 and SW2

SW1 selects between two socketed EEPROMs, one strapped to address 000 (U8), and the other strapped to address 001(U7).

SW2 enables or disables the EEPROM selected by SW1. When the SW1 EEPROMs are disabled, the ‘Safe’ EEPROM is enabled.

The MoBL-USB chip has various start-up modes, which depend on the existence of an EEPROM connected to its SCL and SDA lines. Switches SW1 and SW2 select among three EEPROMs on the board. Each of these EEPROMs has a specific purpose:

- U5 -- SAFE -- Used to select the default VID/PID for the board. Do not overwrite this EEPROM.
- U7 -- Large -- Used for firmware download. User programmable.
- U8 -- Small -- Used for VID/PID programming only. Used for reNumeration or default configuration. The VID/PID allows the operating system to identify your device. You must have your own VID assigned by the USB I/F. The ‘Using Cypress’ VID is not permitted.

On reset, the MoBL-USB I2C controller loads the image from one of these three EEPROMs. As this process completes, the 8051 firmware can use the I^{2}C controller to access the EEPROMs or both devices on the I^{2}C bus. The MoBL-USB bootloader accommodates two EEPROM types, in ‘Small’ and ‘Large’ versions shown in Table 3-2.

Table 3-2. Typical MoBL-USB external EEPROMS

EEPROM Type	Size	A2A1A0	Typical P/N (2.5-3.3v)	Typical P/N (1.8v)
‘Small’	128x8	000	24LC01	24AA01
	256x8	000	24LC02	24AA02
‘Large’	16Kx8	001	24LC128	24AA128

The MoBL-USB loader determines the EEPROM size by first initiating an I^{2}C transfer to address Alignment not proper between these 2 lines.

If the above transfer does not return an ACK pulse, the MoBL-USB loader initiates a second I^{2}C transfer, this time to address 10100001 (1010=EEPROM, sub-address 001). If an ACK is returned by the I^{2}C device, the MoBL-USB loader writes two EEPROM address bytes to initialize the internal EEPROM address pointer to '0'.

If neither transfer returns an ACK pulse, the MoBL-USB Development Board does not connect to USB. MoBL-USB requires a 0xC2 format EEPROM to connect. Three MoBL-USB startup sequences, and the associated settings for SW1 and SW2, are as follows:

1. Safe Mode:SW2 = SAFE, SW1 = either position

   This setting selects the EEPROM located in socket U5. Since the MoBL-USB chip comes out of reset disconnected from USB, an EEPROM is required to connect to the USB. The 'Safe' EEPROM is used for this purpose. The 'Safe' EEPROM contains simple firmware that connects to the USB and responds to descriptor requests with the Cypress VID and the MoBL-USB PID. 'Safe' mode is used to allow the development board to enumerate when no action other than a USB connect is required. For example, the 'safe' setting could be used if one of the other EEPROMs on the board is accidentally programmed with malfunctioning firmware. Once it is running, SW2 can be switched to the LG-SM position to allow 8051 programming or other access to the other EEPROMs. The source firmware for this EEPROM is located in the `<Installed_directory>\<Version>\Firmware\Connect` directory. The actual EEPROM image is stored in the *LP18_safe.iic* file.

2. C2 Load Small EEPROM:SW2 = LG-SM, SW1 = SMALL

   This setting selects the EEPROM located in socket U8. The I^{2}C EEPROM address pins for this socket are strapped to '000'. This socket only supports single-byte address EEPROMs. This EEPROM is pre-programmed at manufacturing with simple firmware which connects to USB and responds to descriptor requests with the Cypress VID (0x04B4) and the MoBL-USB Development Kit PID (0x0086). This VID/PID is associated with a driver which automatically downloads the Keil debug monitor to the development board. The source firmware for this EEPROM is located in the `<Installed_directory>\<Version>\Firmware\Connect` directory. The actual EEPROM image is stored in the *LP18_dvk.iic* file.

3. C2 Load Large EEPROM:SW2 = LG-SM, SW1 = LARGE

   This setting selects the EEPROM located in socket U8. The I^{2}C EEPROM address pins for this socket are strapped to '001'. This socket only supports double-byte address EEPROMs. This EEPROM is pre-programmed at manufacturing with the bulkloop example firmware (VID=0x04B4, PID=0x1004). The source firmware for this EEPROM is located in the following directory:

   `<Installed_directory>\<Version>\Firmware\bulkloop`.

   The actual EEPROM image is stored in the *bulkloop.iic* file. Note that if an EEPROM is connected to the SCL and SDA lines, but does not contain an 0xC2 formatted EEPROM, the device does not connect to USB. Therefore, it cannot be programmed. Always connect to the SAFE EEPROM if you are not using one of the programmed EEPROMs. See the MoBL-USB datasheet or MoBL-USB Technical Reference Manual for additional information on supported EEPROM formats.

3.5 Interface Connectors

Table 3-3. Logic Analyzer Pinout

Agilent 01650-63203 Pod Pins			
CLK1	3	4	D15
D14	5	6	D13
D12	7	8	D11
D10	9	10	D9
D8	11	12	D7
D6	13	14	D5
D4	15	16	D3
D2	17	18	D1
D0	19	20	GND

Six 20-pin headers P1-P6 on the MoBL-USB FX2LP18 Development Board have pins assigned to be compatible with HP (Agilent) logic analyzers, as shown in Table 3-3. The slight bulge in the middle rows of the table (pins 9 and 11) indicates the connector key. The six headers P1-P6 serve three purposes:

- They mate with the prototyping board supplied in the MoBL-USB Development Kit or the one supplied in the CY3687 MoBL-USB FX2LP18 Development Kit.
- They allow direct connection of HP (Agilent) logic analyzer pods (Agilent P/N 01650- 63203).
- They allow general purpose probing by other logic analyzers or oscilloscopes.

Table 3-3 shows the logic analyzer pod pin designations. The MoBL-USB signals on P1-P6 are arranged to fulfill the following requirements:

- High-speed MoBL-USB strobe signals (CLKOUT and IFCLK) are connected to pin 3 of each of the five connectors P1-P6, so that they may be used as the logic analyzer clock CLK1.
- CLK2 is not used. Instead, each connector brings 3.3 V power from the MoBL-USB Development Board up to the prototype board using pin 2.
- The signals are logically grouped. For example, the MoBL-USB FIFO data (which shares PORTB and PORTD pins) is on P1.

Because the 20-pin headers on the prototyping board are stackable, it is possible to build custom circuitry on the proto board, plug the board into the MoBL-USB development board, and still plug logic analyzer pods into the six connectors P1-P6.

Table 3-4 through Table 3-9 show the MoBL-USB pin designations for P1 through P6. For dual-mode pins, the power-on default signal names are shown in bold type, and the alternate pin names are shown in the outside columns.

Table 3-4. P1 Pin Designations

Alternate	Default	P1		Default	Alternate
	NC	**1**	**2**	3.3 V	
	VCCIO	**3**	**4**	PD7	FD[15]
FD[14]	PD6	**5**	**6**	PD5	FD[13]
FD[12]	PD4	**7**	**8**	PD3	FD[11]
FD[10]	PD2	**9**	**10**	PD1	FD[9]
FD[8]	PD0	**11**	**12**	PB7	FD[7]

Table 3-4. P1 Pin Designations *(continued)*

Alternate	Default	P1		Default	Alternate
FD[6]	PB6	**13**	**14**	PB5	FD[5]
FD[4]	PB4	**15**	**16**	PB3	FD[3]
FD[2]	PB2	**17**	**18**	PB1	FD[1]
FD[0]	PB0	**19**	**20**	GND	

Table 3-5. P2 Pin Designations

Alternate	Default	P2		Default	Alternate
	NC	**1**	**2**	3.3 V	
	NC	**3**	**4**	RDY1	SLWR
SLRD	RDY0	**5**	**6**	N.C.	
	NC	**7**	**8**	N.C.	
FLAGC	CTL2	**9**	**10**	CTL1	FLAGB
FLAGA	CTL0	**11**	**12**	PA7	FLAGD
PKTEND	PA6	**13**	**14**	PA5	FIFOADR1
FIFOADR0	PA4	**15**	**16**	PA3	WU2
SLOE	PA2	**17**	**18**	PA1	INT1#
INT0#	PA0	**19**	**20**	GND	

Table 3-6. P3 Pin Designations

Alternate	Default	P3		Default	Alternate
	NC	**1**	**2**	3.3 V	
	VCCIO	**3**	**4**	N.C.	
	NC	**5**	**6**	N.C.	
	NC	**7**	**8**	N.C.	
	RESET#	**9**	**10**	N.C.	
	NC	**11**	**12**	N.C.	
	NC	**13**	**14**	N.C.	
	NC	**15**	**16**	N.C.	
	NC	**17**	**18**	N.C.	
	NC	**19**	**20**	GND	

Table 3-7. P4 Pin Designations

Alternate	Default	P4		Default	Alternate
	N.C.	**1**	**2**	3.3 V	
	CLKOUT	**3**	**4**	GND	
	N.C.	**5**	**6**	NC	
	5 V	**7**	**8**	5 V	
	NC	**9**	**10**	NC	
	NC	**11**	**12**	NC	

Table 3-7. P4 Pin Designations *(continued)*

Alternate	Default	P4		Default	Alternate
	NC	**13**	**14**	NC	
	NC	**15**	**16**	NC	
	NC	**17**	**18**	NC	
	NC	**19**	**20**	GND	

Table 3-8. P5 Pin Designations

Alternate	Default	P5		Default	Alternate
	NC	**1**	**2**	3.3 V	
	IFCLK	**3**	**4**	NC	
	NC	**5**	**6**	NC	
	NC	**7**	**8**	NC	
	NC	**9**	**10**	NC	
	NC	**11**	**12**	NC	
	NC	**13**	**14**	NC	
	NC	**15**	**16**	NC	
	1.8 V	**17**	**18**	1.8 V	
	1.8 V	**19**	**20**	GND	

Table 3-9. P6 Pin Designations

Alternate	Default	P6		Default	Alternate
	NC	**1**	**2**	3.3 V	
	VCCIO	**3**	**4**	NC	
	NC	**5**	**6**	NC	
	NC	**7**	**8**	NC	
	WAKEUP#	**9**	**10**	SDA	
	SCL	**11**	**12**	NC	
	NC	**13**	**14**	NC	
	NC	**15**	**16**	NC	
	NC	**17**	**18**	NC	
	NC	**19**	**20**	GND	

3.6 ATA Connector P7

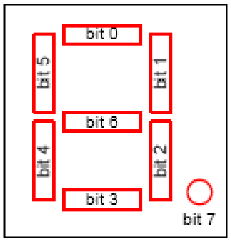
Table 3-10 shows the pinout for P7, a 40-pin connector that interfaces with a standard ATA cable. **Note** This is for ATA use only. SP1, 2, 3, and 4 should be bridged with solder to connect the appropriate pull-up or pull-down resistors required for ATA. An 80-pin cable is required for UDMA transfer modes and recommended for all transfer modes.

Table 3-10. ATA Connector Pinout

P7 (ATA)					
RESET#	PA7	1	2	GND	GND
DD7	PB7	3	4	PD0	DD8
DD6	PB6	5	6	PD1	DD9
DD5	PB5	7	8	PD2	DD10
DD4	PB4	9	10	PD3	DD11
DD3	PB3	11	12	PD4	DD12
DD2	PB2	13	14	PD5	DD13
DD1	PB1	15	16	PD6	DD14
DD0	PB0	17	18	PD7	DD15
GND	GND	19	20	N.C.	KEYPIN
DMARQ	RDY1	21	22	GND	GND
DIOW#	CTL0	23	24	GND	GND
DIOR#	CTL1	25	26	GND	GND
IORDY	RDY0	27	28	GND	CSEL
DMACK#	CTL2	29	30	GND	GND
INTRQ	PA0	31	32	N.C.	RESERVED
DA1	PA2	33	34	N.C.	PDIAG#
DA0	PA1	35	36	PA3	DA2
CS0#	PA4	37	38	PA5	CS1#
DASP#	10K Pull-up	39	40	GND	GND

3.7 I^{2}C Expanders

U2 and U4 are Philips PCF8574 I/O expanders. They connect to the I^{2}C bus SCL and SDA pins, and provide eight general-purpose input-output pins. U4 provides eight output bits, connected to the seven-segment readout U1. U2 provides eight input bits, four of which connect to push buttons S1-S4, and four of which are available for your use. U4 connects to the 7-segment readout (U1) using the following bit assignments.



U4 has the group address 0100 and is strapped to unit address 001. Therefore to write a value to the 7-segment readout, 8051 firmware sends a control byte of 01000010 (the LSB indicates a write operation), followed by the data byte.

U2 uses its I/O pins as inputs connected to S1-S4 according to the following table:

Bit	Switch
0	S1
1	S2
2	S3
3	S4

U2 has the group address 0100, and is strapped to unit address 000. Therefore to read the switch values, 8051 firmware sends a control byte of 01000001 (the LSB indicates a read operation), and then reads the data byte.

3.8 LED Indicators

LEDs D1, D2, and D4 indicate available power on the three power rails (3.3 V, 2.5 V, and 1.8 V).

LED D3 indicates drive activity on the ATA connector. LED D5 indicates that the debugger is active.