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Ultra37000 CPLD Family

5V, 3.3V, ISR™ High-Performance CPLDs

Features

- **In-System Reprogrammable™ (ISR™) CMOS CPLDs**
  - **— JTAG interface for reconfigurability**
  - **— Design changes do not cause pinout changes**
  - **— Design changes do not cause timing changes**
- **High density**
  - **— 32 to 512 macrocells**
  - **— 32 to 264 I/O pins**
  - **— Five dedicated inputs including four clock pins**
- **Simple timing model**
  - **— No fanout delays**
  - **— No expander delays**
  - **— No dedicated vs. I/O pin delays**
  - **— No additional delay through PIM**
  - **— No penalty for using full 16 product terms**
  - **— No delay for steering or sharing product terms**
- **3.3V and 5V versions**
- **PCI-compatible**[1]
- **Programmable bus-hold capabilities on all I/Os**
- **Intelligent product term allocator provides:**
  - **— 0 to 16 product terms to any macrocell**
  - **— Product term steering on an individual basis**
  - **— Product term sharing among local macrocells**
- **Flexible clocking**
  - **— Four synchronous clocks per device**
  - **— Product term clocking**
  - **— Clock polarity control per logic block**
- **Consistent package/pinout offering across all densities**
  - **— Simplifies design migration**
  - **— Same pinout for 3.3V and 5.0V devices**
- **Packages**
  - **— 44 to 400 leads in PLCC, CLCC, PQFP, TQFP, CQFP, BGA, and Fine-Pitch BGA packages**
  - **— Lead (Pb)-free packages available**

General Description

The Ultra37000™ family of CMOS CPLDs provides a range of high-density programmable logic solutions with unparalleled system performance. The Ultra37000 family is designed to bring the flexibility, ease of use, and performance of the 22V10 to high-density CPLDs. The architecture is based on a number of logic blocks that are connected by a Programmable Interconnect Matrix (PIM). Each logic block features its own product term array, product term allocator, and 16 macrocells. The PIM distributes signals from the logic block outputs and all input pins to the logic block inputs.

All of the Ultra37000 devices are electrically erasable and In-System Reprogrammable (ISR), which simplifies both design and manufacturing flows, thereby reducing costs. The ISR feature provides the ability to reconfigure the devices without having design changes cause pinout or timing changes. The Cypress ISR function is implemented through a JTAG-compliant serial interface. Data is shifted in and out through the TDI and TDO pins, respectively. Because of the superior routability and simple timing model of the Ultra37000 devices, ISR allows users to change existing logic designs while simultaneously fixing pinout assignments and maintaining system performance.

The entire family features JTAG for ISR and boundary scan, and is compatible with the PCI Local Bus specification, meeting the electrical and timing requirements. The Ultra37000 family features user programmable bus-hold capabilities on all I/Os.

Ultra37000 5.0V Devices

The Ultra37000 devices operate with a 5V supply and can support 5V or 3.3V I/O levels. V_{CCO} connections provide the capability of interfacing to either a 5V or 3.3V bus. By connecting the V_{CCO} pins to 5V the user insures 5V TTL levels on the outputs. If V_{CCO} is connected to 3.3V the output levels meet 3.3V JEDEC standard CMOS levels and are 5V tolerant. These devices require 5V ISR programming.

Ultra37000V 3.3V Devices

Devices operating with a 3.3V supply require 3.3V on all V_{CCO} pins, reducing the device's power consumption. These devices support 3.3V JEDEC standard CMOS output levels, and are 5V-tolerant. These devices allow 3.3V ISR programming.

Note:
1. Due to the 5V-tolerant nature of 3.3V device I/Os, the I/Os are not clamped to V_{CC}, PCI V_{IH} = 2V.

Selection Guide

5.0V Selection Guide

General Information

Device	Macrocells	Dedicated Inputs	I/O Pins	Speed (t_{PD})	Speed (f_{MAX})
CY37032	32	5	32	6	200
CY37064	64	5	32/64	6	200
CY37128	128	5	64/128	6.5	167
CY37192	192	5	120	7.5	154
CY37256	256	5	128/160/192	7.5	154
CY37384	384	5	160/192	10	118
CY37512	512	5	160/192/264	10	118

Speed Bins

Device	200	167	154	143	125	100	83	66
CY37032	X		X		X			
CY37064	X		X		X			
CY37128		X			X	X		
CY37192			X		X		X	
CY37256			X		X		X	
CY37384					X		X	
CY37512					X	X	X	

Device-Package Offering and I/O Count

Device	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	160-Lead CQFP	208-Lead PQFP	208-Lead CQFP	292-Lead PBGA	388-Lead PBGA
CY37032	37	37										
CY37064	37	37	37	69		69						
CY37128				69	69	69	133					
CY37192							125					
CY37256							133	133	165		197	
CY37384									165		197	
CY37512									165	165	197	269

3.3V Selection Guide

General Information

Device	Macrocells	Dedicated Inputs	I/O Pins	Speed (t_{PD})	Speed (f_{MAX})
CY37032V	32	5	32	8.5	143
CY37064V	64	5	32/64	8.5	143
CY37128V	128	5	64/80/128	10	125
CY37192V	192	5	120	12	100
CY37256V	256	5	128/160/192	12	100
CY37384V	384	5	160/192	15	83
CY37512V	512	5	160/192/264	15	83

Speed Bins

Device	200	167	154	143	125	100	83	66
CY37032V				X		X		
CY37064V				X		X		
CY37128V					X		X	
CY37192V						X		X
CY37256V						X		X
CY37384V							X	X
CY37512V							X	X

Device-Package Offering and I/O Count

Device	44-Lead TQFP	44-Lead CLCC	48-Lead FBGA	84-Lead CLCC	100-Lead TQFP	100-Lead FBGA	160-Lead TQFP	160-Lead CQFP	208-Lead PQFP	208-Lead CQFP	292-Lead PBGA	256-Lead FBGA	388-Lead PBGA	400-Lead FBGA
CY37032V	37		37											
CY37064V	37	37	37		69	69								
CY37128V				69	69	85	133							
CY37192V							125							
CY37256V							133	133	165		197	197		
CY37384V									165		197			
CY37512V									165	165	197		269	269

Architecture Overview of Ultra37000 Family

Programmable Interconnect Matrix

The PIM consists of a completely global routing matrix for signals from I/O pins and feedbacks from the logic blocks. The PIM provides extremely robust interconnection to avoid fitting and density limitations.

The inputs to the PIM consist of all I/O and dedicated input pins and all macrocell feedbacks from within the logic blocks. The number of PIM inputs increases with pin count and the number of logic blocks. The outputs from the PIM are signals routed to the appropriate logic blocks. Each logic block receives 36 inputs from the PIM and their complements, allowing for 32-bit operations to be implemented in a single pass through the device. The wide number of inputs to the logic block also improves the routing capacity of the Ultra37000 family.

An important feature of the PIM is its simple timing. The propagation delay through the PIM is accounted for in the timing specifications for each device. There is no additional delay for traveling through the PIM. In fact, all inputs travel through the PIM. As a result, there are no route-dependent timing parameters on the Ultra37000 devices. The worst-case PIM delays are incorporated in all appropriate Ultra37000 specifications.

Routing signals through the PIM is completely invisible to the user. All routing is accomplished by software—no hand routing is necessary. *Warp*® and third-party development packages automatically route designs for the Ultra37000 family in a matter of minutes. Finally, the rich routing resources of the Ultra37000 family accommodate last minute logic changes while maintaining fixed pin assignments.

Logic Block

The logic block is the basic building block of the Ultra37000 architecture. It consists of a product term array, an intelligent product-term allocator, 16 macrocells, and a number of I/O cells. The number of I/O cells varies depending on the device used. Refer to *Figure 1* for the block diagram.

Product Term Array

Each logic block features a 72 x 87 programmable product term array. This array accepts 36 inputs from the PIM, which originate from macrocell feedbacks and device pins. Active LOW and active HIGH versions of each of these inputs are generated to create the full 72-input field. The 87 product terms in the array can be created from any of the 72 inputs.

Of the 87 product terms, 80 are for general-purpose use for the 16 macrocells in the logic block. Four of the remaining seven product terms in the logic block are output enable (OE) product terms. Each of the OE product terms controls up to eight of the 16 macrocells and is selectable on an individual macrocell basis. In other words, each I/O cell can select between one of two OE product terms to control the output buffer. The first two of these four OE product terms are available to the upper half of the I/O macrocells in a logic block. The other two OE product terms are available to the lower half of the I/O macrocells in a logic block.

The next two product terms in each logic block are dedicated asynchronous set and asynchronous reset product terms. The final product term is the product term clock. The set, reset, OE and product term clock have polarity control to realize OR functions in a single pass through the array.

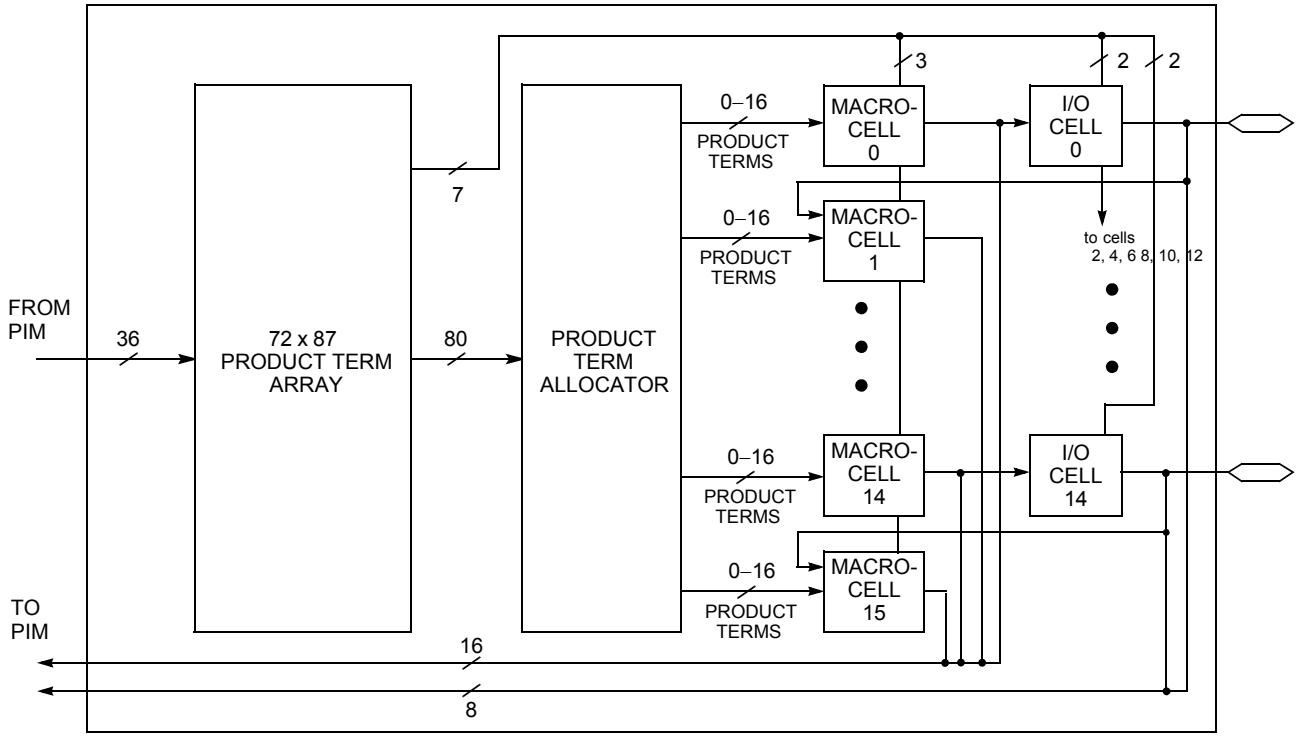


Figure 1. Logic Block with 50% Buried Macrocells

Low-Power Option

Each logic block can operate in high-speed mode for critical path performance, or in low-power mode for power conservation. The logic block mode is set by the user on a logic block by logic block basis.

Product Term Allocator

Through the product term allocator, software automatically distributes product terms among the 16 macrocells in the logic block as needed. A total of 80 product terms are available from the local product term array. The product term allocator provides two important capabilities without affecting performance: product term steering and product term sharing.

Product Term Steering

Product term steering is the process of assigning product terms to macrocells as needed. For example, if one macrocell requires ten product terms while another needs just three, the product term allocator will “steer” ten product terms to one macrocell and three to the other. On Ultra37000 devices, product terms are steered on an individual basis. Any number between 0 and 16 product terms can be steered to any macrocell. Note that 0 product terms is useful in cases where a particular macrocell is unused or used as an input register.

Product Term Sharing

Product term sharing is the process of using the same product term among multiple macrocells. For example, if more than one output has one or more product terms in its equation that are common to other outputs, those product terms are only programmed once. The Ultra37000 product term allocator allows sharing across groups of four output macrocells in a variable fashion. The software automatically takes advantage of this capability—the user does not have to intervene.

Note that neither product term sharing nor product term steering have any effect on the speed of the product. All worst-case steering and sharing configurations have been incorporated in the timing specifications for the Ultra37000 devices.

Ultra37000 Macrocell

Within each logic block there are 16 macrocells. Macrocells can either be I/O Macrocells, which include an I/O Cell which is associated with an I/O pin, or buried Macrocells, which do not connect to an I/O. The combination of I/O Macrocells and buried Macrocells varies from device to device.

Buried Macrocell

Figure 2 displays the architecture of buried macrocells. The buried macrocell features a register that can be configured as combinatorial, a D flip-flop, a T flip-flop, or a level-triggered latch.

The register can be asynchronously set or asynchronously reset at the logic block level with the separate set and reset product terms. Each of these product terms features programmable polarity. This allows the registers to be set or reset based on an AND expression or an OR expression.

Clocking of the register is very flexible. Four global synchronous clocks and a product term clock are available to clock the register. Furthermore, each clock features programmable polarity so that registers can be triggered on falling as well as rising edges (see the Clocking section). Clock polarity is chosen at the logic block level.

The buried macrocell also supports input register capability. The buried macrocell can be configured to act as an input register (D-type or latch) whose input comes from the I/O pin associated with the neighboring macrocell. The output of all buried macrocells is sent directly to the PIM regardless of its configuration.

I/O Macrocell

Figure 2 illustrates the architecture of the I/O macrocell. The I/O macrocell supports the same functions as the buried macrocell with the addition of I/O capability. At the output of the macrocell, a polarity control mux is available to select active LOW or active HIGH signals. This has the added advantage of allowing significant logic reduction to occur in many applications.

The Ultra37000 macrocell features a feedback path to the PIM separate from the I/O pin input path. This means that if the macrocell is buried (fed back internally only), the associated I/O pin can still be used as an input.

Bus Hold Capabilities on all I/Os

Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device's performance. As a latch, bus-hold maintains the last state of a pin when the pin is placed in a high-impedance state, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to V_{CC} or GND. For more information, see the application note *Understanding Bus-Hold—A Feature of Cypress CPLDs*.

Programmable Slew Rate Control

Each output has a programmable configuration bit, which sets the output slew rate to fast or slow. For designs concerned with meeting FCC emissions standards the slow edge provides for lower system noise. For designs requiring very high performance the fast edge rate provides maximum system performance.

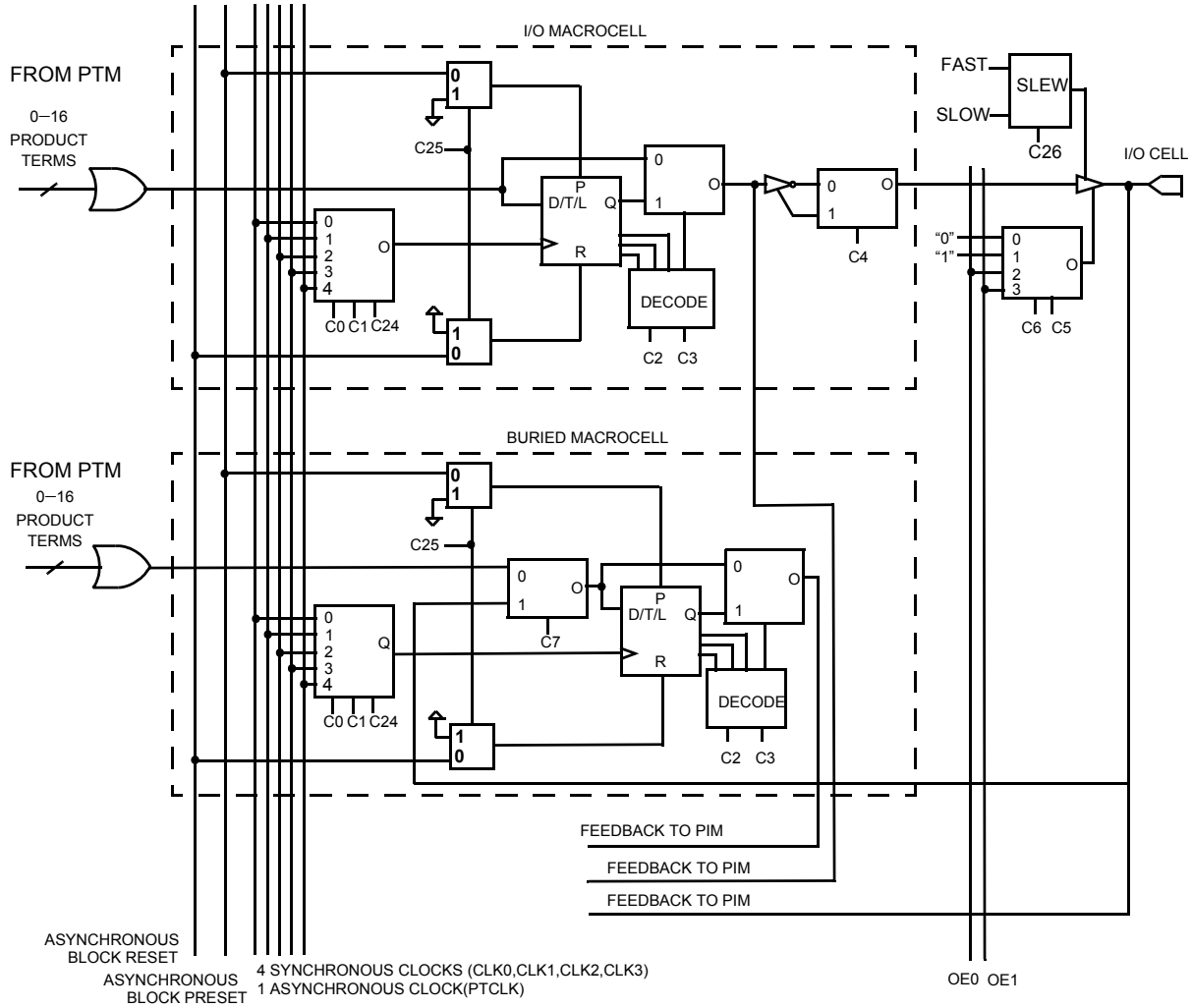


Figure 2. I/O and Buried Macrocells

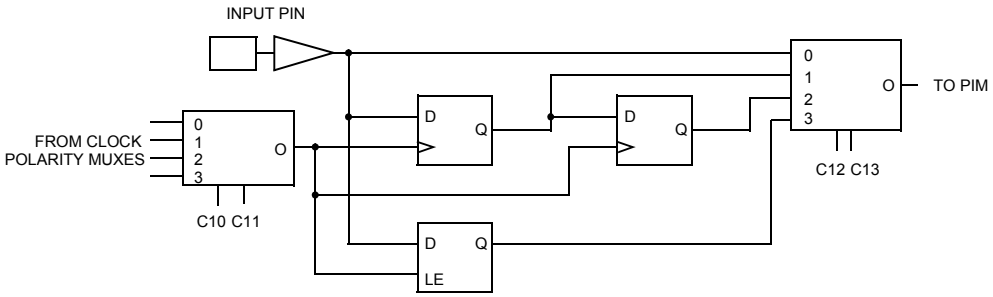


Figure 3. Input Macrocell

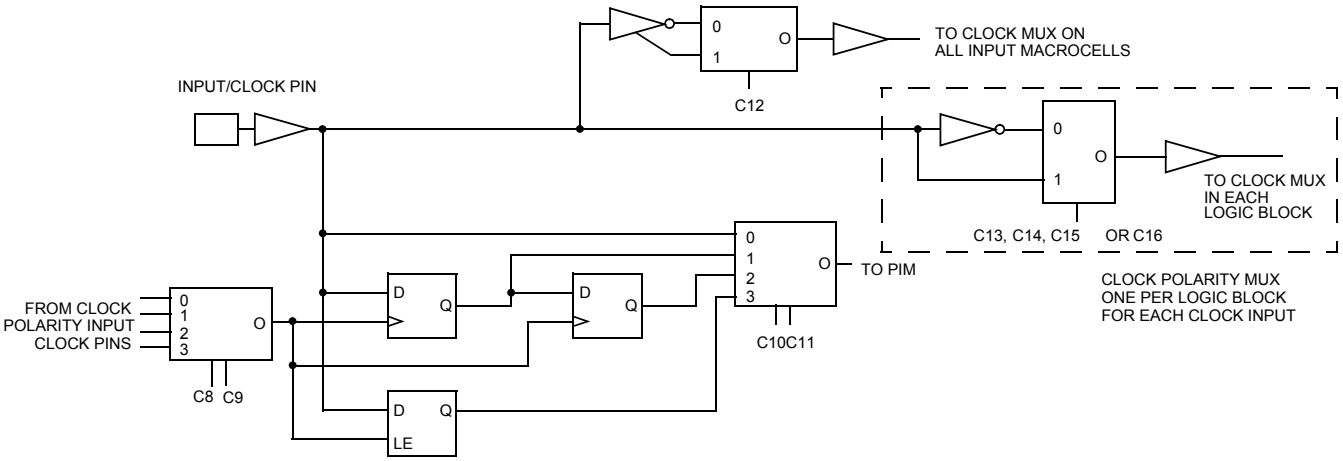


Figure 4. Input/Clock Macrocell

Clocking

Each I/O and buried macrocell has access to four synchronous clocks (CLK0, CLK1, CLK2 and CLK3) as well as an asynchronous product term clock PTCLK. Each input macrocell has access to all four synchronous clocks.

Dedicated Inputs/Clocks

Five pins on each member of the Ultra37000 family are designated as input-only. There are two types of dedicated inputs on Ultra37000 devices: input pins and input/clock pins. *Figure 3* illustrates the architecture for input pins. Four input options are available for the user: combinatorial, registered, double-registered, or latched. If a registered or latched option is selected, any one of the input clocks can be selected for control.

Figure 4 illustrates the architecture for the input/clock pins. Like the input pins, input/clock pins can be combinatorial, registered, double-registered, or latched. In addition, these pins feed the clocking structures throughout the device. The clock path at the input has user-configurable polarity.

Product Term Clocking

In addition to the four synchronous clocks, the Ultra37000 family also has a product term clock for asynchronous clocking. Each logic block has an independent product term clock which is available to all 16 macrocells. Each product term clock also supports user configurable polarity selection.

Timing Model

One of the most important features of the Ultra37000 family is the simplicity of its timing. All delays are worst case and system performance is unaffected by the features used. *Figure 5* illustrates the true timing model for the 167-MHz devices in high speed mode. For combinatorial paths, any input to any output incurs a 6.5-ns worst-case delay regardless of the amount of logic used. For synchronous systems, the input set-up time to the output macrocells for any input is 3.5 ns and the clock to output time is also 4.0 ns. These measurements are for any output and synchronous clock, regardless of the logic used.

The Ultra37000 features:

- No fanout delays
- No expander delays
- No dedicated vs. I/O pin delays
- No additional delay through PIM
- No penalty for using 0–16 product terms
- No added delay for steering product terms
- No added delay for sharing product terms
- No routing delays
- No output bypass delays

The simple timing model of the Ultra37000 family eliminates unexpected performance penalties.

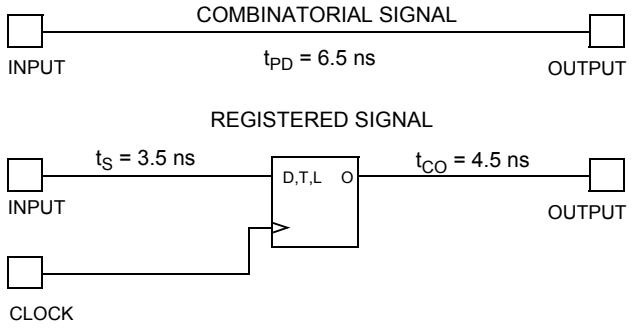


Figure 5. Timing Model for CY37128

JTAG and PCI Standards

PCI Compliance

5V operation of the Ultra37000 is fully compliant with the PCI Local Bus Specification published by the PCI Special Interest Group. The 3.3V products meet all PCI requirements except for the output 3.3V clamp, which is in direct conflict with 5V tolerance. The Ultra37000 family's simple and predictable timing model ensures compliance with the PCI AC specifications independent of the design.

IEEE 1149.1-compliant JTAG

The Ultra37000 family has an IEEE 1149.1 JTAG interface for both Boundary Scan and ISR.

Boundary Scan

The Ultra37000 family supports Bypass, Sample/Preload, Extest, Idcode, and Usercode boundary scan instructions. The JTAG interface is shown in *Figure 6*.

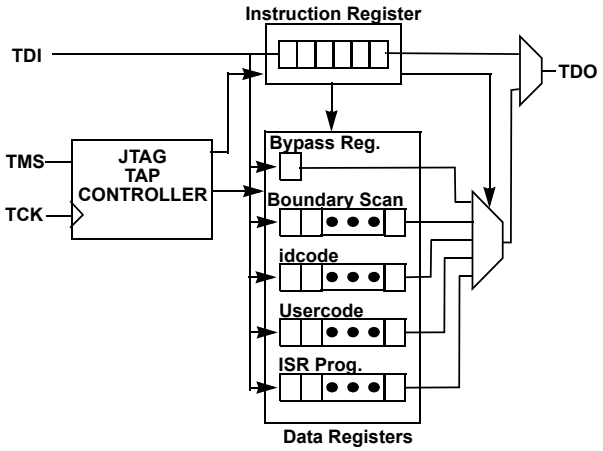


Figure 6. JTAG Interface

In-System Reprogramming (ISR)

In-System Reprogramming is the combination of the capability to program or reprogram a device on-board, and the ability to support design changes without changing the system timing or device pinout. This combination means design changes during debug or field upgrades do not cause board respins. The Ultra37000 family implements ISR by providing a JTAG compliant interface for on-board programming, robust routing resources for pinout flexibility, and a simple timing model for consistent system performance.

Development Software Support

Warp

Warp is a state-of-the-art compiler and complete CPLD design tool. For design entry, Warp provides an IEEE-STD-1076/1164 VHDL text editor, an IEEE-STD-1364 Verilog text editor, and a graphical finite state machine editor. It provides optimized synthesis and fitting by replacing basic circuits with ones pre-optimized for the target device, by implementing logic in unused memory and by perfect communication between fitting and synthesis. To facilitate design and debugging, Warp provides graphical timing simulation and analysis.

Warp Professional™

Warp Professional contains several additional features. It provides an extra method of design entry with its graphical block diagram editor. It allows up to 5 ms timing simulation instead of only 2 ms. It allows comparison of waveforms before and after design changes.

Warp Enterprise™

Warp Enterprise provides even more features. It provides unlimited timing simulation and source-level behavioral simulation as well as a debugger. It has the ability to generate graphical HDL blocks from HDL text. It can even generate testbenches.

Warp is available for PC and UNIX platforms. Some features are not available in the UNIX version. For further information see the *Warp* for PC*, Warp* for UNIX, *Warp* Professional and *Warp* Enterprise data sheets on Cypress's web site (www.cypress.com).

Third-Party Software

Although *Warp* is a complete CPLD development tool on its own, it interfaces with nearly every third party EDA tool. All major third-party software vendors provide support for the Ultra37000 family of devices. Refer to the third-party software data sheet or contact your local sales office for a list of currently supported third-party vendors.

Programming

There are four programming options available for Ultra37000 devices. The first method is to use a PC with the 37000 UltraISR programming cable and software. With this method, the ISR pins of the Ultra37000 devices are routed to a connector at the edge of the printed circuit board. The 37000 UltraISR programming cable is then connected between the parallel port of the PC and this connector. A simple configuration file instructs the ISR software of the programming operations to be performed on each of the Ultra37000 devices in the system. The ISR software then automatically completes all of the necessary data manipulations required to accomplish the programming, reading, verifying, and other ISR functions. For more information on the Cypress ISR Interface, see the ISR Programming Kit data sheet (CY3700i).

The second method for programming Ultra37000 devices is on automatic test equipment (ATE). This is accomplished through a file created by the ISR software. Check the Cypress website for the latest ISR software download information.

The third programming option for Ultra37000 devices is to utilize the embedded controller or processor that already exists in the system. The Ultra37000 ISR software assists in this method by converting the device JEDEC maps into the ISR serial stream that contains the ISR instruction information and the addresses and data of locations to be programmed. The embedded controller then simply directs this ISR stream to the chain of Ultra37000 devices to complete the desired reconfiguring or diagnostic operations. Contact your local sales office for information on availability of this option.

The fourth method for programming Ultra37000 devices is to use the same programmer that is currently being used to program FLASH370i devices.

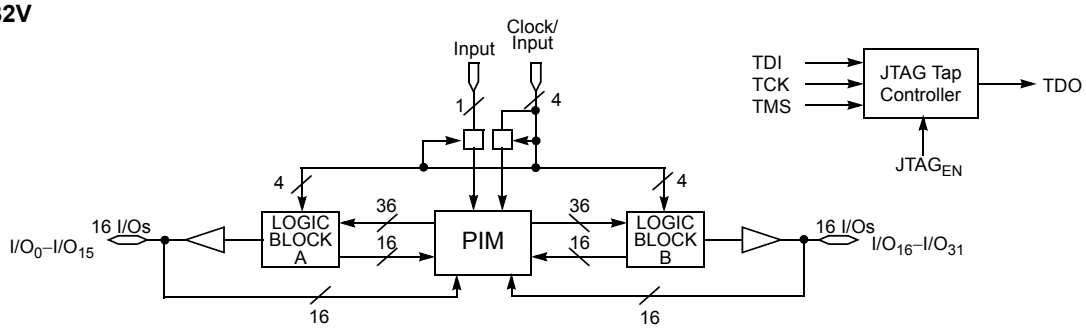
For all pinout, electrical, and timing requirements, refer to device data sheets. For ISR cable and software specifications, refer to the UltraISR kit data sheet (CY3700i).

Third-Party Programmers

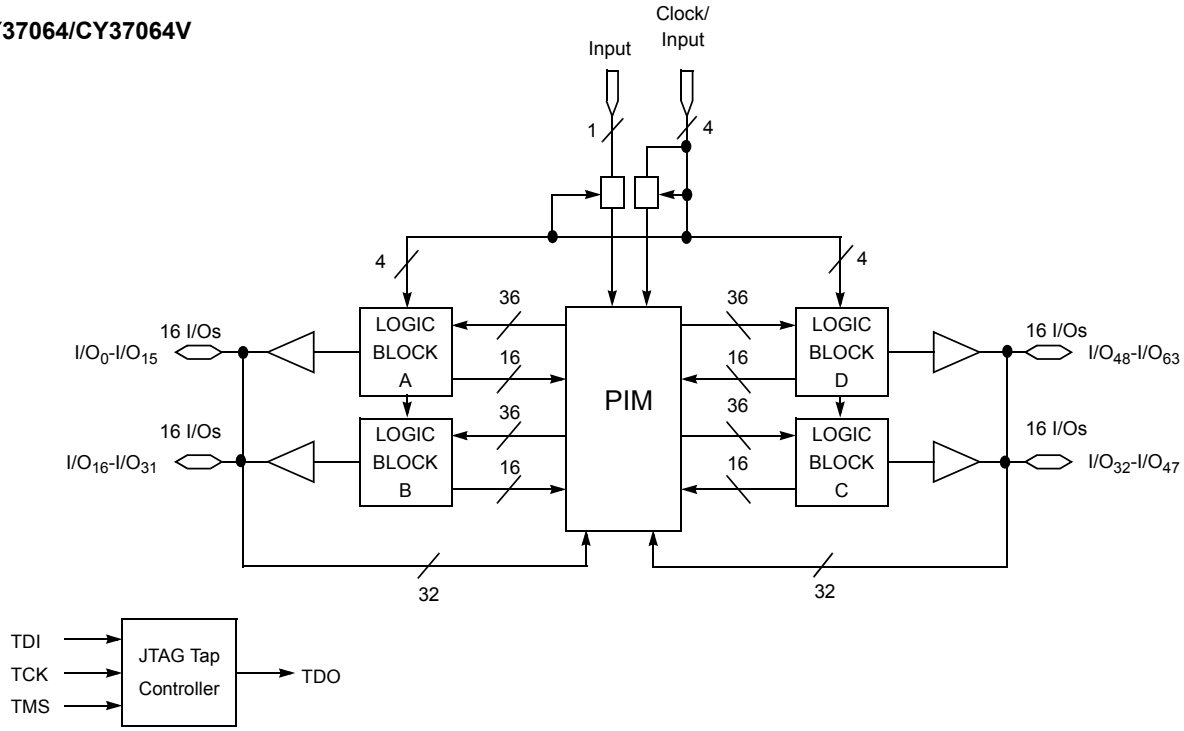
As with development software, Cypress support is available on a wide variety of third-party programmers. All major third-party programmers (including BP Micro, Data I/O, and SMS) support the Ultra37000 family.

Logic Block Diagrams

CY37032/CY37032V

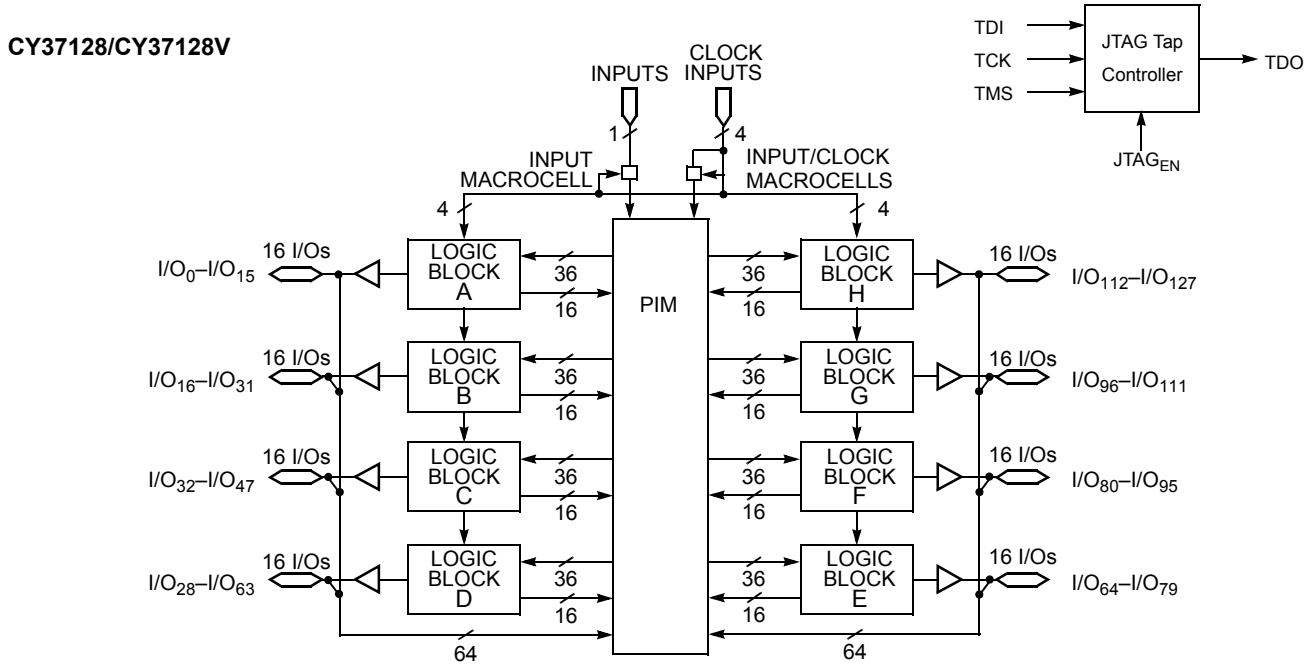


CY37064/CY37064V

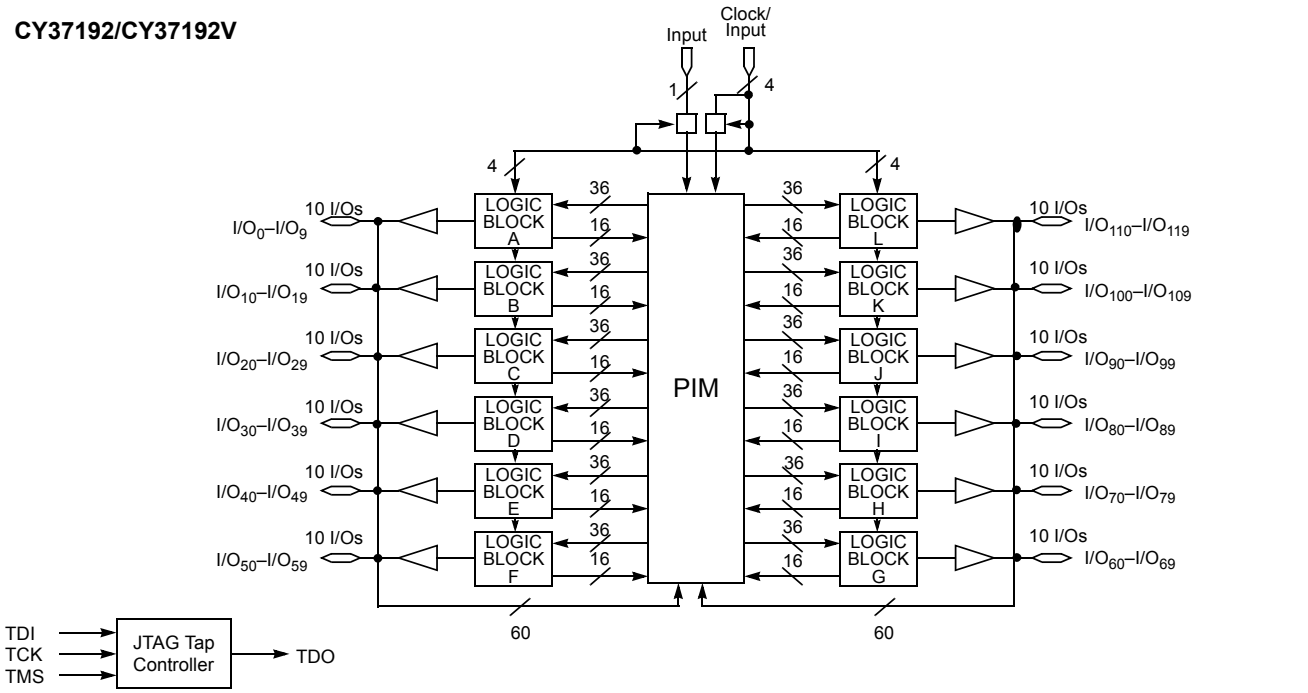


Logic Block Diagrams (continued)

CY37128/CY37128V

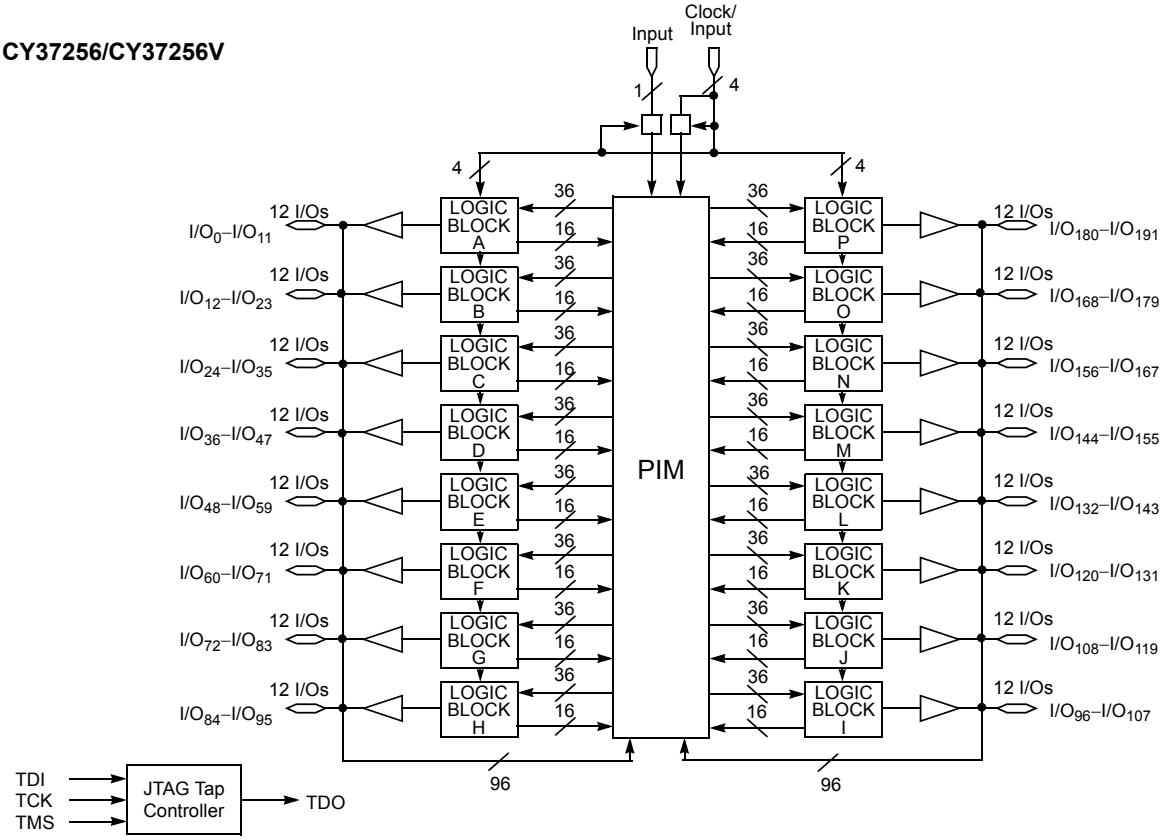


CY37192/CY37192V



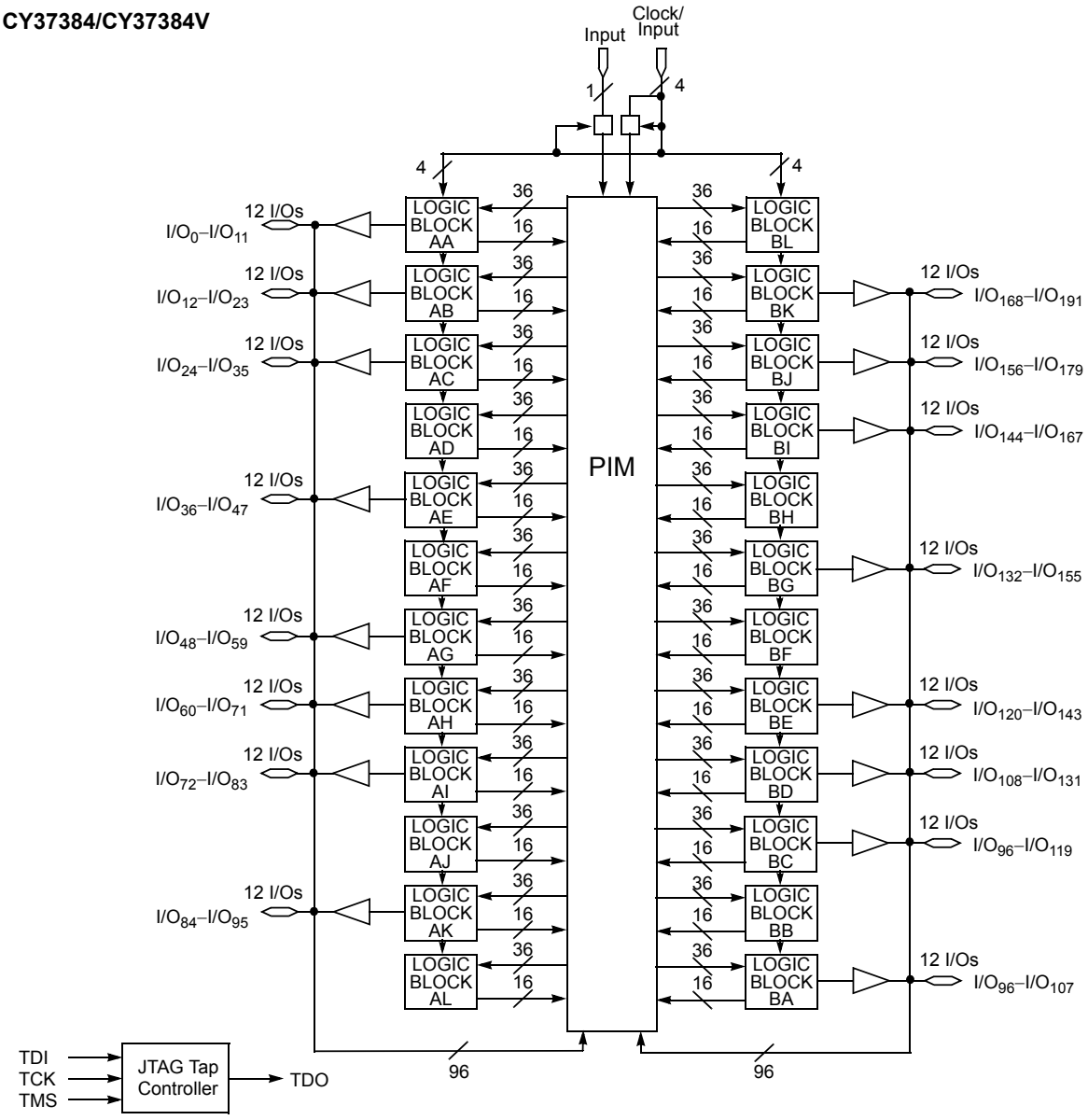
Logic Block Diagrams (continued)

CY37256/CY37256V



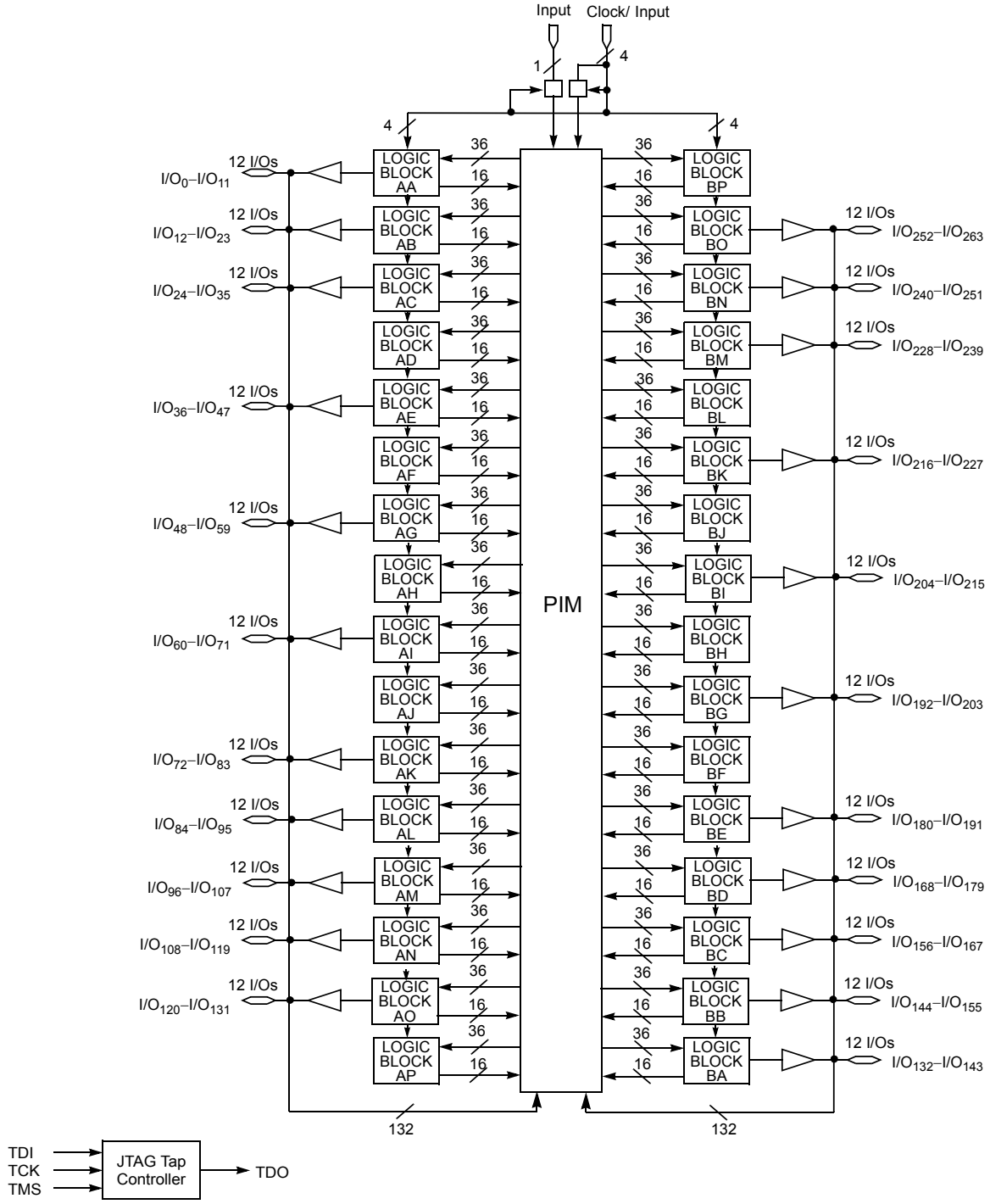
Logic Block Diagrams (continued)

CY37384/CY37384V



Logic Block Diagrams (continued)

CY37512/CY37512V



5.0V Device Characteristics Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High-Z State..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

DC Program Voltage..... 4.5 to 5.5V

Current into Outputs ..... 16 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Operating Range[2]

Range	Ambient Temperature[2]	Junction Temperature	Output Condition	V_{CC}	V_{CCO}
Commercial	0°C to +70°C	0°C to +90°C	5V	5V ± 0.25V	5V ± 0.25V
			3.3V	5V ± 0.25V	3.3V ± 0.3V
Industrial	–40°C to +85°C	–40°C to +105°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V
Military[3]	–55°C to +125°C	–55°C to +130°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V

5.0V Device Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3.2 mA (Com'l/Ind)[4]	2.4			V
			I_{OH} = –2.0 mA (Mil)[4]	2.4			V
V_{OHZ}	Output HIGH Voltage with Output Disabled[5]	V_{CC} = Max.	I_{OH} = 0 µA (Com'l)[6]			4.2	V
			I_{OH} = 0 µA (Ind/Mil)[6]			4.5	V
			I_{OH} = –100 µA (Com'l)[6]			3.6	V
			I_{OH} = –150 µA (Ind/Mil)[6]			3.6	V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 16 mA (Com'l/Ind)[4]			0.5	V
			I_{OL} = 12 mA (Mil)[4]			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs[7]		2.0		V_{CCmax}	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs[7]		–0.5		0.8	V
I_{IX}	Input Load Current	V_I = GND OR V_{CC}, Bus-Hold Disabled		–10		10	µA
I_{OZ}	Output Leakage Current	V_O = GND or V_{CC}, Output Disabled, Bus-Hold Disabled		–50		50	µA
I_{OS}	Output Short Circuit Current[5, 8]	V_{CC} = Max., V_{OUT} = 0.5V		–30		–160	mA
I_{BHL}	Input Bus-Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75			µA
I_{BHH}	Input Bus-Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75			µA
I_{BHLO}	Input Bus-Hold LOW Overdrive Current	V_{CC} = Max.				+500	µA
I_{BHHO}	Input Bus-Hold HIGH Overdrive Current	V_{CC} = Max.				–500	µA

Notes:

2. Normal Programming Conditions apply across Ambient Temperature Range for specified programming methods. For more information on programming the Ultra37000 Family devices, please refer to the Application Note titled "An Introduction to In System Reprogramming with the Ultra37000."
3. T_A is the "Instant On" case temperature.
4. I_{OH} = –2 mA, I_{OL} = 2 mA for TDO.
5. Tested initially and after any design or process changes that may affect these parameters.
6. When the I/O is output disabled, the bus-hold circuit can weakly pull the I/O to above 3.6V if no leakage current is allowed. Note that all I/Os are output disabled during ISR programming. Refer to the application note "Understanding Bus-Hold" for additional information.
7. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
8. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

Inductance[5]

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 5.0V at f = 1 MHz	2	5	2	8	5	8	9	11	nH

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	10	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	12	pF
C_{DP}	Dual-Function Pins[9]	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	16	pF

Endurance Characteristics[5]

Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

3.3V Device Characteristics Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State ..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

DC Program Voltage ..... 3.0 to 3.6V

Current into Outputs ..... 8 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

Operating Range[2]

Range	Ambient Temperature[2]	Junction Temperature	V_{CC}[10]
Commercial	0°C to +70°C	0°C to +90°C	3.3V ± 0.3V
Industrial	–40°C to +85°C	–40°C to +105°C	3.3V ± 0.3V
Military[3]	–55°C to +125°C	–55°C to +130°C	3.3V ± 0.3V

3.3V Device Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –4 mA (Com'l)[4]	2.4		V
			I_{OH} = –3 mA (Mil)[4]			
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8 mA (Com'l)[4]		0.5	V
			I_{OL} = 6 mA (Mil)[4]			
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs[7]		2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs[7]		–0.5	0.8	V
I_{IX}	Input Load Current	V_I = GND OR V_{CC}, Bus-Hold Disabled		–10	10	µA
I_{OZ}	Output Leakage Current	V_O = GND or V_{CC}, Output Disabled, Bus-Hold Disabled		–50	50	µA
I_{OS}	Output Short Circuit Current[5, 8]	V_{CC} = Max., V_{OUT} = 0.5V		–30	–160	mA
I_{BHL}	Input Bus-Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75		µA
I_{BHH}	Input Bus-Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75		µA
I_{BHLO}	Input Bus-Hold LOW Overdrive Current	V_{CC} = Max.			+500	µA
I_{BHHO}	Input Bus-Hold HIGH Overdrive Current	V_{CC} = Max.			–500	µA

Notes:
9. Dual pins are I/O with JTAG pins.
10. For CY37064VP100-143AC, CY37064VP100-143BBC, CY37064VP44-143AC, CY37064VP48-143BAC; Operating Range: V_{CC} is 3.3V± 0.16V.

Inductance[5]

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 3.3V at f = 1 MHz	2	5	2	8	5	8	9	11	nH

Capacitance[5]

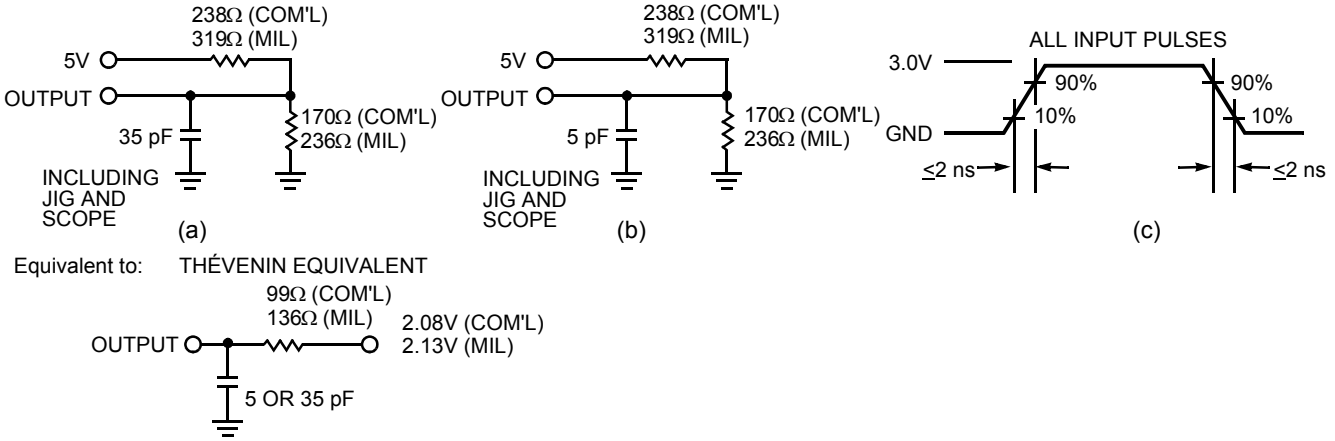
Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	8	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	12	pF
C_{DP}	Dual Functional Pins[9]	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	16	pF

Endurance Characteristics[5]

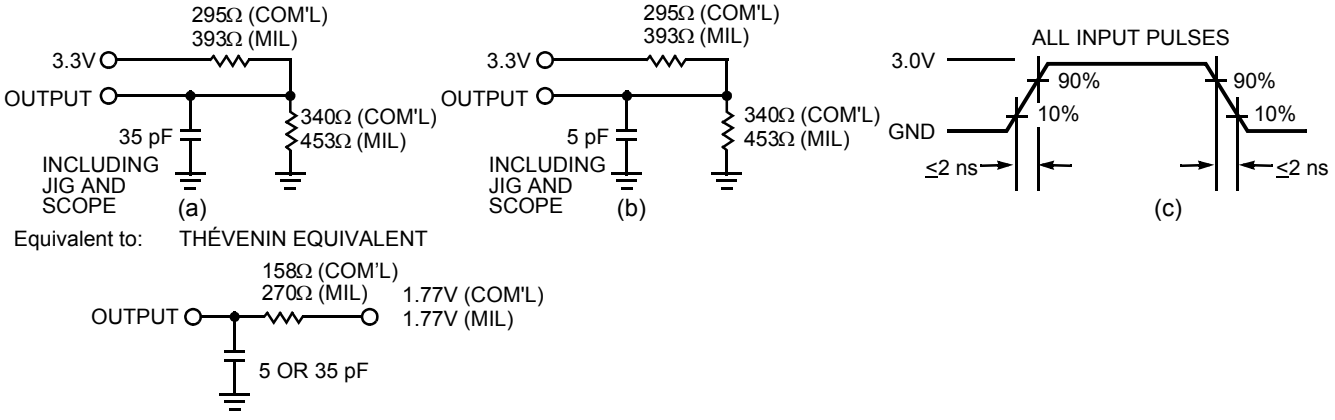
Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

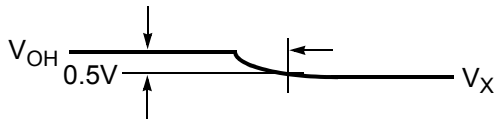
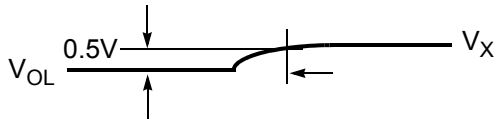
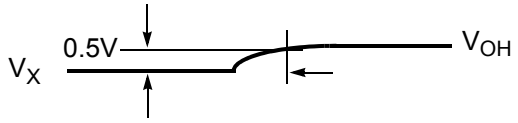
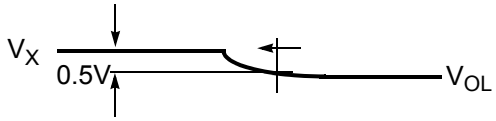
AC Characteristics

5.0V AC Test Loads and Waveforms



3.3V AC Test Loads and Waveforms



Parameter[11]	V_X	Output Waveform—Measurement Level
$t_{ER(-)}$	1.5V	
$t_{ER(+)}$	2.6V	
$t_{EA(+)}$	1.5V	
$t_{EA(-)}$	V_{the}	

(d) Test Waveforms

Switching Characteristics Over the Operating Range [12]

Parameter	Description	Unit
Combinatorial Mode Parameters		
t_{PD}[13, 14, 15]	Input to Combinatorial Output	ns
t_{PDL}[13, 14, 15]	Input to Output Through Transparent Input or Output Latch	ns
t_{PDLL}[13, 14, 15]	Input to Output Through Transparent Input and Output Latches	ns
t_{EA}[13, 14, 15]	Input to Output Enable	ns
t_{ER}[11, 13]	Input to Output Disable	ns
Input Register Parameters		
t_{WL}	Clock or Latch Enable Input LOW Time[8]	ns
t_{WH}	Clock or Latch Enable Input HIGH Time[8]	ns
t_{IS}	Input Register or Latch Set-up Time	ns
t_{IH}	Input Register or Latch Hold Time	ns
t_{ICO}[13, 14, 15]	Input Register Clock or Latch Enable to Combinatorial Output	ns
t_{ICOL}[13, 14, 15]	Input Register Clock or Latch Enable to Output Through Transparent Output Latch	ns
Synchronous Clocking Parameters		
t_{CO}[14, 15]	Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output	ns
t_S[13]	Set-Up Time from Input to Sync. Clk (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	ns
t_H	Register or Latch Data Hold Time	ns
t_{CO2}[13, 14, 15]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Combinatorial Output Delay (Through Logic Array)	ns
t_{SCS}[13]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable (Through Logic Array)	ns
t_{SL}[13]	Set-Up Time from Input Through Transparent Latch to Output Register Synchronous Clock (CLK_0 CLK_1, CLK_2, or CLK_3) or Latch Enable	ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	ns

Notes:
11. t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.
12. All AC parameters are measured with two outputs switching and 35-pF AC Test Load.
13. Logic Blocks operating in Low-Power Mode, add t_{LP} to this spec.
14. Outputs using Slow Output Slew Rate, add t_{SLEW} to this spec.
15. When V_{CCO} = 3.3V, add $t_{3.3IO}$ to this spec.

Switching Characteristics Over the Operating Range (continued)[12]

Parameter	Description	Unit
Product Term Clocking Parameters		
t_{COPT}[13, 14, 15]	Product Term Clock or Latch Enable (PTCLK) to Output	ns
t_{SPT}	Set-Up Time from Input to Product Term Clock or Latch Enable (PTCLK)	ns
t_{HPT}	Register or Latch Data Hold Time	ns
t_{ISPT}[13]	Set-Up Time for Buried Register used as an Input Register from Input to Product Term Clock or Latch Enable (PTCLK)	ns
t_{IHPT}	Buried Register Used as an Input Register or Latch Data Hold Time	ns
t_{CO2PT}[13, 14, 15]	Product Term Clock or Latch Enable (PTCLK) to Output Delay (Through Logic Array)	ns
Pipelined Mode Parameters		
t_{ICS}[13]	Input Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) to Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3)	ns
Operating Frequency Parameters		
f_{MAX1}	Maximum Frequency with Internal Feedback (Lesser of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[5]	MHz
f_{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)[5]	MHz
f_{MAX3}	Maximum Frequency with External Feedback (Lesser of $1/(t_{CO} + t_S)$ or $1/(t_{WL} + t_{WH})$[5]	MHz
f_{MAX4}	Maximum Frequency in Pipelined Mode (Lesser of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)[5]	MHz
Reset/Preset Parameters		
t_{RW}	Asynchronous Reset Width[5]	ns
t_{RR}[13]	Asynchronous Reset Recovery Time[5]	ns
t_{RO}[13, 14, 15]	Asynchronous Reset to Output	ns
t_{PW}	Asynchronous Preset Width[5]	ns
t_{PR}[13]	Asynchronous Preset Recovery Time[5]	ns
t_{PO}[13, 14, 15]	Asynchronous Preset to Output	ns
User Option Parameters		
t_{LP}	Low Power Adder	ns
t_{SLEW}	Slow Output Slew Rate Adder	ns
$t_{3.3IO}$	3.3V I/O Mode Timing Adder[5]	ns
JTAG Timing Parameters		
$t_{S\ JTAG}$	Set-up Time from TDI and TMS to TCK[5]	ns
$t_{H\ JTAG}$	Hold Time on TDI and TMS[5]	ns
$t_{CO\ JTAG}$	Falling Edge of TCK to TDO[5]	ns
f_{JTAG}	Maximum JTAG Tap Controller Frequency[5]	ns

Switching Characteristics Over the Operating Range [12]

Parameter	200 MHz		167 MHz		154 MHz		143 MHz		125 MHz		100 MHz		83 MHz		66 MHz		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters																	
t_{PD}[13, 14, 15]		6		6.5		7.5		8.5		10		12		15		20	ns
t_{PDL}[13, 14, 15]		11		12.5		14.5		16		16.5		17		19		22	ns
t_{PDLL}[13, 14, 15]		12		13.5		15.5		17		17.5		18		20		24	ns
t_{EA}[13, 14, 15]		8		8.5		11		13		14		16		19		24	ns
t_{ER}[11, 13]		8		8.5		11		13		14		16		19		24	ns
Input Register Parameters																	
t_{WL}	2.5		2.5		2.5		2.5		3		3		4		5		ns
t_{WH}	2.5		2.5		2.5		2.5		3		3		4		5		ns
t_{IS}	2		2		2		2		2		2.5		3		4		ns
t_{IH}	2		2		2		2		2		2.5		3		4		ns
t_{ICO}[13, 14, 15]		11		11		11		12.5		12.5		16		19		24	ns
t_{ICOL}[13, 14, 15]		12		12		12		14		16		18		21		26	ns
Synchronous Clocking Parameters																	
t_{CO}[14, 15]		4		4		4.5		6		6.5[16]		6.5[17]		8[18]		10	ns
t_{S}[13]	4		4		5		5		5.5[16]		6[17]		8[18]		10		ns
t_{H}	0		0		0		0		0		0		0		0		ns
t_{CO2}[13, 14, 15]		9.5		10		11		12		14		16		19		24	ns
t_{SCS}[13]	5		6		6.5		7		8[16]		10		12		15		ns
t_{SL}[13]	7.5		7.5		8.5		9		10		12		15		15		ns
t_{HL}	0		0		0		0		0		0		0		0		ns
Product Term Clocking Parameters																	
t_{COPT}[13, 14, 15]		7		10		10		13		13		13		15		20	ns
t_{SPT}	2.5		2.5		2.5		3		5		5.5		6		7		ns
t_{HPT}	2.5		2.5		2.5		3		5		5.5		6		7		ns
t_{ISPT}[13]	0		0		0		0		0		0		0		0		ns
t_{IHPT}	6		6.5		6.5		7.5		9		11		14		19		ns
t_{CO2PT}[13, 14, 15]		12		14		15		19		19		21		24		30	ns
Pipelined Mode Parameters																	
t_{ICS}[13]	5		6		6		7		8[16]		10		12		15		ns
Operating Frequency Parameters																	
f_{MAX1}	200		167		154		143		125[16]		100		83		66		MHz
f_{MAX2}	200		200		200		167		154		153[17]		125[18]		100		MHz
f_{MAX3}	125		125		105		91		83		80[17]		62.5		50		MHz
f_{MAX4}	167		167		154		125		118		100		83		66		MHz
Reset/Preset Parameters																	
t_{RW}	8		8		8		8		10		12		15		20		ns
t_{RR}[13]	10		10		10		10		12		14		17		22		ns

Notes:

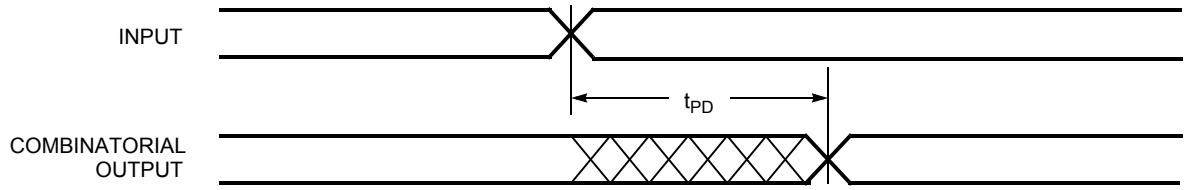
16. The following values correspond to the CY37512 and CY37384 devices: t_{CO} = 5 ns, t_S = 6.5 ns, t_{SCS} = 8.5 ns, t_{ICS} = 8.5 ns, f_{MAX1} = 118 MHz.
17. The following values correspond to the CY37192V and CY37256V devices: t_{CO} = 6 ns, t_S = 7 ns, f_{MAX2} = 143 MHz, f_{MAX3} = 77 MHz, and f_{MAX4} = 100 MHz; and for the CY37512 devices: t_S = 7 ns.
18. The following values correspond to the CY37512V and CY37384V devices: t_{CO} = 6.5 ns, t_S = 9.5 ns, and f_{MAX2} = 105 MHz.

Switching Characteristics Over the Operating Range (continued)[12]

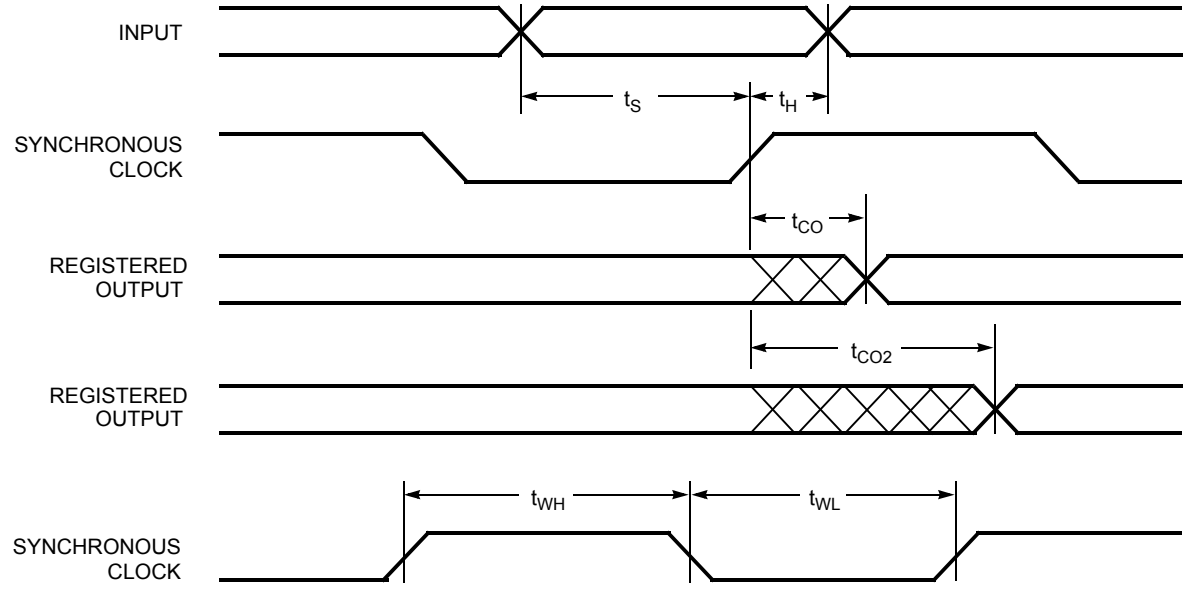
Parameter	200 MHz		167 MHz		154 MHz		143 MHz		125 MHz		100 MHz		83 MHz		66 MHz		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RO}[13, 14, 15]		12		13		13		14		15		18		21		26	ns
t_{PW}	8		8		8		8		10		12		15		20		ns
t_{PR}[13]	10		10		10		10		12		14		17		22		ns
t_{PO}[13, 14, 15]		12		13		13		14		15		18		21		26	ns
User Option Parameters																	
t_{LP}		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
t_{SLEW}		3		3		3		3		3		3		3		3	ns
$t_{3.3IO}$[19]		0.3		0.3		0.3		0.3		0.3		0.3		0.3		0.3	ns
JTAG Timing Parameters																	
$t_{S\ JTAG}$	0		0		0		0		0		0		0		0		ns
$t_{H\ JTAG}$	20		20		20		20		20		20		20		20		ns
$t_{CO\ JTAG}$		20		20		20		20		20		20		20		20	ns
f_{JTAG}		20		20		20		20		20		20		20		20	MHz

Switching Waveforms

Combinatorial Output



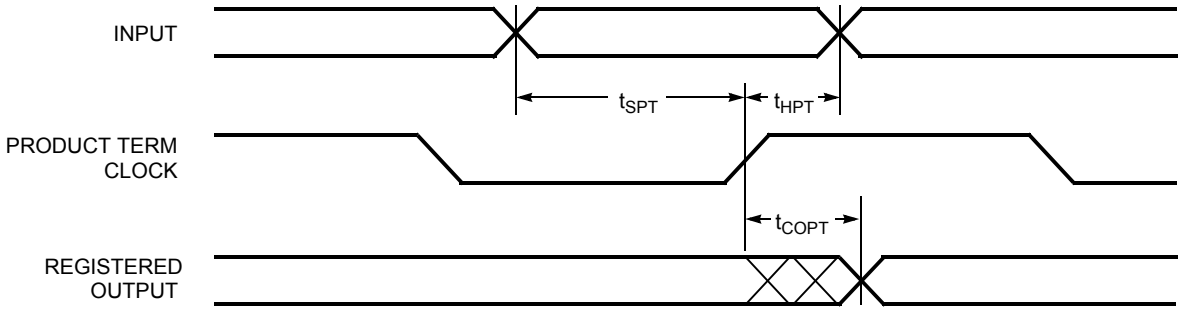
Registered Output with Synchronous Clocking



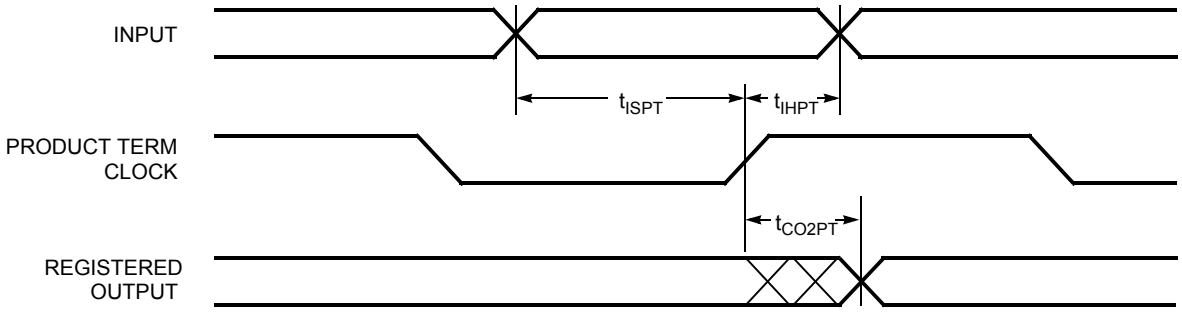
Note:
19. Only applicable to the 5V devices.

Switching Waveforms (continued)

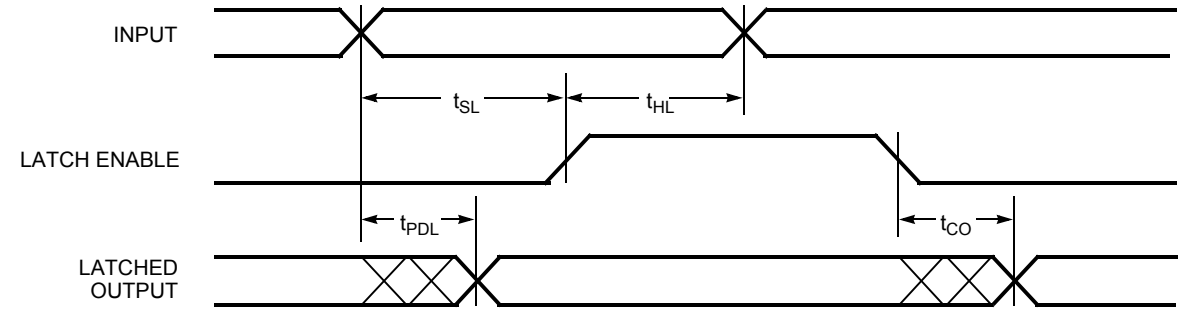
Registered Output with Product Term Clocking Input Going Through the Array



Registered Output with Product Term Clocking Input Coming From Adjacent Buried Register

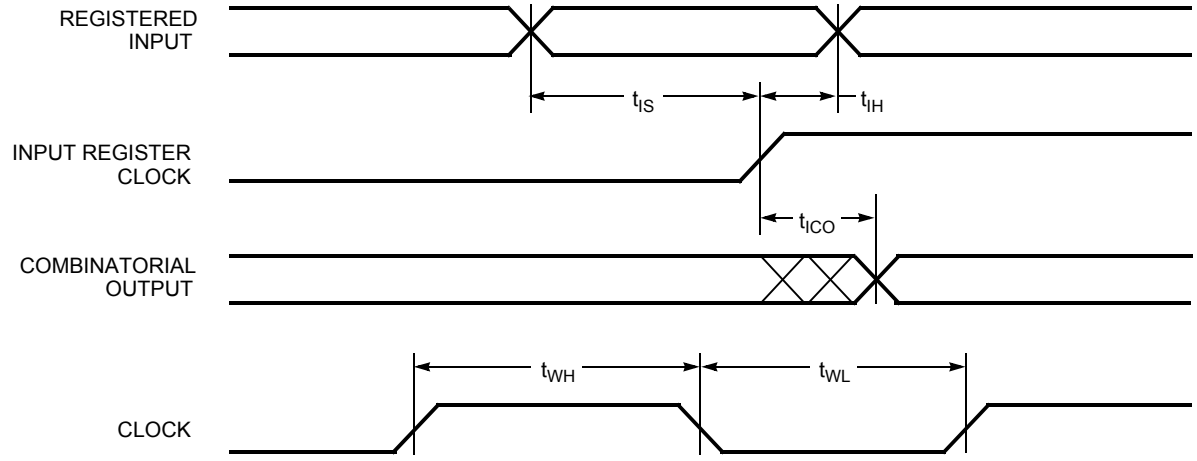


Latched Output

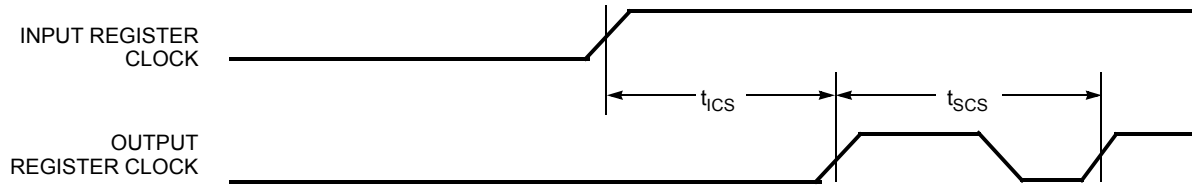


Switching Waveforms (continued)

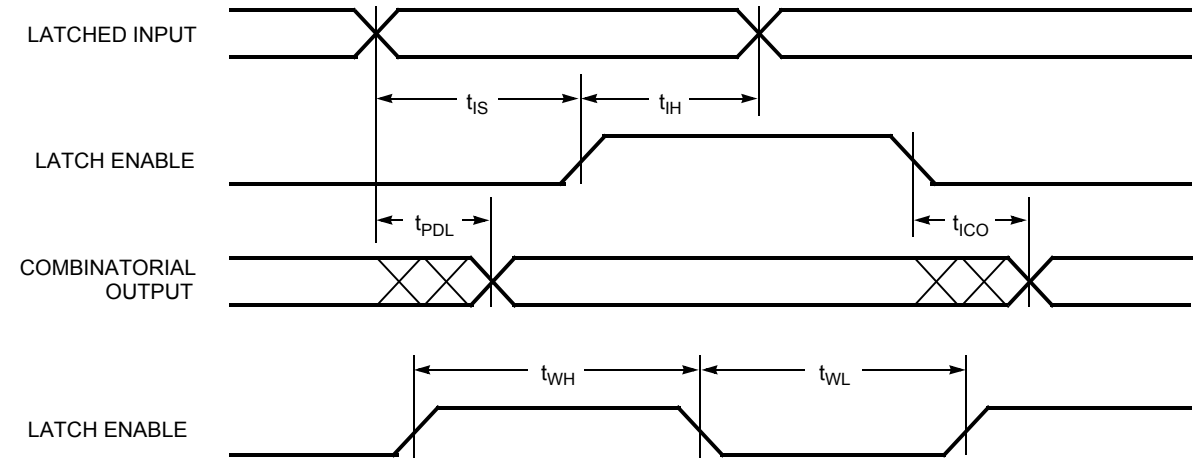
Registered Input



Clock to Clock

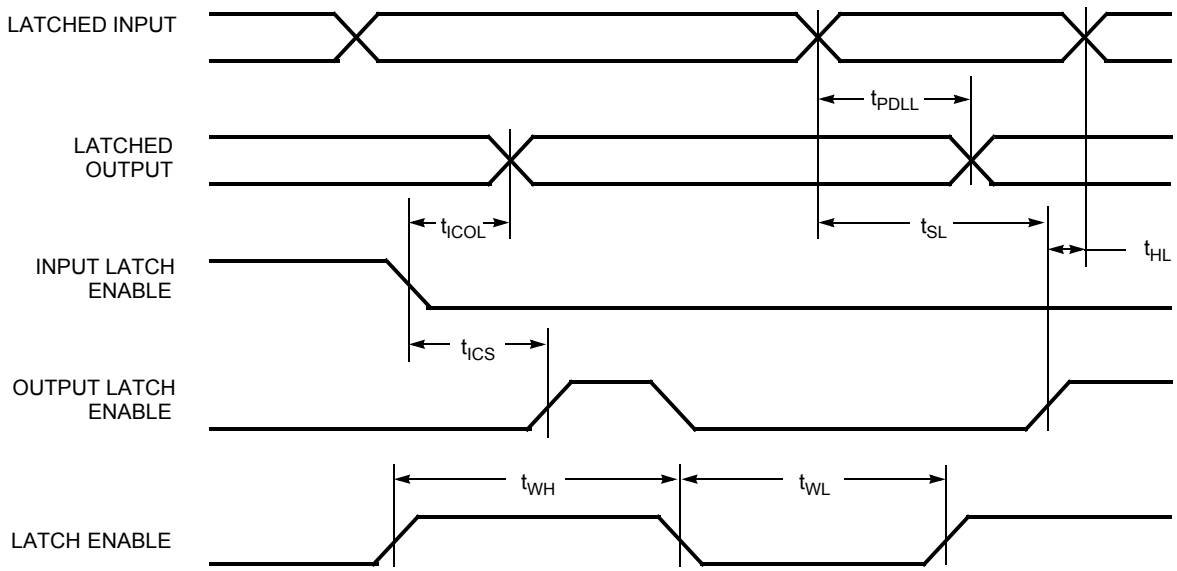


Latched Input

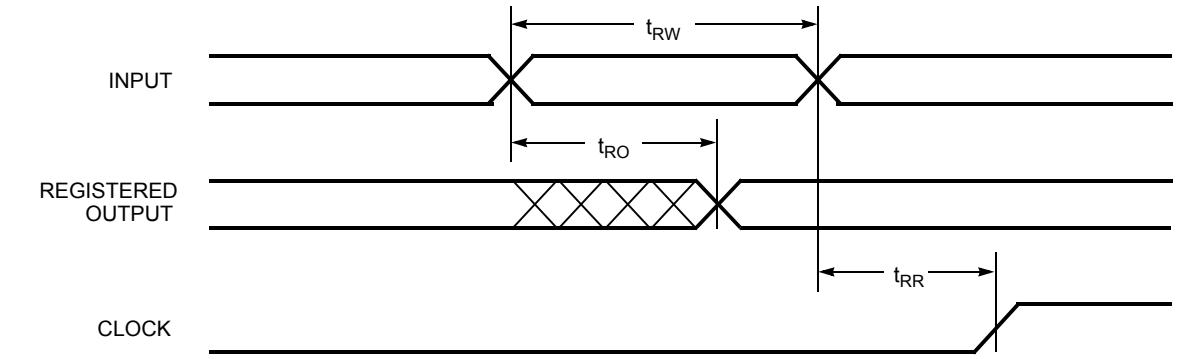


Switching Waveforms (continued)

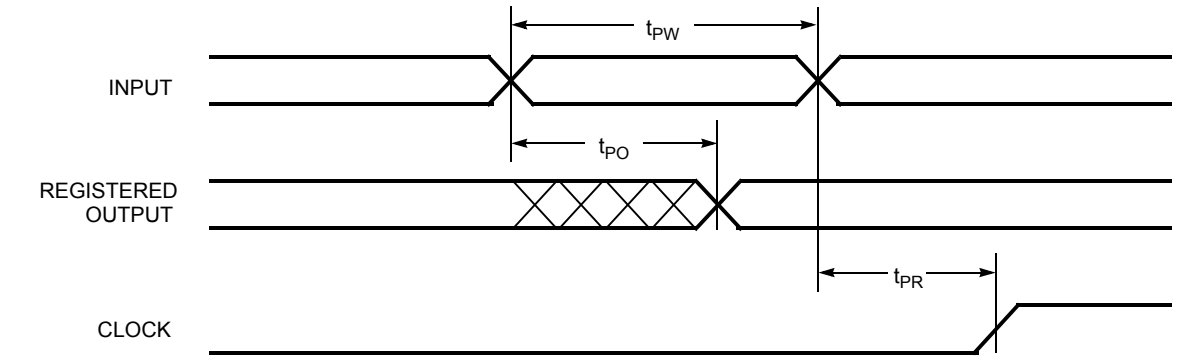
Latched Input and Output



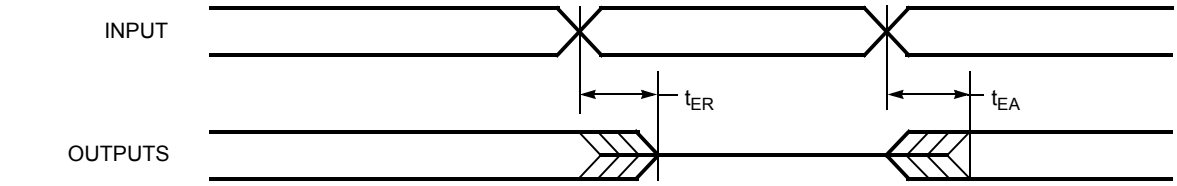
Asynchronous Reset



Asynchronous Preset



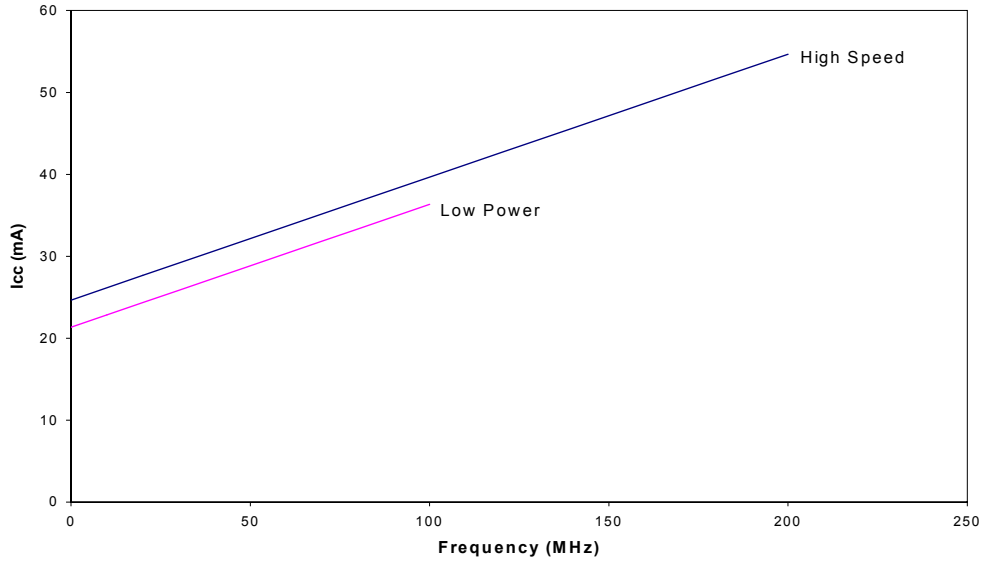
Output Enable/Disable



Power Consumption

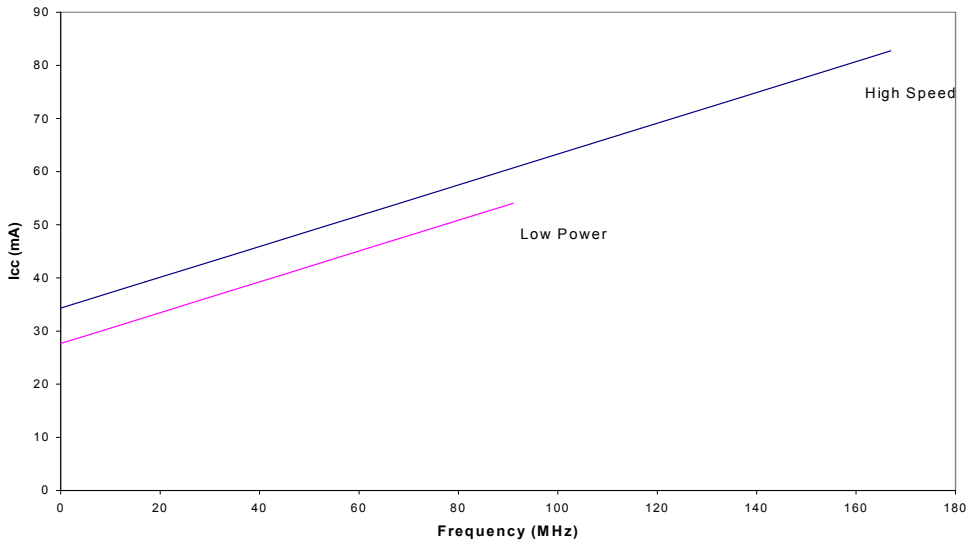
Typical 5.0V Power Consumption

CY37032



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

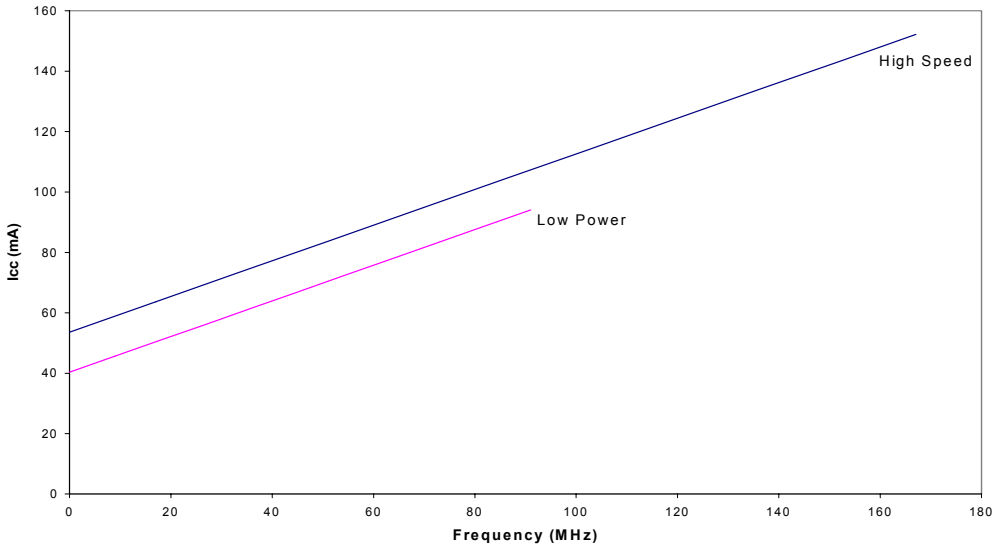
CY37064



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

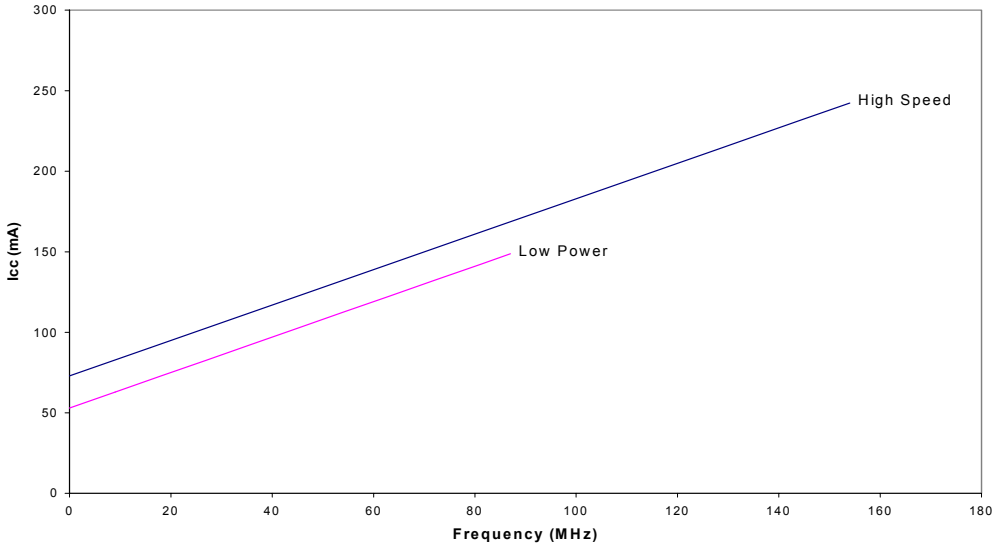
Typical 5.0V Power Consumption (continued)

CY37128



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

CY37192



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature