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CY4501

CCG1 Development Kit Guide

Doc. No. 001-96785 Rev. *E

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Contents

2. Introduction

The CY4501 CCG1 Development Kit (DVK) is based on the CCG1 product family of Cypress's USB microcontrollers. This DVK is primarily intended to be a development vehicle for USB host and client systems that house a Type-C connector as well as for EMCA cables. For USB Power Delivery (PD), the host and client boards available in this kit can be configured as a downstream facing port (DFP), an upstream facing port (UFP), or a dual role port (DRP). The kit also serves as a vehicle to evaluate several features for Type-C, using a SuperSpeed USB demo, a DisplayPort demo and a Power Delivery demo as examples.

2.1 Kit Contents

The CY4501 CCG1 DVK consists of the following contents:

- CCG1 host board
- CCG1 client board
- CCG1 Electronically Marked Cable Assembly (EMCA) board
- SuperSpeed USB Type-A to Type-B cable
- Two USB 2.0 Type-A to Mini-B cables
- MiniProg3
- Quick Start Guide

2.1.1 Hardware Not Included With Kit

The CY4501 CCG1 DVK does not come with all of the hardware needed to perform the demonstrations documented in Kit Operation for SuperSpeed USB Demonstration, Kit Operation for DisplayPort Demonstration, and Kit Operation for Power Delivery Demonstration. The following items are not included:

- USB drive needed for Kit Operation for SuperSpeed USB Demonstration and Kit Operation for DisplayPort Demonstration.
- DisplayPort cables needed for Kit Operation for DisplayPort Demonstration. They are required to make connections from a PC to the CCG1 host board and from the CCG1 client board to the display monitor. If the PC has a mini-DisplayPort, then a mini-DisplayPort to DisplayPort cable will be required.
- A 24 V, 5A output capable Power Supply needed for Kit Operation for Power Delivery Demonstration. This is required to provide 24 V to the client board as an input to the Power Delivery demo.
- A multimeter needed for Kit Operation for Power Delivery Demonstration. A standard multimeter is required to measure the output voltage on the client board to successfully demonstrate Power Delivery functionality.

2.2 Getting Started

For instructions on how to run a quick demonstration and observe kit functionality, refer to Kit Operation for SuperSpeed USB Demonstration.

2.2.1 Configuring the CY4501 CCG1 DVK Host, Client, and EMCA Boards

Refer to Kit Operation for SuperSpeed USB Demonstration for complete instructions on configuring the CY4501 CCG1 DVK host, client, and EMCA boards and to learn about configuring the DVK and connecting it to a PC.

2.3 List of Recommended Hardware

2.3.1 Recommended Cables

See Table 2-1 to obtain a set of cables recommended to work with this kit. This kit is not shipped with these cables and they are required to operate the DisplayPort Alternate Mode Demo explained in the Kit Operation for DisplayPort Demonstration chapter.

Table 2-1. List of Recommended Cables

Description	Manufacturer	MPN	Vendor Link
DisplayPort to DisplayPort Cable (6”, gold plated)	Cable Matters	102005-6	Amazon Link
Mini DisplayPort to DisplayPort Cable (3”, gold plated)	Cable Matters	101007-BLACK-3	Amazon Link

Use item 1 in Table 2-1 if the PC being used has a DisplayPort connector. If the PC has a mini DisplayPort connector, use item 2 in Table 2-1. If the DisplayPort monitor has a regular DisplayPort connector, use item 1 in Table 2-1. Use item 2 in Table 2-1 if the DisplayPort monitor being used has a Mini DisplayPort connector.

2.3.2 Recommended Power Adapter

The recommended power adapter to use when performing the demo described in Kit Operation for Power Delivery Demonstration is the AC/DC desktop adaptor (24 V, 120 W) from Phihong USA (MPN #: PSA120U-240V). The vendor link from Digikey can be found here.

3. Kit Installation

This chapter describes how to perform the installation steps for the CY4501 CCG1 DVK.

3.1 CY4501 CCG1 DVK Kit Software Installation

To install the kit software, follow these steps:

1. Download the latest kit software setup "CY4501 CCG1 DVK COMPLETE SETUP" from the kit's website: www.cypress.com/go/CY4501. This package contains the kit hardware files, user guide, quick start guide, and PSoC Programmer software. Double-click on the executable to start the installation. Click **Next** when the screen shown in Figure 3-1 appears.

Figure 3-1. CY4501 CCG1 DVK Installer Screen

2. Select the required **Installation Type** and click the **Next** button to start the install (Figure 3-2). For first-time installation, it is recommended that you select "Typical" as the **Installation Type**.

Figure 3-2. Installation Wizard

3. Accept the license agreement for the software components and click **Next** (Figure 3-3).

Figure 3-3. License Agreement

4. Figure 3-4 shows the installation progress.

Figure 3-4. Installation Progress

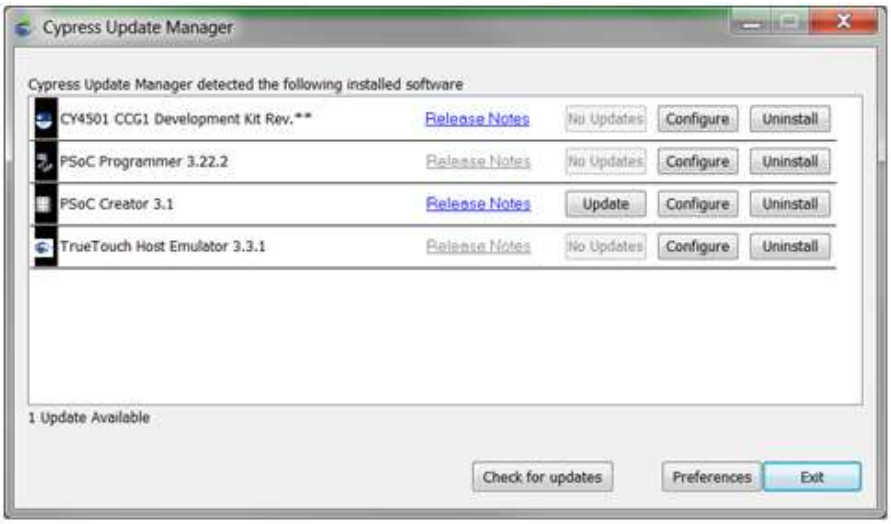
5. Click **Finish** when complete (Figure 3-5).

Figure 3-5. Software Installation Complete

6. When installation is complete, you have the option to **Launch Cypress Update Manager** (Figure 3-6) to ensure you have the latest software package. Click the **Check for updates** button at the bottom of the window. If “No Updates”

appears adjacent to the CY4501 CCG1 DVK, click the **Exit** button. If there are updates, click the **Update** button to download and install the latest kit package.

Figure 3-6. Cypress Update Manager



Note: You can launch the Update Manager at any time from **Windows > Start > All Programs > Cypress > Cypress Update Manager**.

7. After the installation is complete, the contents are available at the following location: `<Install Directory>\CY4501 CCG1 DVK\1.0`.

   Note: On the Windows 32-bit platform, the default <Install Directory> is `C:\Program Files\Cypress`; on the Windows 64-bit platform, it is `C:\Program Files(x86)\Cypress`.

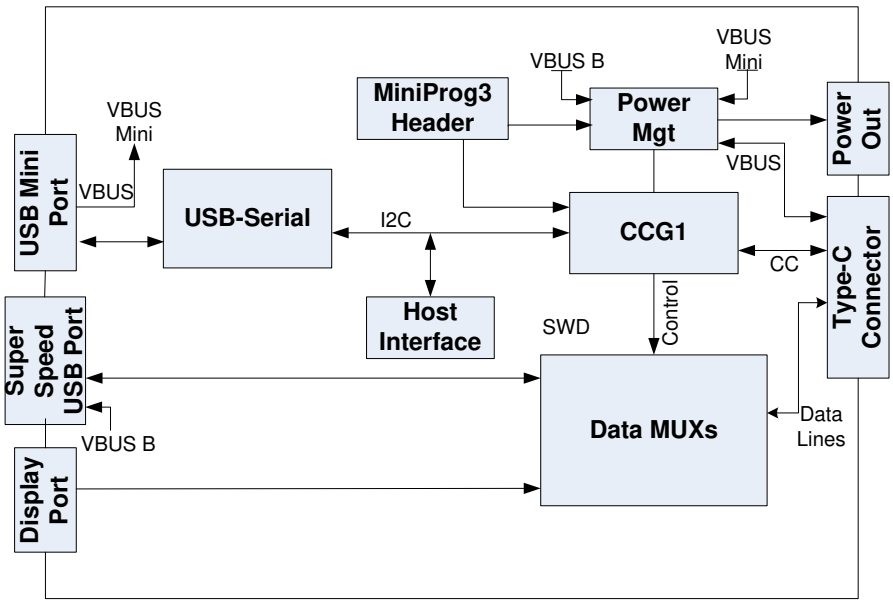
4. CCG1 Host Board

The CCG1 host board is an evaluation board equipped with a CCG1 (CYPD1131-35FNXI), a Type-C connector, a USB Mini-B port, a SuperSpeed USB port Type-B, and a DisplayPort interface. This evaluation board supports notebooks, tablets, smart phones, and other applications that would host a Type-C interface. It is primarily intended as a development vehicle for USB host systems that house a Type-C connector. For USB PD, the board can be configured as a DFP, UFP, or DRP. The user can connect this board to a host processor or embedded controller (EC) to develop USB PD applications. The board also serves as a vehicle to evaluate the Alternate Modes for Type-C, using DisplayPort video as an example. In addition, it can be reconfigured to program and test EMCA cables.

4.1 Block Diagram

Figure 4-1 shows the CCG1 host board block diagram. On the board, the CCG1 device provides a host processor interface (HPI) to a PC via a USB-Serial connection or to an external Embedded Controller (EC) and a Type-C connector for the USB PD interface. Also included is a power connector, a SuperSpeed USB port Type-B, and a DisplayPort connector to source video. The MiniProg3 device shipped with this kit can be connected to a PC to reprogram the firmware in the CCG1 device via the 5-pin programming header J5 using PSoC Programmer software from Cypress. The SuperSpeed USB signals and DisplayPort signals are delivered to the Type-C connector through a high-speed multiplexer controlled by the CCG1 device. The power to this board is connected to a circuit that allows power to be sourced from either a 5 V rail supplied by the USB Mini port, MiniProg3, USB SuperSpeed connector or VBUS that is part of the Type-C connector (when the Type-C port on this host board is acting as a power consumer).

Figure 4-1. CCG1 Host Board Block Diagram



4.2 Features

Table 4-1 shows the features of the CCG1 host board.

Table 4-1. CCG1 Host Board Features

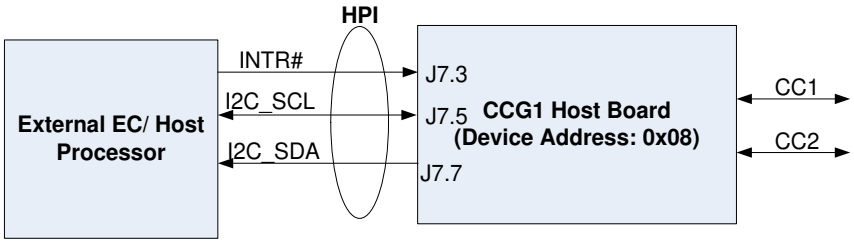
Feature	Description
CCG1 part number	CYPD1131-35FNXI
CCG1 package	35-CSP
USB PD/ Type-C	Ability to support DRP, DFP, and UFP
	Type-C VBUS current setting via a jumper that selects one of the three Rp values. These three values correspond to the three currents as defined in the Type-C specification.
	VBUS provider field-effect transistor (FET) control for cold socket
	VBUS consumer FET control
	VBUS discharge FET control
	Ability to present either Rd or Rp on CC line
	Dead battery support
OVP and OCP	VCONN or VBUS over-current protection
	VBUS overvoltage protection
Plug orientation, Detection and Alternate modes	Five MUX-select pins to select between SuperSpeed USB and 2-lane or 4-lane DisplayPort
	Hot Plug Detect (HPD) for DisplayPort Alternate Mode of operation
USB Type-B Mini	USB Mini-B receptacle connected to USB-to-serial device
I^2C interface	I^2C pins and interrupt output pin for connecting to an Embedded Controller (EC)
Programming	SWD pins to debug/program CCG1 using Cypress MiniProg3
Power	5 V from USB Mini 5 V from SuperSpeed USB Type-B (default power for the board) 5 V from MiniProg3 5 V to 20 V from Type-C connector

4.3 Connecting to Embedded Controller or Host Processor

The CCG1 host board provides a Host Processor Interface (HPI) to interface to an external EC. In terms of hardware, the HPI is a three-pin interface composed of I^2C (SDA and SCL) and an interrupt signal. The CCG1 device on the host board implements the HPI over a 400-kHz I^2C slave interface (CCG1 I^2C slave device address: 0x08) with an interrupt line. The CCG1 HPI allows the EC/host processor to change the configuration, monitor status, update firmware, or transparently interact with connected devices using unstructured vendor-defined messages (VDMs). When connecting the EC to communicate with the CCG1 device on the host board, it is recommended that the USB-Serial device be disconnected from this CCG1 device. This can be done by reconfiguring the I2C pins as input GPIOs using the USB serial configuration utility.

Figure 4-2 shows the how the EC and CCG1 host board are connected. The HPI pins are located on connector J7. Pin 7 of J7 (J7.7) is I2C_SDA, pin 5 (J7.5) is I2C_SCL, and pin 3 (J7.3) is INT (see Table 4-2).

Figure 4-2. Connection Between EC and CCG1 Host Board



4.4 Connectors and Jumper Settings

Figure 4-3 and Figure 4-4 show the CCG1 host board connectors and default jumper settings. Table 4-2 shows a detailed description of the connectors and jumper settings.

Figure 4-3. CCG1 Host Board Connectors

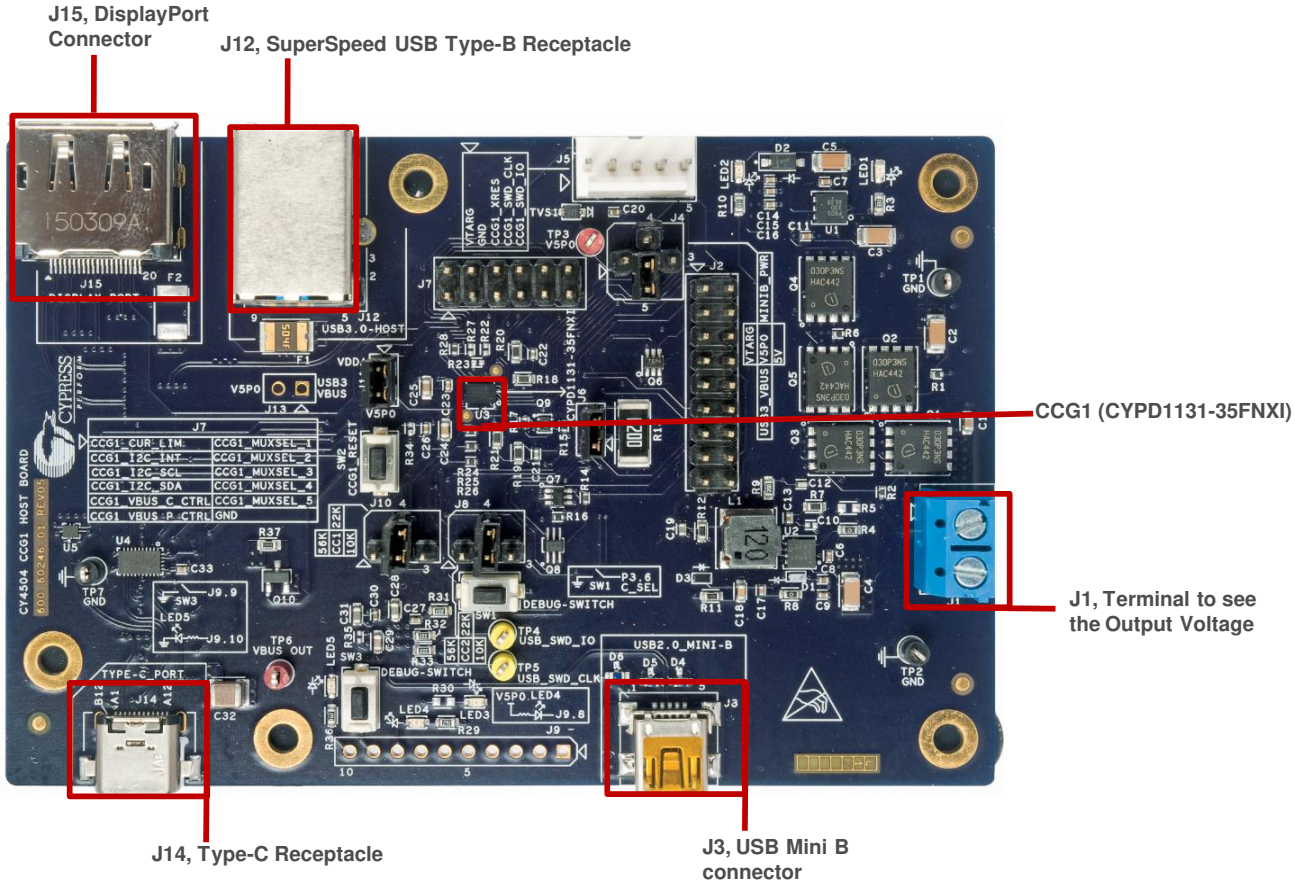


Figure 4-4. CCG1 Host Board Default Jumper Settings

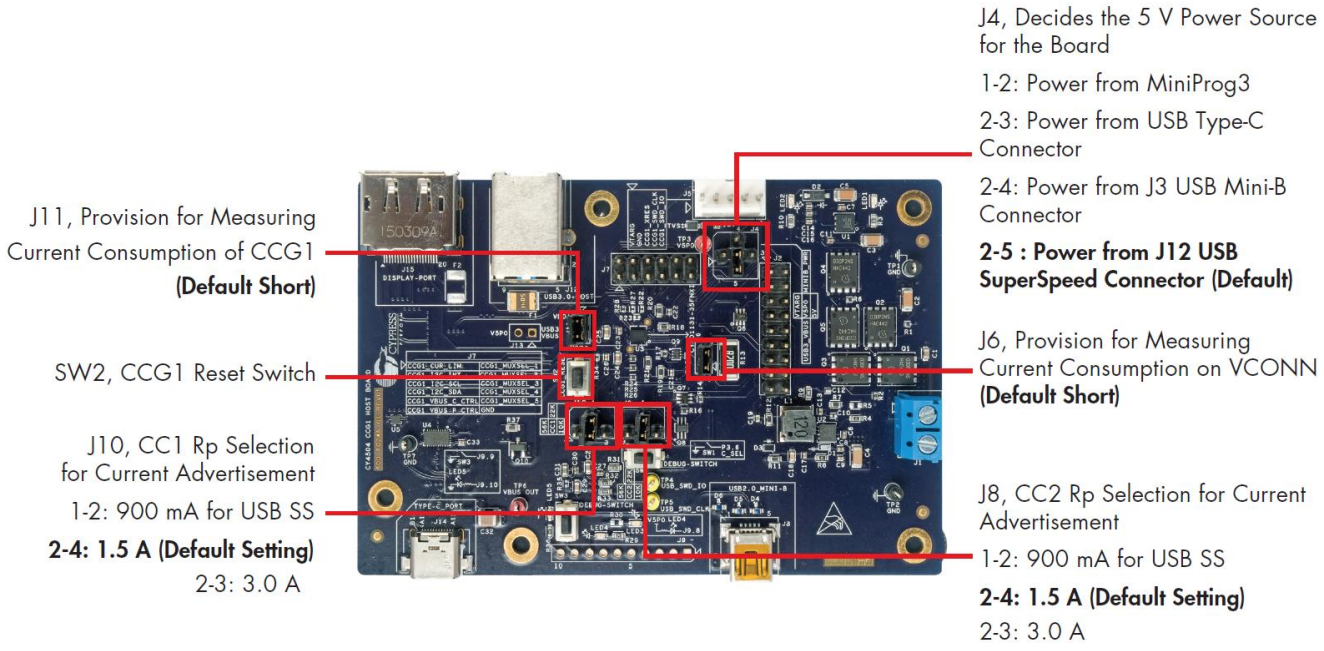


Table 4-2. CCG1 Host Board Jumper Description and Default Settings

Jumper	Description		Default
J1	Terminal Block to measure the incoming voltage from client board		NA
J2	Header for signal probing		NA
	Pin 1: CC1_RP_EXT	Pin 2: CCG1_DEV_DET	
	Pin 3: CC1_RD_EXT	Pin 4: CCG1_CC1_CTRL	
	Pin 5: CC2_RP_EXT	Pin 6: CCG1_CC2_CTRL	
	Pin 7: CC2_RD_EXT	Pin 8: CCG1_CC2	
	Pin 9: CCG1_VBUS_VREF	Pin 10: CCG1_XRES	
	Pin 11: CCG1_VBUS_VMON	Pin 12: CCG1_CC1	
	Pin 13: VBUS_DISCHARGE	Pin 14: CCG1_HOTPLUG_DET	
	Pin 15: NC	Pin 16: NC	
	Pin 17: 5 V supply	Pin 18: GND	
J3	USB 2.0 Mini-B connector (receptacle)		NA
J4	Board power supply selection (ensure J13 is open): 1 and 2 short: Select the power supply from J5, MiniProg3. 2 and 4 short: Select the power supply from J3, USB Mini-B connector. 2 and 3 short: Select the power supply from J14, USB Type-C connector. 2 and 5 short: Select the power supply from J12, SuperSpeed USB connector.		2 and 5 short
J5	Programming Header Pin 1: VTARG Pin 2: GND Pin3: CCG1_XRES Pin4: CCG1_SWD_CLK Pin5: CCG1_SWD_IO		NA
J6	Header for VCONN power consumption measurement: Short: Normal operation. Open: Connect 1 and 2 to ammeter.		Short

Jumper	Description			Default
J7	Pin 1: CCG1_CUR_LIM		Pin 2: CCG1_MUXSEL_1	NA
	Pin 3: CCG1_I2C_INT	For HPI Interface	Pin 4: CCG1_MUXSEL_2	
	Pin 5: CCG1_I2C_SCL		Pin 6: CCG1_MUXSEL_3	
	Pin 7: CCG1_I2C_SDA		Pin 8: CCG1_MUXSEL_4	
	Pin 9: CCG1_VBUS_C_CTRL		Pin 10: CCG1_MUXSEL_5	
	Pin 11: CCG1_VBUS_P_CTRL		Pin 12: GND	
J8	CC2 Rp selection for current advertisement: 1 and 2 short: 500 mA for USB 2.0, 900 mA for SuperSpeed USB (default USB current) 2 and 4 short: 1.5 A 2 and 3 short: 3.0 A			2 and 4 short
J9	USB Serial Debug Header Pin 1: SCB0_0 Pin 2: SCB0_1 Pin 3: SCB0_2 Pin 4: SCB0_3 Pin 5: SCB0_4 Pin 6: SCB0_5 Pin 7: GPIO_0 Pin 8: Connected to cathode of LED4 Pin 9: Connected to Pin2 of SW3 Pin 10: Connected to LED5 via R36			This jumper is not populated
J10	CC1 Rp selection for current advertisement: 1 and 2 short: 500 mA for USB 2.0, 900 mA for SuperSpeed USB (default USB current) 2 and 4 short: 1.5 A 2 and 3 short: 3.0 A			2 and 4 short
J11	Header for CCG1 power consumption measurement: Short: Normal operation. Open: Connect 1 and 2 to ammeter.			Short
J12	SuperSpeed USB Type-B connector (receptacle)			NA
J13	Reserved & not populated.			NA
J14	USB Type-C connector (receptacle)			NA
J15	Display port Connector			NA

4.5 Powering the Host Board

The host board by default is powered up by connecting the SuperSpeed USB connector J12 to a USB SuperSpeed cable (shipped with the board) and its other end to a 5 V (USB Type-A) source. For other options to power up the board, refer to Table 4-2 (selection for jumper J4 and J13).

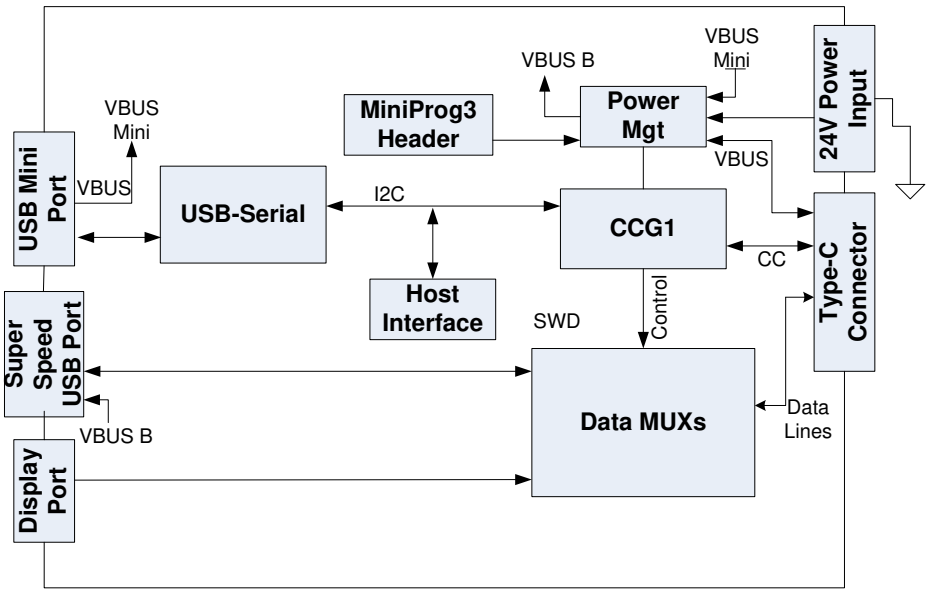
5. CCG1 Client Board

The CCG1 client board is an evaluation board that is equipped with a CCG1 (CYPD1121-40LQXI), a Type-C connector, a SuperSpeed USB port Type-A, and a DisplayPort connector. This development board supports Type-C client applications such as monitors and docking stations. This board is capable of supplying up to 100W (20V, 5A) power over the Type-C connector. It can also be used to evaluate connectivity and communication with Type-C hosts (notebooks, tablets, and mobile phones). It is primarily intended as a development vehicle for USB peripherals that house a Type-C connector. For USB PD, the board can be configured as a DFP, UFP, or DRP. The user can connect this board to a host processor or embedded controller (EC) to develop USB PD applications. The board also serves as a vehicle to evaluate the Alternate Modes for Type-C, using DisplayPort video as an example.

5.1 Block Diagram

Figure 5-1 shows the block diagram of the CCG1 client board. On the board, the CCG1 device provides a host processor interface (HPI) to a PC via a USB-Serial connection or to an external Embedded Controller (EC) and a Type-C connector for the USB PD interface. Also included is a power connector, a SuperSpeed USB port Type-B, and a DisplayPort connector to source video. The MiniProg3 device shipped with this kit can be connected to a PC to reprogram the firmware in the CCG1 device via the 5-pin programming header J8 using PSoC Programmer software from Cypress. The SuperSpeed USB signals and DisplayPort signals are delivered to the Type-C connector through a high-speed multiplexer controlled by the CCG1 device. The power to this board is connected to a circuit that allows power to be sourced from either a 5 V rail supplied by the USB Mini port, MiniProg3, 24 V power jack or VBUS that is part of the Type-C connector.

Figure 5-1. Block Diagram of CCG1 Client Board



5.2 Features

Table 5-1 lists the CCG1 client board features.

Table 5-1. CCG1 Client Board Features

Feature	Description
CCG1 part number	CYPD1121-40LQXI
CCG1 package	40-QFN
USB PD/ Type-C	Ability to support DRP, DFP, and UFP
	Type-C current set via a jumper that selects one of the three resistor Rp values, corresponding to the three Type-C currents defined in the Type-C specification.
	Supports the following PD capabilities (VSEL pins): 5 V at 5 A 12 V at 5 A 20 V at 5 A
	VBUS provider FET control for cold socket
	VBUS discharge control FET
	Rd resistor
OVP and OCP	VCONN over-current protection
	VBUS overvoltage protection
	VBUS over-current protection
Plug orientation, Detection and Alternate modes	Five MUX-select pins to select between SuperSpeed USB and 2-lane or 4-lane DisplayPort
	HPD for DisplayPort Alternate Mode operation
Configuration pin (C_SEL)	One CSEL pin to set configuration profile for firmware operation
USB Type-B Mini	USB Mini connected to USB-to-serial device
Programming	SWD pin debugging/programming using MiniProg3 device
Device detect	FW profile configured DEVICE_DETECT output pin to indicate type of device connected
Power	24 V_{DC} 5 V from USB Mini-B 5 V from MiniProg3 (used when programming CCG1 from MiniProg3) 5 V regulated from Type-C connector

5.3 Connectors and Jumper Settings

Figure 5-2 and Figure 5-3 show the CCG1 client board connectors and default jumper settings. Table 5-2 lists the jumpers and header description and default settings.

Figure 5-2. CCG1 Client Board Connectors

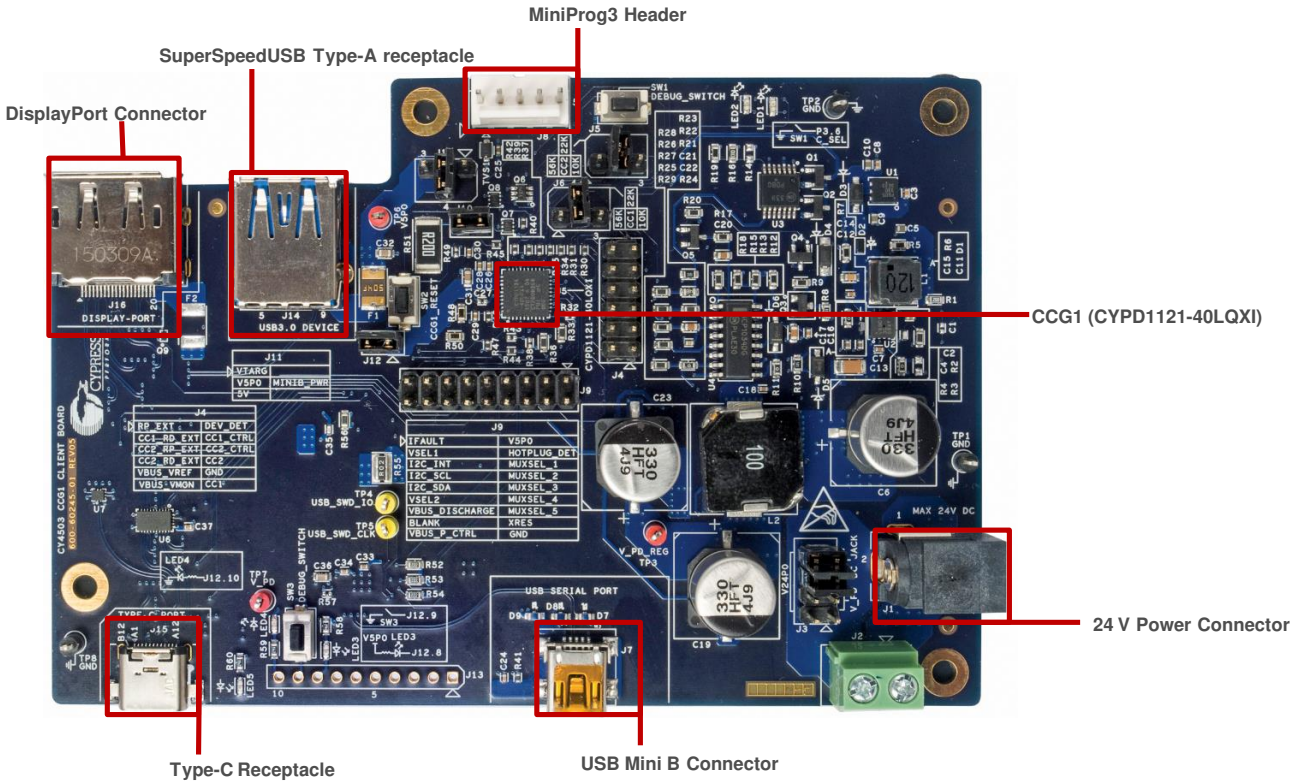


Figure 5-3. CCG1 Client Board Default Jumper Settings

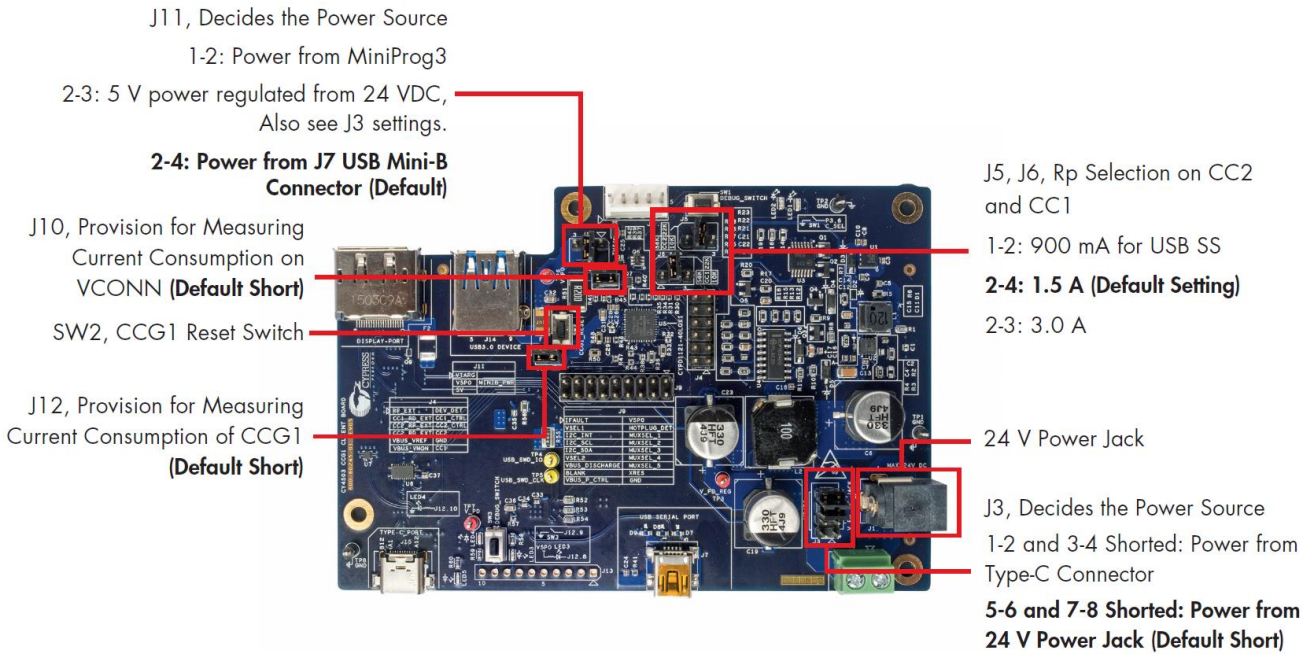


Table 5-2. CCG1 Client Board Jumper Description and Default Settings

Jumper	Description		Default
J1	Terminal Jack for 24 V supply		NA
J2	Terminal Block for 24 V supply		This jumper is not populated
J3	Jumper used to choose board power from Type-C connector and 24 V DC power jack Short 1 & 2 and 3 & 4: Power from Type-C connector Short 5 & 6 and 7 & 8: Power from 24 V power jack (Normal operation)		5 & 6 and 7 & 8 shorted
J4	Header for signal probing		NA
	Pin 1: CC1_RP_EXT	Pin 2: CCG1_DEV_DET	
	Pin 3: CC1_RD_EXT	Pin 4: CCG1_CC1_CTRL	
	Pin 5: CC2_RP_EXT	Pin 6: CCG1_CC2_CTRL	
	Pin 7: CC2_RD_EXT	Pin 8: CCG1_CC2	
	Pin 9: CCG1_VBUS_VREF	Pin 10: GND	
	Pin 11: CCG1_VBUS_VMON	Pin 12: CCG1_CC1	
J5	CC2 Rp selection for current advertisement: 1 and 2 short: 500 mA for USB 2.0, 900 mA for SuperSpeed USB (default USB current) 2 and 4 short: 1.5 A 2 and 3 short: 3.0 A		2 and 4 short
J6	CC1 Rp selection for current advertisement: 1 and 2 short: 500 mA for USB 2.0, 900 mA for SuperSpeed USB (default USB current) 2 and 4 short: 1.5 A 2 and 3 short: 3.0 A		2 and 4 short
J7	USB 2.0 Mini-B connector (receptacle)		NA
J8	Programming Header Pin 1: VTARG Pin 2: GND Pin3: CCG1_XRES Pin4: CCG1_SWD_CLK Pin5: CCG1_SWD_IO		NA
J9	Pin 1: CCG1_IFAULT	Pin 2: 5 V	NA
	Pin 3: CCG1_VSEL1	Pin 4: CCG1_HOTPLUG_DET	
	Pin 5: CCG1_I2C_INT	Pin 6: CCG1_MUXSEL_1	
	Pin 7: CCG1_I2C_SCL	Pin 8: CCG1_MUXSEL_2	
	Pin 9: CCG1_I2C_SDA	Pin 10: CCG1_MUXSEL_3	
	Pin 11: CCG1_VSEL2	Pin 12: CCG1_MUXSEL_4	
	Pin 13: CCG1_VBUS_DISCHARGE	Pin 14: CCG1_MUXSEL_5	
	Pin 15: CCG1_BLANK	Pin 16: CCG1_XRES	
	Pin 17: CCG1_VBUS_P_CTRL	Pin 18: GND	

Jumper	Description	Default
J10	Header for VCONN power consumption measurement: Short: Normal operation. Open: Connect 1 and 2 to ammeter.	Short
J11	Board power supply selection: 1 and 2 short: Select the power supply from MiniProg3 (J8). Settings on J3 can be disregarded for this configuration. 2 and 4 short: Select the power supply from J7, USB Mini-B connector. Settings on J3 can be disregarded for this configuration. 2 and 3 short: Select the power supply from regulated 5 V from 24 V power jack or Type-C connector (this is determined by jumper J3's settings)	2 and 4 short
J12	Header for CCG1 power consumption measurement: Short: Normal operation. Open: Connect 1 and 2 to ammeter.	Short
J13	USB Serial Debug Header Pin 1: SCB0_0 Pin 2: SCB0_1 Pin 3: SCB0_2 Pin 4: SCB0_3 Pin 5: SCB0_4 Pin 6: SCB0_5 Pin 7: GPIO_0 Pin 8: Connected to cathode of LED3 Pin 9: Connected to Pin2 of SW3 Pin 10: Connected to LED4 via R59	NA
J14	SuperSpeed USB Type-A connector (receptacle)	NA
J15	USB Type-C connector (receptacle)	NA
J16	Display port Connector	NA

5.4 Powering the Client Board

The client board by default is powered by connecting the USB Mini-B cable (shipped with the board) to a 5 V (USB Type–A) source. For other options to power the board, refer to Table 5-2 (selections for jumper J3 and J11).

6. CCG1 EMCA Board

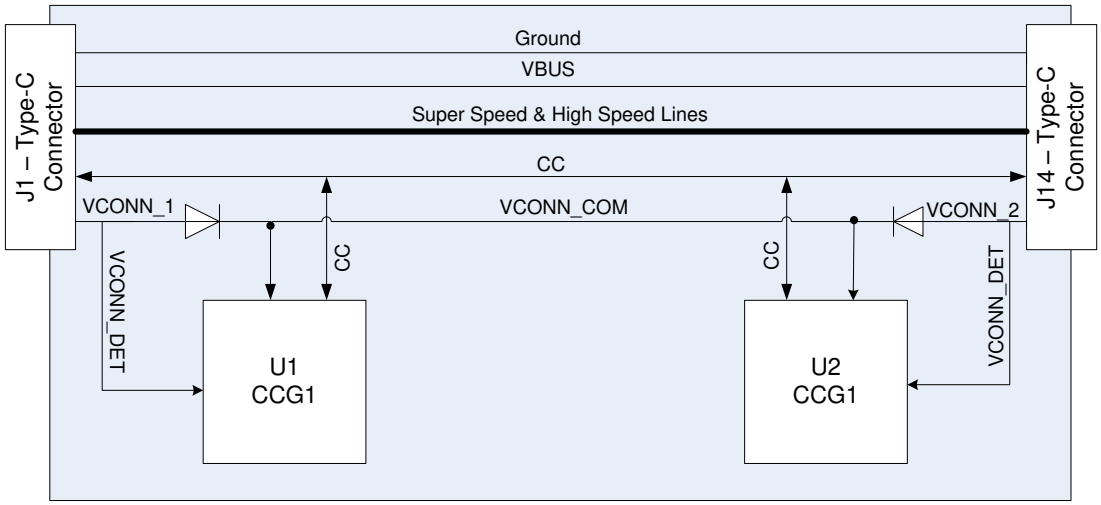
The CCG1 EMCA board is an evaluation vehicle that demonstrates the CCG1 device's capability to act as an electronic marker for cable assemblies. The board is equipped with two CCG1 devices that can demonstrate SOP' and SOP'' communication. It supports three cable configurations:

- SOP': One chip per cable (default setting)
- SOP': Two chips per cable
- SOP'/SOP'': Two chips per cable

6.1 Block Diagram

Figure 6-1 shows the CCG1 EMCA board block diagram. The CCG1 devices are connected to CC to communicate with the DFP (or the power provider) with SOP' or SOP'' packets.

Figure 6-1. CCG1 EMCA Board Block Diagram



6.2 Configurations and Jumper Settings

The CCG1 EMCA board supports three cable configurations by changing jumper settings.

Table 6-1 shows the jumper description and factory settings (default). The following subsections show the block diagrams and jumper settings for each configuration.

Table 6-1. CCG1 EMCA Board Jumper Description and Default Settings

Jumper No.	Description		Default Settings
J1, J14	Type-C connectors		NA
J2	Control disconnection of VCONN Ra resistor for J14 Type-C connector: 2 and 3 short: U1 (far end CCG1) controls disconnection of J14 VCONN Ra resistor. 1 and 2 short: U2 (near end CCG1) controls disconnection of J14 VCONN Ra resistor.		2 and 3 short
J3	Control disconnection of VCONN Ra resistor for J1 Type-C connector: 1 and 2 short: U1 (near end CCG1) controls disconnection of J1 VCONN Ra resistor. 2 and 3 short: U2 (far end CCG1) controls disconnection of J1 VCONN Ra resistor.		1 and 2 short
J4	U2 CC line connection: 1 and 2 short: U2 connects to CC. 1 and 2 open: U2 disconnects from CC.		Open
J5	This jumper is used to measure VCONN power consumption. This jumper must be shorted in all configurations.		1 and 2 short
J6	U1 VDD (power) selection: Short 1 and 2: U1 VDD connects to VCONN_COM. Short 2 and 3: U1's VDD connects to J1's (Type-C connector) VCONN		1 and 2 short
J7	U2 VDD (power) selection: Short 1 and 2: U2 VDD connects to VCONN_COM. Short 2 and 3: U2 VDD connects to J14's (Type-C connector) VCONN.		Open
J8	MiniProg3 SWD programming connector for programming U1 CCG1		NA
J9	MiniProg3 SWD programming connector for programming U2 CCG1		NA
J10	U2 – Check the status of VCONN_DET (J14): 1 and 2 short: Check the status of VCONN_DET (J14) to decide whether to respond to SOP' or SOP". 1 and 2 open: Do not check the status of VCONN_DET (J14) and respond to SOP' only.		Open
J11	U1 – Check the status of VCONN_DET (J1): 1 and 2 short: Check the status of VCONN_DET (J1) to decide whether to respond to SOP' or SOP". 1 and 2 open: Do not check the status of VCONN_DET (J1) and respond to SOP' only.		Open
J12 (for U1 device) and J13 (for U2 device)	Debug Headers		NA
	Pin 1: Ux_GPIO_P4.3	Pin 2: Ux_GPIO_P2.6	
	Pin 3: Ux_GPIO_P4.2	Pin 4: Ux_GPIO_P2.5	
	Pin 5: Ux_GPIO_P0.5	Pin 6: Ux_I2C_SDA	
	Pin 7: Ux_GPIO_P0.6	Pin 8: Ux_I2C_SCL	
	Pin 9: Ux_GPIO_P3.4	Pin 10: Ux_GPIO_P1.7	
	Pin 11: Ux_GPIO_P3.1	Pin 12: NC	
	Pin 13: Ux_GPIO_P1.6	Pin 14: NC	
	Pin 15: Ux_GPIO_P3.0	Pin 16: Ux_TXEN_P0.2`	
	Pin 17: Ux_GPIO_P2.7	Pin 18: GND	

6.2.1 SOP' One-Chip/Cable Configuration

This configuration is the factory default setting, as shown in Figure 6-2. In this configuration, only one CCG1 device (U1) is connected to the CC line and VCONN (power). U2 is disconnected from both CC line and VCONN. The CCG1 EMCA board communicates with the DFP through SOP' packets only. Figure 6-3 and Table 6-2 show the jumper settings for this configuration. In this configuration, the VCONN signal must route through the cable.

Figure 6-2. SOP' One-Chip/Cable Configuration Block Diagram

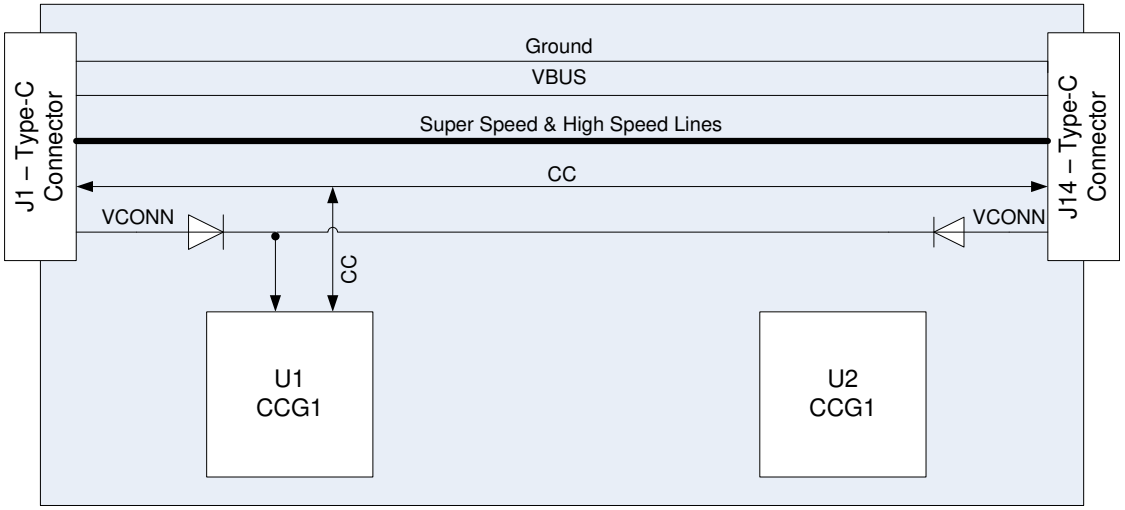


Figure 6-3. Jumper Settings for SOP' One-Chip/Cable Configuration

Table 6-2. Jumper Settings for SOP' One-Chip/Cable Configuration

Jumper No.	Jumper Settings for SOP' One-Chip/Cable Configuration
J2	2 and 3 short
J3	1 and 2 short
J4, J7, J10, J11	Open
J5	1 and 2 short
J6	1 and 2 short

6.2.2 SOP' Two-Chip/Cable Configuration

This configuration allows either of the CCG1 devices to communicate with SOP' packets, depending on which Type-C connector provides VCONN. Figure 6-4 shows the block diagram of this configuration. If VCONN is available at the J1 Type-C connector, the U1 CCG1 device will communicate via SOP' packets and the U2 CCG1 device will not be powered. Similarly, if VCONN is available at the J14 Type-C connector, the U2 CCG1 device will communicate via SOP' packets and the U1 CCG1 device will not be powered. Figure 6-5 and Table 6-3 show the jumper settings for this configuration. In this configuration, VCONN does not need to route through the cable.

Figure 6-4. SOP' Two-Chip/Cable Configuration Block Diagram

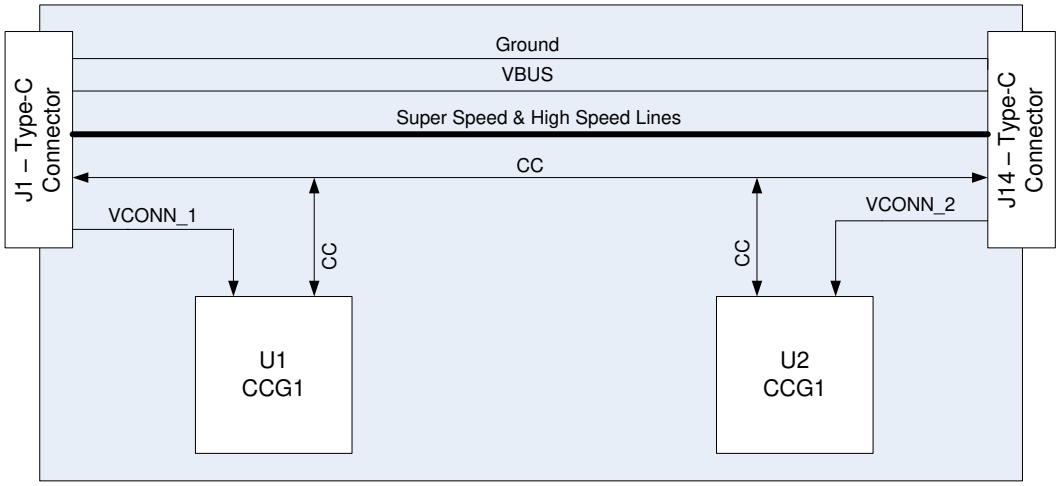


Figure 6-5. Jumper Settings for SOP' Two-Chip/Cable Configuration

Table 6-3. Jumper Settings for SOP' Two-Chip/Cable Configuration

Jumper No.	Jumper Settings for SOP' Two-Chip/Cable Configuration
J2, J3, J4, J5	1 and 2 short
J6	2 and 3 short
J7	2 and 3 short
J10	Open
J11	1 and 2 short

6.2.3 SOP'/SOP'' Two-Chip/Cable Configuration

In this configuration, one of the CCG1 devices communicates with SOP' packets, and the other communicates with SOP'' packets. Figure 6-6 shows the block diagram. In this configuration, one of the CCG1 devices detects the availability of VCONN; the CCG1 device that detects VCONN will communicate with SOP' packets. The CCG1 device that does not detect VCONN will communicate with SOP'' packets. For example, in Figure 6-6, if the U1 CCG1 detects that VCONN is available at the J1 Type-C connector, the U1 CCG1 will communicate with SOP' packets and the U2 CCG1 will communicate with SOP'' packets. Figure 6-7 and Table 6-4 show the jumper settings for this configuration.

Figure 6-6. SOP'/SOP'' Two-Chip/Cable Configuration Block Diagram

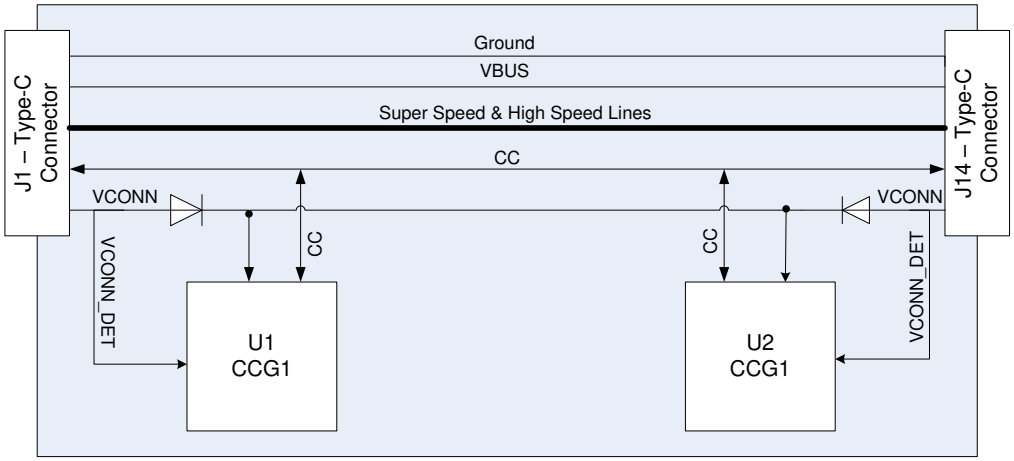


Figure 6-7. Jumper Settings for SOP'/SOP'' Two-Chip/Cable Configuration

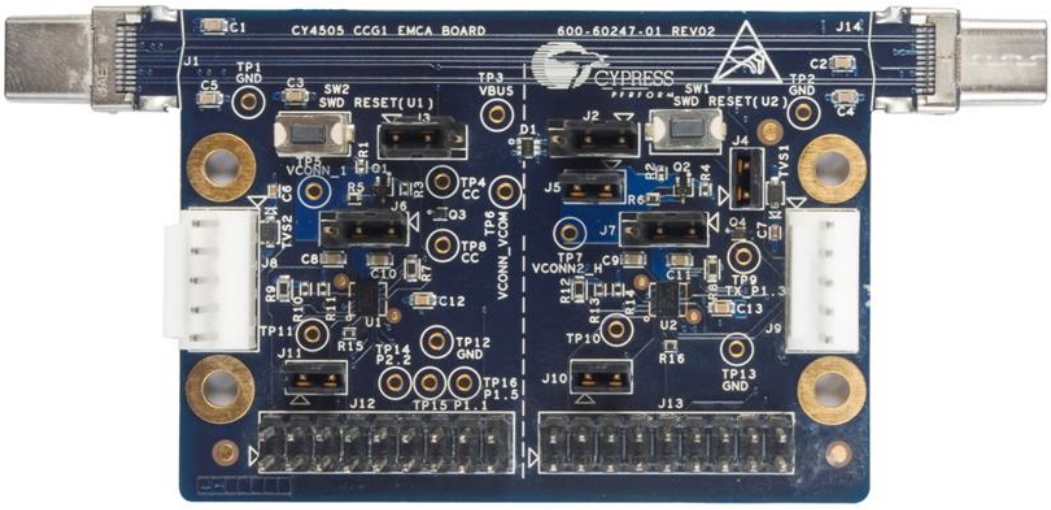


Table 6-4. Jumper Settings for SOP'/SOP'' Two-Chip/Cable Configuration

Jumper No.	Jumper Settings for SOP'/SOP'' Two-Chip/Cable Configuration
J2	1 and 2 short
J3	1 and 2 short
J4	1 and 2 short
J5	1 and 2 short
J6	1 and 2 short
J7	1 and 2 short
J10	1 and 2 short
J11	1 and 2 short