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CY62167DV30 MoBL®

16-Mbit (1 M × 16) Static RAM

Features

- Thin small outline package (TSOP-I) configurable as 1 M × 16 or as 2 M × 8 SRAM
- Wide voltage range: 2.2 V–3.6 V
- Ultra-low active power:
  Typical active current: 2 mA at f = 1 MHz
- Ultra-low standby power
- Easy memory expansion with $\overline{CE}_1$, CE_2 and $\overline{OE}$ features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed / power
- Available in Pb-free and non Pb-free 48-ball very fine-pitch ball grid array (VFBGA) and 48-pin TSOP I package

Functional Description

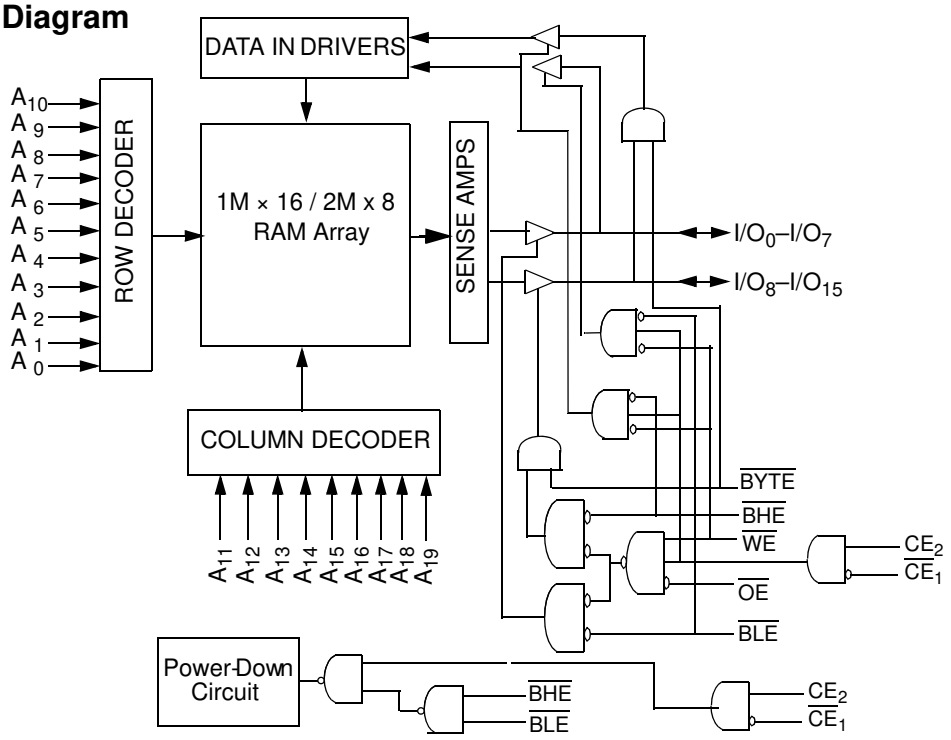
The CY62167DV30 is a high-performance CMOS static RAM organized as 1M words by 16-bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a Write operation ($\overline{CE}_1$ LOW, CE_2 HIGH and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{19}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{19}).

Reading from the device is accomplished by taking Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appear on I/O_8 to I/O_{15}. See the truth table at the back of this data sheet for a complete description of Read and Write modes.

For a complete list of related documentation, click here.

Logic Block Diagram



Contents

Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC}(mA)				Standby I_{SB2}(µA)	
					f = 1 MHz		f = f_{Max}			
	Min	Typ [1]	Max		Typ [1]	Max	Typ [1]	Max	Typ [1]	Max
CY62167DV30LL	2.2	3.0	3.6	55	2	4	15	30	2.5	22
				70			12	25		

Pin Configurations

Figure 1. 48-ball VFBGA pinout (Top View) [2, 3]

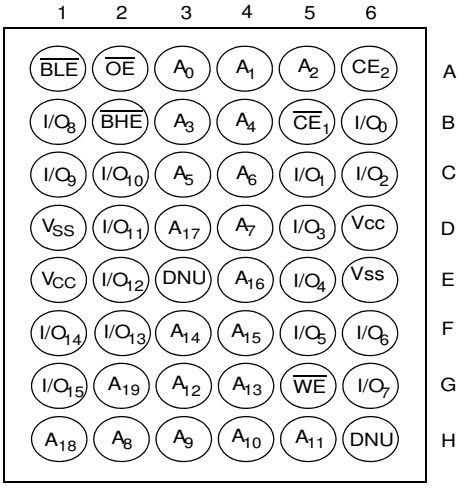
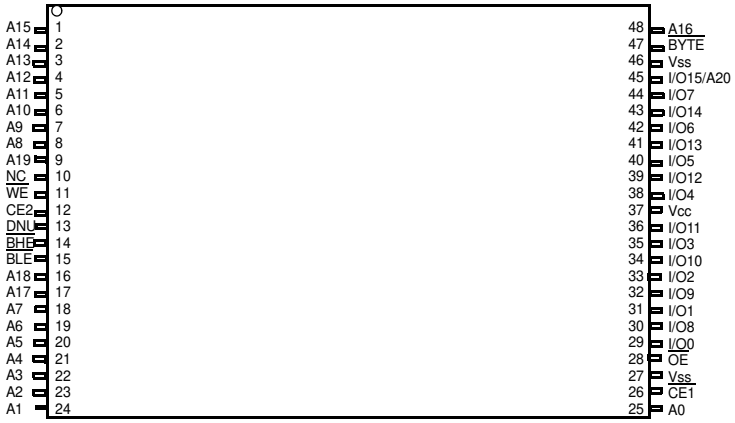


Figure 2. 48-pin TSOP I pinout (Top View) [4]



Notes
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ.)}$, T_A = 25 °C.
2. NC pins are not connected on the die.
3. DNU pins have to be left floating.
4. The BYTE pin in the 48-TSOP I package has to be tied to V_{CC} to use the device as a 1M X 16 SRAM. The 48-TSOP I package can also be used as a 2 M × 8 SRAM by tying the BYTE signal to V_{SS}. In the 2 M × 8 configuration, Pin 45 is A20, while BHE, BLE and I/O8 to I/O14 pins are not used (DNU).

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential ..... –0.2 V to V_{CC} + 0.3 V

DC voltage applied to outputs in High-Z state [5, 6] ..... –0.2 V to V_{CC} + 0.3 V

DC input voltage [5, 6] ..... –0.2 V to V_{CC} + 0.3 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[7]
CY62167DV30LL	Industrial	–40 °C to +85 °C	2.20 V to 3.60 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		CY62167DV30-55			CY62167DV30-70			Unit
				Min	Typ [8]	Max	Min	Typ [8]	Max	
V_{OH}	Output HIGH voltage	I_{OH} = –0.1 mA	V_{CC} = 2.20 V	2.0	–	–	2.0	–	–	V
		I_{OH} = –1.0 mA	V_{CC} = 2.70 V	2.4			2.4			
V_{OL}	Output LOW voltage	I_{OL} = 0.1 mA	V_{CC} = 2.20 V	–	–	0.4		–	0.4	V
		I_{OL} = 2.1 mA	V_{CC} = 2.70 V							
V_{IH}	Input HIGH voltage	V_{CC} = 2.2 V to 2.7 V		1.8	–	V_{CC} + 0.3	1.8	–	V_{CC} + 0.3	V
		V_{CC} = 2.7 V to 3.6 V		2.2			2.2			
V_{IL}	Input LOW voltage	V_{CC} = 2.2 V to 2.7 V		–0.3	–	0.6	–0.3	–	0.6	V
		V_{CC}= 2.7 V to 3.6 V				0.8			0.8	
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	–	+1	–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, output disabled		–1	–	+1	–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	V_{CC} = $V_{CC(max)}$ I_{OUT} = 0 mA CMOS levels	f = f_{Max} = $1/t_{RC}$	–	15	30	–	12	25	mA
			f = 1 MHz		2	4		2	4	
I_{SB1}	Automatic power-down current – CMOS inputs	$\overline{CE_1}$ ≥ V_{CC} – 0.2 V or CE_2 ≤ 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V, V_{IN} ≤ 0.2 V, f = f_{Max} (address and data only), f = 0 ($\overline{OE}$, $\overline{WE}$), V_{CC} = 3.60 V		–	2.5	22	–	2.5	22	µA
I_{SB2}	Automatic power-down current – CMOS Inputs	$\overline{CE_1}$ ≥ V_{CC} – 0.2 V or CE_2 ≤ 0.2 V V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2V, f = 0, V_{CC} = 3.60 V		–	2.5	22	–	2.5	22	µA

Notes
5. $V_{IL(min.)}$ = –2.0 V for pulse durations less than 20 ns.
6. $V_{IH(max)}$ = V_{CC} + 0.75 V for pulse durations less than 20 ns.
7. Full Device AC operation requires linear V_{CC} ramp from 0 to $V_{CC(min.)}$ and V_{CC} must be stable at $V_{CC(min)}$ for 500 µs.
8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.

Capacitance

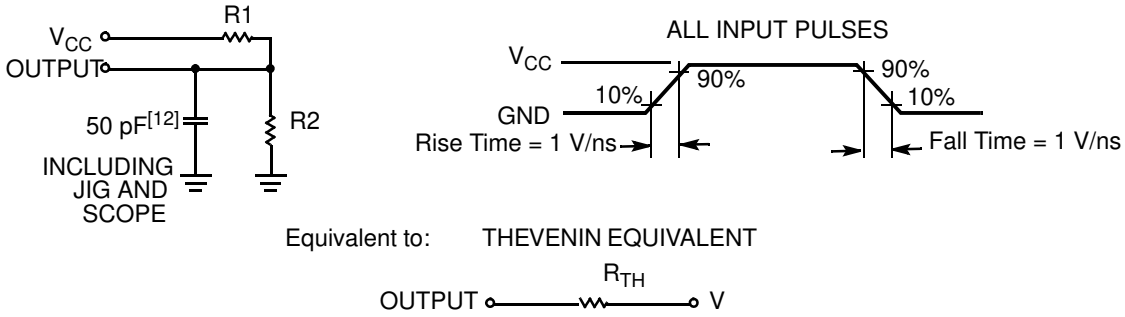
Parameter [10]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	8	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [10]	Description	Test Conditions	VFBGA	TSOP I	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, 2-layer printed circuit board	55	60	°C/W
θ_{JC}	Thermal resistance (junction to case)		16	4.3	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Parameters	2.5 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

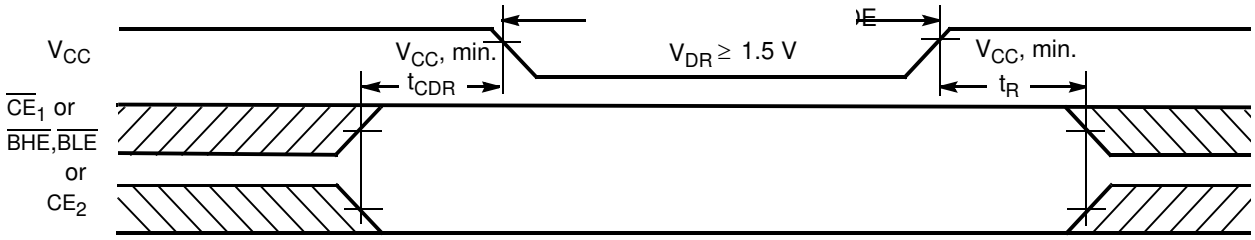
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions		Min	Typ [9]	Max	Unit
V_{DR}	V_{CC} for data retention			1.5	–	–	V
I_{CCDR}	Data retention current	V_{CC} = 1.5 V, $\overline{CE_1} \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V		–	–	10	µA
t_{CDR}[10]	Chip deselect to data retention time			0	–	–	ns
t_R[11]	Operation recovery time		CY62167DV30LL-55	55	–	–	ns
			CY62167DV30LL-70	70			

Data Retention Waveform

Figure 4. Data Retention Waveform [12]



Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
10. Tested initially and after any design or process changes that may affect these parameters.
11. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs.
12. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Over the Operating Range

Parameter [13]	Description	55 ns		70 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	55	–	70	–	ns
t_{AA}	Address to data valid	–	55	–	70	ns
t_{OHA}	Data hold from address change	10	–	10	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid	–	55	–	70	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	25	–	35	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [14]	5	–	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [14, 15]	–	20	–	25	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to low Z [14]	10	–	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to high Z [14, 15]	–	20	–	25	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to power-up	0	–	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to power-down	–	55	–	70	ns
t_{DBE}	BLE/BHE LOW to data valid	–	55	–	70	ns
t_{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to low Z [14]	10	–	10	–	ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to high Z [14, 15]	–	20	–	25	ns
Write Cycle [16]						
t_{WC}	Write cycle time	55	–	70	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	40	–	60	–	ns
t_{AW}	Address setup to write end	40	–	60	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	40	–	45	–	ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to write end	40	–	60	–	ns
t_{SD}	Data setup to write end	25	–	30	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high-Z [14, 15]	–	20	–	25	ns
t_{LZWE}	$\overline{WE}$ HIGH to low-Z [14]	10	–	10	–	ns

Notes

13. Test conditions for all parameters other than Tri-state parameters assume signal transition time of 1 ns/V, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the “AC Test Loads and Waveforms” section.
14. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
15. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
16. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the Write.

Switching Waveforms

Figure 5. Read Cycle 1 (Address Transition Controlled) [17, 18]

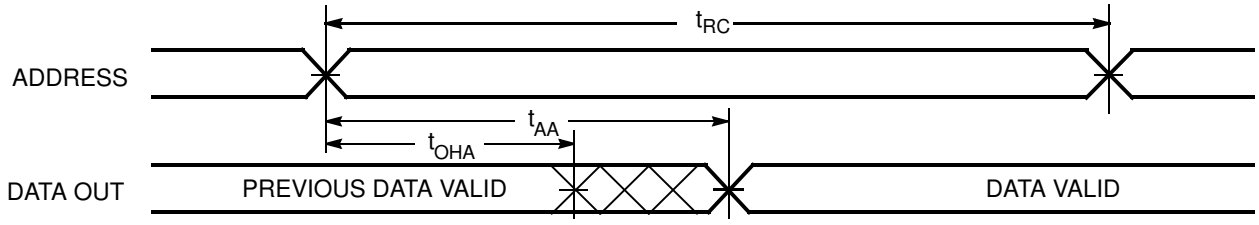
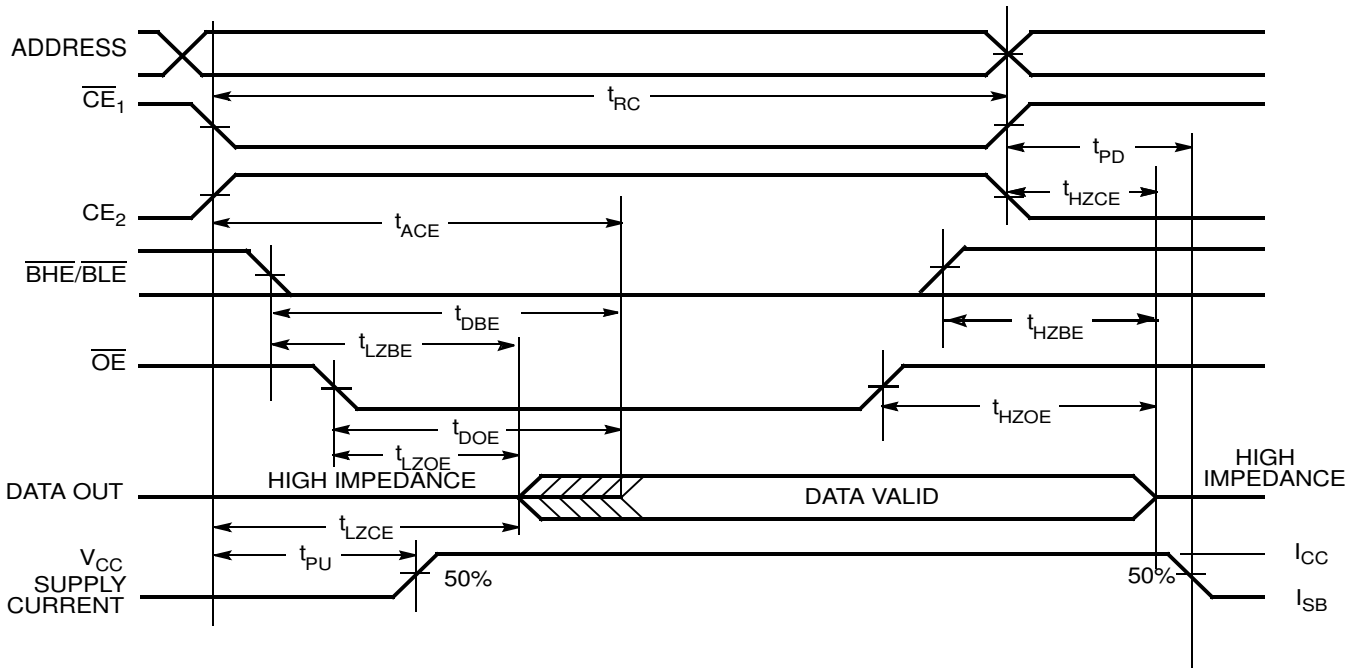


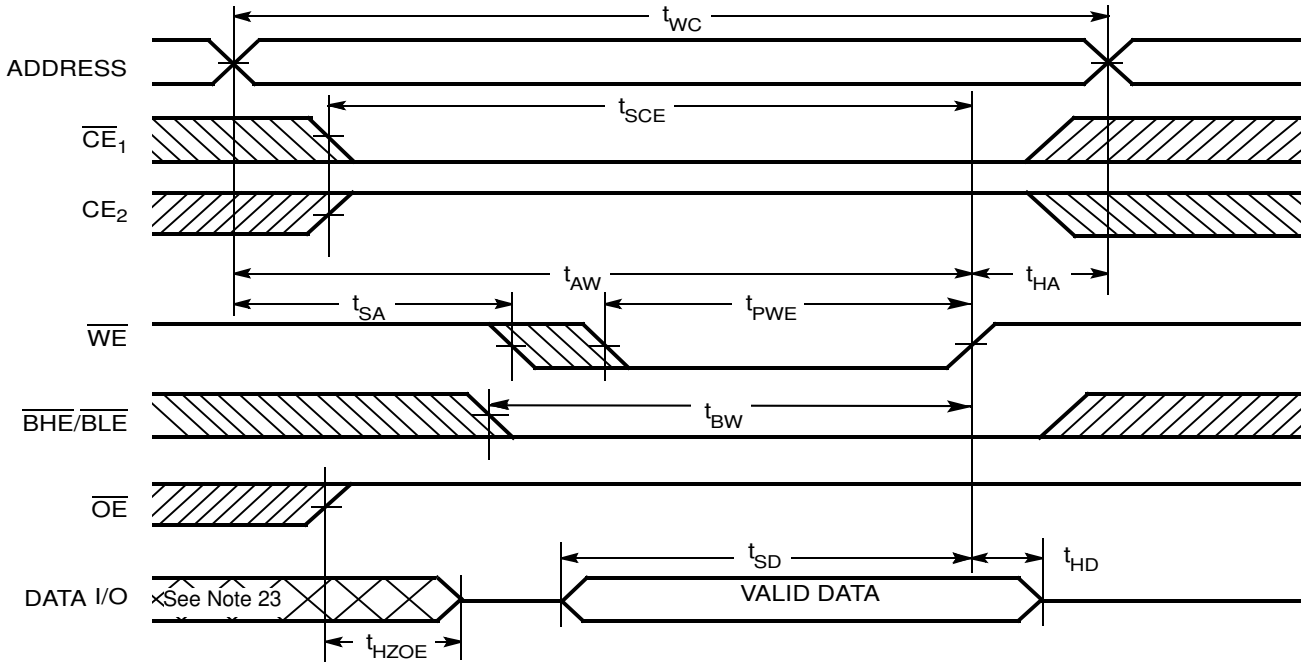
Figure 6. Read Cycle 2 ($\overline{OE}$ Controlled) [18, 19]



Notes
17. The device is continuously selected. $\overline{OE}$, $\overline{CE_1} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$.
18. $\overline{WE}$ is HIGH for read cycle.
19. Address valid prior to or coincident with $\overline{CE_1}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 7. Write Cycle 1 ($\overline{WE}$ Controlled) [20, 21, 22]



Notes

20. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE_1}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the Write.
21. Data I/O is high-impedance if $\overline{OE}$ = V_{IH}.
22. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high-impedance state.
23. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 8. Write Cycle 2 ($\overline{CE}_1$ or CE_2 Controlled) [24, 25, 26]

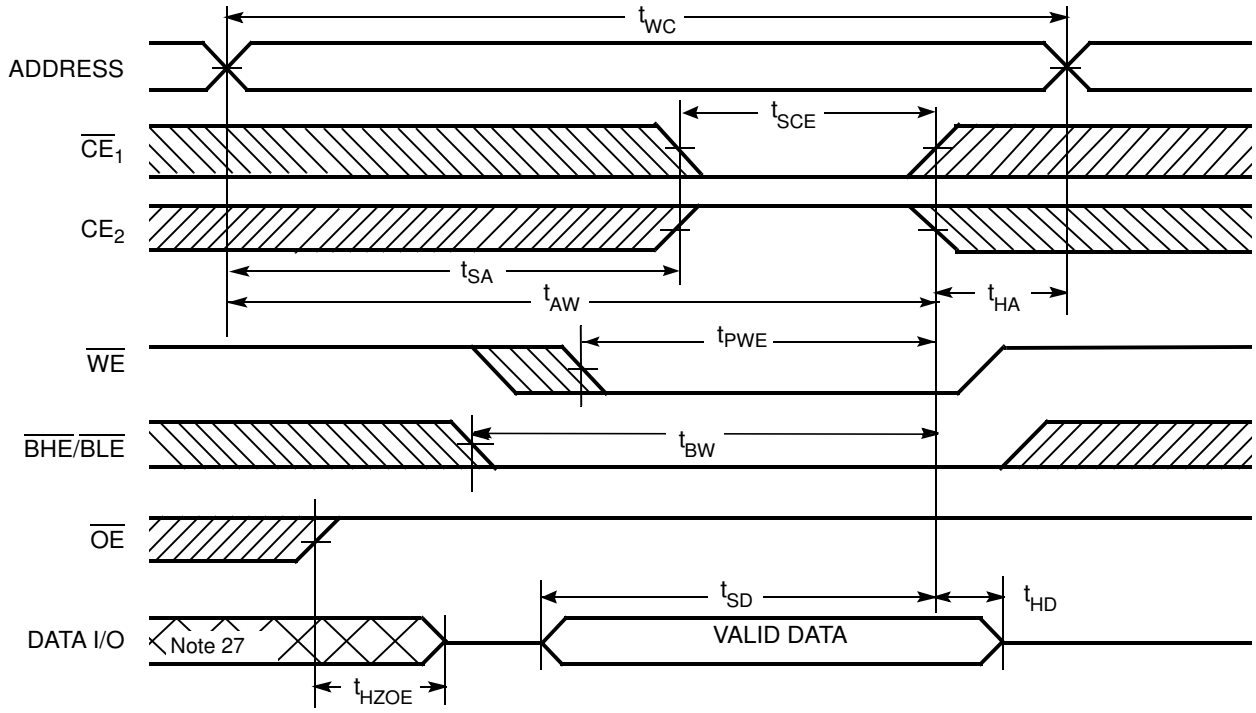
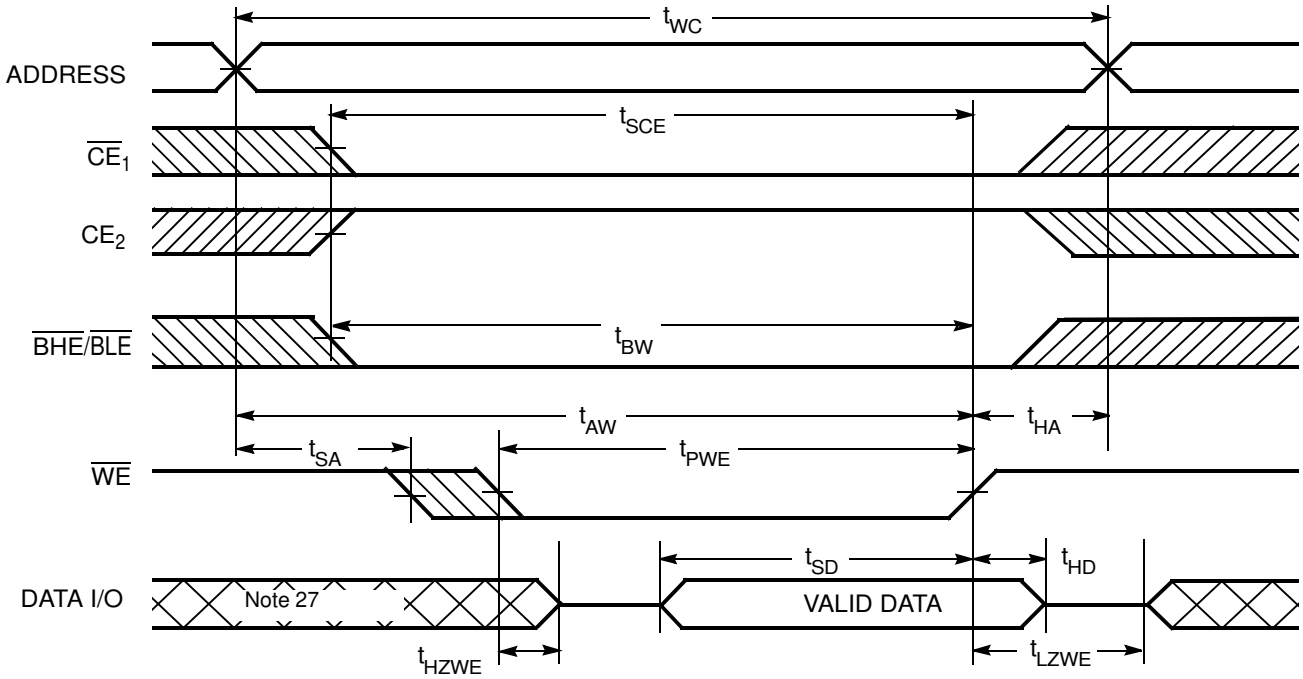


Figure 9. Write Cycle 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [26]

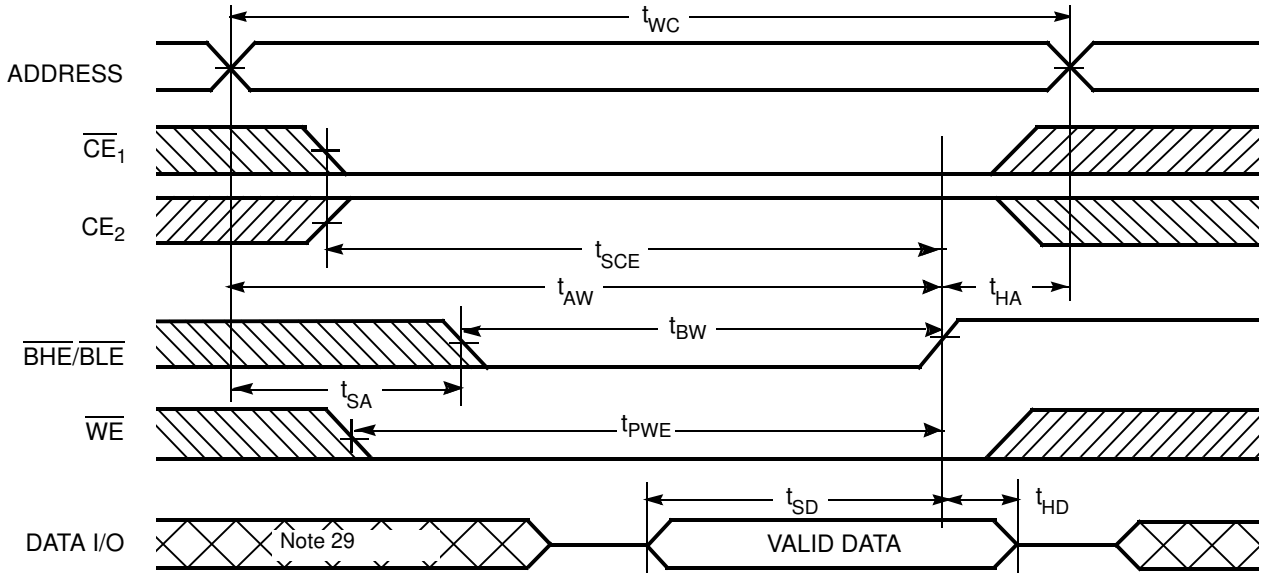


Notes

24. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the Write.
25. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
26. If $\overline{CE}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high-impedance state.
27. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 10. Write Cycle 4 ($\overline{BHE}$/$\overline{BLE}$ Controlled, $\overline{OE}$ LOW) [28]



Notes
28. If $\overline{CE}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high-impedance state.
29. During this period, the I/Os are in output state and input signals should not be applied.

Truth Table

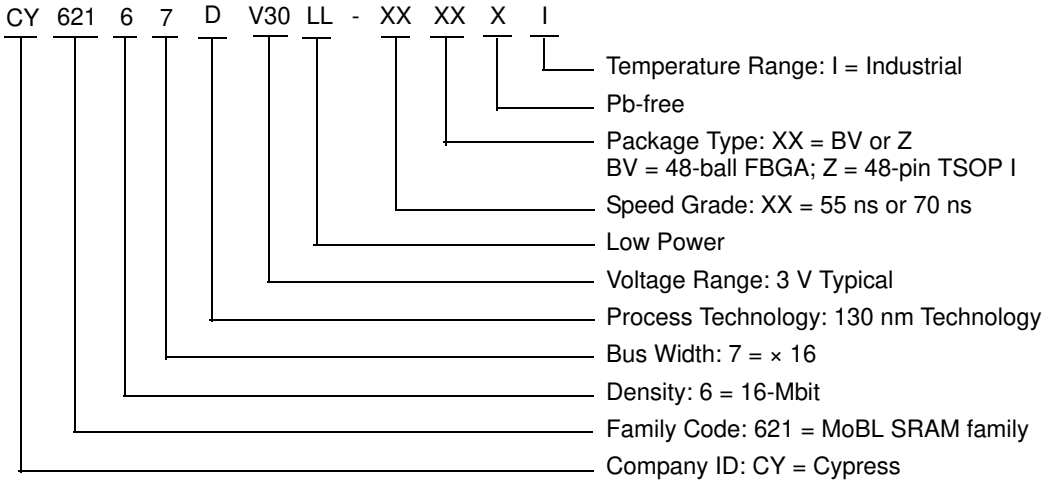
$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X	L	X	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X	X	X	X	H	H	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	L	L	Data out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	High Z (I/O_8–I/O_{15}); Data out (I/O_0–I/O_7)	Read	Active (I_{CC})
L	H	H	L	L	H	Data out (I/O_8–I/O_{15}); High Z (I/O_0–I/O_7)	Read	Active (I_{CC})
L	H	L	X	L	L	Data in (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	High Z (I/O_8–I/O_{15}); Data in (I/O_0–I/O_7)	Write	Active (I_{CC})
L	H	L	X	L	H	Data in (I/O_8–I/O_{15}); High Z (I/O_0–I/O_7)	Write	Active (I_{CC})
L	H	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62167DV30LL-55BVI	51-85178	48-ball FBGA (8 × 9.5 × 1 mm)	Industrial
	CY62167DV30LL-55BVXI		48-ball FBGA (8 × 9.5 × 1 mm) Pb-free	
	CY62167DV30LL-55ZXI	51-85183	48-pin TSOP I (12 × 18.4 × 1 mm) Pb-free	
70	CY62167DV30LL-70BVI	51-85178	48-ball FBGA (8 × 9.5 × 1 mm)	

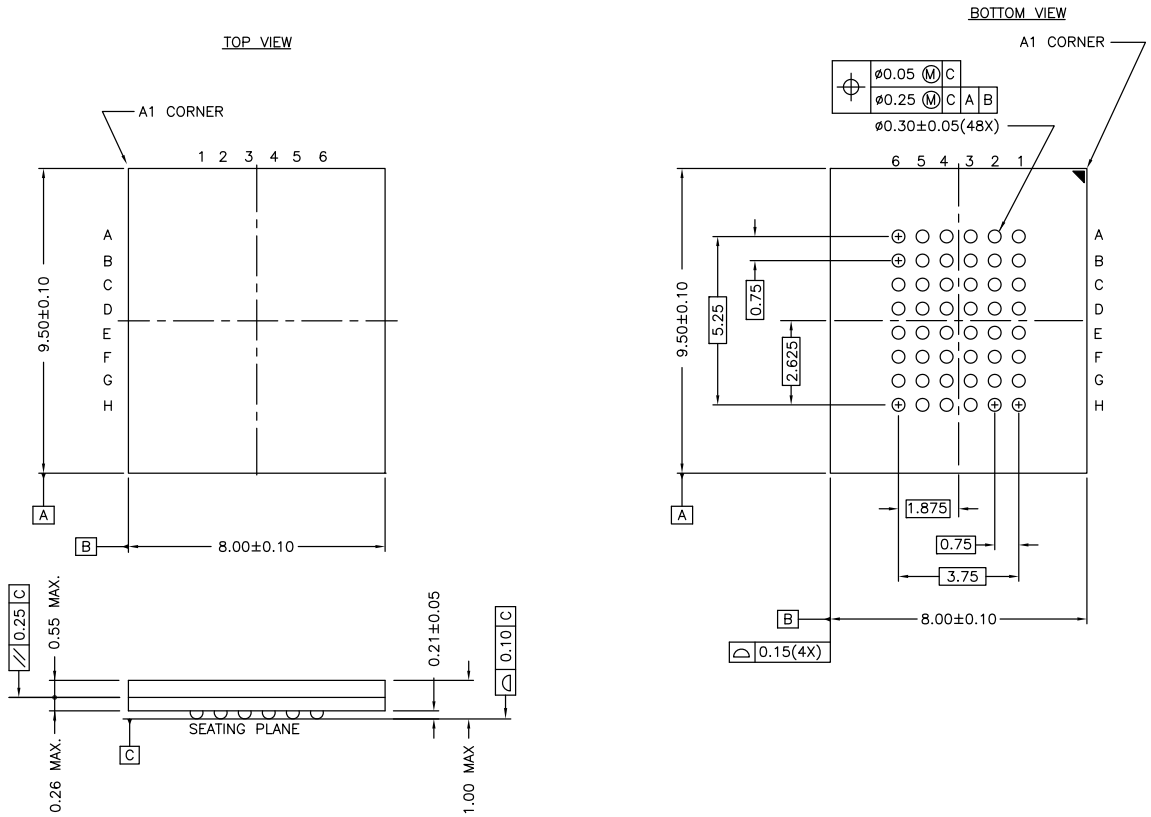
Please contact your local Cypress sales representative for availability of these parts

Ordering Code Definitions



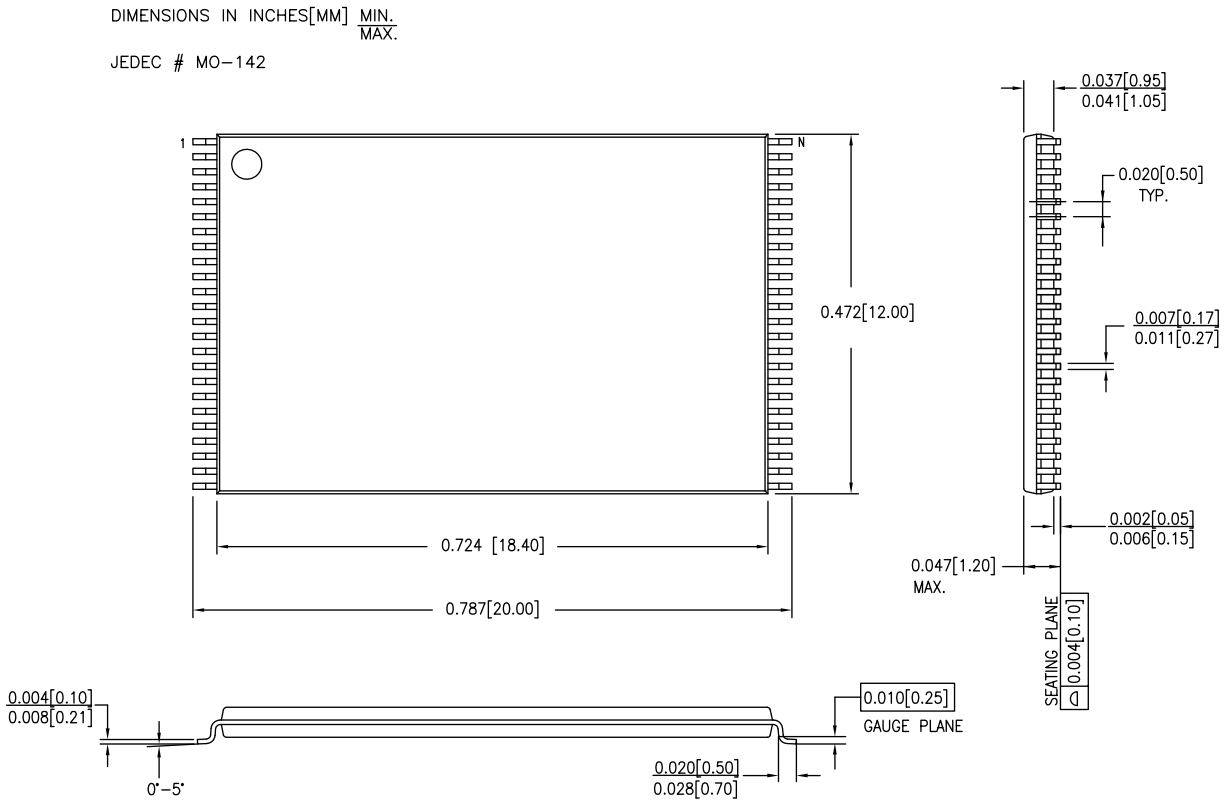
Package Diagrams

Figure 11. 48-ball VFBGA (8 × 9.5 × 1 mm) BV48B Package Outline, 51-85178



Package Diagrams (continued)

Figure 12. 48-pin TSOP I (12 × 18.4 × 1 mm) Z48A Package Outline, 51-85183



Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62167DV30 MoBL®, 16-Mbit (1 M × 16) Static RAM Document Number: 38-05328				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	118408	GUG	09/30/02	New data sheet.
*A	123692	DPM	02/11/03	Changed status from Advanced to Preliminary. Added package diagram
*B	126555	DPM	04/25/03	Minor change: Changed Sunset Owner from DPM to HRT
*C	127841	XRJ	09/10/03	Added 48 TSOP I package
*D	205701	AJU	See ECN	Changed $\overline{\text{BYTE}}$ pin usage description for 48 TSOPI package
*E	238050	KKV/AJU	See ECN	Replaced 48-ball VFBGA package diagram; Modified Package Name in Ordering Information table from BV48A to BV48B
*F	304054	PCI	See ECN	Added 45-ns Speed Bin in AC, DC and Ordering Information tables Added Footnote #12 on page #4 Added Pb-free packages on page # 10
*G	492895	VKN	See ECN	Modified datasheet to explain x8 configurability. Removed L power bin from the product offering Updated Ordering Information Table
*H	2896036	AJU	03/19/10	Removed 45-ns. Removed inactive parts from Ordering Information. Updated Packaging Information Updated links in Sales, Solutions, and Legal Information.
*I	3067267	RAME	11/08/10	Updated datasheet as per new template Added Ordering Code Definitions. Added Acronyms and Units of Measure. Updated all table notes to footnote. Package diagram updated 51-85178 from ** to *A
*J	3329789	RAME	07/27/11	Removed references to AN1064 SRAM system guidelines. Updated template according to current CY standards.
*K	4108382	AJU	08/29/2013	Updated Pin Configurations: Removed the note “Ball H6 for the FBGA package can be used to upgrade to a 32M density” and its reference in Figure 1. Updated Package Diagrams: spec 51-85178 – Changed revision from *A to *C. Updated in new template.
*L	4192919	VINI	11/15/2013	No technical updates. Completing Sunset Review.
*M	4574377	VINI	11/19/2014	Added related documentation hyperlink in page 1.

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