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CY62167DV30 MoBL[®] 16-Mbit (1 M × 16) Static RAM

Features

- Thin small outline package (TSOP-I) configurable as 1 M × 16 or as 2 M × 8 SRAM
- Wide voltage range: 2.2 V–3.6 V
- Ultra-low active power: Typical active current: 2 mA at f = 1 MHz
- Ultra-low standby power
- **Easy** memory expansion with \overline{CE}_1 , CE_2 and \overline{OE} features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed / power
- Available in Pb-free and non Pb-free 48-ball very fine-pitch ball grid array (VFBGA) and 48-pin TSOP I package

Functional Description

The CY62167DV30 is a high-performance CMOS static RAM organized as 1M words by 16-bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life[™] (MoBL[®]) in portable applications such as cellular telephones. The device also has an

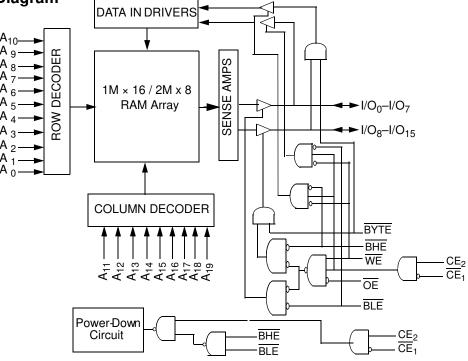
automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected (\overline{CE}_1 HIGH or CE_2 LOW or both BHE and BLE are HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected (\overline{CE}_1 HIGH or CE_2 LOW), outputs are disabled (\overline{OE} HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or during a Write operation (\overline{CE}_1 LOW, CE_2 HIGH and WE LOW).

<u>Writing</u> to the device is accomplished by taking Chip Enables $(\overline{CE}_1 \text{ LOW} \text{ and } CE_2 \text{ HIGH})$ and Write Enable (WE) input LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₉). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₉).

<u>Reading</u> from the device is accomplished by taking Chip Enables $(\overline{CE}_1 \text{ LOW} \text{ and } CE_2 \text{ HIGH})$ and Output Enable $(\overline{OE}) \text{ LOW}$ while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7 . If Byte High Enable (BHE) is LOW, then data from memory appear on I/O_8 to I/O_{15} . See the truth table at the back of this data sheet for a complete description of Read and Write modes.

For a complete list of related documentation, click here.

Logic Block Diagram



Cypress Semiconductor Corporation Document Number: 38-05328 Rev. *M 198 Champion Court

San Jose, CA 95134-1709 • 408-943-2600 Revised November 19, 2014



CY62167DV30 MoBL[®]

Contents

Product Portfolio	3
Pin Configurations	
Maximum Ratings	
Operating Range	
Electrical Characteristics	
Capacitance	5
Thermal Resistance	
AC Test Loads and Waveforms	
Data Retention Characteristics	
Data Retention Waveform	
Switching Characteristics	
Switching Waveforms	
Truth Table	

Ordering Information	13
Ordering Code Definitions	13
Package Diagrams	14
Acronyms	16
Document Conventions	16
Units of Measure	
Document History Page	
Sales, Solutions, and Legal Information	
Worldwide Sales and Design Support	
Products	
PSoC® Solutions	
Cypress Developer Community	
Technical Support	



Product Portfolio

					Power Dissipation						
Product	V	_{CC} Range (V)	Speed				Standby			
FIGUUCI				(ns) $f = 1 \text{ MHz}$ $f = f_{Max}$		f = 1 MHz f = f _{Max}				'SB2(µ~)	
	Min	Тур [1]	Max		Тур [1]	Max	Тур [1]	Мах	Тур [1]	Max	
CY62167DV30LL	2.2	3.0	3.6	55	2	4	15	30	2.5	22	
				70			12	25			

Pin Configurations

Figure 1. 48-ball VFBGA pinout (Top View) ^[2, 3]

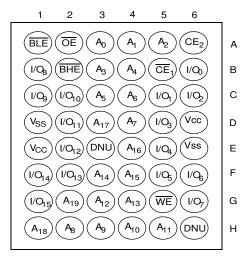


Figure 2. 48-pin TSOP I pinout (Top View)^[4]

	10
A15 = 1	48 – <u>A16</u>
A14 a 2 A13 a 3	47 BYTE
A13 🗖 3	46 🗖 Vss
A12 🗖 4	45 🗖 I/O15/A20
A11 🖬 5	46 = Vss 45 = V015/A20 44 = V07
A10 🖬 6	43 🗖 1/014
A11 🖬 5 A10 🖬 6 A9 🖬 7	42 🗖 1/06
A8 🗖 8	41 = I/O13
A19 🖬 9	40 🖬 1/05
NC 🖬 10	40 = 1/05 39 = 1/012
NC = 10 WE = 11	38 🗖 1/04
CE2 12	37 🗖 Vcc
DNU= 13	36 🗖 1/011
BHB= 14	35 🗖 1/03
BLE = 15	35 = 1/03 34 = 1/010 33 = 1/02
A18 🗖 16	33 🗖 1/02
A17 = 17	32 🖬 1/09
A7 🗖 18	31 = 1/01
A6 🗖 19	30 🗖 1/08
A5 🗖 20	29 1/00
A4 🗖 21	29 = <u>1/00</u> 28 = OE
A3 🗖 22	27 Ves
A2 = 23	27 = <u>Vss</u> 26 = CE1
A1 2 4	25 = A0
AI 24	25 AU

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25 °C.
- 2. NC pins are not connected on the die.
- DNU pins have to be left floating.
 DNU pins have to be left floating.
 The BYTE pin in the 48-TSOP I package has to be tied to V_{CC} to use the device as <u>a 1M X 16</u> SRAM. The 48-TSOP I package can also be used as a 2 M × 8 SRAM by tying the BYTE signal to V_{SS}. In the 2 M × 8 configuration, Pin 45 is A20, while BHE, BLE and I/O8 to I/O14 pins are not used (DNU).



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature65 °C to +1	50 °C
Ambient temperature with power applied55 °C to +1	25 °C
Supply voltage to ground potential \dots –0.2 V to V _{CC} +	0.3 V
DC voltage applied to outputs in High-Z state $^{[5,\ 6]}$ 0.2 V to V_{CC} +	0.3 V
DC input voltage $^{[5,\ 6]}$ 0.2 V to V _{CC} +	0.3 V
Output current into outputs (LOW)2	20 mA

Static discharge voltage	
(per MIL-STD-883, Method 3015)	> 2001 V
Latch-up current	> 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} ^[7]
CY62167DV30LL	Industrial	–40 °C to +85 °C	2.20 V to 3.60 V

Electrical Characteristics

Over the Operating Range

Deremeter	Description	Test Conditions		CY62167DV30-55			CY62167DV30-70			L locit
Parameter	Description	lest Col			Typ ^[8]	Max	Min	Typ ^[8]	Max	Unit
V _{OH}	Output HIGH voltage	I _{OH} = -0.1 mA	$V_{CC} = 2.20 V$	2.0	-	-	2.0	-	_	V
		I _{OH} = -1.0 mA	$V_{CC} = 2.70 V$	2.4			2.4			
V _{OL}	Output LOW voltage	I _{OL} = 0.1 mA	V _{CC} = 2.20 V	-	-	0.4		-	0.4	V
		I _{OL} = 2.1 mA	V _{CC} = 2.70 V							
V _{IH}	Input HIGH voltage	$V_{CC} = 2.2 V \text{ to } 2$	2.7 V	1.8	-	$V_{CC} + 0.3$	1.8	-	V _{CC} + 0.3	V
		$V_{CC} = 2.7 V \text{ to } 3$	3.6 V	2.2			2.2			
V _{IL}	Input LOW voltage	$V_{CC} = 2.2 \text{ V to } 2$	2.7 V	-0.3	-	0.6	-0.3	-	0.6	V
		V _{CC} = 2.7 V to 3.6 V				0.8			0.8	
I _{IX}	Input leakage current	$GND \leq V_I \leq V_{CC}$		-1	-	+1	-1	-	+1	μA
I _{OZ}	Output leakage current	$\begin{array}{l} GND \leq V_O \leq V_{CC}, \mbox{ output} \\ \mbox{ disabled} \end{array}$		-1	-	+1	-1	-	+1	μA
I _{CC}	V _{CC} operating supply	$V_{CC} = V_{CC(max)}$	$f = f_{Max} = 1/t_{RC}$	Ι	15	30	Ι	12	25	mA
	current	I _{OUT} = 0 mA CMOS levels	f = 1 MHz		2	4		2	4	
I _{SB1}	Automatic power-down current – CMOS inputs	$\overline{CE}_{1} \ge V_{CC} - 0.2$ $V_{IN} \ge V_{CC} - 0.2$ $f = f_{Max} \text{ (address)}$	/, $V_{IN} ≤ 0.2$ V, and data only),	_	2.5	22	_	2.5	22	μA
I _{SB2}	Automatic power-down current – CMOS Inputs	$ \begin{split} f &= 0 \; (\overline{OE}, \overline{WE}), V \\ \overline{CE}_1 &\geq V_{CC} - 0 \\ CE_2 &\leq 0.2 \; V \\ V_{IN} &\geq V_{CC} - 0.2 \\ f &= 0, \; V_{CC} = 3.6 \end{split} $	2 V or V or V _{IN} ≤0.2V,		2.5	22	_	2.5	22	μΑ

- Notes
 5. V_{IL(min.)} = -2.0 V for pulse durations less than 20 ns.
 6. V_{IH(max)} = V_{CC} + 0.75 V for pulse durations less than 20 ns.
 7. Full Device AC operation requires linear V_{CC} ramp from 0 to V_{CC(min.)} and V_{CC} must be stable at V_{CC(min)} for 500 μs.
 8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.



Capacitance

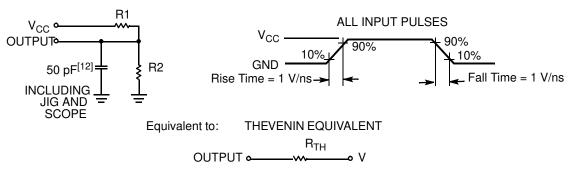
Parameter ^[10]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	$T_A = 25 \text{ °C}, f = 1 \text{ MHz}, V_{CC} = V_{CC(typ)}$	8	pF
C _{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter ^[10]	Description	Test Conditions	VFBGA	TSOP I	Unit
θ_{JA}		Still air, soldered on a 3 × 4.5 inch, 2-layer printed circuit board	55	60	°C/W
θ ^{JC}	Thermal resistance (junction to case)		16	4.3	°C/W

AC Test Loads and Waveforms





Parameters	2.5 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R _{TH}	8000	645	Ω
V _{TH}	1.20	1.75	V

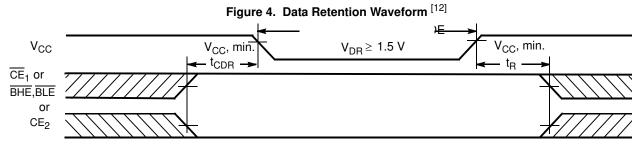


Data Retention Characteristics

Over the Operating Range

Parameter	Description	C	onditions	Min	Typ ^[9]	Max	Unit
V _{DR}	V_{CC} for data retention			1.5	-	-	V
I _{CCDR}	Data retention current	$\frac{V_{CC}}{CE} = 1.5 \text{ V},$ $\frac{\overline{CE}_{1}}{V_{CC}} = V_{CC} - 0$ $V_{IN} \ge V_{CC} - 0$.2 V or CE ₂ ≤ 0.2 V, 0.2 V or V _{IN} ≤ 0.2 V	-	-	10	μΑ
t _{CDR} ^[10]	Chip deselect to data retention time			0	-	-	ns
t _R ^[11]	Operation recovery time		CY62167DV30LL-55	55	-	_	ns
			CY62167DV30LL-70	70			

Data Retention Waveform



Notes

- 9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25 \text{ °C}$. 10. Tested initially and after any design or process changes that may affect these parameters. 11. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \ge 100 \,\mu\text{s}$ or stable at $V_{CC(min.)} \ge 100 \,\mu\text{s}$.

12. BHE.BLE is the AND of both BHE and BLE. Chip can be deselected by either disabling the chip enable signals or by disabling both BHE and BLE.



Switching Characteristics

Over the Operating Range

Parameter ^[13]	Description	55	ns	70 ns		
	Description	Min	Max	Min	Max	Unit
Read Cycle						
t _{RC}	Read cycle time	55	-	70	_	ns
t _{AA}	Address to data valid	-	55	-	70	ns
t _{OHA}	Data hold from address change	10	_	10	-	ns
t _{ACE}	\overline{CE}_1 LOW and CE_2 HIGH to data valid	-	55	-	70	ns
t _{DOE}	OE LOW to data valid	-	25	-	35	ns
t _{LZOE}	OE LOW to low Z [14]	5	_	5	-	ns
t _{HZOE}	OE HIGH to high Z ^[14, 15]	_	20	_	25	ns
t _{LZCE}	CE ₁ LOW and CE ₂ HIGH to low Z ^[14]	10	_	10	-	ns
t _{HZCE}	\overline{CE}_1 HIGH and CE_2 LOW to high Z ^[14, 15]	_	20	_	25	ns
t _{PU}	CE ₁ LOW and CE ₂ HIGH to power-up	0	_	0	-	ns
t _{PD}	CE ₁ HIGH and CE ₂ LOW to power-down	-	55	-	70	ns
t _{DBE}	BLE/BHE LOW to data valid	-	55	-	70	ns
t _{LZBE}	BLE/BHE LOW to low Z ^[14]	10	_	10	-	ns
t _{HZBE}	BLE/BHE HIGH to high Z [14, 15]	-	20	-	25	ns
Write Cycle [16]]					
t _{WC}	Write cycle time	55	_	70	_	ns
t _{SCE}	\overline{CE}_1 LOW and CE_2 HIGH to write end	40	_	60	-	ns
t _{AW}	Address setup to write end	40	_	60	-	ns
t _{HA}	Address hold from write end	0	_	0	-	ns
t _{SA}	Address setup to write start	0	_	0	-	ns
t _{PWE}	WE pulse width	40	_	45	-	ns
t _{BW}	BLE/BHE LOW to write end	40	-	60	-	ns
t _{SD}	Data setup to write end	25	-	30	-	ns
t _{HD}	Data hold from write end	0	-	0	-	ns
t _{HZWE}	WE LOW to high-Z ^[14, 15]	-	20	-	25	ns
t _{LZWE}	WE HIGH to low-Z [14]	10	_	10	-	ns

- Notes
 13. Test conditions for all parameters other than Tri-state parameters assume signal transition time of 1 ns/V, timing reference levels of V_{CC(typ)}/2, input pulse levels of 0 to V_{CC(typ)}, and output loading of the specified |_{0L}/l_{OH} as shown in the "AC Test Loads and Waveforms" section.
 14. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZCE}, t_{HZDE}, and t_{HZWE} is less than t_{LZCE} for any device.
 15. t_{HZOE}, t_{HZCE}, t_{HZEE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
 16. The internal Write time of the memory is defined by the overlap of WE, CE₁ = V_{IL}, BHE and/or BLE = V_{IL}, and CE₂ = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the Write.



Switching Waveforms

Figure 5. Read Cycle 1 (Address Transition Controlled) ^[17, 18]

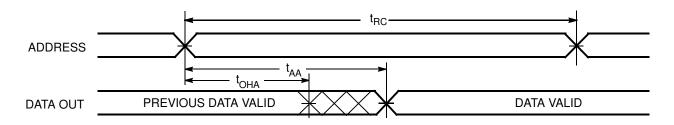
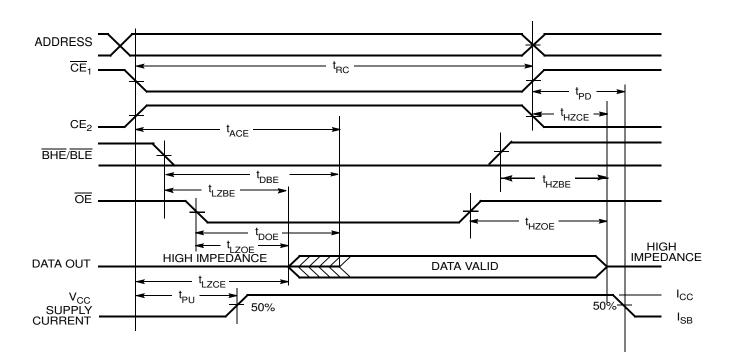


Figure 6. Read Cycle 2 (OE Controlled) ^[18, 19]



- 17. The device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. 18. \overline{WE} is HIGH for read cycle. 19. Address valid prior to or coincident with \overline{CE}_1 , \overline{BHE} , \overline{BLE} transition LOW and CE_2 transition HIGH.



Switching Waveforms (continued)

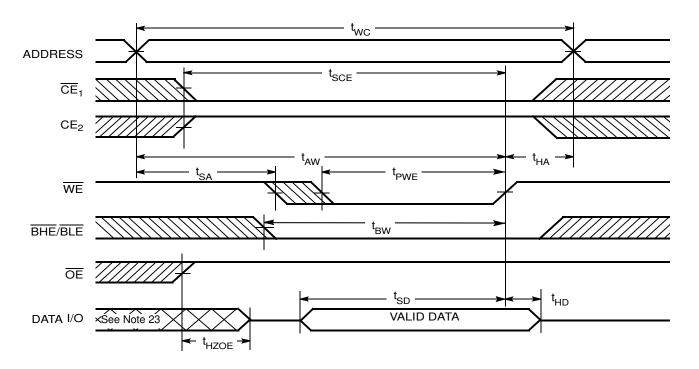
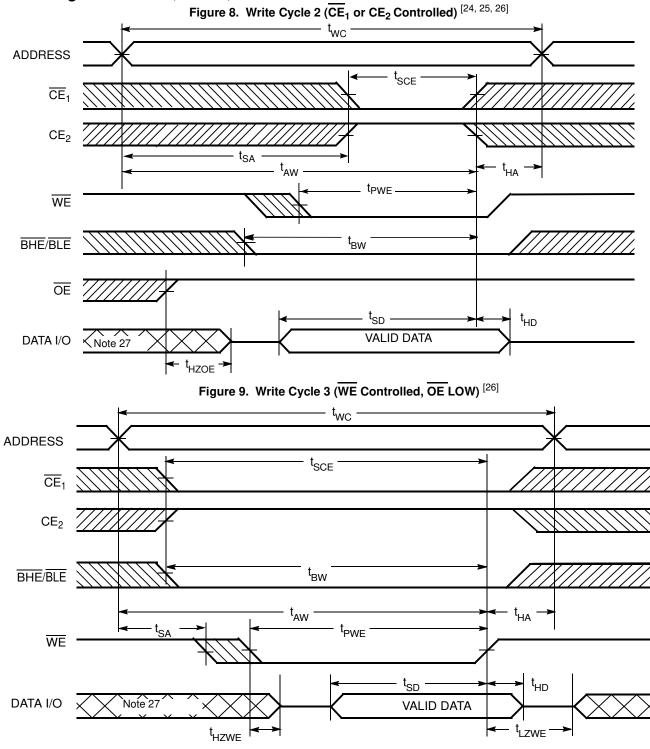


Figure 7. Write Cycle 1 ($\overline{\text{WE}}$ Controlled) ^[20, 21, 22]

- 20. The internal Write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the Write.
- 21. Data I/O is high-impedance if $\overline{OE} = V_{IH}$. 22. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high-impedance state. 23. During this period, the I/Os are in output state and input signals should not be applied.



Switching Waveforms (continued)



- 24. The internal Write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the Write.
- 25. Data I/O is high-impedance if $\overline{OE} = V_{IH}$. 26. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high-impedance state. 27. During this period, the I/Os are in output state and input signals should not be applied.



Switching Waveforms (continued)

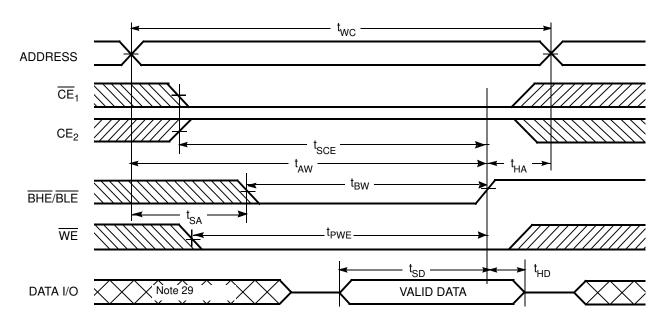


Figure 10. Write Cycle 4 (BHE/BLE Controlled, OE LOW) ^[28]

Notes ______ 28. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high-impedance state. 29. During this period, the I/Os are in output state and input signals should not be applied.





Truth Table

CE ₁	CE ₂	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
Н	Х	Х	Х	Х	Х	High Z	Deselect/Power-down	Standby (I _{SB})
Х	L	Х	Х	Х	Х	High Z	Deselect/Power-down	Standby (I _{SB})
Х	Х	Х	Х	Н	Н	High Z	Deselect/Power-down	Standby (I _{SB})
L	Н	Н	L	L	L	Data out (I/O ₀ -I/O ₁₅)	Read	Active (I _{CC})
L	Н	Н	L	Н	L	High Z (I/O ₈ -I/O ₁₅); Data out (I/O ₀ -I/O ₇)	Read	Active (I _{CC})
L	Н	Η	L	L	Н	Data out (I/O ₈ –I/O ₁₅); High Z (I/O ₀ –I/O ₇)	Read	Active (I _{CC})
L	Н	L	Х	L	L	Data in (I/O ₀ -I/O ₁₅)	Write	Active (I _{CC})
L	Н	L	Х	Н	L	High Z (I/O ₈ –I/O ₁₅); Data in (I/O ₀ –I/O ₇)	Write	Active (I _{CC})
L	Н	L	Х	L	Н	Data in (I/O ₈ –I/O ₁₅); High Z (I/O ₀ –I/O ₇)	Write	Active (I _{CC})
L	Н	Н	Н	L	Н	High Z	Output disabled	Active (I _{CC})
L	Н	Н	Н	Н	L	High Z	Output disabled	Active (I _{CC})
L	Н	Н	Н	L	L	High Z	Output disabled	Active (I _{CC})

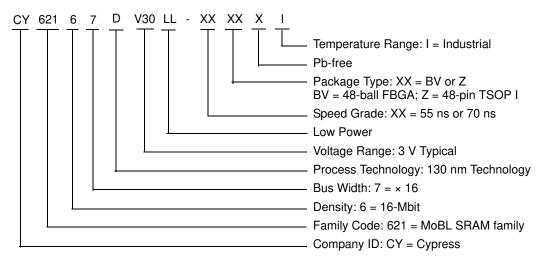


Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62167DV30LL-55BVI	51-85178	48-ball FBGA (8 × 9.5 × 1 mm)	Industrial
	CY62167DV30LL-55BVXI		48-ball FBGA (8 × 9.5 × 1 mm) Pb-free	
	CY62167DV30LL-55ZXI	51-85183	48-pin TSOP I (12 × 18.4 × 1 mm) Pb-free	
70	CY62167DV30LL-70BVI	51-85178	48-ball FBGA (8 × 9.5 × 1 mm)	

Please contact your local Cypress sales representative for availability of these parts

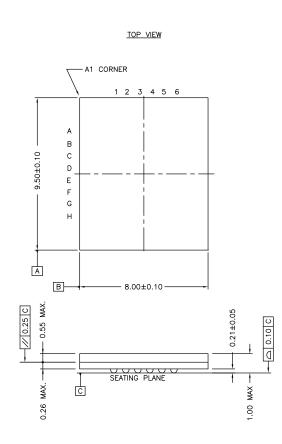
Ordering Code Definitions

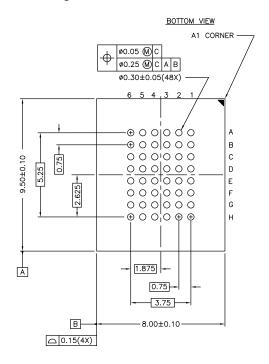




Package Diagrams

Figure 11. 48-ball VFBGA (8 × 9.5 × 1 mm) BV48B Package Outline, 51-85178





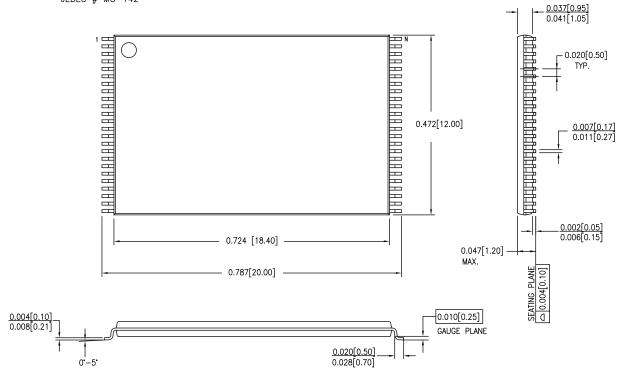
51-85178 *C



Package Diagrams (continued) Figure 12. 48-pin TSOP I (12 × 18.4 × 1 mm) Z48A Package Outline, 51-85183

DIMENSIONS IN INCHES[MM] MIN. MAX.

JEDEC # MO-142



51-85183 *C



Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array

Document Conventions

Units of Measure

Symbol	Unit of Measure		
°C	degrees Celsius		
MHz	megahertz		
μA	microampere		
mA	milliampere		
ns	nanosecond		
Ω	ohm		
pF	picofarad		
V	volt		
W	watt		





Document History Page

Document Title: CY62167DV30 MoBL [®] , 16-Mbit (1 M × 16) Static RAM Document Number: 38-05328				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	118408	GUG	09/30/02	New data sheet.
*A	123692	DPM	02/11/03	Changed status from Advanced to Preliminary. Added package diagram
*B	126555	DPM	04/25/03	Minor change: Changed Sunset Owner from DPM to HRT
*C	127841	XRJ	09/10/03	Added 48 TSOP I package
*D	205701	AJU	See ECN	Changed BYTE pin usage description for 48 TSOPI package
*E	238050	KKV/AJU	See ECN	Replaced 48-ball VFBGA package diagram; Modified Package Name in Ordering Information table from BV48A to BV48B
*F	304054	PCI	See ECN	Added 45-ns Speed Bin in AC, DC and Ordering Information tables Added Footnote #12 on page #4 Added Pb-free packages on page # 10
*G	492895	VKN	See ECN	Modified datasheet to explain x8 configurability. Removed L power bin from the product offering Updated Ordering Information Table
*H	2896036	AJU	03/19/10	Removed 45-ns. Removed inactive parts from Ordering Information. Updated Packaging Information Updated links in Sales, Solutions, and Legal Information.
*	3067267	RAME	11/08/10	Updated datasheet as per new template Added Ordering Code Definitions. Added Acronyms and Units of Measure. Updated all table notes to footnote. Package diagram updated 51-85178 from ** to *A
*J	3329789	RAME	07/27/11	Removed references to AN1064 SRAM system guidelines. Updated template according to current CY standards.
*K	4108382	AJU	08/29/2013	Updated Pin Configurations: Removed the note "Ball H6 for the FBGA package can be used to upgrade to a 32M density" and its reference in Figure 1. Updated Package Diagrams: spec 51-85178 – Changed revision from *A to *C. Updated in new template.
*L	4192919	VINI	11/15/2013	No technical updates. Completing Sunset Review.
*M	4574377	VINI	11/19/2014	Added related documentation hyperlink in page 1.



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Document Number: 38-05328 Rev. *M

Revised November 19, 2014

Page 18 of 18

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