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Low Skew Clock Buffer

Features

- All outputs skew < 100 ps typical (250 max)
- 15 MHz to 80 MHz output operation
- Zero input to output delay
- 50% duty cycle outputs
- Outputs drive 50 Ω terminated lines
- Low operating current
- 24-pin small-outline integrated circuit (SOIC) package
- Jitter: < 200 ps peak-to-peak, < 25 ps RMS

Functional Description

The CY7B9910 low skew clock buffer offers low skew system clock distribution. These multiple output clock drivers optimize the timing of high performance computer systems. Each of the eight individual drivers can drive terminated transmission lines with impedances as low as 50 Ω . They deliver minimal and specified output skews and full swing logic levels (CY7B9910 TTL).

The completely integrated PLL enables 'zero delay' capability. External divide capability, combined with the internal PLL, allows distribution of a low frequency clock that is multiplied by virtually any factor at the clock destination. This facility minimizes clock distribution difficulty while allowing maximum system clock speed and flexibility.

For a complete list of related documentation, click here.

Block Diagram Description

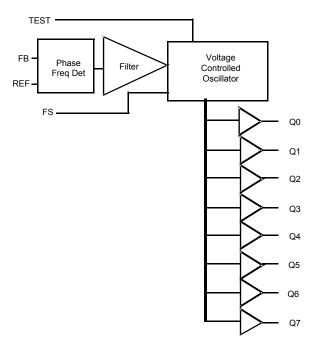
Phase Frequency Detector and Filter

The phase frequency detector and Filter blocks accept inputs from the reference frequency (REF) input and the feedback (FB) input and generate correction information to control the frequency of the voltage controlled oscillator (VCO). These blocks, along with the VCO, form a phase-locked loop (PLL) that tracks the incoming REF signal.

VCO

The VCO accepts analog control inputs from the PLL filter block and generates a frequency. The operational range of the VCO is determined by the FS control pin.

Logic Block Diagram





Contents

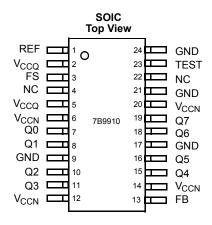
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Pinouts

Figure 1. 24-pin SOIC pinout



Pin Definitions

Signal Name	I/O	Description	
REF ^[1]	I	Reference frequency input. This input supplies the frequency and timing against which all functional variations are measured.	
FB	l	PLL feedback input (typically connected to one of the eight outputs).	
FS ^[1, 2, 3]	l	Three level frequency range select. The ranges are described in the switching characteristics tables.	
TEST	l	Three level select. See Test Mode.	
Q[07]	0	Clock outputs.	
NC	NC	No connect.	
V _{CCN}	PWR	Power supply for output drivers.	
V_{CCQ}	PWR	Power supply for internal circuitry.	
GND	PWR	Ground.	

Test Mode

The TEST input is a three level input. In normal system operation, this pin is connected to ground, allowing the CY7B9910 to operate as described in Block Diagram Description on page 1. For testing purposes, any of the three level inputs can have a removable jumper to ground or be tied LOW through a 100 Ω resistor. This enables an external tester to change the state of these pins.

If the TEST input is forced to its MID or HIGH state, the device operates with its internal phase locked loop disconnected and input levels supplied to REF directly control all outputs. Relative output-to-output functions are the same as in normal mode.

Notes

- When the FS pin is selected HIGH, the REF input must not transition upon power up until V_{CC} reached 4.3 V.
 The level to be set on FS is determined by the "normal" operating frequency (f_{NOM}) of the VCO (see Logic Block Diagram). The frequency appearing at the REF and FB inputs are f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs are f_{NOM} / X when the device is configured for a frequency multiplication by using external division in the feedback path of value X.
- 3. For all three state inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to V_{CC} / 2.



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature -65 °C to +150 °C Ambient temperature with power applied -55 °C to +125 °C Supply voltage to ground potential-0.5 V to +7.0 V DC input voltage-0.5 V to +7.0 V

Output current into outputs (LOW)64 mA	
Static discharge voltage	
(MIL-STD-883, method 3015)> 2001 V	
Latch-up current> 200 mA	

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0 °C to +70 °C	5 V ± 10%
Industrial	–40 °C to +85 °C	5 V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	CY7E	CY7B9910		
Parameter		rest conditions	Min	Max	Unit	
V _{OH}	Output HIGH voltage	$V_{\rm CC}$ = Min, $I_{\rm OH}$ = -16 mA	2.4	_	V	
		V _{CC} = Min, I _{OH} = -40 mA	-	_		
V _{OL}	Output LOW voltage	V _{CC} = Min, I _{OL} = 46 mA	-	0.45	V	
		V _{CC} = Min, I _{OL} = 46 mA	_	_		
V _{IH}	Input HIGH voltage (REF and FB inputs only)		2.0	V _{CC}	V	
V _{IL}	Input LOW voltage (REF and FB inputs only)		-0.5	0.8	V	
V _{IHH}	Three level input HIGH voltage (Test, FS) ^[4]	$Min \leq V_{CC} \leq Max$	V _{CC} -1	V _{CC}	V	
V _{IMM}	Three level input MID voltage (Test, FS) ^[4]	$Min \le V_{CC} \le Max$	$(V_{CC}/2) - 0.5$	$(V_{CC}/2) + 0.5$	V	
V _{ILL}	Three level input LOW voltage (Test, FS) ^[4]	$Min \leq V_{CC} \leq Max$	0.0	1.0	V	

Note

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^{4.} These inputs are normally wired to V_{CC}, GND, or left unconnected (actual threshold voltages vary as a percentage of V_{CC}). Internal termination resistors hold unconnected inputs at V_{CC} / 2. If these inputs are switched, the function and timing of the outputs may glitch and the PLL may require an additional t_{LOCK} time before all datasheet limits are achieved.



Electrical Characteristics (continued)

Over the Operating Range

Doromotor	Description	Toot Conditi	Test Conditions		39910	11:4
Parameter	Description	lest Conditi			Max	— Unit
I _{IH}	Input HIGH leakage current (REF and FB inputs only)	V _{CC} = Max, V _{IN} = Max	V _{CC} = Max, V _{IN} = Max		10	μA
I _{IL}	Input LOW leakage current (REF and FB inputs only)	V_{CC} = Max, V_{IN} = 0.4 V		– 500	_	μA
I _{IHH}	Input HIGH current (Test, FS)	$V_{IN} = V_{CC}$		_	200	μA
I _{IMM}	Input MID current (Test, FS)	$V_{IN} = V_{CC}/2$	$V_{IN} = V_{CC} / 2$		50	μA
I _{ILL}	Input LOW current (Test, FS)	V _{IN} = GND	V _{IN} = GND		-200	μA
I _{OS}	Output short circuit current ^[5]	V _{CC} = Max, V _{OUT} = G only)	V _{CC} = Max, V _{OUT} = GND (25 °C only)		-250	mA
I _{CCQ}	Operating current used by	V _{CCN} = V _{CCQ} = Max	Commercial	-	85	mA
	internal circuitry	All input selects open	Industrial	_	90	\neg
I _{CCN}	Output buffer current per output pair ^[6]	$V_{CCN} = V_{CCQ} = Max$ $I_{OUT} = 0 \text{ mA}$ Input selects open, f_{M}	AX	-	14	mA
PD	Power dissipation per output pair ^[7]	V _{CCN} = V _{CCQ} = Max I _{OUT} = 0 mA Input selects open, f _M	AX	-	78	mW

Notes

- Tested one output at a time, output shorted for less than one second, less than 10% duty cycle. Room temperature only.
- Total output current per output pair is approximated by the following expression that includes device current plus load current: CY7B9910: $ICCN = [(4 + 0.11 \text{ F}) + [((835 3 \text{ F}) / Z) + (.0022 \text{ FC})] \text{ N}] \times 1.1$

Where F = frequency in MHz
C = capacitive load in pF
Z = line impedance in ohms
N = number of loaded outputs; 0, 1, or 2
FC = F × C.
Total power dissipation per output pair is approximated by the following expression that includes device power dissipation plus power dissipation due to the load circuit:
CY7B9910:
PD = [(22 + 0.61 F) + [((1550 - 2.7 F) / Z) + (.0125 FC)] N] x 1.1
See note 3 for variable definition.
CMOS output buffer current and power dissipation specified at 50 MHz reference frequency.

8. CMOS output buffer current and power dissipation specified at 50 MHz reference frequency.



Capacitance

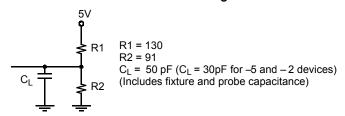
Parameter [9, 10]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	$T_A = 25 ^{\circ}\text{C}, f = 1 \text{MHz}, V_{CC} = 5.0 \text{V}$	10	pF

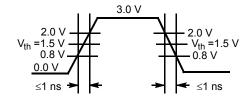
Thermal Resistance

Parameter [10]	Description	Test Conditions	24-pin SOIC Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance,	64	°C/W
$\Theta_{\sf JC}$	Thermal resistance (junction to case)	according to EIA/JESD51.	28	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms





TTL AC Test Load (CY7B9910)

TTL Input Test Waveform (CY7B9910)

Notes

Applies to REF and FB inputs only.
 Tested initially and after any design or process changes that may affect these parameters.



Switching Characteristics

Over the Operating Range

Parameter [11]	Description		CY7B9910-5			11!4
Parameter			Min	Тур	Max	Unit
f _{NOM}	Operating clock frequency in MHz	FS = LOW ^[12, 13]	15	_	30	MHz
		FS = MID ^[12, 13]	25	_	50	1
		FS = HIGH ^[12, 13, 14]	40	_	80	1
t _{RPWH}	REF pulse width HIGH		5.0	-	1	ns
t _{RPWL}	REF pulse width LOW		5.0	_	-	ns
t _{SKEW}	Zero output skew (All outputs) ^[16, 17]		_	0.25	0.5	ns
t _{DEV}	Device-to-device skew ^[18, 19]		-	_	1.0	ns
t _{PD}	Propagation delay, REF rise to FB rise		-0.5	0.0	+0.5	ns
t _{ODCV}	Output duty cycle variation ^[20]		-1.0	0.0	+1.0	ns
t _{ORISE}	Output rise time ^[21, 22]		0.15	1.0	1.5	ns
t _{OFALL}	Output fall time ^[21, 22]		0.15	1.0	1.5	ns
t _{LOCK}	PLL lock time ^[23]		_	_	0.5	ms
t _{JR}	Cycle-to-cycle output jitter	Peak-to-peak ^[18]	_	_	200	ps
		RMS ^[18]	-	_	25	ps

Notes

- 11. Test measurement levels for the CY7B9910 is TTL level (1.5 V to 1.5 V). Test conditions assume signal transition times of 2 ns or less and output loading as shown in the AC Test Loads and Waveforms unless otherwise specified.
- 12. For all three state inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to V_{CC} / 2.
- 13. The level to be set on FS is determined by the "normal" operating frequency (f_{NOM}) of the VCO (see Logic Block Diagram). The frequency appearing at the REF and FB inputs are f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs are f_{NOM} / X when the device is configured for a frequency multiplication by using external division in the feedback path of value X.
- 14. When the FS pin is selected HIGH, the REF input must not transition upon power up until V_{CC} reached 4.3 V.
- 15.
- 16. t_{SKEW} is defined as the time between the earliest and the latest output transition among all outputs when all are loaded with 50 pF and terminated with 50 Ω to 2.06 V (CY7B9910)
- 17. t_{SKEW} is defined as the skew between outputs.
- 18. Guaranteed by statistical correlation. Tested initially and after any design or process changes that may affect these parameters.
- 19. t_{DEV} is the output-to-output skew between any two outputs on separate devices operating under the same conditions (V_{CC}, ambient temperature, air flow, and so on).
- 20. t_{ODCV} is the deviation of the output from a 50% duty cycle.
- 21. Specified with outputs loaded with 30 pF for the CY7B9910–2 and –5 devices and 50 pF for the CY7B9910–7 devices. Devices are terminated through 50 Ω to 2.06 V (CY7B9910)
- 22. t_{ORISE} and t_{OFALL} measured between 0.8 V and 2.0 V for the CY7B9910
- 23. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

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AC Timing Diagrams

Figure 3. AC Timing Diagrams

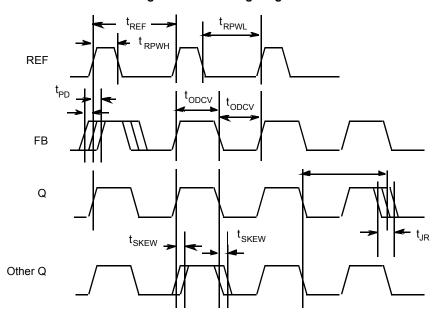
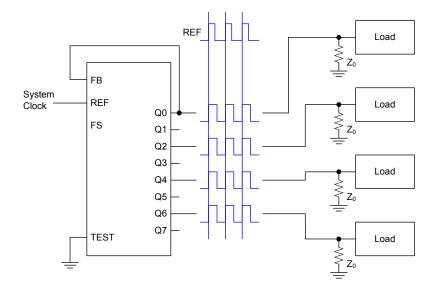


Figure 4. Zero Skew and Zero Delay Clock Driver





Operational Mode Descriptions

Figure 4 on page 8 shows the device configured as a zero skew clock buffer. In this mode the CY7B9910 is used as the basis for a low skew clock distribution tree. The outputs are aligned and may each drive a terminated transmission line to an independent load. The FB input is tied to any output and the operating frequency range is selected with the FS pin. The low skew specification, coupled with the ability to drive terminated transmission

lines (with impedances as low as 50 ohms), enables efficient printed circuit board design.

Figure 3 on page 8 shows the CY7B9910 connected in series to construct a zero skew clock distribution tree between boards. Cascaded clock buffers accumulates low frequency jitter because of the non-ideal filtering characteristics of the PLL filter. Do not connect more than two clock buffers in series.

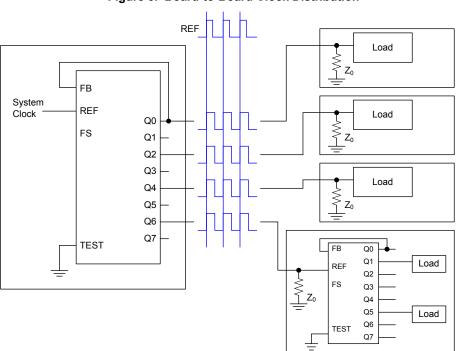


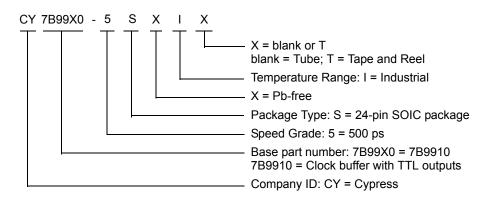
Figure 5. Board-to-Board Clock Distribution



Ordering Information

Accuracy (ps)	Ordering Code	Package Type	Operating Range
Pb-free			
500	CY7B9910-5SXI	24-pin Small Outline IC	Industrial, –40 °C to +85 °C
	CY7B9910-5SXIT	24-pin Small Outline IC – Tape and Reel	Industrial, –40 °C to +85 °C

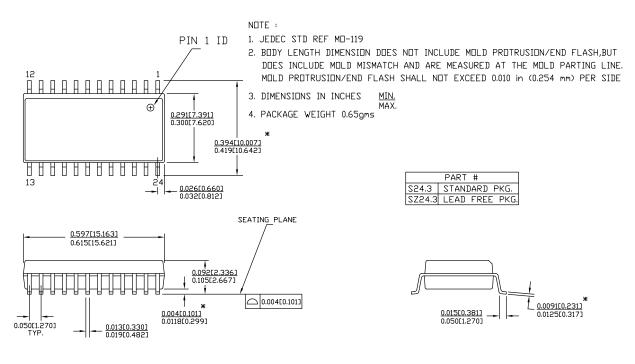
Ordering Code Definitions





Package Diagram

Figure 6. 24-pin SOIC (0.615 × 0.300 × 0.0932 Inches) Package Outline, 51-85025



51-85025 *F



Acronyms

Acronym	Description
FB	Feedback
PLL	Phase-Locked Loop
SOIC	Small-Outline Integrated Circuit
VCO	Voltage Controlled Oscillator

Document Conventions

Units of Measure

Symbol	Unit of Measure			
°C	degree Celsius			
kΩ	kilohm			
MHz	megahertz			
μΑ	microampere			
mA	milliampere			
ms	millisecond			
mW	milliwatt			
ns	nanosecond			
Ω	ohm			
ppm	parts per million			
%	percent			
pF	picofarad			
ps	picosecond			
V	volt			



Document History Page

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	110244	SZV	10/28/01	Change from Specification number: 38-00437 to 38-07135.
*A	1199925	DPF / AESA	See ECN	Updated Ordering Information: Added Pb-free parts in Ordering Information. Added Note "Not recommended for the new design" and referred the same note in CY7B9920-2SC, CY7B9910-7SI, CY7B9920-7SC, CY7B9920-7SI.
*B	1353343	AESA	See ECN	Change status from Preliminary to Final.
*C	2750166	TSAI	08/10/09	Post to external web.
*D	2761988	CXQ	09/10/09	Updated Test Mode: Fixed typo (Replaced 100 W resistor with 100 Ω resistor). Updated Ordering Information: Referred Note "Not recommended for new designs" in CY7B9910-2SC, CY7B9910-2SCT, CY7B9910-5SCT, CY7B9910-5SCT, CY7B9920-5SC, CY7B9920-5SCT, CY7B9920-5SI, CY7B9910-7SC. Fixed incorrect instances (Replaced "Pb" with "Pin").
*E	2896073	CXQ	03/19/10	Updated Ordering Information: Removed inactive parts. Updated Package Diagram.
*F	3010397	KVM	08/18/2010	Added Ordering Code Definitions.
*G	3047620	BASH	10/07/2010	Updated Ordering Information: Removed pruned parts. Removed associated tables.
*H	4163293	CINM	10/17/2013	Updated Package Diagram: spec 51-85025 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.
*	4416541	AJU	06/23/2014	Updated Ordering Information: No change in part numbers. Removed the Note "Not recommended for new design. New designs should use Pb-free devices." and its reference in "CY7B9920-5SI". Added "Not Recommended for New Designs" against the MPN "CY7B9920-5SI". Updated Package Diagram: spec 51-85025 – Changed revision from *E to *F.
*J	4570101	AJU	11/14/2014	Updated Functional Description: Added "For a complete list of related documentation, click here." at the end.
*K	5270360	PSR	05/13/2016	Updated Electrical Characteristics: Updated Note 6 (Replaced "FC = F < C" with "FC = F × C"). Added Thermal Resistance. Updated to new template.
*L	5493470	XHT	11/04/2016	Updated Document Title to read as "CY7B9910, Low Skew Clock Buffer". Removed CY7B9920 part related information in all instances across the document. Updated Ordering Information: Updated part numbers. Updated to new template. Completing Sunset Review.



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