mail

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from, Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts, Customers Priority, Honest Operation, and Considerate Service", our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip, ALPS, ROHM, Xilinx, Pulse, ON, Everlight and Freescale. Main products comprise IC, Modules, Potentiometer, IC Socket, Relay, Connector. Our parts cover such applications as commercial, industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832 Email & Skype: info@chipsmall.com Web: www.chipsmall.com Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





CY7C1010DV33

2-Mbit (256 K × 8) Static RAM

Features

- Pin and function compatible with CY7C1010CV33
- High speed □ t_{AA} = 10 ns
- Low active power □ I_{CC} = 90 mA at 10 ns
- Low CMOS standby power □ I_{SB2} = 10 mA
- 2.0 V data retention
- Automatic power down when deselected
- TTL-compatible inputs and outputs
- **Easy** memory expansion with \overline{CE} and \overline{OE} features
- Available in Pb-free 36-pin SOJ and 44-pin TSOP II packages

Functional Description

The CY7C1010DV33 is a high performance CMOS Static RAM organized as 256 K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}), an active LOW Output Enable (\overline{OE}), and three-state drivers. Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₁₇).

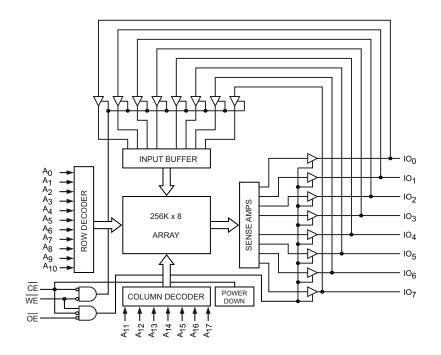
<u>Rea</u>ding from the device is <u>ac</u>complished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input and output pins $(I/O_0 \text{ through } I/O_7)$ are placed in a high impedance state when the device is deselected (CE HIGH), the outputs are disabled (OE HIGH), or during a Write operation (CE LOW, and WE LOW).

The CY7C1010DV33 is available in 36-pin SOJ and 44-pin TSOP II packages with center power and ground (revolutionary) pinout.

For a complete list of related documentation, click here.

Logic Block Diagram



Cypress Semiconductor Corporation Document Number: 001-00062 Rev. *F 198 Champion Court

San Jose, CA 95134-1709 • 408-943-2600 Revised November 19, 2014



CY7C1010DV33

Contents

Selection Guide	
Pin Configuration	
Maximum Ratings	
Operating Range	4
Electrical Characteristics	
Capacitance	5
Thermal Resistance	
AC Test Loads and Waveforms	
Data Retention Characteristics	6
Data Retention Waveform	
AC Switching Characteristics	
Switching Waveforms	
Truth Table	

Ordering Information	11
Ordering Code Definitions	
Package Diagrams	12
Acronyms	14
Document Conventions	14
Units of Measure	14
Document History Page	15
Sales, Solutions, and Legal Information	16
Worldwide Sales and Design Support	16
Products	16
PSoC® Solutions	16
Cypress Developer Community	16
Technical Support	



Selection Guide

Description	-10	Unit
Maximum Access Time	10	ns
Maximum Operating Current	90	mA
Maximum CMOS Standby Current	10	mA

Pin Configuration

Figure 1. 36-pin SOJ pinout ^[1]

$ \begin{array}{c} A_4 \square 1 \\ A_3 \square 2 \end{array} $	36 □ NC 35 □ A ₅
A ₂ 3	34 🗖 A ₆
$A_1 \square 4$	33 🗄 A7
$A_0 \square 5$	32 🗖 A ₈
	31 🗖 🔂
IO ₀	30 🗖 IO7
IO ₁	29 🗖 IO ₆
V _{CC} 🗖 9	28 🗆 GND
GND 🗌 10	27 🗖 V _{CC}
	26 □ IO ₅
$10_3 \square 12$	25 🗖 IO ₄
WE 13	24 🗖 🗛
A ₁₇ 14	23 🗖 A ₁₀
A ₁₆ □ 15	$22 \square A_{11}$
A ₁₅ 16	$21 \square A_{12}$
A ₁₃ 18	19 🗆 NC

Figure 2. 44-pin TSOP II pinout ^[1]

$ \begin{array}{c c} & & & \\ & & & \\ NC & & & \\ & & & \\ NC & & & \\ & & & \\ A_4 & & & \\ & & & \\ A_3 & & & \\ & & & \\ A_3 & & & \\ & & & \\ A_3 & & & \\ A_2 & & & \\ & & & \\ A_3 & & & \\ A_2 & & & \\ & & \\ A_1 & & & \\ A_1 & & \\ V_{CC} & & \\ & & \\ NC & & \\ & & \\ \hline \\ V_{CC} & & \\ & & \\ NC & & \\ \hline \\ V_{CC} & & \\ & & \\ \hline \\ V_{CC} & & \\ & & \\ \hline \\ V_{CC} & & \\ & & \\ \hline \\ V_{CC} & & \\ & & \\ \hline \\ V_{CC} & & \\ \\ V_{CC} & & \\ \hline \\ V_{CC} & & \\$	44 NC 43 NC 42 NC 41 A ₅ 40 A ₆ 39 A ₇ 38 A ₈ 37 OE 36 IO ₇ 35 IO ₆ 34 V _{SS} 33 V _{CC} 32 IO ₅ 31 IO ₄ 30 A ₉ 29 A ₁₁ 27 NC 25 NC 24 NC
A ₁₃	25 🗍 NC

Note
1. NC pins are not connected on the die.



Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature	–65 °C to +150 °C
Ambient Temperature with Power Applied	–55 °C to +125 °C
Supply Voltage on V_{CC} Relative to GND ^[2]	–0.5 V to +4.6 V
DC Voltage Applied to Outputs in High Z State ^[2]	–0.3 V to V _{CC} + 0.3 V

DC Input Voltage [2]	. –0.3 V to V _{CC} + 0.3 V
Current into Outputs (LOW)	20 mA
Static Discharge Voltage (MIL-STD-883, Method 3015)	> 2001 V
Latch Up Current	> 200 mA

Operating Range

Range	Ambient Temperature	V _{cc}
Industrial	–40 °C to +85 °C	$3.3V\pm0.3V$

Electrical Characteristics

Over the Operating Range

Deremeter	Description	Test Conditions		-*	10	
Parameter	Description	Test Conditions	Min	Max	Unit	
V _{OH}	Output HIGH Voltage	V _{CC} = Min; I _{OH} = -4.0 mA		2.4	-	V
V _{OL}	Output LOW Voltage	V _{CC} = Min; I _{OL} = 8.0 mA		-	0.4	V
V _{IH}	Input HIGH Voltage			2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage ^[2]			-0.3	0.8	V
I _{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$		–1	+1	μA
I _{OZ}	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$, Output Disabled		–1	+1	μA
I _{CC}	V _{CC} Operating Supply Current	V_{CC} = Max, f = f _{MAX} = 1/t _{RC}	100 MHz	_	90	mA
			83 MHz	_	80	
			66 MHz	_	70	
			40 MHz	-	60	
I _{SB1}	Automatic CE Power-down Current – TTL Inputs	$\begin{array}{l} \text{Max } V_{CC}, \ \overline{CE} \geq V_{IH}; \ V_{IN} \geq V_{IH} \text{ or } \\ V_{IN} \leq V_{IL}, \ f = f_{MAX} \end{array}$		-	20	mA
I _{SB2}	Automatic CE Power-down Current – CMOS Inputs	$ \begin{array}{l} \mbox{Max V}_{CC}, \ \overline{CE} \geq V_{CC} - 0.3 \ \mbox{V}, \\ \mbox{V}_{IN} \geq V_{CC} - 0.3 \ \mbox{V}, \ \mbox{or V}_{IN} \leq 0.3 \ \mbox{V}, \ \mbox{f} = \end{array} $	0	-	10	mA



Capacitance

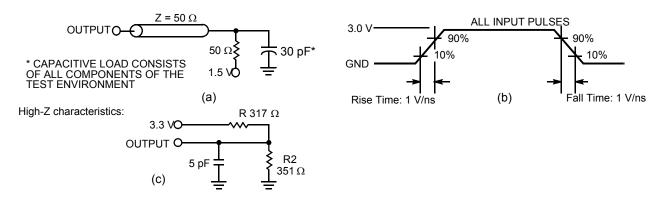
Parameter ^[3]	Description	Test Conditions	36-pin SOJ	44-pin TSOP II	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = 3.3 V	8	8	pF
C _{OUT}	I/O capacitance		8	8	pF

Thermal Resistance

Parameter ^[3]	Description	Test Conditions	36-pin SOJ	44-pin TSOP II	Unit
Θ_{JA}		Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	59.17	50.66	°C/W
30	Thermal resistance (junction to case)		32.63	17.77	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms ^[4]



Notes

Tested initially and after any design or process changes that may affect these parameters. AC characteristics (except High Z) are tested using the load conditions shown in Figure 3 (a). High-Z characteristics are tested for all speeds using the test load shown in Figure 3 (c). 4.

^{3.}



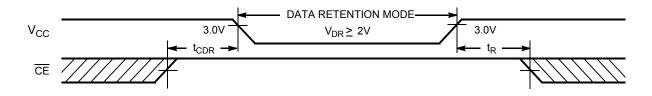
Data Retention Characteristics

Over the Operating Range

Parameter ^[5]	Description	Conditions	Min	Max	Unit
V _{DR}	V _{CC} for Data Retention		2	-	V
I _{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0 \text{ V}, \overline{CE} \ge V_{CC} - 0.3 \text{ V},$ $V_{IN} \ge V_{CC} - 0.3 \text{ V} \text{ or } V_{IN} \le 0.3 \text{ V}$	-	10	mA
t _{CDR} ^[6]	Chip Deselect to Data Retention Time		0	-	ns
t _R ^[7]	Operation Recovery Time		t _{RC}	_	ns

Data Retention Waveform





Notes

- 5. No inputs may exceed V_{CC} + 0.3 V. 6. Tested initially and after any design or process changes that may affect these parameters. 7. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min.)} \geq 50 µs or stable at V_{CC(min.)} \geq 50 µs.



AC Switching Characteristics

Over the Operating Range

Parameter ^[8]	Description	-	-10		
Parameter	Description		Мах	Unit	
Read Cycle			•		
t _{power} [9]	V _{CC} (typical) to the first access	100	-	μS	
t _{RC}	Read Cycle Time	10	-	ns	
t _{AA}	Address to Data Valid	-	10	ns	
t _{OHA}	Data Hold from Address Change	3	-	ns	
t _{ACE}	CE LOW to Data Valid	-	10	ns	
t _{DOE}	OE LOW to Data Valid	-	5	ns	
t _{LZOE}	OE LOW to Low Z ^[10]	0	_	ns	
t _{HZOE}	OE HIGH to High Z ^[10, 11]	-	5	ns	
t _{LZCE}	CE LOW to Low Z ^[10]	3	_	ns	
t _{HZCE}	CE HIGH to High Z ^[10, 11]	-	5	ns	
t _{PU}	CE LOW to Power-up	0	_	ns	
t _{PD}	CE HIGH to Power-down	-	10	ns	
Write Cycle ^{[12,}	13]				
t _{WC}	Write Cycle Time	10	_	ns	
t _{SCE}	CE LOW to Write End	7	-	ns	
t _{AW}	Address Set-up to Write End	7	-	ns	
t _{HA}	Address Hold from Write End	0	-	ns	
t _{SA}	Address Set-up to Write Start	0	-	ns	
t _{PWE}	WE Pulse Width	7	-	ns	
t _{SD}	Data Set-up to Write End	5	_	ns	
t _{HD}	Data Hold from Write End	0	_	ns	
t _{LZWE}	WE HIGH to Low Z ^[10]	3	-	ns	
t _{HZWE}	WE LOW to High Z ^[10, 11]	-	5	ns	

Notes

- 8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.

- test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
 t_{POWER} gives the minimum amount of time that the power supply should be at stable, typical V_{CC} values until the first memory access can be performed.
 At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZWE} for any given device.
 t_{HZOE}, t_{HZOE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of Figure 3 on page 5. Transition is measured when the outputs enter a high impedance state.
 The internal Write time of the memory is defined by the overlap of CE LOW, and WE LOW. CE and WE must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
 The minimum Write cycle time for Write Cycle No. 3 (WE controlled, OE LOW) is the sum of t_{HZWE} and t_{SD}.



HIGH IMPEDANCE

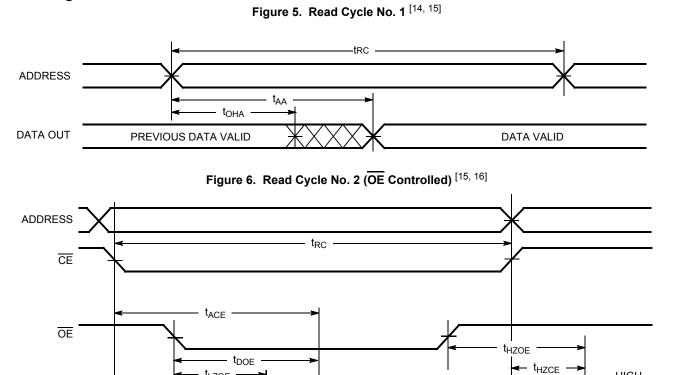
 I_{CC}

 I_{SB}

t_{PD}

50%

Switching Waveforms



DATA VALID

 t_{LZOE}

50%

HIGH IMPEDANCE

t_{LZCE}

t_{PU}

DATA OUT -

V_{CC} SUPPLY

CURRENT

Notes 14. <u>The</u> device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$. 15. WE is HIGH for read cycle. 16. Address valid before or similar to \overline{CE} transition LOW.



Switching Waveforms (continued)

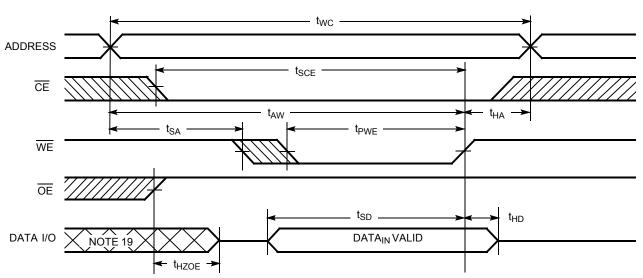
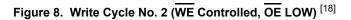
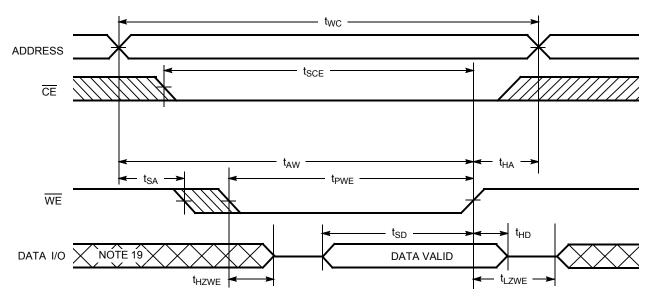


Figure 7. Write Cycle No. 1 (WE Controlled, OE HIGH During Write) ^[17, 18]





Notes

17. Data IO is high impedance if $\overline{OE} = V_{IH}$. 18. If \overline{CE} goes HIGH simultaneously with WE going HIGH, the output remains in a high impedance state.

19. During this period, the I/Os are in output state and input signals should not be applied.



Truth Table

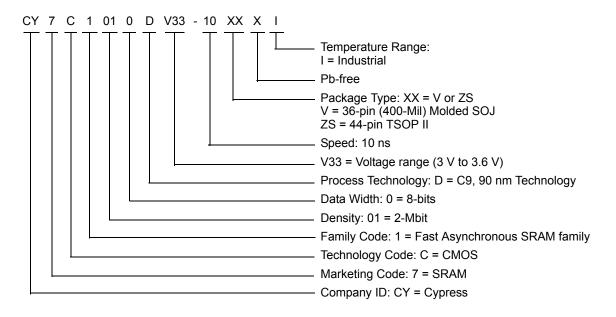
CE	OE	WE	I/O ₀ –I/O ₇	I/O ₈ –I/O ₁₅	Mode	Power
Н	Х	Х	High Z	High Z	Power Down	Standby (I _{SB})
L	L	Н	Data Out	Data Out	Read All Bits	Active (I _{CC})
L	Х	L	Data In	Data In	Write All Bits	Active (I _{CC})
L	Н	Н	High Z	High Z	Selected, Outputs Disabled	Active (I _{CC})



Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1010DV33-10VXI	51-85090	36-pin (400-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C1010DV33-10ZSXI	51-85087	44-pin TSOP II (Pb-free)	

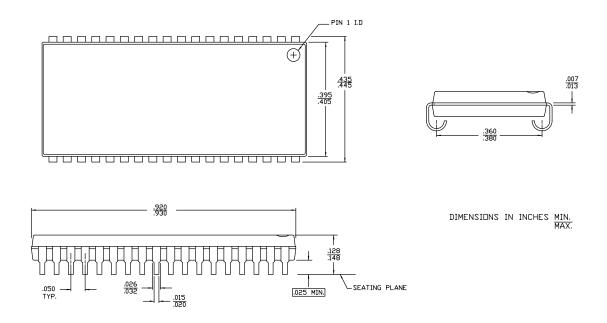
Ordering Code Definitions





Package Diagrams

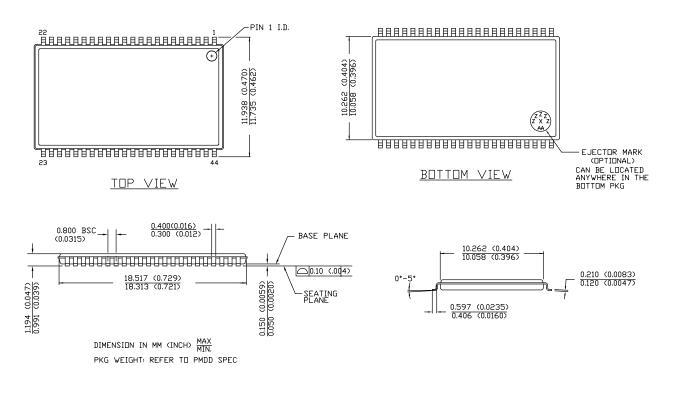
Figure 9. 36-pin SOJ V36.4 (Molded) Package Outline, 51-85090

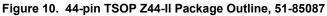


51-85090 *F



Package Diagrams (continued)





51-85087 *E





Acronyms

Acronym	Description		
CE	Chip Enable		
CMOS	Complementary Metal Oxide Semiconductor		
I/O	Input/Output		
OE	Output Enable		
SOJ	Small Outline J-lead		
SRAM	Static Random Access Memory		
TSOP	Thin Small Outline Package		
TTL	Transistor-Transistor Logic		
WE	Write Enable		

Document Conventions

Units of Measure

Symbol	Unit of Measure		
°C	degree Celsius		
MHz	megahertz		
μA	microampere		
μS	microsecond		
mA	milliampere		
mm	millimeter		
mW	milliwatt		
ns	nanosecond		
Ω	ohm		
%	percent		
pF	picofarad		
V	volt		
W	watt		





ocument Title: CY7C1010DV33, 2-Mbit (256 K × 8) Static RAM ocument Number: 001-00062			
ECN No.	Submission Date	Orig. of Change	Description of Change
342195	See ECN	PCI	New data sheet.
459073	See ECN	NXR	Converted Preliminary to Final. Removed Commercial Operating Range from product offering. Removed -8 ns and -12 speed bin Removed the Pin definitions table. Modified Maximum Ratings for DC input voltage from -0.5V to -0.3V and V_{CC} + 0.5V to V_{CC} + 0.3V Changed I _{CC} max from 65 mA to 90 mA Changed the description of I _{IX} from "Input Load Current" to "Input Leakage Current" Updated the Thermal Resistance table. Updated footnote #7 on High-Z parameter measurement Added footnote #12 Updated the Ordering Information and replaced Package Name column with Package Diagram in the Ordering Information table.
2602853	11/07/08	VKN / PYRS	Added 36-pin SOJ package and its related information
3059211	10/14/2010	PRAS	Added Ordering Code Definitions. Updated Package Diagrams.
3272897	06/07/2011	AJU	Updated Functional Description (Removed "Refer to the Cypress application note AN1064, SRAM System Guidelines for best practice recommendations."). Added Acronyms and Units of Measure. Updated in new template.
4207615	12/02/2013	MEMJ	Updated Package Diagrams: spec 51-85090 – Changed revision from *E to *F. spec 51-85087 – Changed revision from *C to *E. Updated in new template. Completing Sunset Review.
	Number: 00 ECN No. 342195 459073 2602853 3059211 3272897	Sumber: 001-00062 ECN No. Submission Date 342195 See ECN 459073 See ECN 2602853 11/07/08 3059211 10/14/2010 3272897 06/07/2011	Submission Date Orig. of Change 342195 See ECN PCI 459073 See ECN NXR 2602853 11/07/08 VKN / PYRS 3059211 10/14/2010 PRAS 3272897 06/07/2011 AJU

*F

4574311

11/19/2014

MEMJ

Added related documentation hyperlink in page 1.



Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products	
Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc
	cypress.com/go/plc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC[®] Solutions

psoc.cypress.com/solutions PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community Community | Forums | Blogs | Video | Training

Technical Support cypress.com/go/support

© Cypress Semiconductor Corporation, 2005-2014. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

Document Number: 001-00062 Rev. *F

Revised November 19, 2014

All products and company names mentioned in this document may be the trademarks of their respective holders.