# imall

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from, Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts, Customers Priority, Honest Operation, and Considerate Service", our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip, ALPS, ROHM, Xilinx, Pulse, ON, Everlight and Freescale. Main products comprise IC, Modules, Potentiometer, IC Socket, Relay, Connector. Our parts cover such applications as commercial, industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



# Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832 Email & Skype: info@chipsmall.com Web: www.chipsmall.com Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





# CY7C1049G CY7C1049GE

# 4-Mbit (512K words × 8 bit) Static RAM with Error-Correcting Code (ECC)

#### Features

- High speed
  - ⊡ t<sub>AA</sub> = 10 ns
- Embedded ECC for single-bit error correction<sup>[1]</sup>
- Low active and standby currents
  Active current: I<sub>CC</sub> = 38 mA typical
  Standby current: I<sub>SB2</sub> = 6 mA typical
- Operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, and 4.5 V to 5.5 V
- 1.0-V data retention
- TTL-compatible inputs and outputs
- Error indication (ERR) pin to indicate 1-bit error detection and correction
- Pb-free 36-pin SOJ and 44-pin TSOP II packages

#### **Functional Description**

CY7C1049G and CY7C1049GE are high-performance CMOS fast static RAM devices with embedded ECC. Both devices are

offered in single and dual chip-enable options and in multiple pin configurations. The CY7C1049GE device includes an ERR pin that signals an error-detection and correction event during a read cycle.

Data writes are performed by asserting the Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW, while providing the data on I/O<sub>0</sub> through I/O<sub>7</sub> and address on A<sub>0</sub> through A<sub>18</sub> pins.

Data reads are performed by asserting the Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) inputs LOW and providing the required address on the address lines. Read data is accessible on the I/O lines (I/O<sub>0</sub> through I/O<sub>7</sub>).

All I/Os (I/O $_0$  through I/O $_7$ ) are placed in a high-impedance state during the following events:

- The device is deselected (CE HIGH)
- The control signal OE is de-asserted

On the CY7C1049GE devices, the detection and correction of a single-bit error in the accessed location is indicated by the assertion of the ERR output  $(ERR = HIGH)^{[1]}$ . See the Truth Table on page 14 for a complete description of read and write modes.

The logic block diagram is on page 2.

Product	Portfolic	)

					Power Dissipation				
Product <sup>[2]</sup>	Features and Options (see Pin Configurations on page 4)	Range	V <sub>CC</sub> Range	Speed (ns)	Operating I <sub>CC</sub> , (mA)		Standby, I <sub>SB2</sub> (mA)		
	Configurations on page 4)		(V)	10/15	f = f <sub>max</sub>				
					<b>Typ</b> <sup>[3]</sup>	Max	<b>Typ</b> <sup>[3]</sup>	Max	
CY7C1049G(E)18	Single or Dual Chip Enables	Industrial	1.65 V–2.2 V	15	_	40	6	8	
CY7C1049G(E)30	Optional ERR pins		2.2 V–3.6 V	10	38	45			
CY7C1049G(E)			4.5 V–5.5 V	10	38	45			

Notes

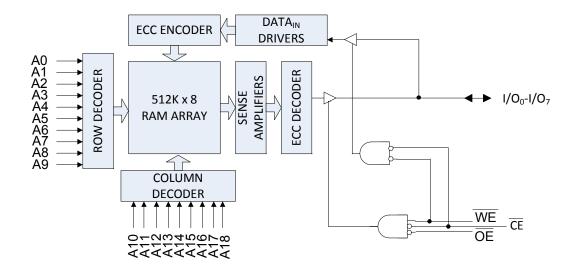
- 1. This device does not support automatic write-back on error detection.
- 2. The ERR pin is available only for devices which have ERR option "E" in the ordering code. Refer Ordering Information on page 15 for details.
- 3. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at  $V_{CC}$  = 1.8 V (for a  $V_{CC}$  range of 1.65 V–2.2 V),  $V_{CC}$  = 3 V (for a  $V_{CC}$  range of 2.2 V–3.6 V), and  $V_{CC}$  = 5 V (for a  $V_{CC}$  range of 4.5 V–5.5 V),  $T_A$  = 25 °C.

198 Champion Court

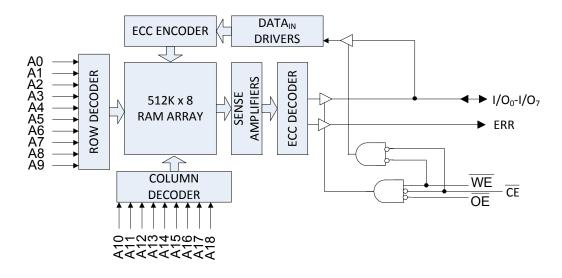
٠



# Logic Block Diagram – CY7C1049G



### Logic Block Diagram – CY7C1049GE





# Contents

Pin Configurations	4
Maximum Ratings	6
Operating Range	6
DC Electrical Characteristics	6
Capacitance	7
Thermal Resistance	
AC Test Loads and Waveforms	7
Data Retention Characteristics	8
Data Retention Waveform	8
AC Switching Characteristics	9
Switching Waveforms	
Truth Table	
ERR Output – CY7C1049GE	14

Ordering Information	. 15
Ordering Code Definitions	
Package Diagrams	. 16
Acronyms	. 17
Document Conventions	. 17
Units of Measure	. 17
Document History Page	. 18
Sales, Solutions, and Legal Information	. 19
Worldwide Sales and Design Support	. 19
Products	. 19
PSoC®Solutions	. 19
Cypress Developer Community	. 19
Technical Support	



# **Pin Configurations**

Figure 1. 36-pin SOJ pinout, Single Chip Enable without ERR - CY7C1049G<sup>[4]</sup>

				1
A0 🗖	•1	$\bigcirc$	36	NC
A1 🗖	2		35	<b>A</b> 18
A2 🗖	3		34	<b>A</b> 17
Аз 🗖	4		33	<b>A</b> 16
A4 🗖	5		32	<b>A</b> 15
CE 🗖	6		31	<b>O</b> E
I/O0 🗖	7		30	<b>I</b> /O7
I/O1 🗖	8		29	<b>I/O</b> 6
Vcc 🗖	9		28	🗖 GND
GND 🗖	10	SOJ	27	■ Vcc
I/O2 🗖	11		26	<b>=</b> I/O5
I/O3 🗖	12		25	<b>=</b> I/O4
WE 🗖	13		24	<b>A</b> 14
A5 🗖	14		23	<b>A</b> 13
A6 🗖	15		22	<b>A</b> 12
A7 🗖	16		21	<b>A</b> 11
A8 🗖	17		20	<b>A</b> 10
A9 🗖	18		19	■ NC
				J



### Pin Configurations (continued)

Figure 2. 44-	oin TSOP II pinout	, Single Chip Enable wi	thout ERR - CY7C1049G <sup>[5]</sup>
---------------	--------------------	-------------------------	--------------------------------------

	_			1
NC 🛛	<b>•</b> 1	0	44	NC NC
NC I	2		43	NC NC
A0 I	3		42	NC NC
A1 🛛	4		41	<b>A</b> 18
A2 🛛	5		40	<b>A</b> 17
A3 🛛	6		39	<b>A</b> 16
A4 I	7		38	<b>A</b> 15
/CE I	8		37	■/OE
I/O0 I	9	44-pin TSOP II	36	<b>I</b> /07
I/O1 I	10		35	<b>=</b> 1/O6
VCC I	11		34	■ VSS
VSS	12		33	■ vcc
I/O2 🛛	13		32	<b>I</b> /O5
I/O3 I	14		31	<b>I</b> /04
/WE 🛛	15		30	<b>A</b> 14
A5 🛛	16		29	<b>A</b> 13
A6 🛛	17		28	<b>A</b> 12
A7 I	18		27	<b>A</b> 11
A8 I	<b>1</b> 9		26	<b>A</b> 10
A9 I	20		25	NC I
NC I	21		24	NC NC
NC I	22		23	■ NC

Figure 3. 44-pin TSOP II pinout, Single Chip Enable with ERR - CY7C1049GE<sup>[5, 6]</sup>

	1	-			1		
NC	9	<b>1</b>	<b>—</b>	44	┝	Ν	С
NC		2		43	Þ	Ν	С
A0		3		42	Þ	Ν	С
A1		4		41	Þ	A	18
A2		5		40	┝	A	17
A3 (		6		39	┝	A	16
A4 (		7		38	Þ	A	15
/CE		8		37	Þ	/C	ЭE
I/O0		9	44-pin TSOP II	36	Þ	1/0	D7
I/01	9	10		35	┝	I/(	D6
VCC	9	11		34	┝	V	SS
VSS		12		33	┝	V	СС
I/O2		13		32	┝	I/(	D5
I/O3	9	14		31	┝	I/(	D4
/WE	9	15		30	┝	A	14
A5	9	16		29	┝	A	13
A6 (		17		28	┝	A	12
A7		18		27	┝	A	11
A8	9	19		26	┝	A	10
A9	9	20		25	┝	Ν	С
NC	-	21		24	╞	E	RR
NC	۲	22		23	╞	N	С

Notes5. NC pins are not connected internally to the die.6. ERR is an output pin.



### **Maximum Ratings**

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature65 °C to +150 °C
Ambient temperature with power applied55 °C to +125 °C
Supply voltage on V_{CC} relative to GND $^{[7]}$
DC voltage applied to outputs in HI-Z State $^{[7]}$ 0.5 V to V_{CC} + 0.5 V

#### **DC Electrical Characteristics**

Over the operating range of -40 °C to 85 °C

DC input voltage [7]	–0.5 V to V <sub>CC</sub> + 0.5 V
Current into outputs (in LOW state)	
Static discharge voltage (MIL-STD-883, Method 3015)	>2001 V
Latch-up current	> 140 mA

#### **Operating Range**

Grade	Ambient Temperature	V <sub>cc</sub>
Industrial	–40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

Demonstern	Description		To at O an ditte	Test Conditions		) ns / 15 r	າຣ	11
Parameter	Desc	ription	Test conditions		Min	<b>Typ</b> <sup>[8]</sup>	Max	Unit
V <sub>OH</sub>	Output HIGH	1.65 V to 2.2 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = –0.1 m	A	1.4	_	_	V
	voltage	2.2 V to 2.7 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = –1.0 m	A	2	_	_	† I
		2.7 V to 3.0 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 m	A	2.2	_	_	İ
		3.0 V to 3.6 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 m	A	2.4	_	_	Ì
		4.5 V to 5.5 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 m	A	2.4	_	_	İ
		4.5 V to 5.5 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.1m/	4	$V_{CC} - 0.5^{[9]}$	_	_	İ
V <sub>OL</sub>	V <sub>OL</sub> Output LOW		V <sub>CC</sub> = Min, I <sub>OL</sub> = 0.1 mA		_	_	0.2	V
	voltage		V <sub>CC</sub> = Min, I <sub>OL</sub> = 2 mA		_	_	0.4	† I
	2.7 V to 3.6 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8 mA		_	_	0.4	† I	
		4.5 V to 5.5 V	5.5 V V <sub>CC</sub> = Min, I <sub>OL</sub> = 8 mA		_	_	0.4	† I
V <sub>IH</sub> Input HIGH voltage	Input HIGH	1.65 V to 2.2 V	-		1.4	_	$V_{\rm CC}$ + 0.2 <sup>[7]</sup>	V
	voltage	2.2 V to 2.7 V	-		2	_	$V_{\rm CC}$ + 0.3 <sup>[7]</sup>	1
		2.7 V to 3.6 V	_		2	_	$V_{\rm CC}$ + 0.3 <sup>[7]</sup>	
		4.5 V to 5.5 V	-		2	_	$V_{\rm CC}$ + 0.5 <sup>[7]</sup>	† I
V <sub>IL</sub>	Input LOW	1.65 V to 2.2 V	-		-0.2 <sup>[7]</sup>	_	0.4	V
	voltage	2.2 V to 2.7 V	-		-0.3 <sup>[7]</sup>	_	0.6	† I
		2.7 V to 3.6 V	-		-0.3 <sup>[7]</sup>	_	0.8	† I
		4.5 V to 5.5 V	-		-0.5 <sup>[7]</sup>	_	0.8	† I
I <sub>IX</sub>	Input leakage c	urrent	GND <u>&lt;</u> V <sub>IN</sub> <u>&lt;</u> V <sub>CC</sub>		-1	_	+1	μA
I <sub>OZ</sub>	Output leakage	current	GND <u>&lt;</u> V <sub>OUT</sub> <u>&lt;</u> V <sub>CC</sub> , Out	put disabled	-1	_	+1	μA
I <sub>CC</sub>	Operating supp	ly current	Max V <sub>CC</sub> , I <sub>OUT</sub> = 0 mA, CMOS levels	f = 100 MHz	_	38	45	mA
			CMOS levels	f = 66.7 MHz	_	_	40	† I
I <sub>SB1</sub>	Automatic CE power-down current – TTL inputs		$\begin{array}{l} \text{Max V}_{\text{CC}}, \overline{\text{CE}} \geq \text{V}_{\text{IH}}, \\ \text{V}_{\text{IN}} \geq \text{V}_{\text{IH}} \text{ or } \text{V}_{\text{IN}} \leq \text{V}_{\text{IL}}, \text{f} \end{array}$	= f <sub>MAX</sub>	_	_	15	mA
I <sub>SB2</sub>	Automatic CE p current – CMOS	ower-down S inputs	$\begin{array}{l} \text{Max V}_{\text{CC}}, \ \overline{\text{CE}} \geq \text{V}_{\text{CC}} - 0, \\ \text{V}_{\text{IN}} \geq \text{V}_{\text{CC}} - 0.2 \ \text{V or V}_{\text{IN}} \end{array}$		-	6	8	mA

#### Notes

7.  $V_{IL(min)}$  = -2.0 V and  $V_{IH(max)}$  =  $V_{CC}$  + 2 V for pulse durations of less than 20 ns.

8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC}$  = 1.8 V (for  $V_{CC}$  range of 1.65 V – 2.2 V),  $V_{CC}$  = 3 V (for  $V_{CC}$  range of 2.2V – 3.6 V), and  $V_{CC}$  = 5 V (for  $V_{CC}$  range of 4.5 V – 5.5 V),  $T_A$  = 25 °C.

9. This parameter is guaranteed by design and not tested.



### Capacitance

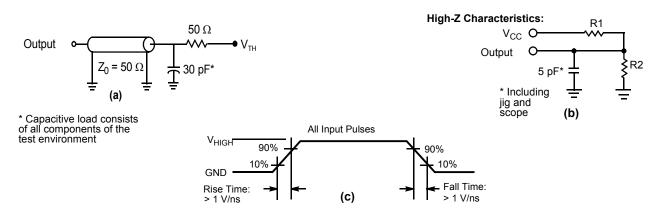
Parameter <sup>[10]</sup>	Description	Test Conditions	36-pin SOJ	44-pin TSOP II	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz,	10	10	pF
C <sub>OUT</sub>	I/O capacitance	$V_{CC} = V_{CC(typ)}$	10	10	pF

#### **Thermal Resistance**

Parameter <sup>[10]</sup>	Description	Test Conditions	36-pin SOJ	44-pin TSOP II	Unit
- JA		Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	59.52	68.85	°C/W
- 30	Thermal resistance (junction to case)		31.48	15.97	°C/W

### AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms <sup>[11]</sup>



Parameters	1.8 V	3.0 V	5.0 V	Unit
R1	1667	317	317	Ω
R2	1538	351	351	Ω
V <sub>TH</sub>	0.9	1.5	1.5	V
V <sub>HIGH</sub>	1.8	3	3	V

#### Notes

- 10. Tested initially and after any design or process changes that may affect these parameters.
- 11. Full-device AC operation assumes a 100- $\mu$ s ramp time from 0 to V<sub>CC(min)</sub> and a 100- $\mu$ s wait time after V<sub>CC</sub> stabilization.



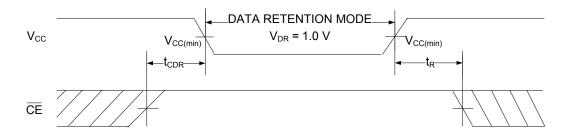
#### **Data Retention Characteristics**

Over the operating range of -40 °C to 85 °C

Parameter	Description	Conditions	Min	Max	Unit
V <sub>DR</sub>	$V_{CC}$ for data retention		1	-	V
I <sub>CCDR</sub>	Data retention current	$V_{CC} = 1.2 \text{ V}, \overline{CE} \ge V_{CC} - 0.2 \text{ V}^{[13]}, V_{IN} \ge V_{CC} - 0.2 \text{ V}, \text{ or } V_{IN} \le 0.2 \text{ V}$	-	8	mA
t <sub>CDR</sub> <sup>[12]</sup>	Chip deselect to data retention time		0	-	ns
t <sub>R</sub> <sup>[12, 13]</sup>	Operation recovery time	$V_{CC} \ge 2.2 V$	10	-	ns
		V <sub>CC</sub> < 2.2 V	15	_	ns

### **Data Retention Waveform**

#### Figure 5. Data Retention Waveform<sup>[13]</sup>



#### Notes

12. These parameters are guaranteed by design. 13. Full-device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub>  $\geq$  100 µs or stable at V<sub>CC (min)</sub>  $\geq$  100 µs.



# **AC Switching Characteristics**

Over the operating range of -40 °C to 85 °C

Parameter [14]	Description	10	ns	15	ns	11
Parameter	Description	Min	Max	Min	Мах	– Unit
Read Cycle				•		•
t <sub>RC</sub>	Read cycle time	10	-	15	_	ns
t <sub>AA</sub>	Address to data / ERR valid	-	10	-	15	ns
t <sub>OHA</sub>	Data / ERR hold from address change	3	_	3	_	ns
t <sub>ACE</sub>	CE LOW to data / ERR valid	-	10	-	15	ns
t <sub>DOE</sub>	OE LOW to data / ERR valid	-	4.5	-	8	ns
t <sub>LZOE</sub>	OE LOW to low impedance <sup>[15]</sup>	0	_	0	_	ns
t <sub>HZOE</sub>	OE HIGH to HI-Z <sup>[15]</sup>	-	5	-	8	ns
t <sub>LZCE</sub>	CE LOW to low impedance <sup>[15]</sup>	3	_	3	_	ns
t <sub>HZCE</sub>	CE HIGH to HI-Z <sup>[15]</sup>	-	5	-	8	ns
t <sub>PU</sub>	CE LOW to power-up <sup>[16, 17]</sup>	0	_	0	_	ns
t <sub>PD</sub>	CE HIGH to power-down <sup>[16, 17]</sup>	-	10	-	15	ns
Write Cycle [1]	7, 18]					
t <sub>WC</sub>	Write cycle time	10	-	15	_	ns
t <sub>SCE</sub>	CE LOW to write end	7	-	12	_	ns
t <sub>AW</sub>	Address setup to write end	7	-	12	_	ns
t <sub>HA</sub>	Address hold from write end	0	_	0	_	ns
t <sub>SA</sub>	Address setup to write start	0	-	0	_	ns
t <sub>PWE</sub>	WE pulse width	7	_	12	_	ns
t <sub>SD</sub>	Data setup to write end	5	_	8	_	ns
t <sub>HD</sub>	Data hold from write end	0	-	0	_	ns
t <sub>LZWE</sub>	WE HIGH to low impedance <sup>[15]</sup>	3	-	3	_	ns
t <sub>HZWE</sub>	WE LOW to HI-Z <sup>[15]</sup>	_	5	_	8	ns

Notes

- 14. Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for  $V_{CC} \ge 3$  V) and  $V_{CC}/2$  (for  $V_{CC} \le 3$  V), and input pulse levels of 0 to 3 V (for  $V_{CC} \ge 3$  V) and 0 to  $V_{CC}$  (for  $V_{CC} \le 3$  V). Test conditions for the read cycle use output loading, as shown in part (a) of Figure 4 on page 7, unless specified otherwise.
- 15. t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZOE</sub>, t<sub>LZOE</sub>, t<sub>LZOE</sub>, t<sub>LZOE</sub>, and t<sub>LZWE</sub> are specified with a load capacitance of 5 pF, as shown in part (b) of Figure 4 on page 7. Transition is measured ±200 mV from steady state voltage.

16. These parameters are guaranteed by design and are not tested.

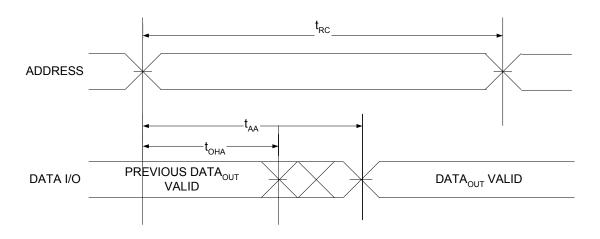
17. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{|L}$ ,  $\overline{CE} = V_{|L}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

18. The minimum write cycle pulse width in Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be equal to sum of  $t_{\overline{DS}}$  and  $t_{HZWE}$ .

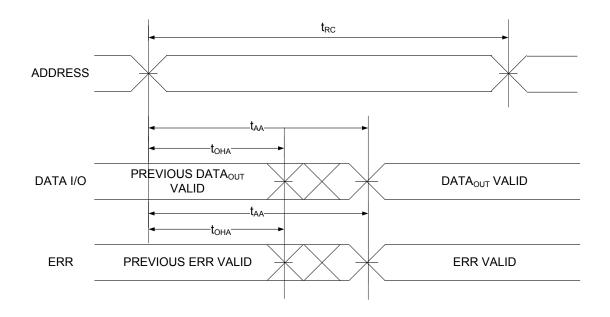


#### **Switching Waveforms**







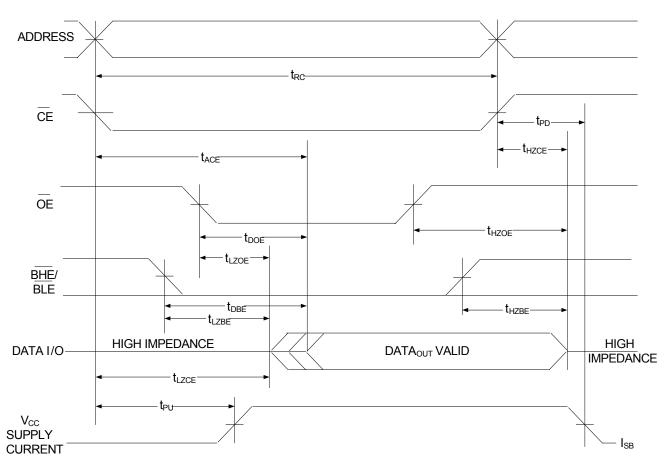


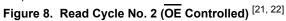
Notes

19. The device is continuously selected,  $\overline{OE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ . 20.  $\overline{WE}$  is HIGH for the read cycle.



#### Switching Waveforms (continued)



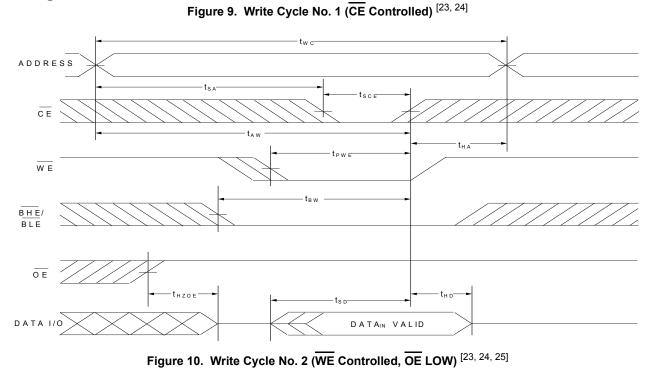


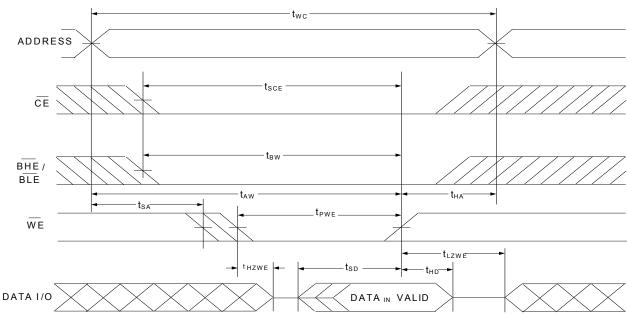
 $\begin{array}{l} \textbf{Notes} \\ \textbf{21. WE} \text{ is HIGH for the read cycle.} \end{array}$ 

22. Address valid prior to or coincident with  $\overline{CE}$  LOW transition.



#### Switching Waveforms (continued)





- **Notes** 23. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 24. Data I/O is in HI-Z state if  $\overline{CE} = V_{IH}$ , or  $\overline{OE} = V_{IH}$ .

25. The minimum write cycle pulse width should be equal to sum of  $t_{\text{SD}}$  and  $t_{\text{HZWE}}$ .



#### Switching Waveforms (continued)

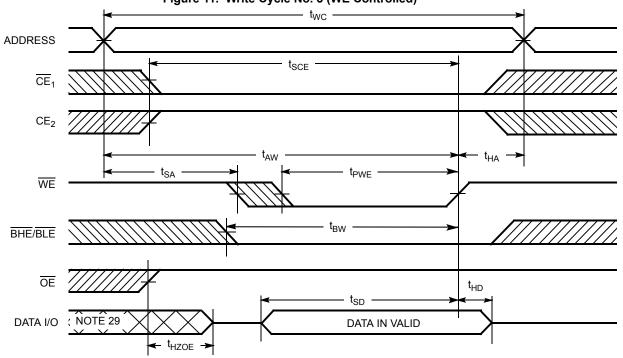


Figure 11. Write Cycle No. 3 (WE Controlled) <sup>[26, 27, 28]</sup>

Notes

26. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write. 27. Data I/O is in HI-Z state if  $\overline{CE} = V_{IH}$ , or  $\overline{OE} = V_{IH}$ .

28. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ . 29. During this period the I/Os are in output state. Do not apply input signals.



#### **Truth Table**

CE	OE	WE	I/O <sub>0</sub> -I/O <sub>7</sub>	Mode	Power
Н	X <sup>[30]</sup>	X <sup>[30]</sup>	HI-Z	Power down	Standby (I <sub>SB</sub> )
L	L	Н	Data out	Read all bits	Active (I <sub>CC</sub> )
L	Х	L	Data in	Write all bits	Active (I <sub>CC</sub> )
L	Н	Н	HI-Z	Selected, outputs disabled	Active (I <sub>CC</sub> )

### ERR Output – CY7C1049GE

Output <sup>[31]</sup>	Mode			
0	Read operation, no single-bit error in the stored data.			
1	Read operation, single-bit error detected and corrected.			
HI-Z	Device deselected or outputs disabled or Write operation.			

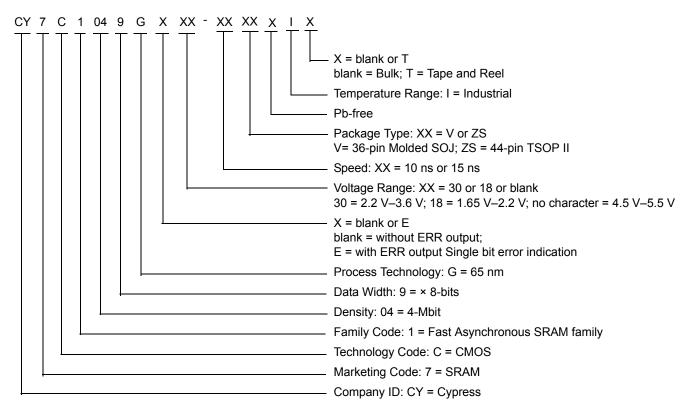
 $<sup>\</sup>begin{array}{l} \textbf{Notes} \\ \textbf{30. The input voltage levels on these pins should be either at V_{IH} or V_{IL}. \\ \textbf{31. ERR pin is an output pin. It should be left floating when not used.} \end{array}$ 



### **Ordering Information**

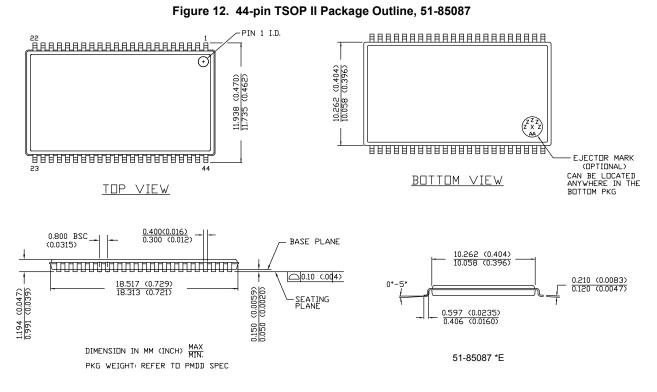
Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (all Pb-free)	Operating Range
10	2.2 V–3.6 V	CY7C1049G30-10VXI	51-85090	36-pin Molded SOJ	Industrial
		CY7C1049G30-10VXIT	51-85090	36-pin Molded SOJ, Tape and Reel	
		CY7C1049GE30-10ZSXI	51-85087	44-pin TSOP II, ERR output	
		CY7C1049GE30-10ZSXIT	51-85087	44-pin TSOP II, ERR output, Tape and Reel	
		CY7C1049G30-10ZSXI	51-85087	44-pin TSOP II	
		CY7C1049G30-10ZSXIT	51-85087	44-pin TSOP II, Tape and Reel	
15	1.65 V–2.2 V	CY7C1049G18-15ZSXI	51-85087	44-pin TSOP II	
		CY7C1049G18-15ZSXIT	51-85087	44-pin TSOP II, Tape and Reel	
10	4.5 V–5.5 V	CY7C1049G-10VXI	51-85090	36-pin Molded SOJ	
		CY7C1049G-10VXIT	51-85090	36-pin Molded SOJ, Tape and Reel	
		CY7C1049G-10ZSXI	51-85087	44-pin TSOP II	
		CY7C1049G-10ZSXIT	51-85087	44-pin TSOP II, Tape and Reel	

#### **Ordering Code Definitions**

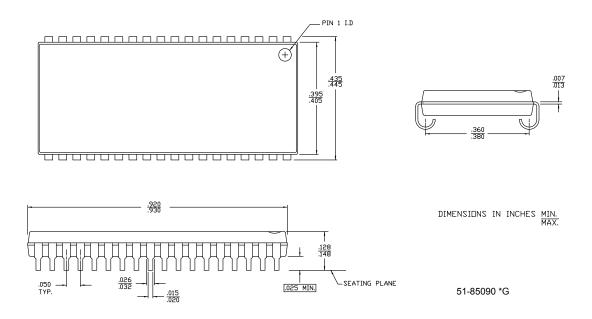




#### Package Diagrams









# Acronyms

Acronym	Description
BHE	Byte High Enable
BLE	Byte Low Enable
CE	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
OE	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
WE	Write Enable

#### **Document Conventions**

#### **Units of Measure**

Symbol	Unit of Measure
°C	degrees Celsius
MHz	megahertz
μA	microampere
μS	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt



# **Document History Page**

	ocument Title: CY7C1049G/CY7C1049GE, 4-Mbit (512K words × 8 bit) Static RAM with Error-Correcting Code (ECC) ocument Number: 001-95412				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change	
**	4685774	VINI	03/13/2015	New data sheet.	
*A	4831087	NILE	07/10/2015	Updated Package Diagrams: Added spec 51-85090 *G (Figure 13). Removed spec 51-85082 *E. Removed spec 51-85150 *H.	
*В	4968879	NILE	10/16/2015	Fixed typo in bookmarks.	
*C	5020573	VINI	11/25/2015	Changed status from Preliminary to Final. Updated Pin Configurations: Removed figure "36-pin SOJ Single Chip Enable with ERR CY7C1049GE". Updated Ordering Information: Updated part numbers.	
*D	5429076	NILE	09/07/2016	Updated Maximum Ratings: Updated Note 7 (Replaced "2 ns" with "20 ns"). Updated DC Electrical Characteristics: Removed Operating Range "2.7 V to 3.6 V" and all values corresponding to $V_{OH}$ parameter. Included Operating Ranges "2.7 V to 3.0 V" and "3.0 V to 3.6 V" and all values corresponding to $V_{OH}$ parameter. Changed minimum value of $V_{IH}$ parameter from 2.2 V to 2 V corresponding to Operating Range "4.5 V to 5.5 V". Updated Ordering Information: Updated part numbers. Updated to new template.	



#### Sales, Solutions, and Legal Information

#### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

#### Products

ARM <sup>®</sup> Cortex <sup>®</sup> Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Lighting & Power Control	cypress.com/powerpsoc
Memory	cypress.com/memory
PSoC	cypress.com/psoc
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless/RF	cypress.com/wireless

PSoC<sup>®</sup>Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community Forums | Projects | Video | Blogs | Training | Components

Technical Support cypress.com/support

© Cypress Semiconductor Corporation, 2015-2016. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and other sont, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infinged by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

Document Number: 001-95412 Rev. \*D