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Cypress Embedded in Tomorrow™

CY7C1061G/CY7C1061GE

16-Mbit (1M words × 16 bit) Static RAM with Error-Correcting Code (ECC)

Features

- High speed
  - t_{AA} = 10 ns/15 ns
- Embedded error-correcting code (ECC) for single-bit error correction
- Low active and standby currents
  - I_{CC} = 90 mA typical at 100 MHz
  - I_{SB2} = 20 mA typical
- Operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, and 4.5 V to 5.5 V
- 1.0 V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Error indication (ERR) pin to indicate 1-bit error detection and correction
- Available in Pb-free 48-pin TSOP I, 54-pin TSOP II, and 48-ball VFBGA packages

Functional Description

CY7C1061G and CY7C1061GE are high-performance CMOS fast static RAM devices with embedded ECC[1]. Both devices are offered in single and dual chip enable options and in multiple pin configurations. The CY7C1061GE device includes an ERR pin that signals a single-bit error-detection and correction event during a read cycle.

To access devices with a single chip enable input, assert the chip enable ($\overline{CE}$) input LOW. To access dual chip enable devices, assert both chip enable inputs – $\overline{CE}_1$ as LOW and CE_2 as HIGH.

To perform data writes, assert the Write Enable ($\overline{WE}$) input LOW, and provide the data and address on the device data pins (I/O_0 through I/O_{15}) and address pins (A_0 through A_{19}) respectively. The Byte High Enable ($\overline{BHE}$) and Byte Low Enable ($\overline{BLE}$) inputs control byte writes, and write data on the corresponding I/O lines to the memory location specified. $\overline{BHE}$ controls I/O_8 through I/O_{15} and $\overline{BLE}$ controls I/O_0 through I/O_7.

To perform data reads, assert the Output Enable ($\overline{OE}$) input and provide the required address on the address lines. Read data is accessible on I/O lines (I/O_0 through I/O_{15}). You can perform byte accesses by asserting the required byte enable signal ($\overline{BHE}$ or $\overline{BLE}$) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH for a single chip enable device and $\overline{CE}_1$ HIGH / CE_2 LOW for a dual chip enable device), or control signals are de-asserted ($\overline{OE}$, $\overline{BLE}$, $\overline{BHE}$).

On the CY7C1061GE devices, the detection and correction of a single-bit error in the accessed location is indicated by the assertion of the ERR output (ERR = High). See the Truth Table on page 16 for a complete description of read and write modes.

The logic block diagrams are on page 2.

The CY7C1061G and CY7C1061GE devices are available in 48-pin TSOP I, 54-pin TSOP II, and 48-ball VFBGA packages.

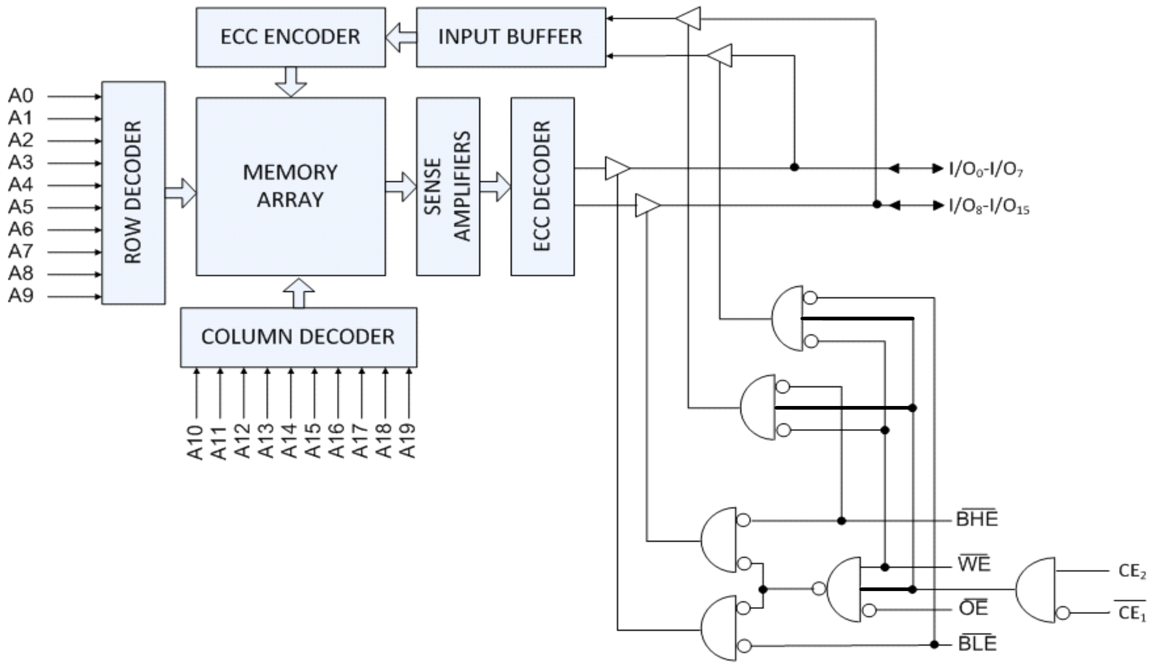
For a complete list of related documentation, click here.

Product Portfolio

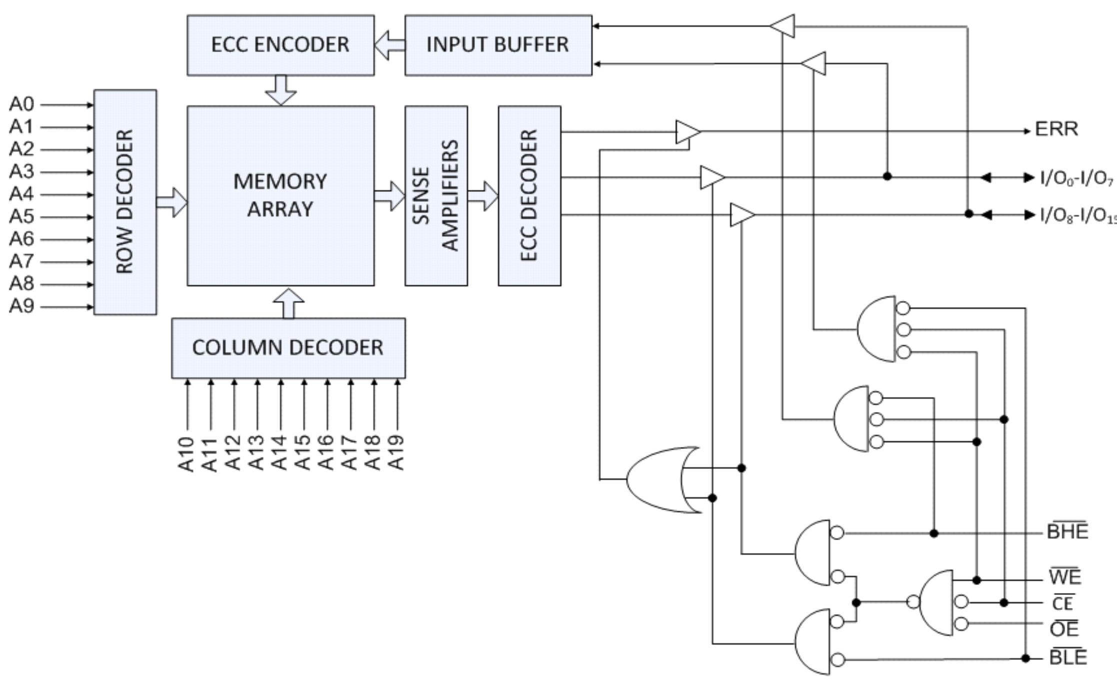
Product	Features and Options (see Pin Configurations on page 4)	Range	V_{CC} Range (V)	Speed (ns) 10/15	Current Consumption			
					Operating I_{CC}, (mA) f = f_{max}		Standby, I_{SB2} (mA)	
					Typ[2]	Max	Typ[2]	Max
CY7C1061G18	Single or dual chip enables	Industrial	1.65 V–2.2 V	15	70	80	20	30
CY7C1061G(E)30	Optional ERR pins		2.2 V–3.6 V	10	90	110		
CY7C1061G	Address MSB A_{19} pin placement options compatible with Cypress and other vendors		4.5 V–5.5 V	10	90	110		

Notes
1. This device does not support automatic write-back on error detection.
2. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for a V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for a V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for a V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.

Logic Block Diagram – CY7C1061G



Logic Block Diagram – CY7C1061GE



Contents

Pin Configurations

Figure 1. 48-ball VFBGA (6 × 8 × 1.0 mm) Pinout, Dual Chip Enable without ERR, Address MSB A19 at Ball G2, CY7C1061G[3] Package/Grade ID: BVJXI

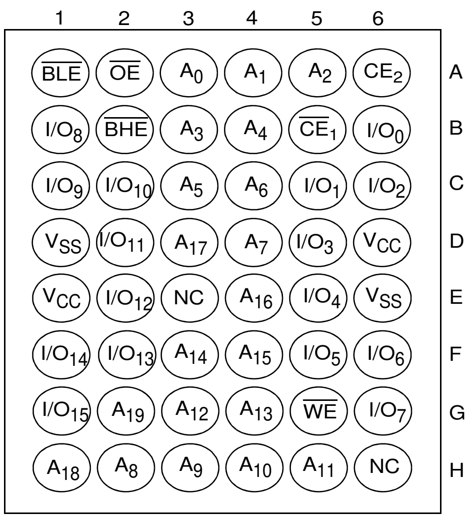


Figure 2. 48-ball VFBGA (6 × 8 × 1.0 mm) Pinout, Dual Chip Enable without ERR, Address MSB A19 at Ball H6, CY7C1061G[3] Package/Grade ID: BVXI

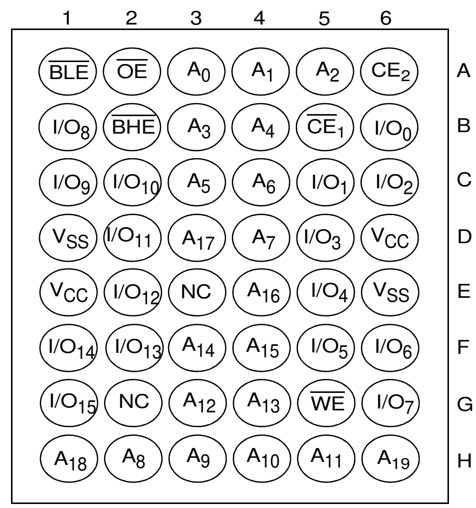
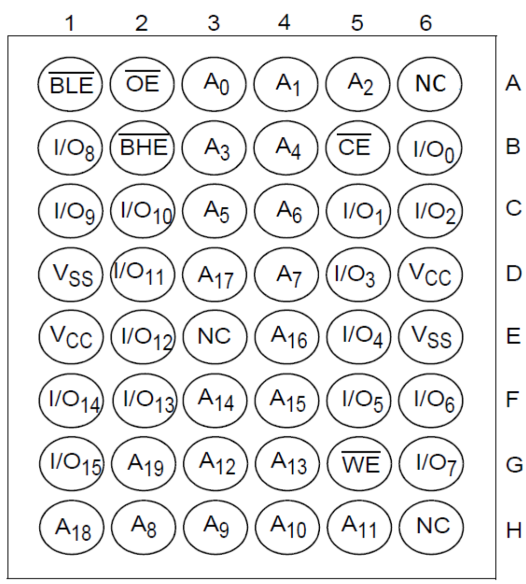


Figure 3. 48-ball VFBGA (6 × 8 × 1.0 mm) Pinout, Single Chip Enable without ERR, Address MSB A19 at Ball G2, CY7C1061G[3] Package/Grade ID: BV1XI



Note
3. NC pins are not connected internally to the die.

Pin Configurations (continued)

Figure 4. 48-ball VFBGA (6 × 8 × 1.0 mm) Pinout, Single Chip Enable with ERR, Address MSB A19 at Ball G2, CY7C1061GE[4, 5] Package/Grade ID: BV1XI

	1	2	3	4	5	6
A	$\overline{BLE}$	$\overline{OE}$	A_0	A_1	A_2	ERR
B	I/O_8	$\overline{BHE}$	A_3	A_4	$\overline{CE}$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2
D	V_{SS}	I/O_{11}	A_{17}	A_7	I/O_3	V_{CC}
E	V_{CC}	I/O_{12}	NC	A_{16}	I/O_4	V_{SS}
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	A_{19}	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	A_{18}	A_8	A_9	A_{10}	A_{11}	NC

Figure 5. 48-ball VFBGA (6 × 8 × 1.0 mm) Pinout, Dual Chip Enable with ERR, Address MSB A19 at Ball G2, CY7C1061GE[4, 5] Package/Grade ID: BVJXI

	1	2	3	4	5	6
A	$\overline{BLE}$	$\overline{OE}$	A_0	A_1	A_2	CE_2
B	I/O_8	$\overline{BHE}$	A_3	A_4	$\overline{CE}_1$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2
D	V_{SS}	I/O_{11}	A_{17}	A_7	I/O_3	V_{CC}
E	V_{CC}	I/O_{12}	ERR	A_{16}	I/O_4	V_{SS}
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	A_{19}	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	A_{18}	A_8	A_9	A_{10}	A_{11}	NC

Figure 6. 48-ball VFBGA (6 × 8 × 1.0 mm) Pinout, Dual Chip Enable with ERR, Address MSB A19 at Ball H6, CY7C1061GE[4, 5] Package/Grade ID: BVXI

	1	2	3	4	5	6
A	$\overline{BLE}$	$\overline{OE}$	A_0	A_1	A_2	CE_2
B	I/O_8	$\overline{BHE}$	A_3	A_4	$\overline{CE}_1$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2
D	V_{SS}	I/O_{11}	A_{17}	A_7	I/O_3	V_{CC}
E	V_{CC}	I/O_{12}	ERR	A_{16}	I/O_4	V_{SS}
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	A_{18}	A_8	A_9	A_{10}	A_{11}	A_{19}

Notes
4. NC pins are not connected internally to the die.
5. ERR is an Output pin. If not used, this pin should be left floating.

Pin Configurations (continued)

Figure 7. 48-pin TSOP I (12 × 18.4 × 1 mm) Pinout, Single Chip Enable with ERR, CY7C1061GE[6, 7] Package/Grade ID: ZXI

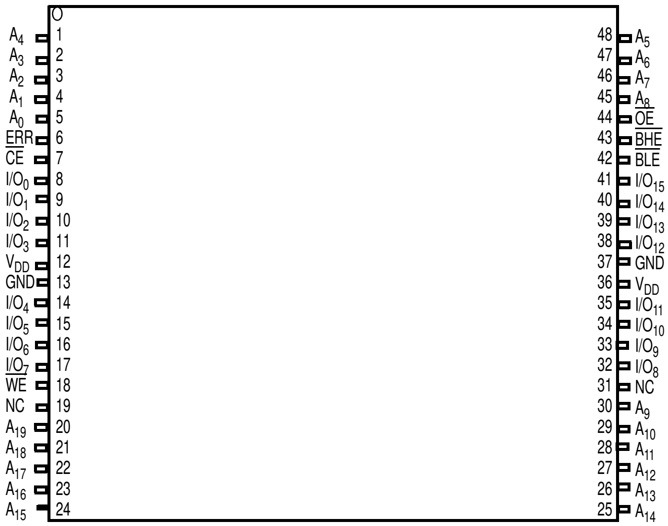


Figure 8. 48-pin TSOP I (12 × 18.4 × 1 mm) Pinout, Single Chip Enable without ERR, CY7C1061G[6] Package/Grade ID: ZXI

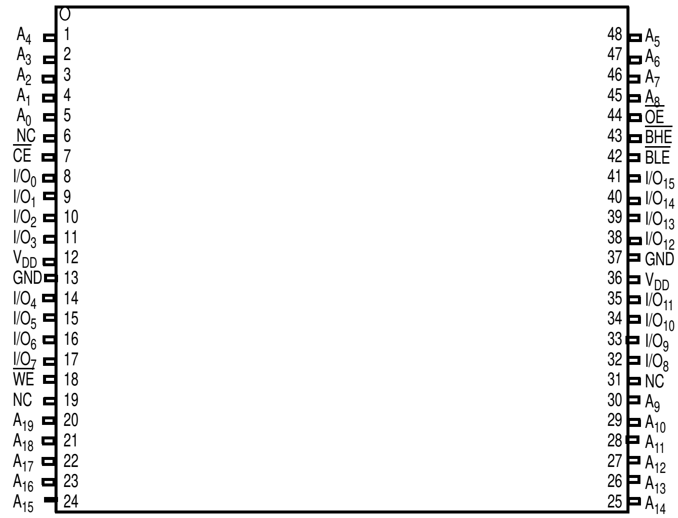


Figure 9. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) pinout, Dual Chip Enable without ERR, CY7C1061G[6] Package/Grade ID: ZSXI

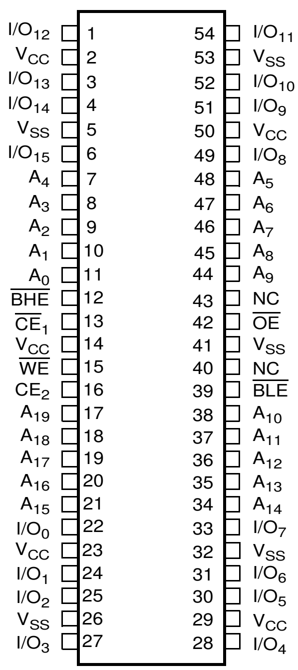
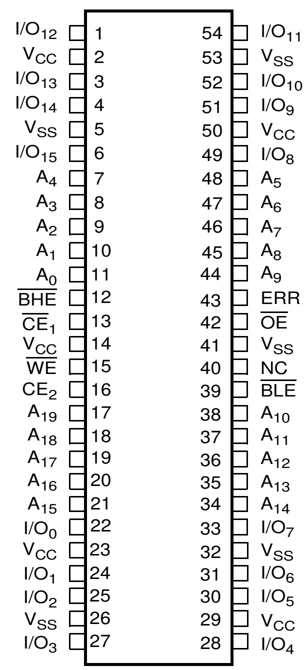


Figure 10. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) pinout, Dual Chip Enable with ERR, CY7C1061GE[6, 7] Package/Grade ID: ZSXI



Notes
6. NC pins are not connected internally to the die.
7. ERR is an Output pin. If not used, this pin should be left floating.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Ambient temperature
with power applied .... –55 °C to +125 °C

Supply voltage
on V_{CC} relative to GND .... –0.5 V to V_{CC} + 0.5 V

DC voltage applied to outputs
in High Z State [8] .... –0.5 V to V_{CC} + 0.5 V

DC input voltage[8] .... –0.5 V to V_{CC} + 0.5 V

Current into outputs (LOW) .... 20 mA

Static discharge voltage
(MIL-STD-883, Method 3015) .... > 2001 V

Latch-up current .... > 140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

DC Electrical Characteristics

Over the operating range of –40 °C to 85 °C

Parameter	Description		Test Conditions	10 ns / 15 ns			Unit
				Min	Typ [9]	Max	
V_{OH}	Output HIGH voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OH} = –0.1 mA	1.4	–	–	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –1.0 mA	2.0	–	–	
		2.7 V to 3.0 V	V_{CC} = Min, I_{OH} = –4.0 mA	2.2	–	–	
		3.0 V to 3.6 V	V_{CC} = Min, I_{OH} = –4.0 mA	2.4	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –4.0 mA	2.4	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –0.1 mA	V_{CC} – 0.4 [10]	–	–	
V_{OL}	Output LOW voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OL} = 0.1 mA	–	–	0.2	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 2 mA	–	–	0.4	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 8 mA	–	–	0.4	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OL} = 8 mA	–	–	0.4	
V_{IH}[8]	Input HIGH voltage	1.65 V to 2.2 V		1.4	–	V_{CC} + 0.2	V
		2.2 V to 2.7 V		2.0	–	V_{CC} + 0.3	
		2.7 V to 3.6 V		2.0	–	V_{CC} + 0.3	
		4.5 V to 5.5 V		2.0	–	V_{CC} + 0.5	
V_{IL}[8]	Input LOW voltage	1.65 V to 2.2 V		–0.2	–	0.4	V
		2.2 V to 2.7 V		–0.3	–	0.6	
		2.7 V to 3.6 V		–0.3	–	0.8	
		4.5 V to 5.5 V		–0.5	–	0.8	
I_{IX}	Input leakage current		GND ≤ V_{IN} ≤ V_{CC}	–1.0	–	+1.0	µA
I_{OZ}	Output leakage current		GND ≤ V_{OUT} ≤ V_{CC}, Output disabled	–1.0	–	+1.0	µA
I_{CC}	Operating supply current		V_{CC} = Max, I_{OUT} = 0 mA, CMOS levels; f = 100 MHz	–	90.0	110.0	mA
			f = 66.7 MHz	–	70.0	80.0	
I_{SB1}	Automatic CE power down current – TTL inputs		Max V_{CC}, $\overline{CE}$ ≥ V_{IH} [11], V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	–	–	40.0	mA
I_{SB2}	Automatic CE power down current – CMOS inputs		Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.2 V[11], V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0	–	20.0	30.0	mA

Notes

8. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 20 ns.
9. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for a V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for a V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for a V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.
10. This parameter is guaranteed by design and is not tested.
11. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.

Capacitance

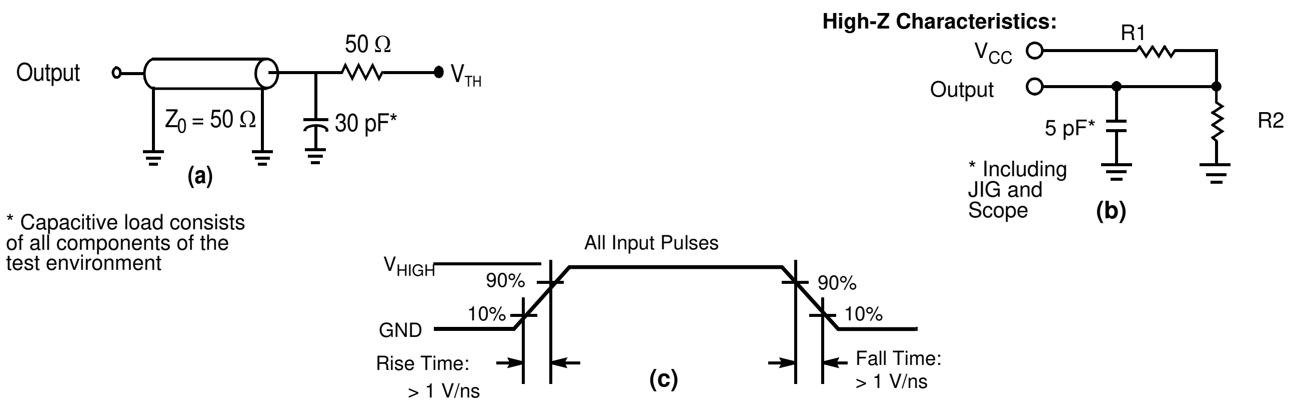
Parameter [12]	Description	Test Conditions	54-pin TSOP II	48-ball VFBGA	48-pin TSOP I	Unit
C_{IN}	Input capacitance	$T_A = 25\ °C$, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	10	10	pF
C_{OUT}	I/O capacitance		10	10	10	pF

Thermal Resistance

Parameter [12]	Description	Test Conditions	54-pin TSOP II	48-ball VFBGA	48-pin TSOP I	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	93.63	31.50	57.99	°C/W
Θ_{JC}	Thermal resistance (junction to case)		21.58	15.75	13.42	°C/W

AC Test Loads and Waveforms

Figure 11. AC Test Loads and Waveforms[13]



Parameters	1.8 V	3.0 V	5.0 V	Unit
R1	1667	317	317	Ω
R2	1538	351	351	Ω
V_{TH}	0.9	1.5	1.5	V
V_{HIGH}	1.8	3	3	V

Notes
12. Tested initially and after any design or process changes that may affect these parameters.
13. Full-device AC operation assumes a 100-µs ramp time from 0 to V_{CC} (min) and 100-µs wait time after V_{CC} stabilizes to its operational value.

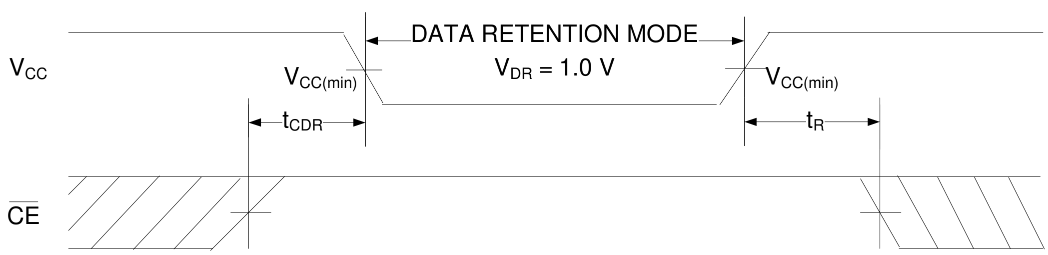
Data Retention Characteristics

Over the operating range of –40 °C to 85 °C

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention		1.0	–	V
I_{CCDR}	Data retention current	$V_{CC} = V_{DR}$, $\overline{CE} \geq V_{CC} - 0.2$ V[14], $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	30.0	mA
t_{CDR}[15]	Chip deselect to data retention time		0	–	ns
t_R[15, 16]	Operation recovery time	$V_{CC} \geq 2.2$ V	10.0	–	ns
		$V_{CC} < 2.2$ V	15.0	–	ns

Data Retention Waveform

Figure 12. Data Retention Waveform [14]



Notes

14. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
15. This parameter is guaranteed by design and is not tested
16. Full-device operation requires linear V_{CC} ramp from V_{DR} to V_{CC} (min) $\geq$ 100 µs or stable at V_{CC} (min) $\geq$ 100 µs.

AC Switching Characteristics

Over the operating range of –40 °C to 85 °C

Parameter [17]	Description	10 ns		15 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{POWER}	V_{CC} (stable) to the first access [18, 19]	100.0	–	100.0	–	µs
t_{RC}	Read cycle time	10.0	–	15.0	–	ns
t_{AA}	Address to data / ERR valid	–	10.0	–	15.0	ns
t_{OHA}	Data / ERR hold from address change	3.0	–	3.0	–	ns
t_{ACE}	$\overline{CE}$ LOW to data / ERR valid [20]	–	10.0	–	15.0	ns
t_{DOE}	$\overline{OE}$ LOW to data / ERR valid	–	5.0	–	8.0	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [21, 22, 23]	0	–	1.0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [21, 22, 23]	–	5.0	–	8.0	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z [20, 21, 22, 23]	3.0	–	3.0	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z [20, 21, 22, 23]	–	5.0	–	8.0	ns
t_{PU}	$\overline{CE}$ LOW to power-up [19, 20]	0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down [19, 20]	–	10.0	–	15.0	ns
t_{DBE}	Byte enable to data valid	–	5.0	–	8.0	ns
t_{LZBE}	Byte enable to low Z [21, 22]	0	–	1.0	–	ns
t_{HZBE}	Byte disable to high Z [21, 22]	–	6.0	–	8.0	ns
Write Cycle [24, 25]						
t_{WC}	Write cycle time	10.0	–	15.0	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end [20]	7.0	–	12.0	–	ns
t_{AW}	Address setup to write end	7.0	–	12.0	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	7.0	–	12.0	–	ns
t_{SD}	Data setup to write end	5.0	–	8.0	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [21, 22, 23]	3.0	–	3.0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [21, 22, 23]	–	5.0	–	8.0	ns
t_{BW}	Byte Enable to write end	7.0	–	12.0	–	ns

Notes

17. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$V). Test conditions for the read cycle use the output loading, shown in part (a) of Figure 11 on page 8, unless specified otherwise.
18. t_{POWER} gives the minimum amount of time that the power supply is at stable V_{CC} until the first memory access is performed.
19. These parameters are guaranteed by design and are not tested.
20. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
21. t_{HZOE}, t_{HZCE}, t_{HZWE}, and t_{HZBE} are specified with a load capacitance of 5 pF, as shown in part (b) of Figure 11 on page 8. Hi-Z, Lo-Z transition is measured ±200 mV from steady state voltage.
22. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
23. Tested initially and after any design or process changes that may affect these parameters.
24. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$, and $\overline{BHE}$ or $\overline{BLE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
25. The minimum write pulse width for Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 13. Read Cycle No. 1 of CY7C1061G (Address Transition Controlled) [26, 27]

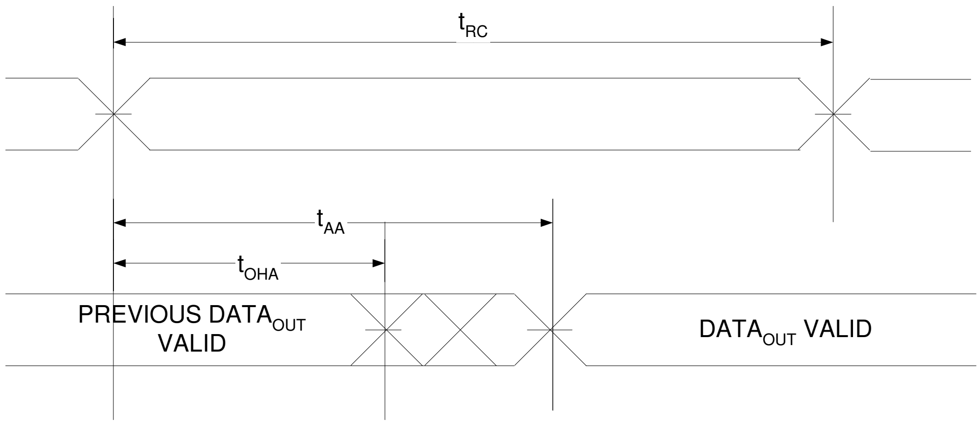
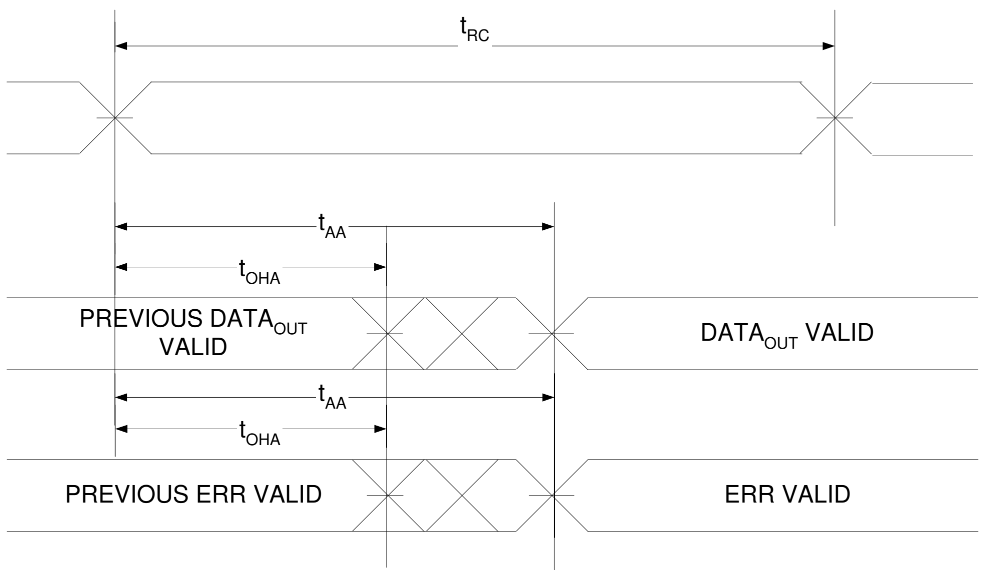


Figure 14. Read Cycle No. 2 of CY7C1061GE (Address Transition Controlled) [26, 27]

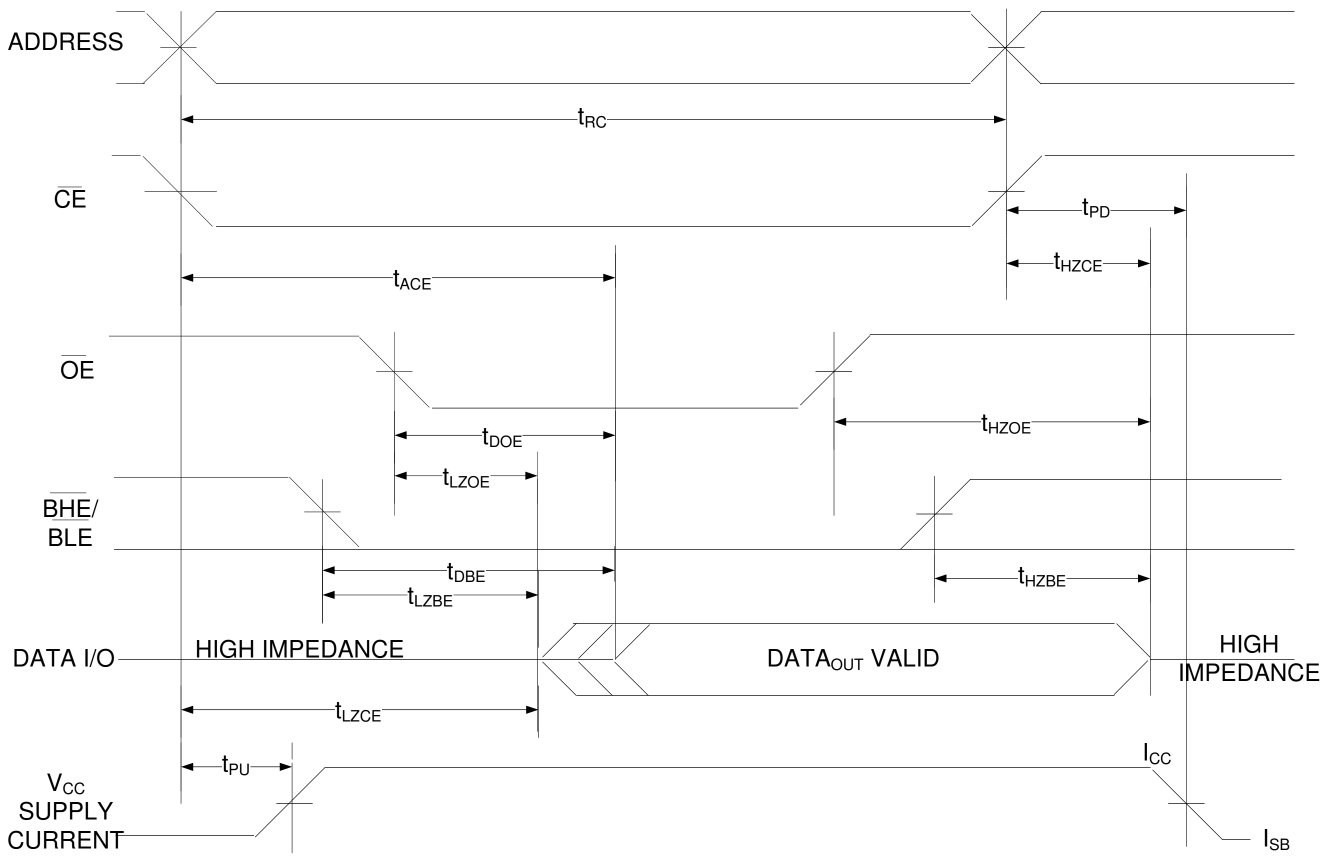


Notes

26. The device is continuously selected, $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}.
27. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Figure 15. Read Cycle No. 3 ($\overline{OE}$ Controlled) [28, 29, 30]



Notes
28. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
29. $\overline{WE}$ is HIGH for read cycle.
30. Address valid prior to or coincident with $\overline{CE}$ LOW transition.

Switching Waveforms (continued)

Figure 16. Write Cycle No. 1 ($\overline{CE}$ Controlled) [31, 32, 33]

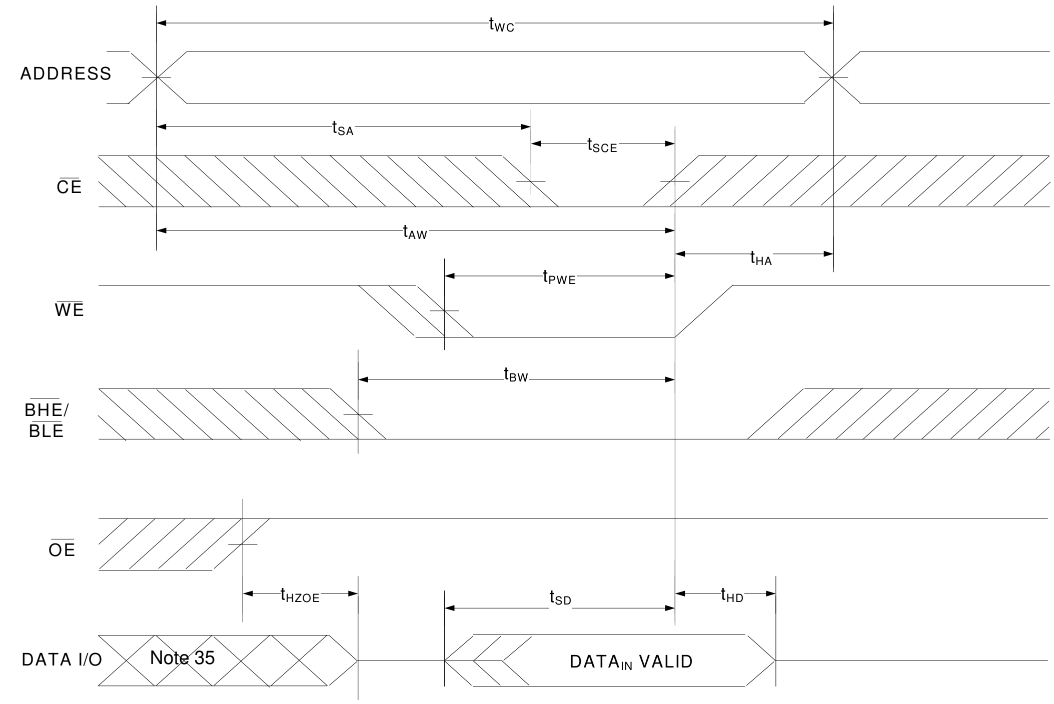
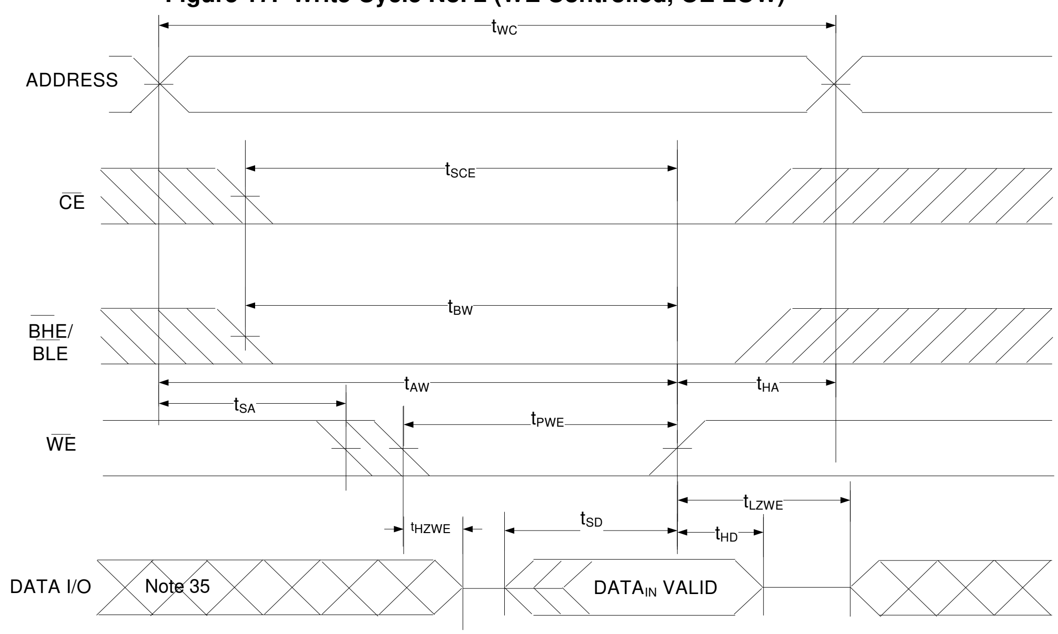


Figure 17. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [31, 32, 33, 34]

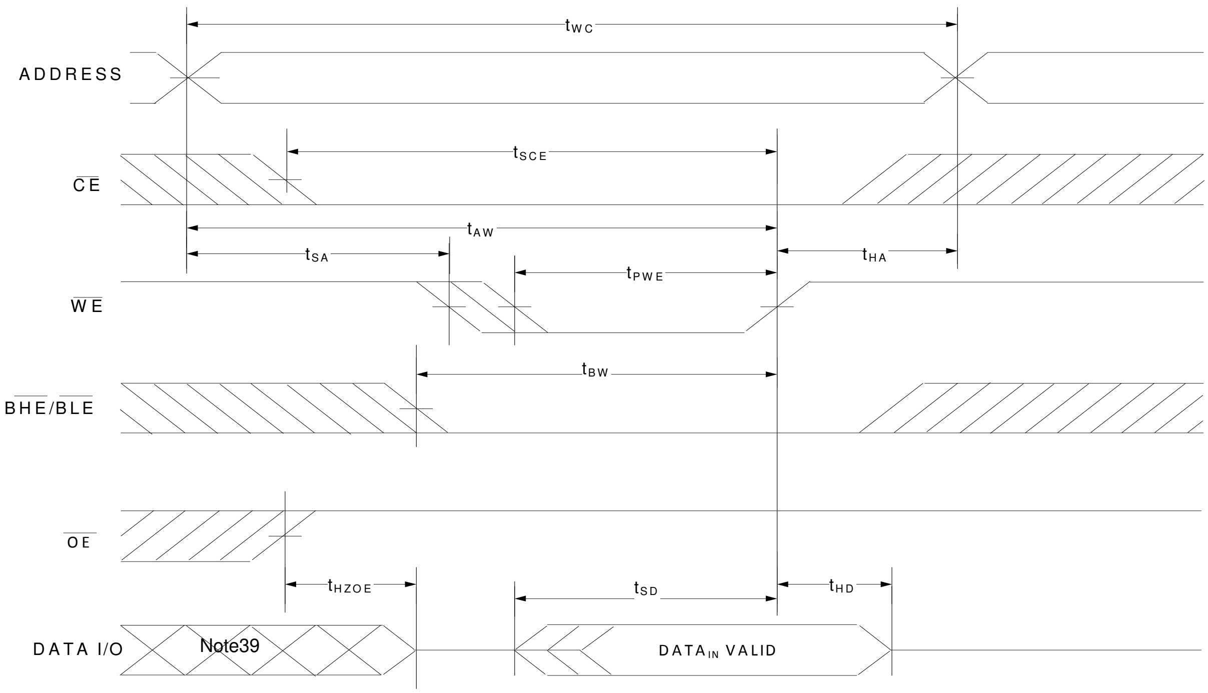


Notes

31. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
32. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL} and $\overline{BHE}$ or $\overline{BLE}$ = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
33. Data I/O is in high-impedance state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH} or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
34. The minimum write cycle pulse width should be equal to sum of t_{HZWE} and t_{SD}.
35. During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 18. Write Cycle No. 3 ($\overline{WE}$ Controlled) [36, 37, 38]

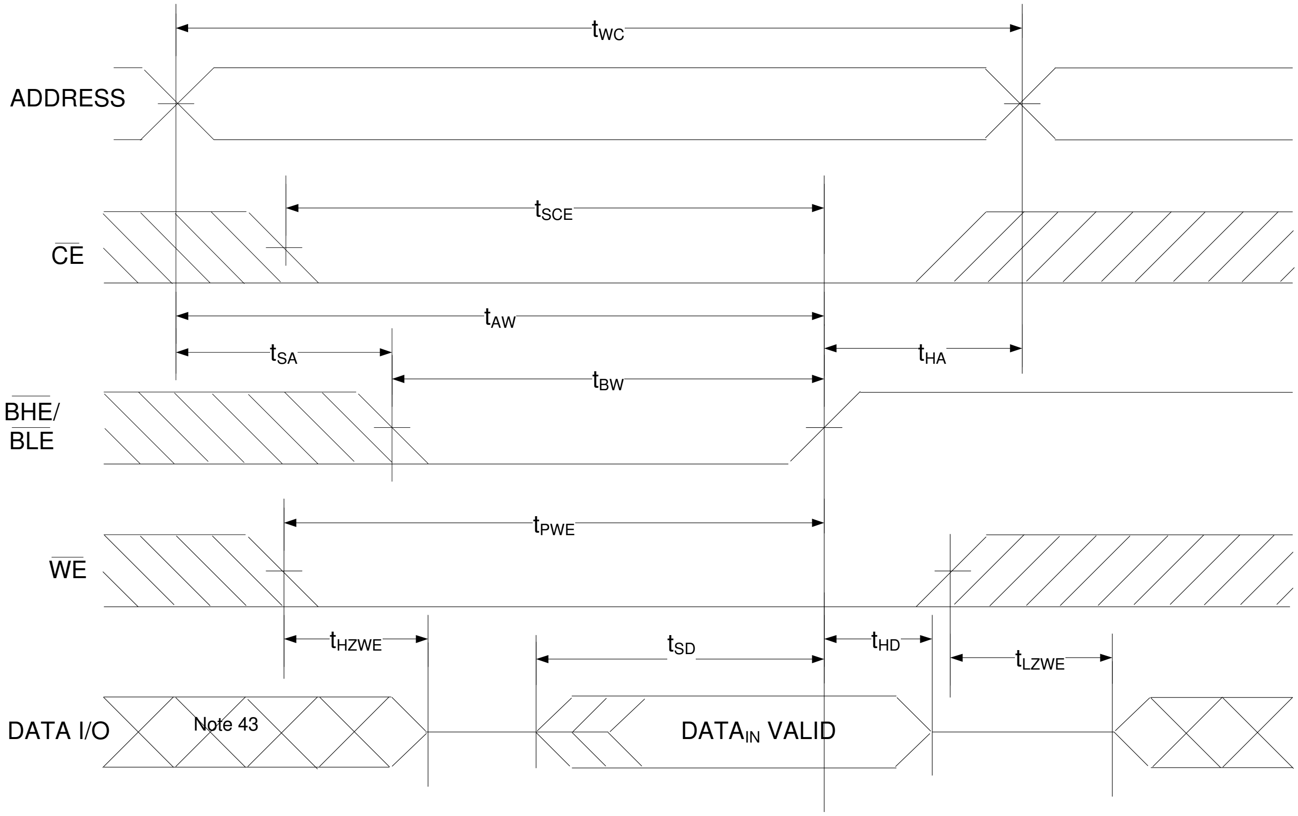


Notes

36. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
37. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$ and $\overline{BHE}$ or $\overline{BLE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
38. Data I/O is in high-impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.
39. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 19. Write Cycle No. 4 ($\overline{BLE}$ or $\overline{BHE}$ Controlled) [40, 41, 42]



Notes

40. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
41. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL} and $\overline{BHE}$ or $\overline{BLE}$ = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
42. Data I/O is in high-impedance state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH} or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
43. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE}$ [44]	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_0–I/O_7	I/O_8–I/O_{15}	Mode	Power
H	X[45]	X[45]	X[45]	X[45]	High-Z	High-Z	Power down	Standby (I_{SB})
L	L	H	L	L	Data out	Data out	Read all bits	Active (I_{CC})
L	L	H	L	H	Data out	High-Z	Read lower bits only	Active (I_{CC})
L	L	H	H	L	High-Z	Data out	Read upper bits only	Active (I_{CC})
L	X	L	L	L	Data in	Data in	Write all bits	Active (I_{CC})
L	X	L	L	H	Data in	High-Z	Write lower bits only	Active (I_{CC})
L	X	L	H	L	High-Z	Data in	Write upper bits only	Active (I_{CC})
L	H	H	X	X	High-Z	High-Z	Selected, outputs disabled	Active (I_{CC})
L	X	X	H	H	High-Z	High-Z	Selected, outputs disabled	Active (I_{CC})

ERR Output – CY7C1061GE

Output [46]	Mode
0	Read operation, no single-bit error in the stored data.
1	Read operation, single-bit error detected and corrected.
High-Z	Device deselected or outputs disabled or Write operation

Notes

44. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE_1}$ and CE_2. When $\overline{CE_1}$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE_1}$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
45. The input voltage levels on these pins should be either at V_{IH} or V_{IL}.
46. ERR is an Output pin. If not used, this pin should be left floating.

Ordering Information

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (all Pb-free)	Key Features / Differentiators	ERR Pin / Ball	Operating Range
10	4.5 V–5.5 V	CY7C1061G-10BV1XI	51-85150	48-ball VFBGA	Single Chip Enable, Address MSB A19 at ball G2	No	Industrial
		CY7C1061GE-10BV1XI				Yes	
		CY7C1061G-10BVJXI			Dual Chip Enable, Address MSB A19 at ball G2	No	
		CY7C1061GE-10BVJXI				Yes	
		CY7C1061G-10BVXI			Dual Chip Enable, Address MSB A19 at ball H6	No	
		CY7C1061GE-10BVXI				Yes	
		CY7C1061G-10ZSXI	51-85160	54-pin TSOP II	Dual Chip Enable	No	
		CY7C1061GE-10ZSXI				Yes	
		CY7C1061G-10ZXI	51-85183	48-pin TSOP I	Single Chip Enable	No	
		CY7C1061GE-10ZXI				Yes	
	2.2 V–3.6 V	CY7C1061G30-10BV1XI	51-85150	48-ball VFBGA	Single Chip Enable, Address MSB A19 at ball G2	No	
		CY7C1061GE30-10BV1XI				Yes	
		CY7C1061G30-10BVJXI			Dual Chip Enable, Address MSB A19 at ball G2	No	
		CY7C1061GE30-10BVJXI				Yes	
		CY7C1061G30-10BVXI			Dual Chip Enable, Address MSB A19 at ball H6	No	
		CY7C1061GE30-10BVXI				Yes	
		CY7C1061G30-10ZSXI	51-85160	54-pin TSOP II	Dual Chip Enable	No	
		CY7C1061GE30-10ZSXI				Yes	
		CY7C1061G30-10ZXI	51-85183	48-pin TSOP I	Single Chip Enable	No	
		CY7C1061GE30-10ZXI				Yes	
15	1.65 V–2.2 V	CY7C1061GE18-15BV1XI	51-85150	48-ball VFBGA	Single Chip Enable, Address MSB A19 at ball G2	Yes	
		CY7C1061G18-15BV1XI				No	
		CY7C1061GE18-15BVJXI			Dual Chip Enable, Address MSB A19 at ball G2	Yes	
		CY7C1061G18-15BVJXI				No	
		CY7C1061GE18-15BVXI			Dual Chip Enable, Address MSB A19 at ball H6	Yes	
		CY7C1061G18-15BVXI				No	
		CY7C1061GE18-15ZSXI	51-85160	54-pin TSOP II	Dual Chip Enable	Yes	
		CY7C1061G18-15ZSXI				No	
		CY7C1061GE18-15ZXI	51-85183	48-pin TSOP I	Single Chip Enable	Yes	
		CY7C1061G18-15ZXI				No	

Ordering Information (continued)

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (all Pb-free)	Key Features / Differentiators	ERR Pin / Ball	Operating Range
10	4.5 V–5.5 V	CY7C1061G-10BV1XIT	51-85150	48-ball VFBGA	Single Chip Enable, Address MSB A19 at ball G2, Tape and Reel	No	Industrial
		CY7C1061GE-10BV1XIT				Yes	
		CY7C1061G-10BVJXIT			Dual Chip Enable, Address MSB A19 at ball G2, Tape and Reel	No	
		CY7C1061GE-10BVJXIT				Yes	
		CY7C1061G-10BVXIT			Dual Chip Enable, Address MSB A19 at ball H6, Tape and Reel	No	
		CY7C1061GE-10BVXIT				Yes	
		CY7C1061G-10ZSXIT	51-85160	54-pin TSOP II	Dual Chip Enable, Tape and Reel	No	
		CY7C1061GE-10ZSXIT				Yes	
		CY7C1061G-10ZXIT	51-85183	48-pin TSOP I	Single Chip Enable, Tape and Reel	No	
		CY7C1061GE-10ZXIT				Yes	
	2.2 V–3.6 V	CY7C1061G30-10BV1XIT	51-85150	48-ball VFBGA	Single Chip Enable, Address MSB A19 at ball G2, Tape and Reel	No	
		CY7C1061GE30-10BV1XIT				Yes	
		CY7C1061G30-10BVJXIT			Dual Chip Enable, Address MSB A19 at ball G2, Tape and Reel	No	
		CY7C1061GE30-10BVJXIT				Yes	
		CY7C1061G30-10BVXIT			Dual Chip Enable, Address MSB A19 at ball H6, Tape and Reel	No	
		CY7C1061GE30-10BVXIT				Yes	
		CY7C1061G30-10ZSXIT	51-85160	54-pin TSOP II	Dual Chip Enable, Tape and Reel	No	
		CY7C1061GE30-10ZSXIT				Yes	
		CY7C1061G30-10ZXIT	51-85183	48-pin TSOP I	Single Chip Enable, Tape and Reel	No	
		CY7C1061GE30-10ZXIT				Yes	
15	1.65 V–2.2 V	CY7C1061GE18-15BV1XIT	51-85150	48-ball VFBGA	Single Chip Enable, Address MSB A19 at ball G2, Tape and Reel	Yes	
		CY7C1061G18-15BV1XIT				No	
		CY7C1061GE18-15BVJXIT			Dual Chip Enable, Address MSB A19 at ball G2, Tape and Reel	Yes	
		CY7C1061G18-15BVJXIT				No	
		CY7C1061GE18-15BVXIT			Dual Chip Enable, Address MSB A19 at ball H6, Tape and Reel	Yes	
		CY7C1061G18-15BVXIT				No	
		CY7C1061GE18-15ZSXIT	51-85160	54-pin TSOP II	Dual Chip Enable, Tape and Reel	Yes	
		CY7C1061G18-15ZSXIT				No	
		CY7C1061GE18-15ZXIT	51-85183	48-pin TSOP I	Single Chip Enable, Tape and Reel	Yes	
		CY7C1061G18-15ZXIT				No	

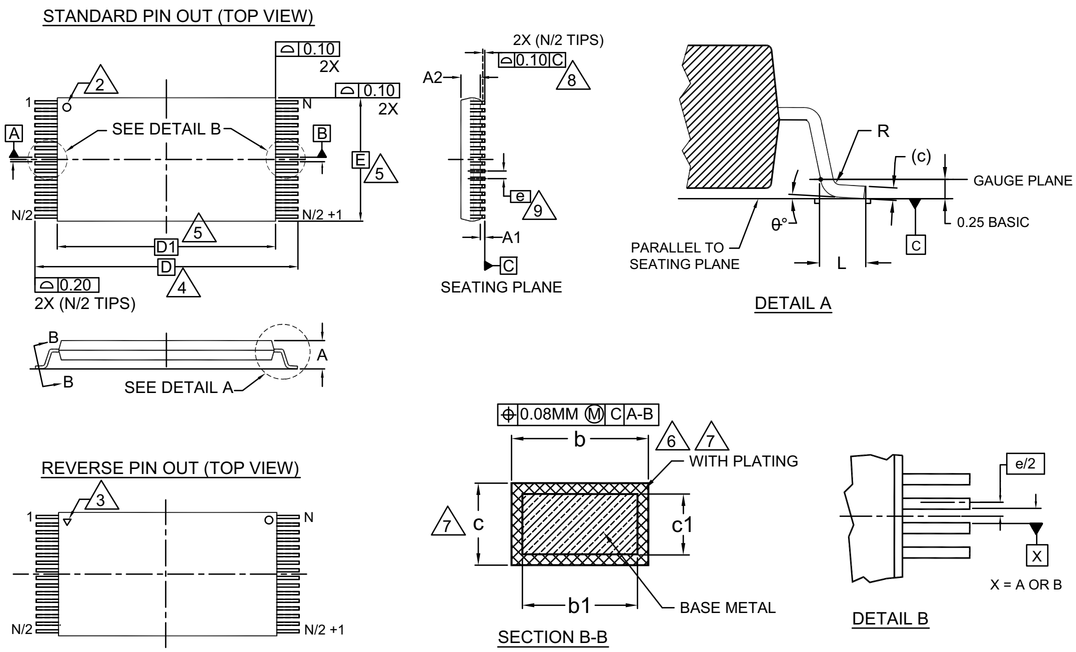
Ordering Code Definitions

CY 7 C 1 06 1 G E XX - XX XX X I X

- X = blank or T
  blank = Bulk; T = Tape and Reel
- Temperature Range: I = Industrial
- Pb-free
- Package Type: XX = BV or ZS or Z
  BV = 48-ball VFBGA; ZS = 54-pin TSOP II; Z = 48-pin TSOP I
- Speed: XX = 10 ns or 15 ns
- Voltage Range: XX = no character or 30 or 18
  no character = 4.5 V–5.5 V; 30 = 2.2 V–3.6 V; 18 = 1.65 V–2.2 V
- X = blank or E
  blank = without ERR output;
  E = with ERR output, Single bit error correction indicator
- Process Technology: Revision Code “G” = 65 nm
- Data Width: 1 = × 16-bits
- Density: 06 = 16-Mbit
- Family Code: 1 = Fast Asynchronous SRAM family
- Technology Code: C = CMOS
- Marketing Code: 7 = SRAM
- Company ID: CY = Cypress

Package Diagrams

Figure 20. 48-pin TSOP I (12 × 18.4 × 1.0 mm) Z48A Package Outline, 51-85183



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	20.00 BASIC		
D1	18.40 BASIC		
E	12.00 BASIC		
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	—	8
R	0.08	—	0.20
N	48		

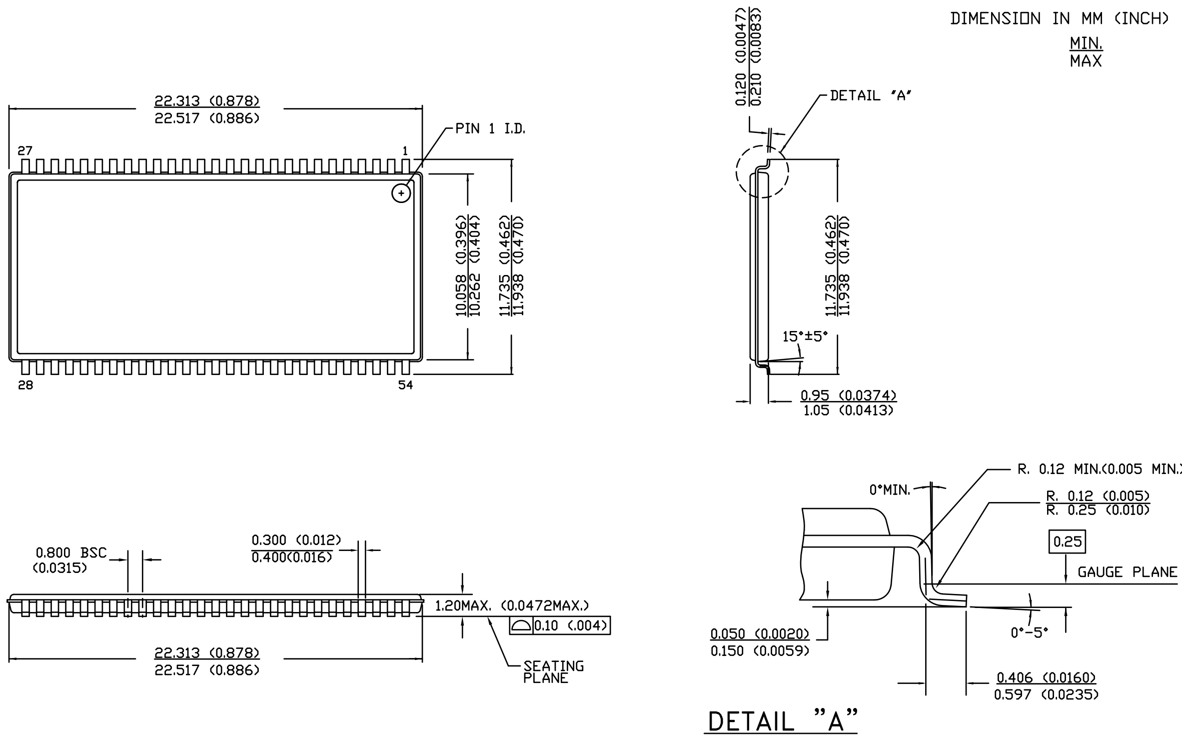
NOTES:

1. DIMENSIONS ARE IN MILLIMETERS (mm).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C- . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm .
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
10. JEDEC SPECIFICATION NO. REF: MO-142(D)DD.

51-85183 *F

Package Diagrams (continued)

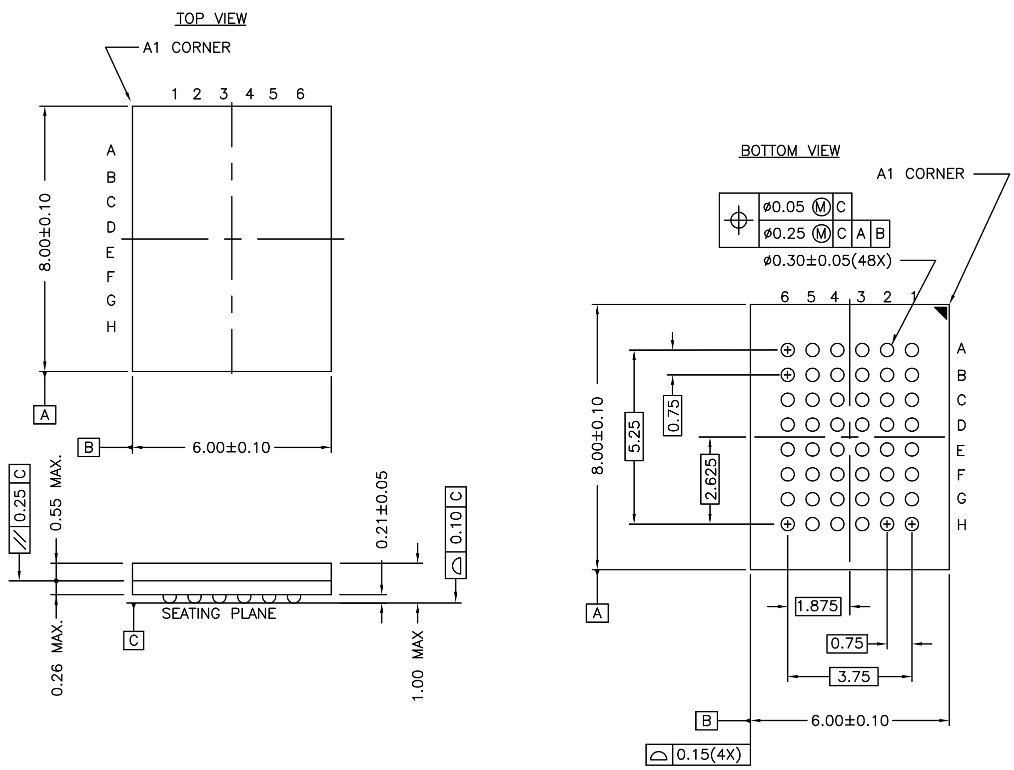
Figure 21. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Z54-II Package Outline, 51-85160



51-85160 *E

Package Diagrams (continued)

Figure 22. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Acronyms

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1061G/CY7C1061GE, 16-Mbit (1M words × 16 bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-81540				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*P	4791835	NILE	06/09/2015	Changed status from Preliminary to Final.
*Q	5436639	NILE	09/14/2016	Updated Maximum Ratings: Updated Note 8 (Replaced “2 ns” with “20 ns”). Updated DC Electrical Characteristics: Removed Operating Range “2.7 V to 3.6 V” and all values corresponding to V_{OH} parameter. Included Operating Ranges “2.7 V to 3.0 V” and “3.0 V to 3.6 V” and all values corresponding to V_{OH} parameter. Changed minimum value of V_{IH} parameter from 2.2 V to 2 V corresponding to Operating Range “4.5 V to 5.5 V”. Updated Ordering Information: Updated part numbers. Updated to new template.
*R	5580947	NILE	01/10/2017	Updated Logic Block Diagram – CY7C1061G. Updated 48-pin TSOP package diagram. Updated links in Sales, Solutions, and Legal Information.

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