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**16-Mbit (1M words × 16 bit) Static RAM**

**Features**

- High speed
  - $t_{AA} = 10 \text{ ns}/15 \text{ ns}$
- Low active power
  - $I_{CC} = 90 \text{ mA}$  at 100 MHz
- Low CMOS standby current
  - $I_{SB2} = 20 \text{ mA}$  (typ)
- Operating voltages of 2.2 V to 3.6 V
- 1.0 V data retention
- Automatic power down when deselected
- TTL compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}_1$  and  $CE_2$  features
- Available in Pb-free 48-pin TSOP I, 54-pin TSOP II, and 48-ball VFBGA packages
- Offered in dual Chip Enable options

**Functional Description**

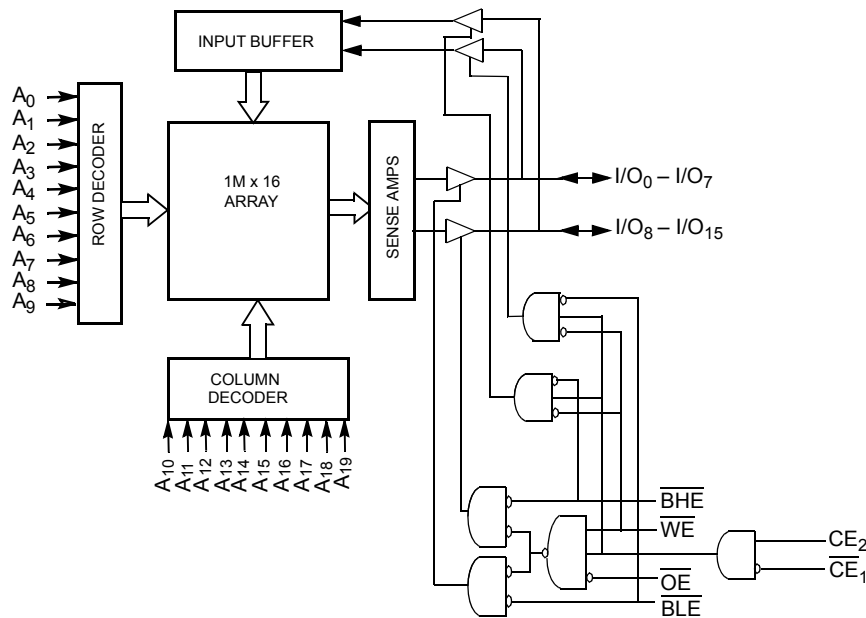
The CY7C1061GN/CY7C10612GN is a high performance CMOS Static RAM organized as 1,048,576 words by 16 bits.

To write to the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable ( $\overline{WE}$ ) input LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_0$  through  $I/O_7$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ).

To read from the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appears on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory appears on  $I/O_8$  to  $I/O_{15}$ . See Truth Table on page 13 for a complete description of Read and Write modes.

The input or output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high impedance state when the device is deselected ( $\overline{CE}_1$  HIGH/ $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), the  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW).

**Logic Block Diagram**



**Contents**

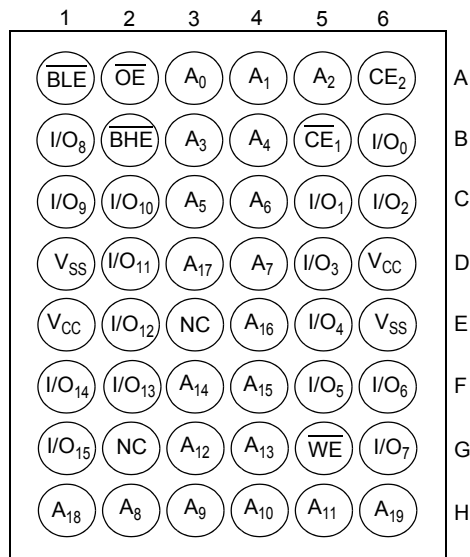
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### Selection Guide

Description	-10	-15	Unit
Maximum access time	10	15	ns
Maximum operating current	110	80	mA
Maximum CMOS standby current	30	30	mA

### Pin Configurations

Figure 1. 48-ball VFBGA (8 × 9.5 × 1 mm) Dual Chip Enable pinout, Package/Grade ID: BVXI <sup>[1]</sup>

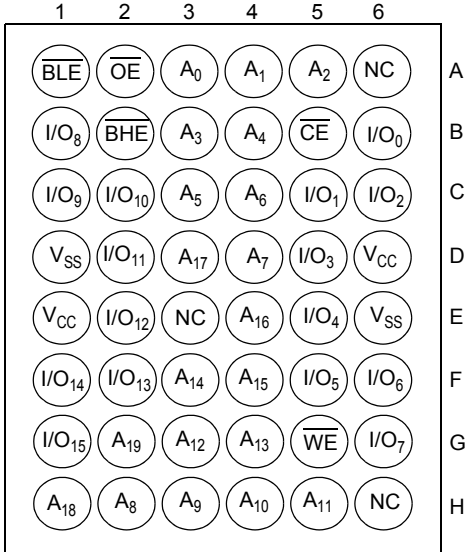


**Note**

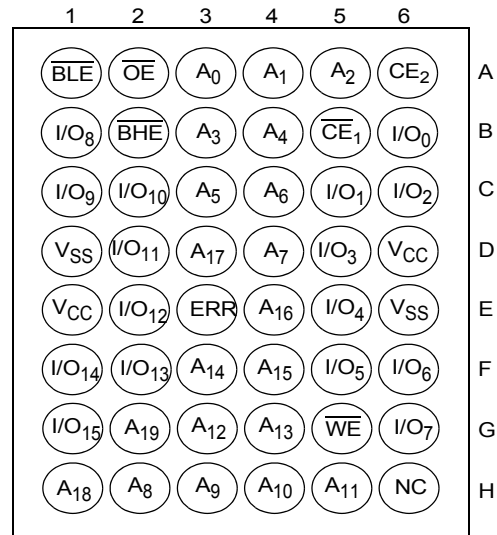
1. NC pins are not connected internally to the die.

**Pin Configurations** (continued)

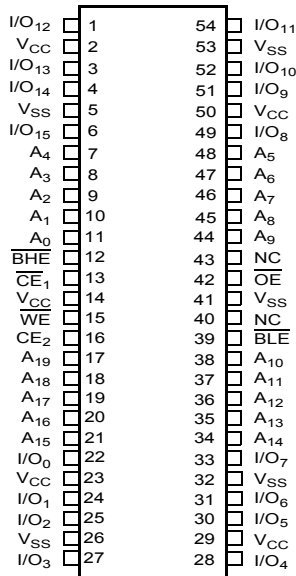
**Figure 2. 48-ball VFBGA (6 × 8 × 1.0 mm)**  
Single Chip Enable pinout, Package/Grade ID: BV1XI [2]



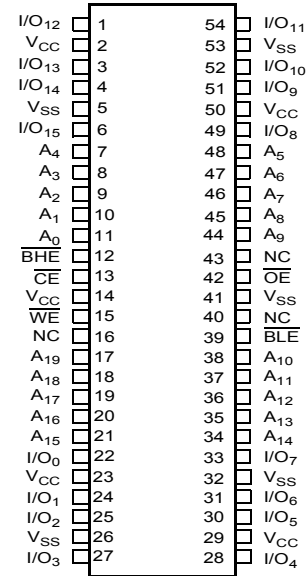
**Figure 3. 48-ball VFBGA (6 × 8 × 1.0 mm)**  
Dual Chip Enable pinout, Package/Grade ID: BVJXI [2]



**Figure 4. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm)**  
Dual Chip Enable pinout (Top View) [2]



**Figure 5. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm)**  
Single Chip Enable pinout (Top View) [2]

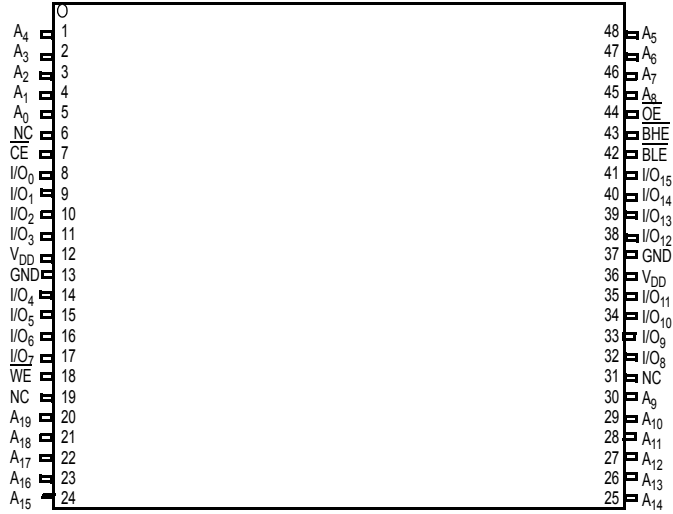


**Note**

2. NC pins are not connected internally to the die.

**Pin Configurations** (continued)

**Figure 6. 48-pin TSOP I (12 × 18.4 × 1 mm) pinout (Top View) <sup>[3]</sup>**



**Note**

3. NC pins are not connected internally to the die.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65 °C to +150 °C  
 Ambient Temperature  
 with Power Applied ..... -55 °C to +125 °C  
 Supply Voltage  
 on  $V_{CC}$  relative to GND <sup>[4]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V  
 DC Voltage Applied to Outputs  
 in High Z State <sup>[4]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

DC Input Voltage <sup>[4]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V  
 Current into Outputs (LOW) ..... 20 mA  
 Static Discharge Voltage  
 (MIL-STD-883, Method 3015) ..... >2001 V  
 Latch Up Current ..... >200 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$
Industrial	-40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V

## DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	10 ns/15 ns			Unit	
			Min	Typ <sup>[5]</sup>	Max		
$V_{OH}$	Output HIGH voltage	1.65 V to 2.2 V $V_{CC} = \text{Min}, I_{OH} = -0.1 \text{ mA}$	1.4	-	-	V	
		2.2 V to 2.7 V $V_{CC} = \text{Min}, I_{OH} = -0.1 \text{ mA}$	2.0	-	-		
		2.7 V to 3.0 V $V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.2	-	-		
		3.0 V to 3.6 V $V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.4	-	-		
$V_{OL}$	Output LOW voltage	1.65 V to 2.2 V $V_{CC} = \text{Min}, I_{OL} = 0.1 \text{ mA}$	-	-	0.2	V	
		2.2 V to 2.7 V $V_{CC} = \text{Min}, I_{OL} = 2 \text{ mA}$	-	-	0.4		
		2.7 V to 3.6 V $V_{CC} = \text{Min}, I_{OL} = 8 \text{ mA}$	-	-	0.4		
$V_{IH}$	Input HIGH voltage <sup>[4]</sup>	1.65 V to 2.2 V -	1.4	-	$V_{CC} + 0.2$	V	
		2.2 V to 2.7 V -	2.0	-	$V_{CC} + 0.3$		
		2.7 V to 3.6 V -	2.0	-	$V_{CC} + 0.3$		
$V_{IL}$	Input LOW voltage <sup>[4]</sup>	1.65 V to 2.2 V -	-0.2	-	0.4	V	
		2.2 V to 2.7 V -	-0.3	-	0.6		
		2.7 V to 3.6 V -	-0.3	-	0.8		
$I_{IX}$	Input leakage current	$GND \leq V_I \leq V_{CC}$	-1	-	+1	$\mu\text{A}$	
$I_{OZ}$	Output leakage current	$GND \leq V_{OUT} \leq V_{CC}$ , Output disabled	-1	-	+1	$\mu\text{A}$	
$I_{CC}$	$V_{CC}$ operating supply current	$V_{CC} = \text{Max}, I_{OUT} = 0 \text{ mA}$ , CMOS levels	$f = 100 \text{ MHz}$	-	90	110	mA
			$f = 66.7 \text{ MHz}$	-	70	80	
$I_{SB1}$	Automatic CE power down current – TTL inputs <sup>[6]</sup>	$\text{Max } V_{CC}$ , $CE_1 \geq V_{IH}, CE_2 \leq V_{IL}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}, f = f_{MAX}$	-	-	40	mA	
$I_{SB2}$	Automatic CE power down current – CMOS inputs <sup>[6]</sup>	$\text{Max } V_{CC}$ , $\overline{CE}_1 \geq V_{CC} - 0.3 \text{ V}, CE_2 \leq 0.3 \text{ V}$ , $V_{IN} \geq V_{CC} - 0.3 \text{ V}$ or $V_{IN} \leq 0.3 \text{ V}, f = 0$	-	20	30	mA	

### Notes

- $V_{IL(\text{min})} = -2.0 \text{ V}$  and  $V_{IH(\text{max})} = V_{CC} + 2 \text{ V}$  for pulse durations of less than 20 ns.
- Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at  $V_{CC} = 1.8 \text{ V}$  (for a  $V_{CC}$  range of 1.65 V–2.2 V),  $V_{CC} = 3 \text{ V}$  (for a  $V_{CC}$  range of 2.2 V–3.6 V) at  $T_A = 25 \text{ }^\circ\text{C}$ .
- For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.

### Capacitance

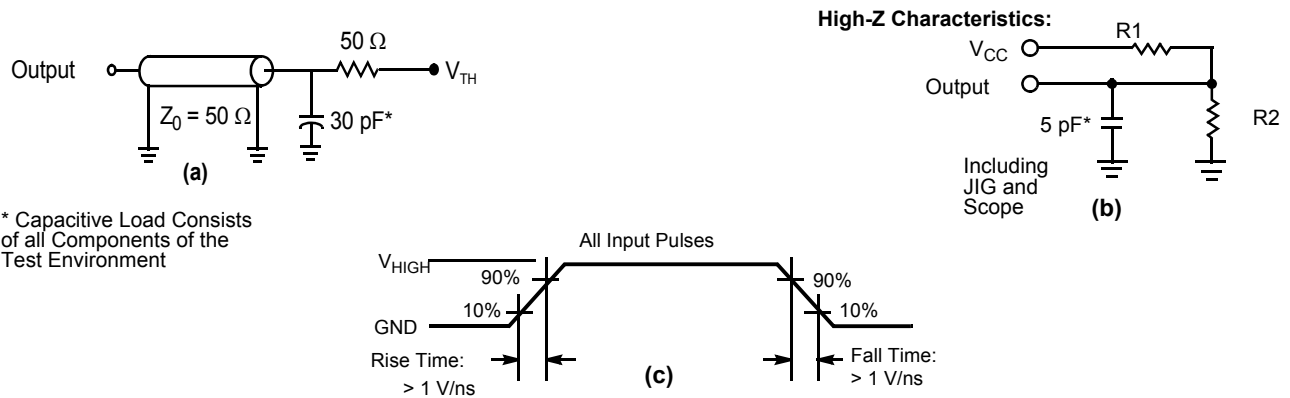
Parameter [7]	Description	Test Conditions	48-pin TSOP I	54-pin TSOP II	48-ball VFBGA	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 3.3 V	10	10	10	pF
C <sub>OUT</sub>	I/O capacitance		10	10	10	pF

### Thermal Resistance

Parameter [7]	Description	Test Conditions	48-pin TSOP I	54-pin TSOP II	48-ball VFBGA	Unit
θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	57.99	93.63	31.50	°C/W
θ <sub>JC</sub>	Thermal resistance (junction to case)		13.42	21.58	15.75	°C/W

### AC Test Loads and Waveforms

Figure 7. AC Test Loads and Waveforms [8]



Parameters	1.8 V	3.0 V	Unit
R1	1667	317	Ω
R2	1538	351	Ω
V <sub>TH</sub>	0.9	1.5	V
V <sub>HIGH</sub>	1.8	3	V

**Notes**

- 7. Tested initially and after any design or process changes that may affect these parameters.
- 8. Full-device AC operation assumes a 100-μs ramp time from 0 to V<sub>CC</sub> (min) and 100-μs wait time after V<sub>CC</sub> stabilizes to its operational value.



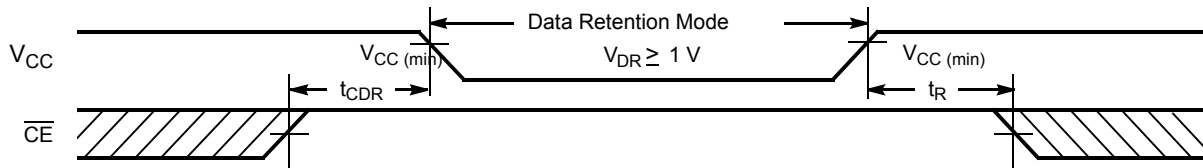
### Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention	–	1	–	V
$I_{CCDR}$	Data retention current	$V_{CC} = 1.2\text{ V}$ , $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ , $CE_2 \leq 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	30	mA
$t_{CDR}^{[9]}$	Chip deselect to data retention time	–	0	–	ns
$t_R^{[10]}$	Operation recovery time	$V_{CC} \geq 2.2\text{ V}$	10	–	ns
		$V_{CC} < 2.2\text{ V}$	15	–	

### Data Retention Waveform

Figure 8. Data Retention Waveform <sup>[11]</sup>



**Notes**

- 9. Tested initially and after any design or process changes that may affect these parameters.
- 10. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} \geq 100\ \mu\text{s}$  or stable at  $V_{CC(min.)} \geq 100\ \mu\text{s}$ .
- 11.  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.

## AC Switching Characteristics

Over the Operating Range

Parameter <sup>[12]</sup>	Description	-10		-15		Unit
		Min	Max	Min	Max	
<b>Read Cycle</b>						
$t_{power}$	$V_{CC}$ (typical) to the first access <sup>[13]</sup>	100	–	100	–	μs
$t_{RC}$	Read cycle time	10	–	15	–	ns
$t_{AA}$	Address to data valid	–	10	–	15	ns
$t_{OHA}$	Data hold from address change	3	–	3	–	ns
$t_{ACE}$	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to data valid	–	10	–	15	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	5	–	8	ns
$t_{LZOE}$	$\overline{OE}$ LOW to low Z <sup>[14]</sup>	0	–	1	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to high Z <sup>[14, 15]</sup>	–	5	–	8	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to low Z <sup>[14]</sup>	3	–	3	–	ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH/ $CE_2$ LOW to high Z <sup>[14, 15]</sup>	–	5	–	8	ns
$t_{PU}$	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to power-up <sup>[16]</sup>	0	–	0	–	ns
$t_{PD}$	$\overline{CE}_1$ HIGH/ $CE_2$ LOW to power-down <sup>[16]</sup>	–	10	–	15	ns
$t_{DBE}$	Byte enable to data valid	–	5	–	8	ns
$t_{LZBE}$	Byte enable to low Z	0	–	1	–	ns
$t_{HZBE}$	Byte disable to high Z	–	6	–	8	ns
<b>Write Cycle <sup>[17, 18]</sup></b>						
$t_{WC}$	Write cycle time	10	–	15	–	ns
$t_{SCE}$	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to write end <sup>[19]</sup>	7	–	12	–	ns
$t_{AW}$	Address setup to write end	7	–	12	–	ns
$t_{HA}$	Address hold from write end	0	–	0	–	ns
$t_{SA}$	Address setup to write start	0	–	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	7	–	12	–	ns
$t_{SD}$	Data setup to write end	5	–	8	–	ns
$t_{HD}$	Data hold from write end	0	–	0	–	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to low Z <sup>[14]</sup>	3	–	3	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to high Z <sup>[14, 15]</sup>	–	5	–	8	ns
$t_{BW}$	Byte Enable to End of Write	7	–	12	–	ns

### Notes

- Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for  $V_{CC} \geq 3$  V) and  $V_{CC}/2$  (for  $V_{CC} < 3$  V), and input pulse levels of 0 to 3 V (for  $V_{CC} \geq 3$  V) and 0 to  $V_{CC}$  (for  $V_{CC} < 3$  V). Test conditions for the read cycle use the output loading, shown in part (a) of Figure 7 on page 7, unless specified otherwise.
- $t_{POWER}$  gives the minimum amount of time that the power supply is at typical  $V_{CC}$  values until the first memory access is performed.
- At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
- $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZWE}$ , and  $t_{HZBE}$  are specified with a load capacitance of 5 pF, as shown in part (b) of Figure 7 on page 7. Hi-Z, Lo-Z transition is measured  $\pm 200$  mV from steady state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ , and  $CE_2 = V_{IH}$ . Chip enables must be active and  $\overline{WE}$  and byte enables must be LOW to initiate a write, and the transition of any of these signals can terminate. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .
- For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.

### Switching Waveforms

Figure 9. Read Cycle No. 1 (Address Transition Controlled) [20, 21]

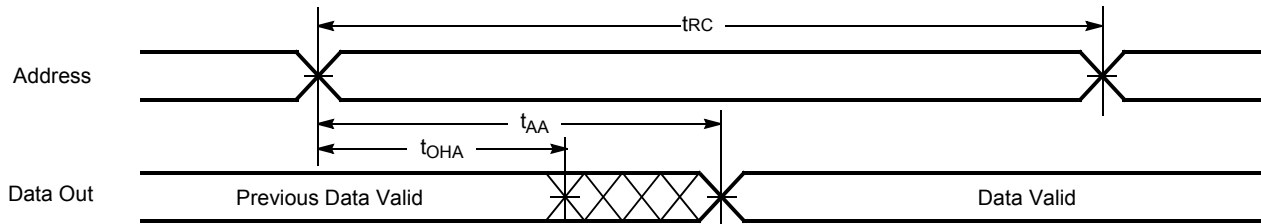
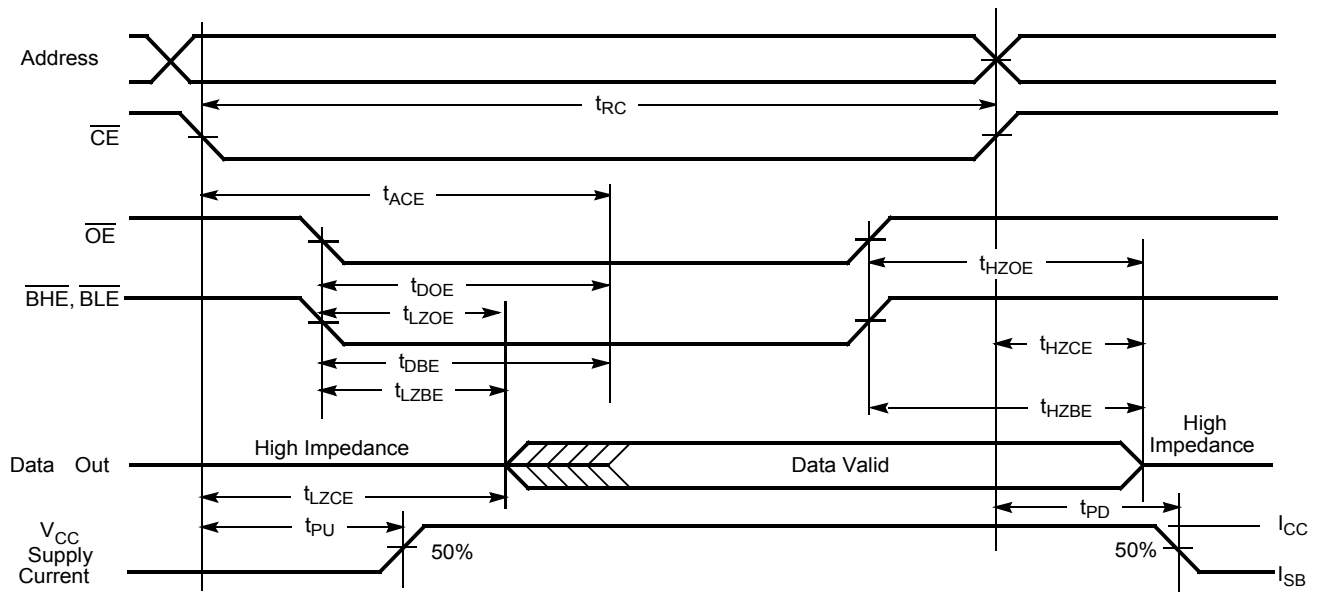


Figure 10. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [21, 22, 23]



**Notes**

20. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  or both =  $V_{IL}$ .

21.  $\overline{WE}$  is HIGH for read cycle.

22.  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.

23. Address valid before or similar to  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

Figure 11. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled) [24, 25, 26]

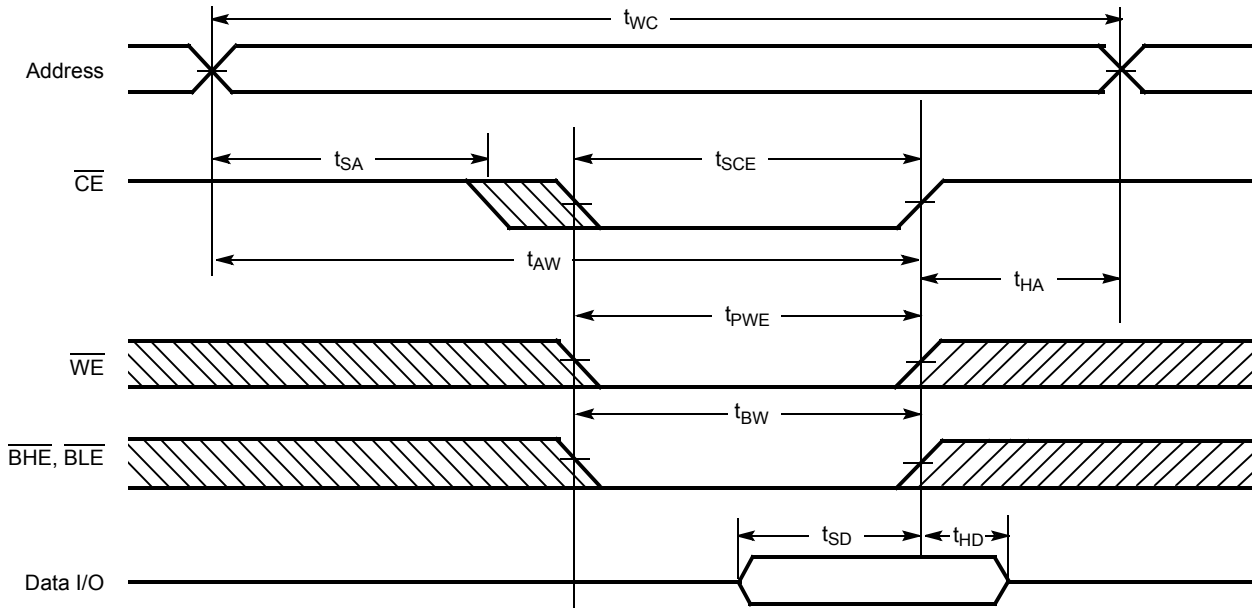
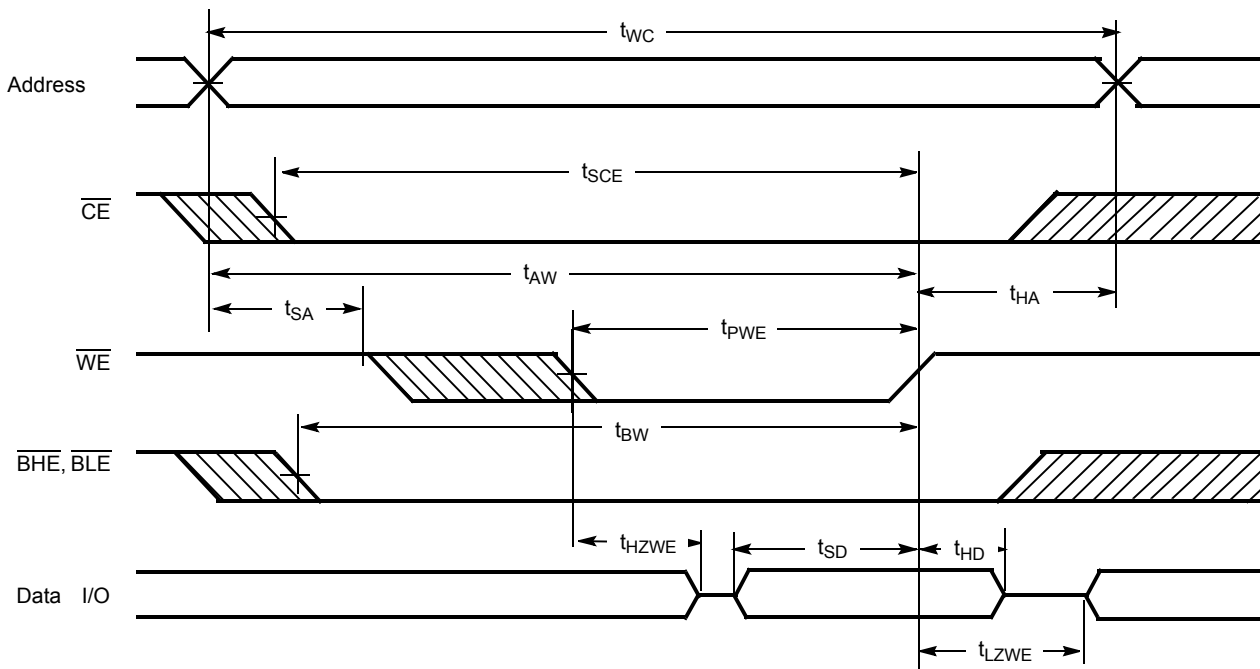


Figure 12. Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [24, 25, 26]



Notes

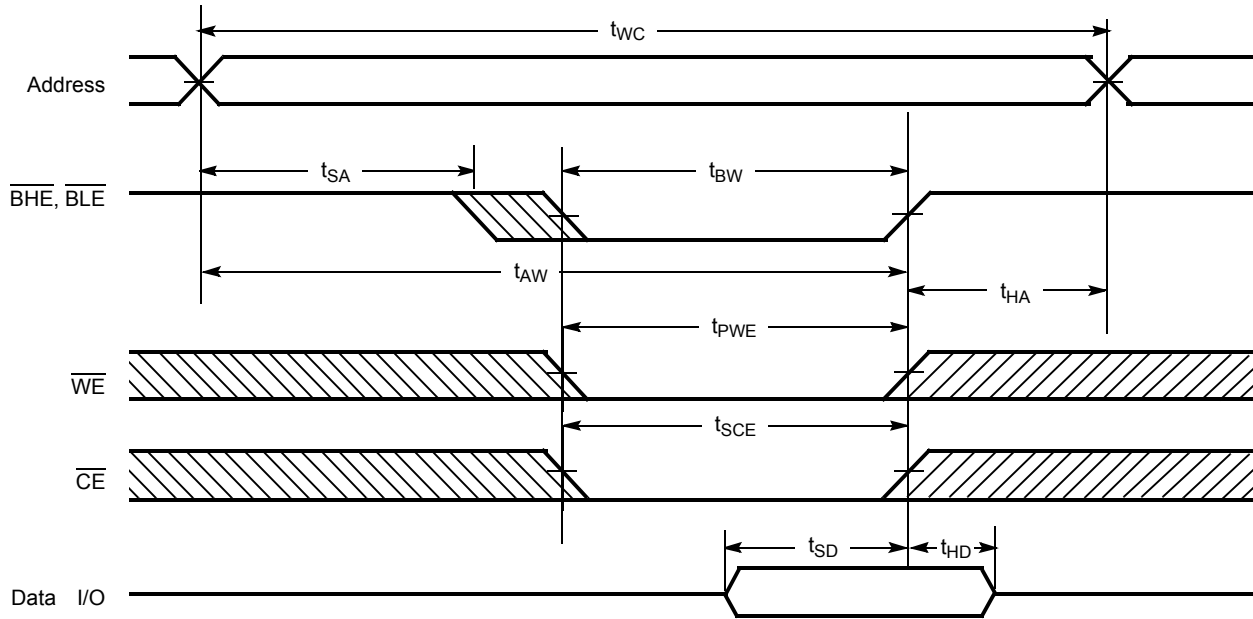
24.  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.

25. Data I/O is high impedance if  $\overline{\text{OE}}$ ,  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{IH}$ .

26. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Figure 13. Write Cycle No. 3 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled) <sup>[27]</sup>



Note

27.  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.

**Truth Table**

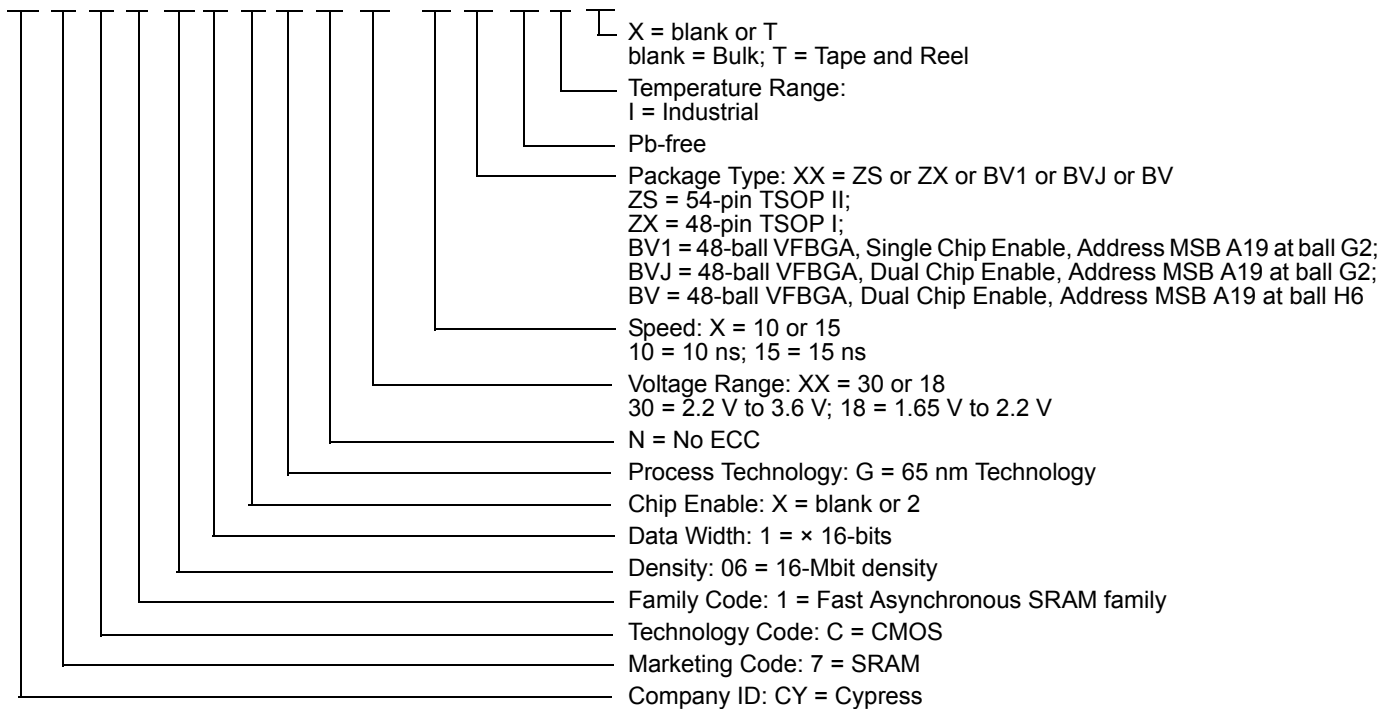
$\overline{CE}_1$	$CE_2$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>0</sub> –I/O <sub>7</sub>	I/O <sub>8</sub> –I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	X	High Z	High Z	Power down	Standby (I <sub>SB</sub> )
X	L	X	X	X	X	High Z	High Z	Power down	Standby (I <sub>SB</sub> )
L	H	L	H	L	L	Data out	Data out	Read all bits	Active (I <sub>CC</sub> )
L	H	L	H	L	H	Data out	High Z	Read lower bits only	Active (I <sub>CC</sub> )
L	H	L	H	H	L	High Z	Data out	Read upper bits only	Active (I <sub>CC</sub> )
L	H	X	L	L	L	Data in	Data in	Write all bits	Active (I <sub>CC</sub> )
L	H	X	L	L	H	Data in	High Z	Write lower bits only	Active (I <sub>CC</sub> )
L	H	X	L	H	L	High Z	Data in	Write upper bits only	Active (I <sub>CC</sub> )
L	H	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I <sub>CC</sub> )

**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type (Pb-free)	Operating Range
10	CY7C1061GN30-10ZSXI	51-85160	54-pin TSOP II, Dual Chip Enable	Industrial
	CY7C1061GN30-10ZSXIT	51-85160	54-pin TSOP II, Dual Chip Enable, Tape and Reel	
	CY7C10612GN30-10ZSXI	51-85160	54-pin TSOP II, Single Chip Enable	
	CY7C10612GN30-10ZSXIT	51-85160	54-pin TSOP II, Single Chip Enable, Tape and Reel	
	CY7C1061GN30-10ZXI	51-85183	48-pin TSOP I, Single Chip Enable	
	CY7C1061GN30-10ZXIT	51-85183	48-pin TSOP I, Single Chip Enable, Tape and Reel	
	CY7C1061GN30-10BV1XI	51-85150	48-ball VFBGA, Single Chip Enable, Address MSB A19 at ball G2	
	CY7C1061GN30-10BV1XIT	51-85150	48-ball VFBGA, Single Chip Enable, Address MSB A19 at ball G2, Tape and Reel	
	CY7C1061GN30-10BVJXI	51-85150	48-ball VFBGA, Dual Chip Enable, Address MSB A19 at ball G2	
	CY7C1061GN30-10BVJXIT	51-85150	48-ball VFBGA, Dual Chip Enable, Address MSB A19 at ball G2, Tape and Reel	
	CY7C1061GN30-10BVXI	51-85150	48-ball VFBGA, Dual Chip Enable, Address MSB A19 at ball H6	
	CY7C1061GN30-10BVXIT	51-85150	48-ball VFBGA, Dual Chip Enable, Address MSB A19 at ball H6, Tape and Reel	
15	CY7C1061GN18-15ZSXI	51-85160	54-pin TSOP II	Industrial
	CY7C1061GN18-15ZSXIT	51-85160	54-pin TSOP II, Tape and Reel	

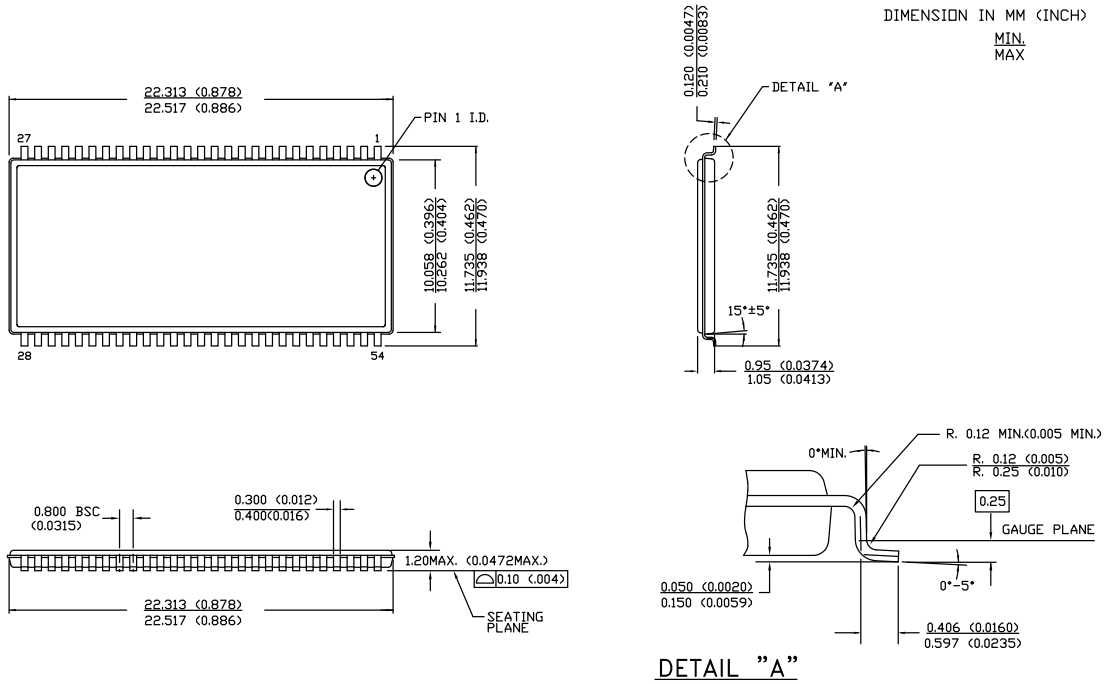
**Ordering Code Definitions**

CY 7 C 1 06 1 X G N XX - X XX X I X



Package Diagrams

Figure 14. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Z54-II Package Outline, 51-85160



51-85160 \*E

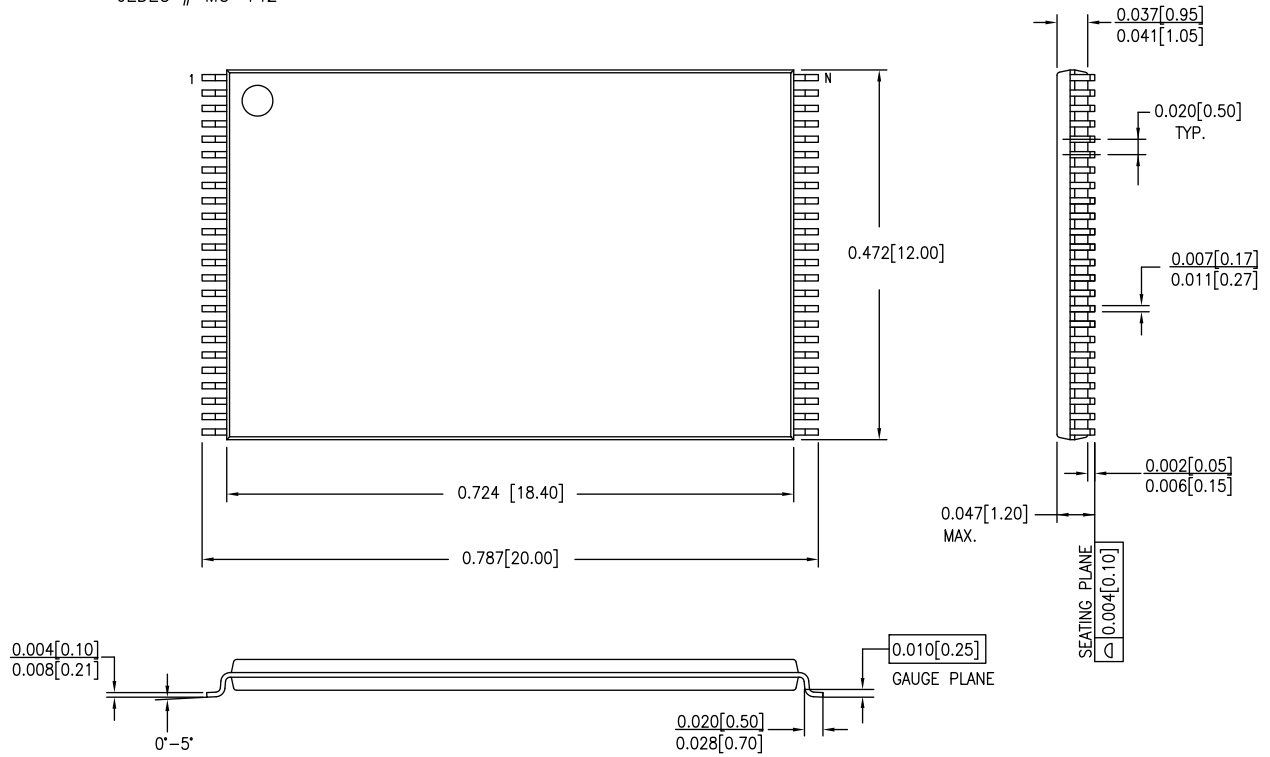


Package Diagrams (continued)

Figure 15. 48-pin TSOP I (12 × 18.4 × 1.0 mm) Z48A Package Outline, 51-85183

DIMENSIONS IN INCHES[MM] MIN.  
MAX.

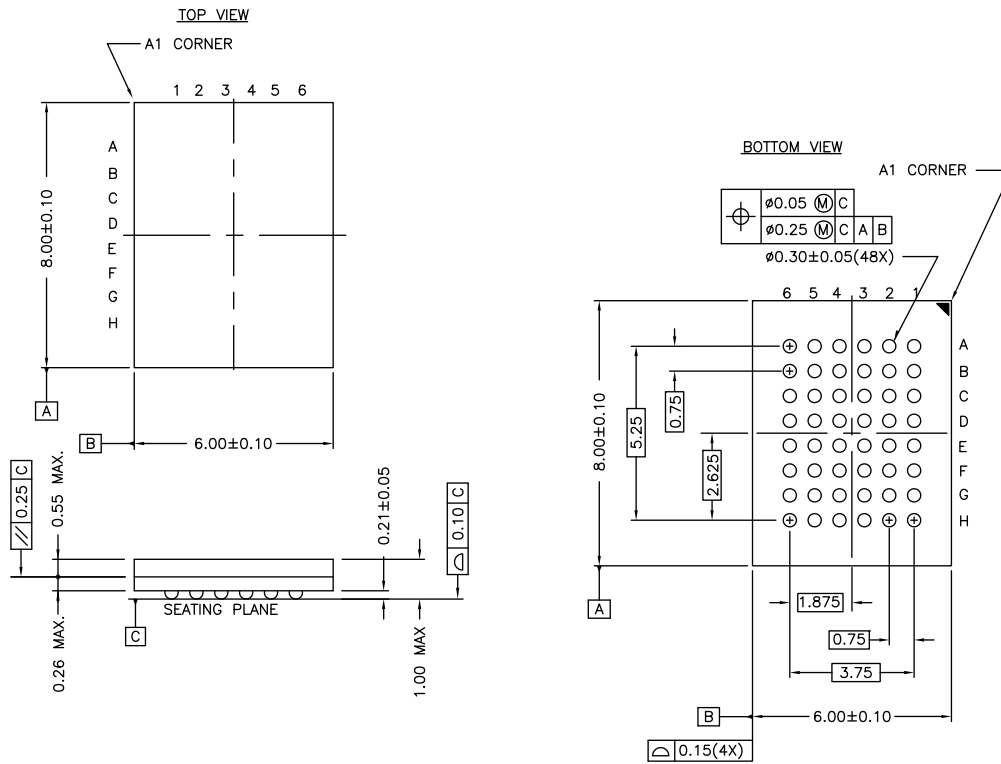
JEDEC # MO-142



51-85183 \*D

Package Diagrams (continued)

Figure 16. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:  
 PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD)  
 posted on the Cypress web.

51-85150 \*H

## Acronyms

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

**Document History Page**

Document Title: CY7C1061GN/CY7C10612GN, 16-Mbit (1M words × 16 bit) Static RAM				
Document Number: 001-93680				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	4505531	VINI	01/02/2015	New data sheet.
*A	4900408	NILE	09/11/2015	<p>Updated <a href="#">DC Electrical Characteristics</a>:            Updated details in "Test Conditions" column of V<sub>OH</sub> and V<sub>OL</sub> parameters.            Updated <a href="#">Ordering Information</a>:            No change in part numbers.            Replaced "51-85178" with "51-85150" in "Package Diagram" column.            Replaced "8 × 9.5 × 1 mm" with "6 × 8 × 1.0 mm" in "Package Type" column.            Updated <a href="#">Package Diagrams</a>:            Removed spec 51-85178 *C.            Added spec 51-85150 *H.            Updated to new template.</p>
*B	5415385	NILE	09/07/2016	<p>Updated Document Title to read as "CY7C1061GN/CY7C10612GN, 16-Mbit (1M words × 16 bit) Static RAM".            Added CY7C10612GN part related information in all instances across the document.            Added "1.65 V to 2.2 V" voltage range related information in all instances across the document.            Added 48-pin TSOP I package related information in all instances across the document.            Added 15 ns speed bin related information in all instances across the document.            Updated <a href="#">Pin Configurations</a>:            Added <a href="#">Figure 2</a>.            Added <a href="#">Figure 3</a>.            Added <a href="#">Figure 4</a>.            Added <a href="#">Figure 5</a>.            Added <a href="#">Figure 6</a>.            Removed figure "54-pin TSOP II (22.4 × 11.84 × 1.0 mm) pinout (Top View)".            Updated <a href="#">DC Electrical Characteristics</a>:            Updated details in "Test Conditions" column of I<sub>CC</sub> parameter (Added condition "f = 66.7 MHz" and added corresponding values).            Added Note 6 and referred the same note in description of I<sub>SB1</sub> and I<sub>SB2</sub> parameters.            Updated <a href="#">AC Test Loads and Waveforms</a>:            Updated Note 8 referred in <a href="#">Figure 7</a>.            Updated <a href="#">AC Switching Characteristics</a>:            Updated Note 12.            Added Note 14 and referred the same note in description of t<sub>LZOE</sub>, t<sub>HZOE</sub>, t<sub>LZCE</sub>, t<sub>HZCE</sub> parameters.            Updated Note 15.            Added Note 19 and referred the same note in description of t<sub>SCE</sub> parameter.            Updated <a href="#">Ordering Information</a>:            Updated part numbers.            Updated <a href="#">Package Diagrams</a>:            Added spec 51-85183 *D.            Updated to new template.</p>

**Document History Page** (continued)

Document Title: CY7C1061GN/CY7C10612GN, 16-Mbit (1M words × 16 bit) Static RAM				
Document Number: 001-93680				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*C	5454555	NILE	09/29/2016	Updated <a href="#">Maximum Ratings</a> : Updated Note 4 (Replaced “2 ns” with “20 ns”). Updated <a href="#">DC Electrical Characteristics</a> : Removed Operating Range “2.7 V to 3.6 V” and all values corresponding to V <sub>OH</sub> parameter. Included Operating Ranges “2.7 V to 3.0 V” and “3.0 V to 3.6 V” and all values corresponding to V <sub>OH</sub> parameter. Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated <a href="#">Ordering Code Definitions</a> .

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