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CY7C1061GN30

16-Mbit (1 M words × 16 bit) Static RAM

Features

- High speed □ t_{AA} = 10 ns
- Low active power □ I_{CC} = 90 mA at 100 MHz
- Low CMOS standby current I_{SB2} = 20 mA (typ)
- Operating voltages of 2.2 V to 3.6 V
- 1.0 V data retention
- Automatic power down when deselected
- TTL compatible inputs and outputs
- Easy memory expansion with CE₁ and CE₂ features
- Available in Pb-free 54-pin TSOP II, and 48-ball VFBGA packages
- Offered in dual Chip Enable options

Functional Description

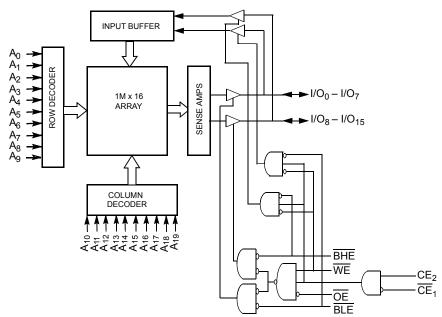
The CY7C1061GN30 is a high performance CMOS Static RAM organized as 1,048,576 words by 16 bits.

To write to the device, tak<u>e</u> Chip Enables (\overline{CE}_1 LOW and CE_2 <u>HIGH</u>) and Write Enable (\overline{WE}) input LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{19}). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through address pins (A_0 through A_{19}).

To read from the device, take <u>Chip</u> Enables (\overline{CE}_1 LOW and CE_2 HIGH) <u>and</u> Output Enable (\overline{OE}) LOW <u>while</u> forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified <u>by the</u> address pins appears on I/O₀ to I/O₇. If Byte High Enable (BHE) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See Truth Table on page 12 for a complete description of Read and Write modes.

The input or output pins (I/O₀ through I/O₁₅) are <u>placed</u> in a high impedance state when the device is deselected ($\overline{CE_1}$ HIGH/ $\overline{CE_2}$ LOW), the outputs are disabled (\overline{OE} HIGH), the BHE and <u>BLE</u> are disabled (BHE, BL<u>E</u> HIGH), or during a write operation ($\overline{CE_1}$ LOW, CE₂ HIGH, and WE LOW).

Logic Block Diagram



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CY7C1061GN30

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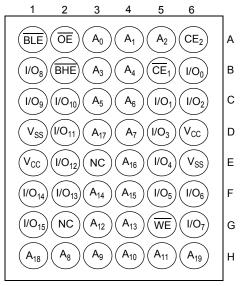


Selection Guide

Description	-10	Unit
Maximum access time	10	ns
Maximum operating current	110	mA
Maximum CMOS standby current	30	mA

Pin Configurations

Figure 1. 48-ball VFBGA (8 × 9.5 × 1 mm) Dual Chip Enable pinout (Top View) ^[1]





Pin Configurations (continued)

Figure 2.	54-pin TSOP II	22.4 × 11.84 × 1.0 mm) pinout (Top View) ^[2]
-----------	----------------	-----------------------	------------------------------------

	54 I/O ₁₁
	53 🗆 V _{SS}
I/O ₁₃ 3	52 I/O ₁₀
I/O ₁₄ 4	51 🗌 I/O ₉
V _{SS} 5	50 🗌 V _{CC}
I/O ₁₅ 🗖 6	49 🗌 I/O ₈
A4 🗖 7	48 🗖 A ₅
A ₃ 🗖 8	47 🗖 A ₆
A ₂ 🗖 9	46 🗖 A ₇
A ₁ 🗖 10	45 🗖 A ₈
A ₀ 🗖 11	44 🗖 A ₉
BHE 12	43 🗖 NC
CE1 13	42 🗖 OE
V _{CC} □ 14	41 🗆 V _{SS}
WE 15	40 🗖 NC
CE ₂ 16	39 🗖 BLE
A ₁₉ 17	38 🗖 A ₁₀
A ₁₈ 🗖 18	37 🗖 A ₁₁
A ₁₇ 19	36 🗖 A ₁₂
A ₁₆ 20	35 🗖 A ₁₃
A ₁₅ 21	34 🗖 A ₁₄
I/O ₀ 22	33 🔲 I/O ₇
V _{CC} 23	32 🗖 V _{SS}
I/O ₁ 24	31 🔲 I/O ₆
1/O ₂ 25	30 I/O ₅
V _{SS} 26	29 🗖 V _{CC}
I/O ₃ □27	28 🗆 I/O ₄



Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature	65 °C to +150 °C
Ambient Temperature with Power Applied	–55 °C to +125 °C
Supply Voltage on V_{CC} relative to GND $^{[3]}$.	–0.5 V to V _{CC} + 0.5 V
DC Voltage Applied to O in High Z State ^[3]	utputs –0.5 V to V _{CC} + 0.5 V

DC Input Voltage ^[3]	-0.5 V to V _{CC} + 0.5 V
Current into Outputs (LOW)	20 mA
Static Discharge Voltage (MIL-STD-883, Method 3015)	>2001 V
Latch Up Current	>200 mA

Operating Range

Range	Ambient Temperature	V _{cc}
Industrial	–40 °C to +85 °C	2.2 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range

Devenueter	Description	Test Conditions	-10			Unit	
Parameter	Desc	cription	Test Conditions	Min	Typ ^[4]	Мах	Unit
V _{OH}	Output HIGH	2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = -0.1 mA	2.0	_	_	V
	voltage	2.7 V to 3.6 V	V_{CC} = Min, I_{OH} = -4.0 mA	2.2	-	_	1
V _{OL}	Output LOW	2.2 V to 2.7 V	V _{CC} = Min, I _{OL} = 2 mA	_	-	0.4	V
	voltage	2.7 V to 3.6 V	V _{CC} = Min, I _{OL} = 8 mA	_	-	0.4	1
V _{IH}	Input HIGH	2.2 V to 2.7 V	-	2.0	-	V _{CC} + 0.3	V
	voltage [3]	2.7 V to 3.6 V	-	2.0	-	V _{CC} + 0.3	
V _{IL}	Input LOW	2.2 V to 2.7 V	-	-0.3	_	0.6	V
	voltage [3]	2.7 V to 3.6 V	-	-0.3	_	0.8	
I _{IX}	Input leakage o	urrent	$GND \le V_1 \le V_{CC}$	-1	-	+1	μA
I _{OZ}	Output leakage	current	$GND \leq V_{OUT} \leq V_{CC}$, Output disabled	-1	_	+1	μA
I _{CC}	V _{CC} operating	supply current	V _{CC} = Max,	_	90	110	mA
			$f = f_{MAX} = 1/t_{RC},$				
			I _{OUT} = 0 mA,				
			CMOS levels				
I _{SB1}	Automatic CE p		Max V _{CC} ,	_	-	40	mA
	current – TTL i	nputs	$\overline{CE}_1 \ge V_{IH}, CE_2 \le V_{IL},$				
			$V_{IN} \ge V_{IH} \text{ or } V_{IN} \le V_{IL},$				
			$f = f_{MAX}$				
I _{SB2}	Automatic CE p current – CMO		Max V _{CC} ,	-	20	30	mA
			$\overline{\text{CE}}_1 \ge \text{V}_{\text{CC}} - 0.3 \text{ V}, \text{CE}_2 \le 0.3 \text{ V},$				
			$V_{IN} \ge V_{CC} - 0.3 \text{ V or } V_{IN} \le 0.3 \text{ V},$				
			f = 0				

Note
3. V_{IL(min)} = -2.0 V and V_{IH(max)} = V_{CC} + 2 V for pulse durations of less than 2 ns.
4. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V (for a V_{CC} range of 2.2 V–3.6 V), T_A = 25 °C.



Capacitance

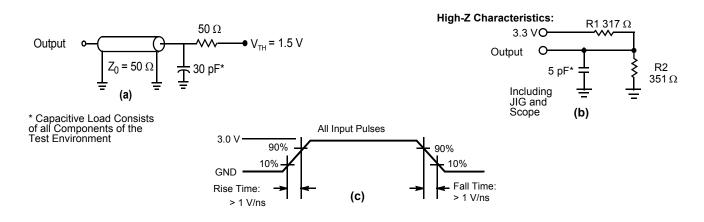
Parameter ^[5]	Description	Test Conditions	54-pin TSOP II	48-ball VFBGA	Unit
C _{IN}	Input capacitance	$T_{A} = 25 \circ C, f = 1 \text{ MHz},$	10	10	pF
C _{OUT}	I/O capacitance	V _{CC} = 3.3 V	10	10	pF

Thermal Resistance

Parameter ^[5]	Description	Test Conditions	54-pin TSOP II	48-ball VFBGA	Unit
- JA		Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	93.63	31.50	°C/W
30	Thermal resistance (junction to case)		21.58	15.75	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms ^[6]



Notes

- Tested initially and after any design or process changes that may affect these parameters.
 Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0 V). 100 µs (t_{power}) after reaching the minimum operating V_{DD}, normal SRAM operation begins including reduction in V_{DD} to the data retention (V_{CCDR}, 1.0 V) voltage.



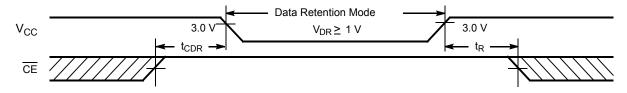
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Max	Unit
V _{DR}	V_{CC} for data retention	-	1	-	V
I _{CCDR}	Data retention current	V _{CC} = 1.2 V,	-	30	mA
		$\overline{\text{CE}}_1 \ge \text{V}_{\text{CC}} - 0.2 \text{ V}, \text{CE}_2 \le 0.2 \text{ V},$			
		$V_{IN} \ge V_{CC} - 0.2 \text{ V or } V_{IN} \le 0.2 \text{ V}$			
t _{CDR} ^[7]	Chip deselect to data retention time	-	0	-	ns
t _R ^[8]	Operation recovery time	-	10	-	ns

Data Retention Waveform

Figure 4. Data Retention Waveform ^[9]



Notes

- 7. Tested initially and after any design or process changes that may affect these parameters.
- 8. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min.)} \geq 100 µs or stable at V_{CC(min.)} \geq 100 µs.
- 9. \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.



AC Switching Characteristics

Over the Operating Range

Parameter [10]	Description	-	-10		
Parameter	Description	Min	Min Max		
Read Cycle		·			
t _{power}	V _{CC} (typical) to the first access ^[11]	100	-	μS	
t _{RC}	Read cycle time	10	-	ns	
t _{AA}	Address to data valid	-	10	ns	
t _{OHA}	Data hold from address change	3	-	ns	
t _{ACE}	CE ₁ LOW/CE ₂ HIGH to data valid	-	10	ns	
t _{DOE}	OE LOW to data valid	-	5	ns	
t _{LZOE}	OE LOW to low Z ^[12]	0	-	ns	
t _{HZOE}	OE HIGH to high Z ^[12]	-	5	ns	
t _{LZCE}	CE ₁ LOW/CE ₂ HIGH to low Z ^[12]	3	-	ns	
t _{HZCE}	CE ₁ HIGH/CE ₂ LOW to high Z ^[12]	-	5	ns	
t _{PU}	CE ₁ LOW/CE ₂ HIGH to power-up ^[13]	0	-	ns	
t _{PD}	CE ₁ HIGH/CE ₂ LOW to power-down ^[13]	-	10	ns	
t _{DBE}	Byte enable to data valid	-	5	ns	
t _{LZBE}	Byte enable to low Z	0	_	ns	
t _{HZBE}	Byte disable to high Z	-	6	ns	
Write Cycle [14	, 15]		•	•	
t _{WC}	Write cycle time	10	-	ns	
t _{SCE}	CE ₁ LOW/CE ₂ HIGH to write end	7	_	ns	
t _{AW}	Address setup to write end	7	-	ns	
t _{HA}	Address hold from write end	0	-	ns	
t _{SA}	Address setup to write start	0	-	ns	
t _{PWE}	WE pulse width	7	_	ns	
t _{SD}	Data setup to write end	5	_	ns	
t _{HD}	Data hold from write end	0	_	ns	
t _{LZWE}	WE HIGH to low Z ^[12,13.]	3	-	ns	
t _{HZWE}	WE LOW to high Z ^[12,13.]	-	5	ns	
t _{BW}	Byte Enable to End of Write	7	-	ns	

Notes

13. These parameters are guaranteed by design and are not tested. 14. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. Chip enables must be active and \overline{WE} and byte enables must be LOW to initiate a write, and the transition of any of these signals can terminate. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

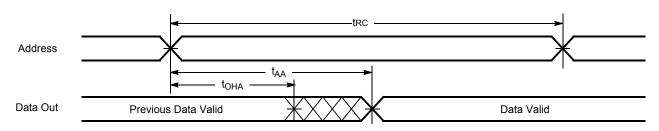
^{10.} Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V. Test conditions for the read cycle use output loading shown in part (a) of Figure 3 on page 6, unless specified otherwise.
11. t_{POWER} gives the minimum amount of time that the power supply is at typical V_{CC} values until the first memory access is performed.
12. t_{HZCE}, t_{HZCE}, t_{HZCE}, t_{HZCE}, t_{LZCE}, t_L

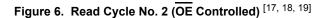
^{15.} The minimum write cycle time for Write Cycle No. 2 (WE Controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD}.

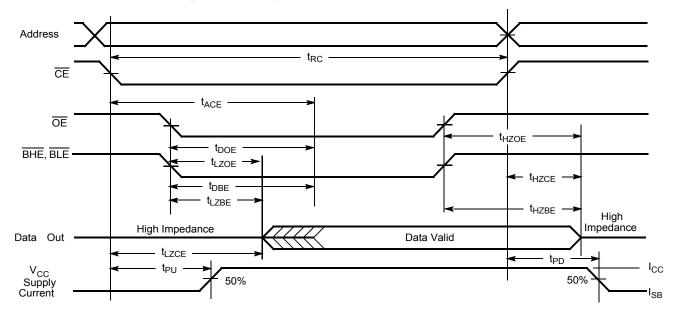


Switching Waveforms

Figure 5. Read Cycle No. 1 (Address Transition Controlled) ^[16, 17]





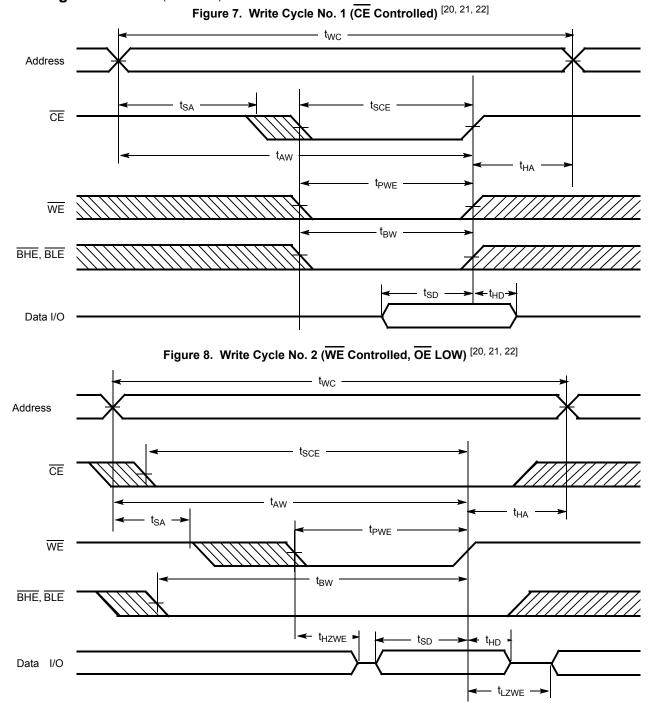


Notes

- 16. The device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$, \overline{BHE} , \overline{BLE} or both = V_{IL} .
- 17. $\overline{\text{WE}}$ is HIGH for read cycle.
- 18. \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.
- 19. Address valid before or similar to \overline{CE} transition LOW.



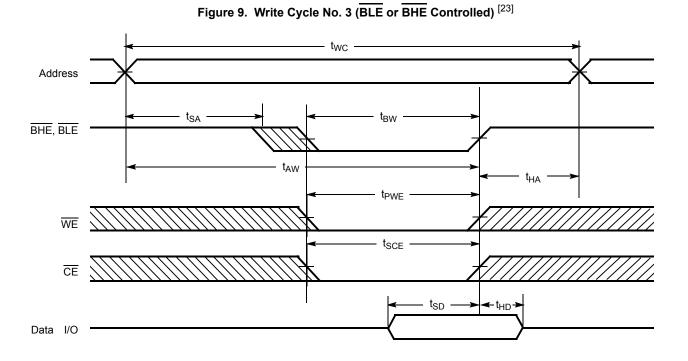
Switching Waveforms (continued)



- Notes 20. \overline{CE} is the logical combination of \overline{CE}_1 and \overline{CE}_2 . When \overline{CE}_1 is LOW and \overline{CE}_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or \overline{CE}_2 is LOW, \overline{CE} is HIGH.
- 21. Data I/O is high impedance if \overline{OE} , \overline{BHE} , and/or $\overline{BLE} = V_{IH}$.
- 22. If TE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.



Switching Waveforms (continued)



Note 23. \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.





Truth Table

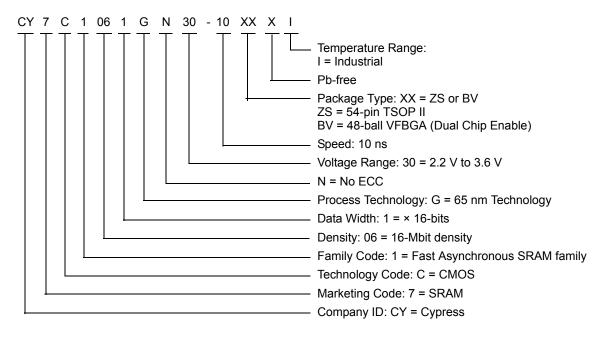
CE ₁	CE ₂	OE	WE	BLE	BHE	I/O ₀ –I/O ₇	I/O ₈ -I/O ₁₅	Mode	Power
Н	Х	Х	Х	Х	Х	High Z	High Z	Power down	Standby (I _{SB})
Х	L	Х	Х	Х	Х	High Z	High Z	Power down	Standby (I _{SB})
L	Н	L	Н	L	L	Data out	Data out	Read all bits	Active (I _{CC})
L	Н	L	Н	L	Н	Data out	High Z	Read lower bits only	Active (I _{CC})
L	Н	L	Н	Н	L	High Z	Data out	Read upper bits only	Active (I _{CC})
L	Н	Х	L	L	L	Data in	Data in	Write all bits	Active (I _{CC})
L	Н	Х	L	L	Н	Data in	High Z	Write lower bits only	Active (I _{CC})
L	Н	Х	L	Н	L	High Z	Data in	Write upper bits only	Active (I _{CC})
L	Н	Н	Н	Х	Х	High Z	High Z	Selected, outputs disabled	Active (I _{CC})



Ordering Information

Speed (ns)	Ordering Code	Package Diagram		Operating Range
10	CY7C1061GN30-10ZSXI	51-85160	54-pin TSOP II (22.4 × 11.84 × 1.0 mm) (Pb-free)	Industrial
	CY7C1061GN30-10BVXI	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm) (Pb-free) (Dual Chip Enable)	

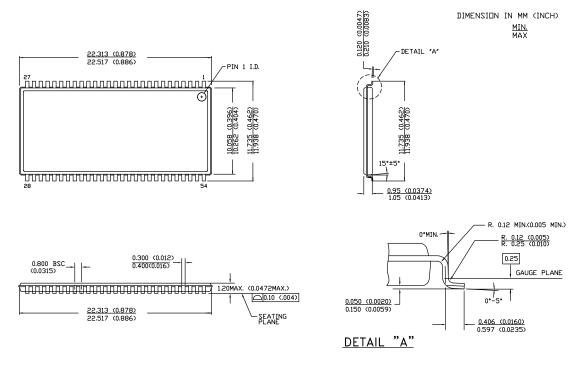
Ordering Code Definitions





Package Diagrams

Figure 10. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Z54-II Package Outline, 51-85160



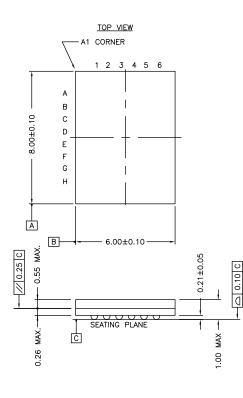
51-85160 *E

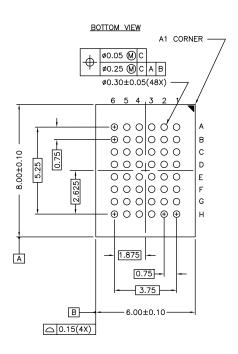




Package Diagrams (continued)







NOTE:

PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H





Acronyms

Acronym	Description			
BHE	Byte High Enable			
BLE	Byte Low Enable			
CE	Chip Enable			
CMOS	Complementary Metal Oxide Semiconductor			
I/O	Input/Output			
OE	Output Enable			
SRAM	Static Random Access Memory			
TSOP	Thin Small Outline Package			
TTL	Transistor-Transistor Logic			
VFBGA	Very Fine-Pitch Ball Grid Array			
WE	Write Enable			

Document Conventions

Units of Measure

Symbol	Unit of Measure			
°C	degree Celsius			
MHz	megahertz			
μA	microampere			
μS	microsecond			
mA	milliampere			
mm	millimeter			
ns	nanosecond			
Ω	ohm			
%	percent			
pF	picofarad			
V	volt			
W	watt			



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Document Number: 001-93060				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	4505531	VINI	01/02/2015	New data sheet.
*A	4900408	NILE	09/11/2015	Updated DC Electrical Characteristics: Updated details in "Test Conditions" column of V _{OH} and V _{OL} parameters. Updated Ordering Information: No change in part numbers. Replaced "51-85178" with "51-85150" in "Package Diagram" column. Replaced "8 × 9.5 × 1 mm" with "6 × 8 × 1.0 mm" in "Package Type" column. Updated Package Diagrams: Removed spec 51-85178 *C. Added spec 51-85150 *H. Updated to new template.



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