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# 512K x 32 Static RAM

## Features

- **High speed**
  - $t_{AA} = 8 \text{ ns}$
- **Low active power**
  - 1080 mW (max.)
- **Operating voltages of  $3.3 \pm 0.3\text{V}$**
- **2.0V data retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with  $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$  features**
- **Available in non Pb-free 119-ball PBGA package**

## Functional Description

The CY7C1062AV33 is a high-performance CMOS Static RAM organized as 524,288 words by 32 bits.

Writing to the device is accomplished by enabling the chip ( $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$  LOW) and forcing the Write Enable (WE) input LOW. If Byte Enable A ( $\overline{B}_A$ ) is LOW, then data from I/O

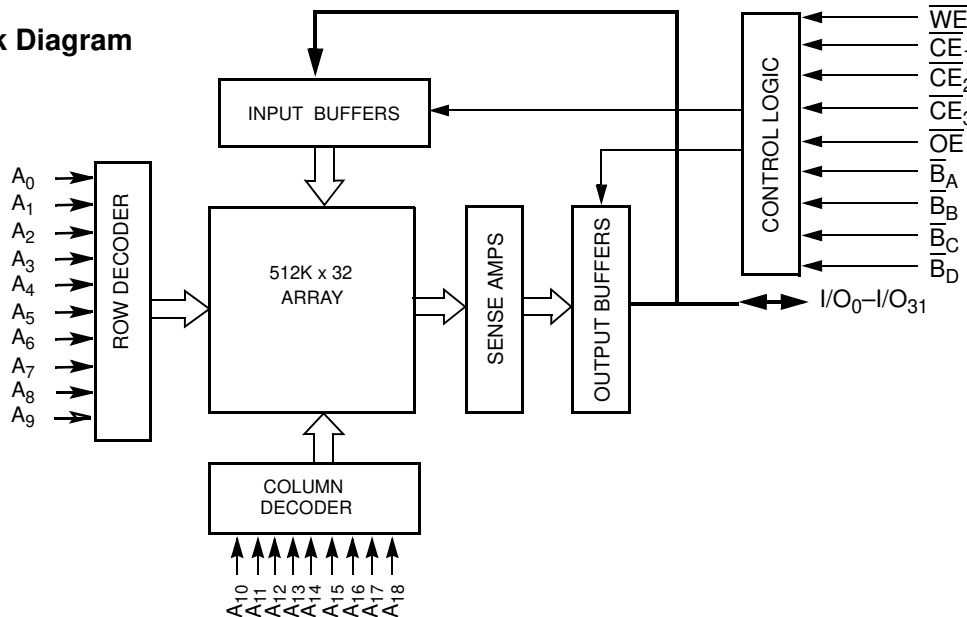
pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>18</sub>). If Byte Enable B ( $\overline{B}_B$ ) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>18</sub>). Likewise,  $\overline{B}_C$  and  $\overline{B}_D$  correspond with the I/O pins I/O<sub>16</sub> to I/O<sub>23</sub> and I/O<sub>24</sub> to I/O<sub>31</sub>, respectively.

Reading from the device is accomplished by enabling the chip ( $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$  LOW) while forcing the Output Enable ( $\overline{OE}$ ) LOW and Write Enable (WE) HIGH. If the first Byte Enable ( $\overline{B}_A$ ) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte Enable B ( $\overline{B}_B$ ) is LOW, then data from memory will appear on I/O<sub>8</sub> to I/O<sub>15</sub>. Similarly,  $\overline{B}_C$  and  $\overline{B}_D$  correspond to the third and fourth bytes. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O<sub>0</sub> through I/O<sub>31</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{CE}_1$ ,  $\overline{CE}_2$  or  $\overline{CE}_3$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the byte selects are disabled ( $\overline{B}_{A-D}$  HIGH), or during a write operation ( $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$  LOW, and WE LOW).

The CY7C1062AV33 is available in a 119-ball pitch ball grid array (PBGA) package.

## Logic Block Diagram



## Selection Guide

		-8	-10	-12	Unit
Maximum Access Time		8	10	12	ns
Maximum Operating Current	Com'l	300	275	260	mA
	Ind'l	300	275	260	
Maximum CMOS Standby Current	Com'l/Ind'l	50	50	50	mA

**Pin Configurations<sup>[1, 2]</sup>**
**119-ball PBGA**
**(Top View)**

	<b>1</b>	<b>2</b>	<b>3</b>	<b>4</b>	<b>5</b>	<b>6</b>	<b>7</b>
<b>A</b>	I/O <sub>16</sub>	A	A	A	A	A	I/O <sub>0</sub>
<b>B</b>	I/O <sub>17</sub>	A	A	$\overline{CE}_1$	A	A	I/O <sub>1</sub>
<b>C</b>	I/O <sub>18</sub>	$\overline{B}_c$	$\overline{CE}_2$	NC	$\overline{CE}_3$	$\overline{B}_a$	I/O <sub>2</sub>
<b>D</b>	I/O <sub>19</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O <sub>3</sub>
<b>E</b>	I/O <sub>20</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	I/O <sub>4</sub>
<b>F</b>	I/O <sub>21</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O <sub>5</sub>
<b>G</b>	I/O <sub>22</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	I/O <sub>6</sub>
<b>H</b>	I/O <sub>23</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O <sub>7</sub>
<b>J</b>	NC	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	DNU
<b>K</b>	I/O <sub>24</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O <sub>8</sub>
<b>L</b>	I/O <sub>25</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	I/O <sub>9</sub>
<b>M</b>	I/O <sub>26</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O <sub>10</sub>
<b>N</b>	I/O <sub>27</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	I/O <sub>11</sub>
<b>P</b>	I/O <sub>28</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O <sub>12</sub>
<b>R</b>	I/O <sub>29</sub>	A	$\overline{B}_d$	NC	$\overline{B}_b$	A	I/O <sub>13</sub>
<b>T</b>	I/O <sub>30</sub>	A	A	$\overline{WE}$	A	A	I/O <sub>14</sub>
<b>U</b>	I/O <sub>31</sub>	A	A	$\overline{OE}$	A	A	I/O <sub>15</sub>

**Notes:**

1. NC pins are not connected on the die.
2. DNU pins have to be left floating or tied to VSS to ensure proper application.



**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied ..... -55°C to +125°C  
 Supply Voltage on  $V_{CC}$  to Relative GND<sup>[3]</sup> .... -0.5V to +4.6V  
 DC Voltage Applied to Outputs in High-Z State<sup>[3]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[3]</sup> ..... -0.5V to  $V_{CC} + 0.5V$   
 Current into Outputs (LOW) ..... 20 mA

**Operating Range**

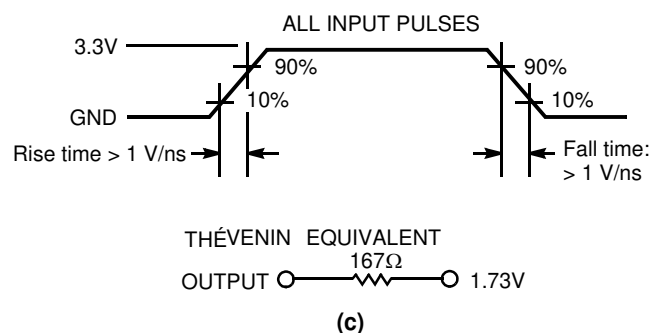
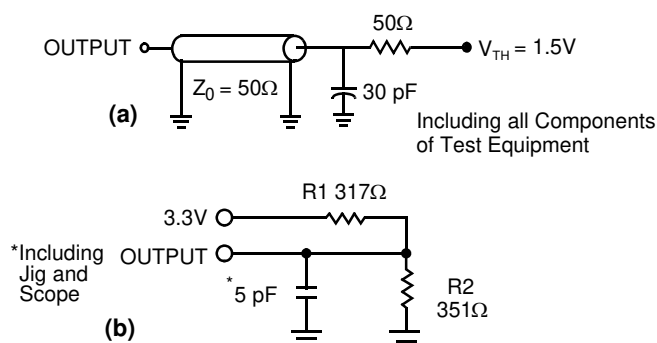
Range	Ambient Temperature	$V_{CC}$
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	-40°C to +85°C	

**DC Electrical Characteristics Over the Operating Range**

Parameter	Description	Test Conditions	-8		-10		-12		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4		0.4	V
$V_{IH}$	Input HIGH Voltage		2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW Voltage <sup>[3]</sup>		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
$I_{IX}$	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	-1	+1	µA
$I_{OZ}$	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$ , Output Disabled	-1	+1	-1	+1	-1	+1	µA
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}, f = f_{MAX} = 1/t_{RC}$	Com'l	300		275		260	mA
			Ind'l	300		275		260	mA
$I_{SB1}$	Automatic CE Power-down Current — TTL Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$		70		70		70	mA
$I_{SB2}$	Automatic CE Power-down Current — CMOS Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ , or $V_{IN} \leq 0.3V$ , $f = 0$	Com'l/ Ind'l	50		50		50	mA

**Capacitance<sup>[4]</sup>**

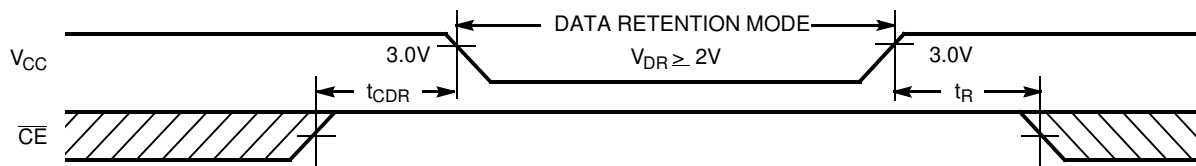
Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz}, V_{CC} = 3.3V$	8	pF
$C_{OUT}$	I/O Capacitance		10	pF

**AC Test Loads and Waveforms<sup>[5]</sup>**

**Notes:**

- $V_{IL}$  (min.) = -2.0V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.
- Valid SRAM operation does not occur until the power supplies have reached the minimum operating  $V_{DD}$  (3.0V). As soon as 1 ms ( $T_{power}$ ) after reaching the minimum operating  $V_{DD}$ , normal SRAM operation can begin including reduction in  $V_{DD}$  to the data retention ( $V_{CCDR}$ , 2.0V) voltage.

**AC Switching Characteristics** Over the Operating Range<sup>[6]</sup>

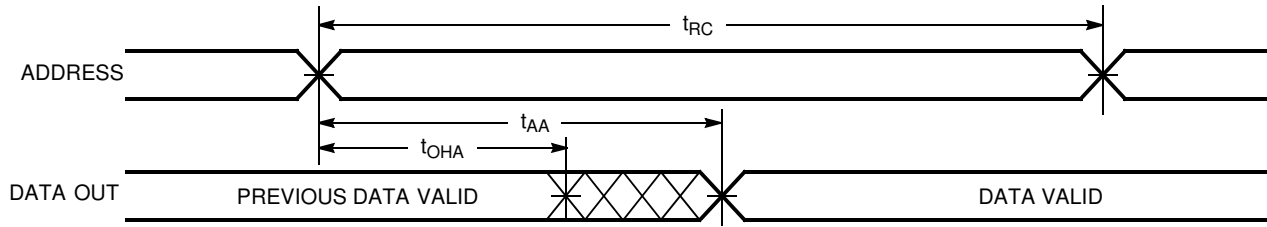
Parameter	Description	-8		-10		-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>								
$t_{power}$	$V_{CC}$ (typical) to the first access <sup>[7]</sup>	1		1		1		ms
$t_{RC}$	Read Cycle Time	8		10		12		ns
$t_{AA}$	Address to Data Valid		8		10		12	ns
$t_{OHA}$	Data Hold from Address Change	3		3		3		ns
$t_{ACE}$	$\overline{CE}_1$ , $\overline{CE}_2$ , or $\overline{CE}_3$ LOW to Data Valid		8		10		12	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		5		5		6	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low-Z <sup>[8]</sup>	1		1		1		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High-Z <sup>[8]</sup>		5		5		6	ns
$t_{LZCE}$	$\overline{CE}_1$ , $\overline{CE}_2$ , or $\overline{CE}_3$ LOW to Low-Z <sup>[8]</sup>	3		3		3		ns
$t_{HZCE}$	$\overline{CE}_1$ , $\overline{CE}_2$ , or $\overline{CE}_3$ HIGH to High-Z <sup>[8]</sup>		5		5		6	ns
$t_{PU}$	$\overline{CE}_1$ , $\overline{CE}_2$ , or $\overline{CE}_3$ LOW to Power-up <sup>[9]</sup>	0		0		0		ns
$t_{PD}$	$\overline{CE}_1$ , $\overline{CE}_2$ , or $\overline{CE}_3$ HIGH to Power-down <sup>[9]</sup>		8		10		12	ns
$t_{DBE}$	Byte Enable to Data Valid		5		5		6	ns
$t_{LZBE}$	Byte Enable to Low-Z <sup>[8]</sup>	1		1		1		ns
$t_{HZBE}$	Byte Disable to High-Z <sup>[8]</sup>		5		5		6	ns
<b>Write Cycle</b> <sup>[10, 11]</sup>								
$t_{WC}$	Write Cycle Time	8		10		12		ns
$t_{SCE}$	$\overline{CE}_1$ , $\overline{CE}_2$ , or $\overline{CE}_3$ LOW to Write End	6		7		8		ns
$t_{AW}$	Address Set-up to Write End	6		7		8		ns
$t_{HA}$	Address Hold from Write End	0		0		0		ns
$t_{SA}$	Address Set-up to Write Start	0		0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	6		7		8		ns
$t_{SD}$	Data Set-up to Write End	5		5.5		6		ns
$t_{HD}$	Data Hold from Write End	0		0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low-Z <sup>[8]</sup>	3		3		3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High-Z <sup>[8]</sup>		5		5		6	ns
$t_{BW}$	Byte Enable to End of Write	6		7		8		ns

**Data Retention Waveform**

**Notes:**

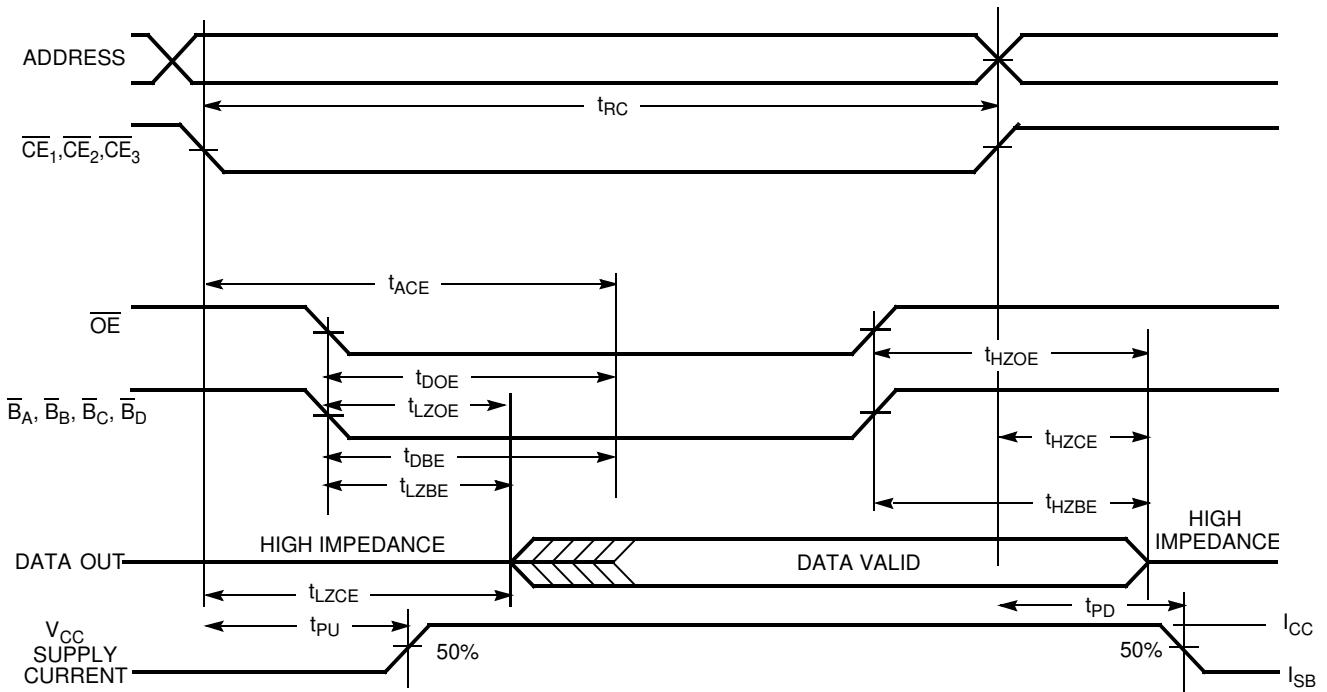
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and transmission line loads. Test conditions for the read cycle use output loading as shown in (a) of AC Test Loads, unless specified otherwise.
- This part has a voltage regulator that steps down the voltage from 3V to 2V internally.  $t_{power}$  time has to be provided initially before a read/write operation is started.
- $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZWE}$ ,  $t_{HZBE}$ , and  $t_{LZOE}$ ,  $t_{LZCE}$ ,  $t_{LZWE}$ , and  $t_{LZBE}$  are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured  $\pm 200$  mV from steady-state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW,  $\overline{CE}_2$  HIGH,  $\overline{CE}_3$  LOW, and  $\overline{WE}$  LOW. The chip enables must be active and  $\overline{WE}$  must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

Switching Waveforms

Read Cycle No. 1<sup>[12, 13]</sup>



Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[13, 14]</sup>

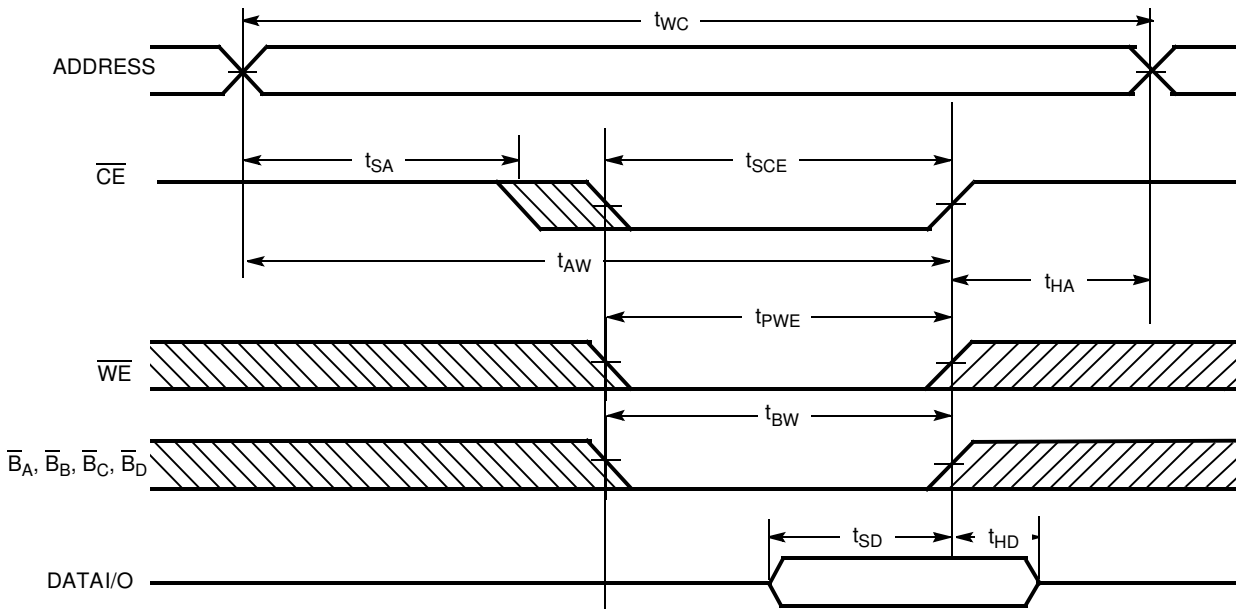


Notes:

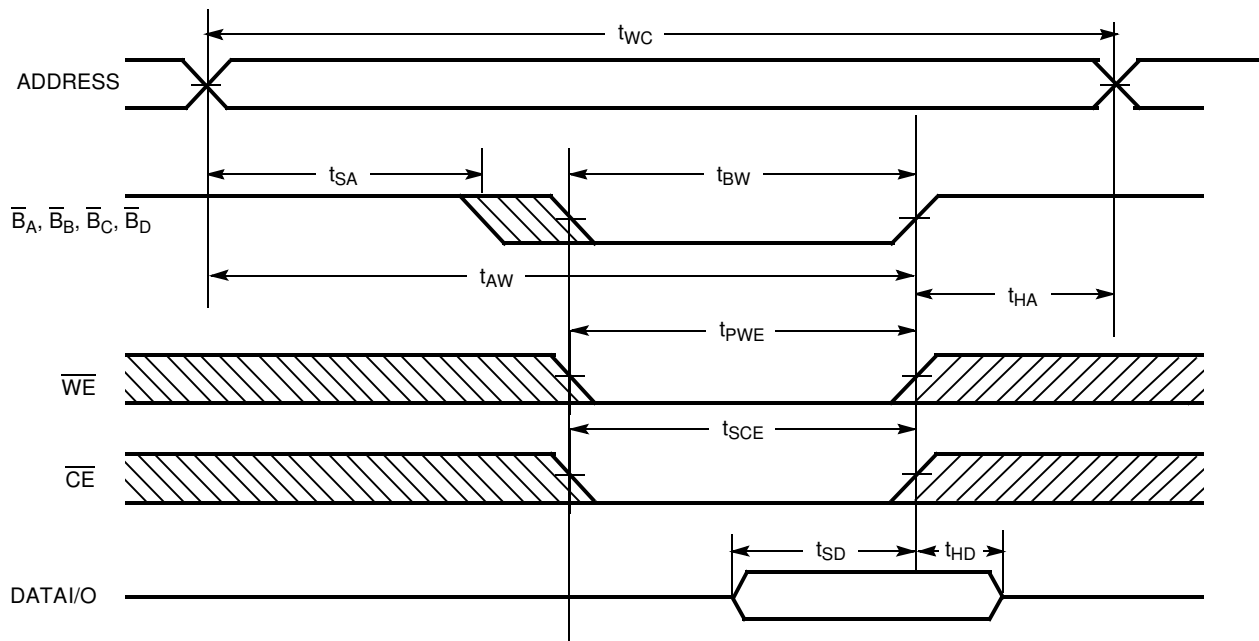
- 12. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_A$ ,  $\overline{B}_A$ ,  $\overline{B}_B$ ,  $\overline{B}_C$ ,  $\overline{B}_D = V_{IL}$ .
- 13.  $\overline{WE}$  is HIGH for read cycle.
- 14. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ( $\overline{CE}$  Controlled)<sup>[15, 16, 17]</sup>



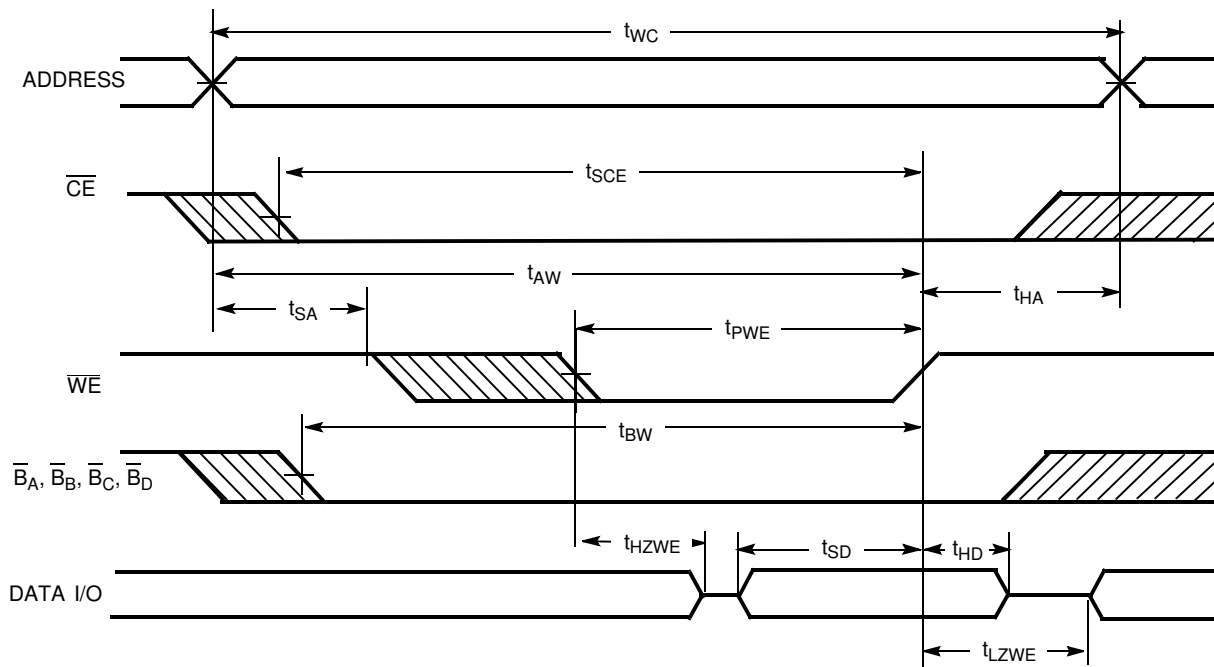
Write Cycle No. 2 ( $\overline{BLE}$  or  $\overline{BHE}$  Controlled)<sup>[15, 16, 17]</sup>



Notes:

- 15.  $\overline{CE}$  indicates a combination of all three chip enables. When ACTIVE LOW,  $\overline{CE}$  indicates the  $\overline{CE_1}, \overline{CE_2},$  and  $\overline{CE_3}$  are LOW.
- 16. Data I/O is high-impedance if  $\overline{OE}$  or  $\overline{B_A}, \overline{B_B}, \overline{B_C}, \overline{B_D} = V_{IH}$ .
- 17. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.

**Switching Waveforms** (continued)

**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)**

**Truth Table**

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{CE}_3$	$\overline{OE}$	$\overline{WE}$	$\overline{B}_A$	$\overline{B}_B$	$\overline{B}_C$	$\overline{B}_D$	I/O <sub>0</sub> – I/O <sub>7</sub>	I/O <sub>8</sub> – I/O <sub>15</sub>	I/O <sub>16</sub> – I/O <sub>23</sub>	I/O <sub>24</sub> – I/O <sub>31</sub>	Mode	Power
H	X	X	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Power Down	(I <sub>SB</sub> )
X	H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Power Down	(I <sub>SB</sub> )
X	X	H	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Power Down	(I <sub>SB</sub> )
L	L	L	L	H	L	L	L	L	Data Out	Data Out	Data Out	Data Out	Read All Bits	(I <sub>CC</sub> )
L	L	L	L	H	L	H	H	H	Data Out	High-Z	High-Z	High-Z	Read Byte A Bits Only	(I <sub>CC</sub> )
L	L	L	L	H	H	L	H	H	High-Z	Data Out	High-Z	High-Z	Read Byte B Bits Only	(I <sub>CC</sub> )
L	L	L	L	H	H	H	L	H	High-Z	High-Z	Data Out	High-Z	Read Byte C Bits Only	(I <sub>CC</sub> )
L	L	L	L	H	H	H	H	L	High-Z	High-Z	High-Z	Data Out	Read Byte D Bits Only	(I <sub>CC</sub> )
L	L	L	X	L	L	L	L	L	Data In	Data In	Data In	Data In	Write All Bits	(I <sub>CC</sub> )
L	L	L	X	L	L	H	H	H	Data In	High-Z	High-Z	High-Z	Write Byte A Bits Only	(I <sub>CC</sub> )
L	L	L	X	L	H	L	H	H	High-Z	Data In	High-Z	High-Z	Write Byte B Bits Only	(I <sub>CC</sub> )
L	L	L	X	L	H	H	L	H	High-Z	High-Z	Data In	High-Z	Write Byte C Bits Only	(I <sub>CC</sub> )
L	L	L	X	L	H	H	H	L	High-Z	High-Z	High-Z	Data In	Write Byte D Bits Only	(I <sub>CC</sub> )
L	L	L	H	H	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Selected, Outputs Disabled	(I <sub>CC</sub> )

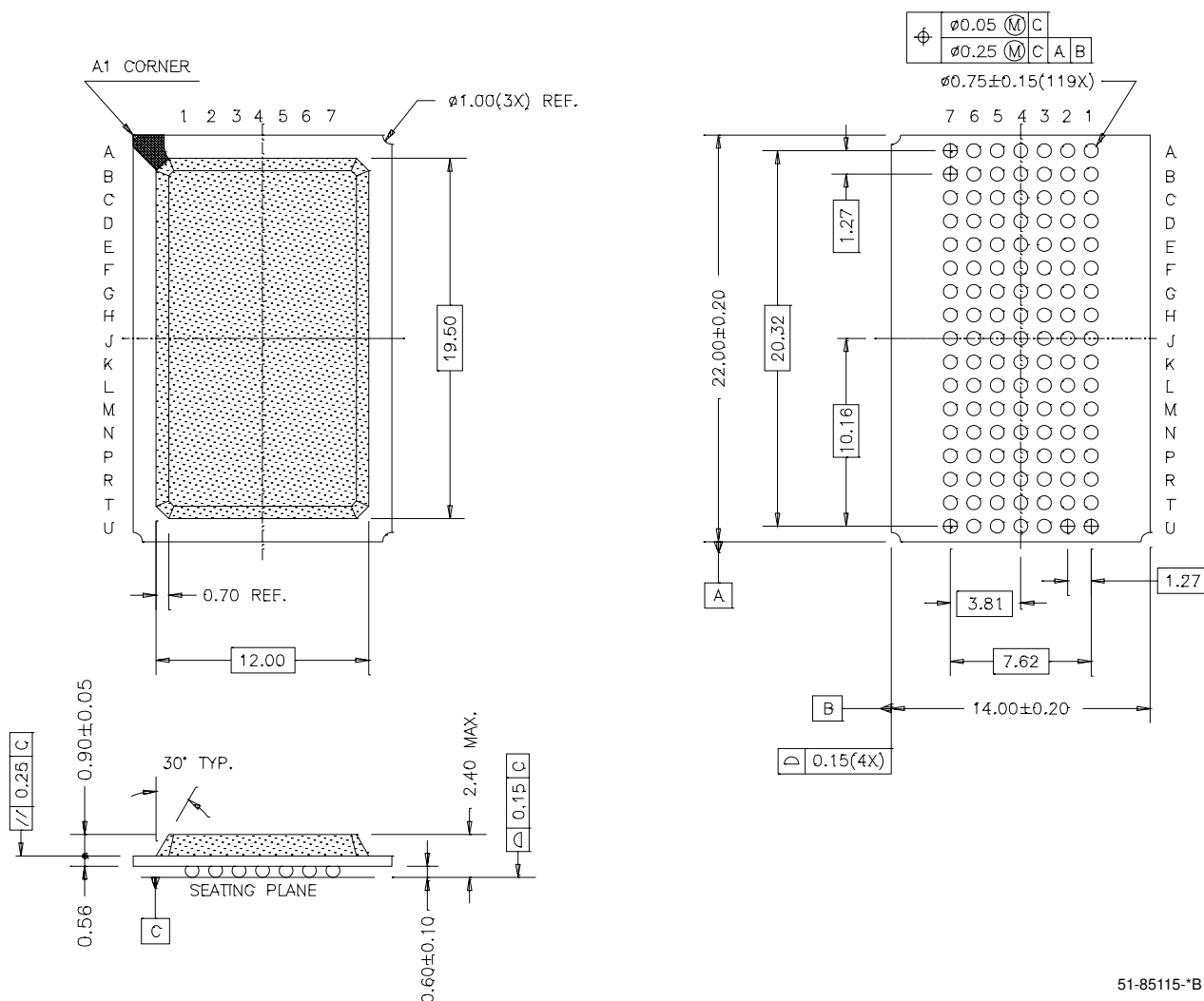


**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7C1062AV33-8BGC	51-85115	119-ball (14 x 22 x 2.4 mm) PBGA	Commercial
10	CY7C1062AV33-10BGC			Industrial
	CY7C1062AV33-10BGI			Commercial
12	CY7C1062AV33-12BGC			Industrial
	CY7C1062AV33-12BGI			

**Package Diagram**

**119-ball PBGA (14 x 22 x 2.4 mm) (51-85115)**



51-85115-\*B

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Document History Page

Document Title: CY7C1062AV33 512K x 32 Static RAM				
Document Number: 38-05137				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	109752	02/27/02	HGK	New Data Sheet
*A	117059	09/19/02	DFP	Removed 15-ns bin and added 8-ns bin. Changed $\overline{CE}_2$ TO $\overline{CE}_2$ . Changed $C_{IN}$ – input capacitance – from 6 pF to 8 pF. Changed $C_{OUT}$ – output capacitance – from 8 pF to 10 pF.
*B	119389	10/07/02	DFP	Updated $I_{CC}$ , $T_{sd}$ , and $T_{doe}$ parameters. Removed note 7 ( $I_Z/h_Z$ comment).
*C	120384	11/13/02	DFP	Final Data Sheet. Removed note 2. Added note 3 to “AC Test Loads and Waveforms” and note 7 to $t_{pu}$ and $t_{pd}$ .
*D	124440	2/25/03	MEG	Changed ISB1 from 100 mA to 70 mA
*E	329638	See ECN	RKF	Removed $\overline{CE}_2$ waveform showing Active High signal timing on Page #5, and included it with the $\overline{CE}_1$ , $\overline{CE}_3$ waveform. Corrected Truth Table on page 7 with $\overline{CE}_2$ active low information
*F	492137	See ECN	NXR	Included note #1 and 2 on page #2 Changed the description of $I_{IX}$ from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Updated Ordering Information Table