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# CY7C1069GN

# 16-Mbit (2M × 8) Static RAM

## Features

- High speed
  - $t_{AA}$ = 10 ns
- Low active power
  - $I_{CC}$ = 90 mA at 100 MHz
- Low complementary metal oxide semiconductor (CMOS) standby power
  - $I_{SB2}$ = 20 mA (typical)
- Operating voltages of 2.2 V to 3.6 V
- 1.0 V data retention
- Automatic power-down when deselected
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Easy memory expansion with $\overline{CE}_1$ and $CE_2$ features
- Available in Pb-free 54-pin thin small outline package (TSOP) Type II and 48-ball very fine-pitch ball grid array (VFBGA) packages.

## Functional Description

The CY7C1069GN is a high performance CMOS Static RAM organized as 2,097,152 words by 8 bits.

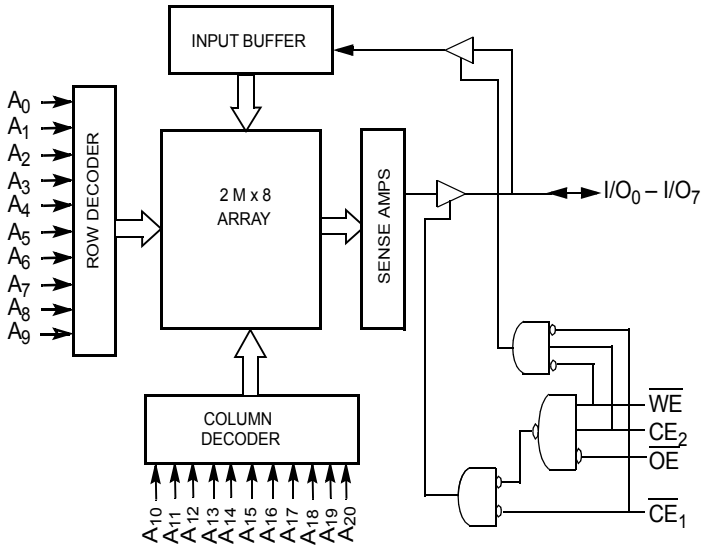
To write to the device, take Chip Enables ($\overline{CE}_1$ LOW and $CE_2$ HIGH) and Write Enable ($\overline{WE}$) input LOW. Data on the eight I/O pins ($I/O_0$ through $I/O_7$) is then written into the location specified on the address pins ($A_0$ through $A_{20}$).

To read from the device, take Chip Enables ($\overline{CE}_1$ LOW and $CE_2$ HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins. See Truth Table on page 10 for a complete description of Read and Write modes.

The input and output pins ($I/O_0$ through $I/O_7$) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH or $CE_2$ LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, $CE_2$ HIGH, and $\overline{WE}$ LOW).

The CY7C1069GN is available in a 54-pin TSOP II and a 48-ball very fine-pitch ball grid array (VFBGA) package.

## Logic Block Diagram



## Contents

## Selection Guide

| Description | -10 | Unit |
|---|---|---|
| Maximum access time | 10 | ns |
| Maximum operating current | 110 | mA |
| Maximum CMOS standby current | 30 | mA |

## Pin Configurations

**Figure 1. 54-pin TSOP II pinout (Top View)** [1]

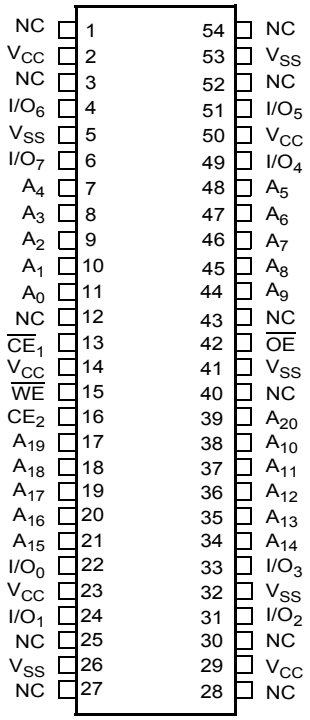
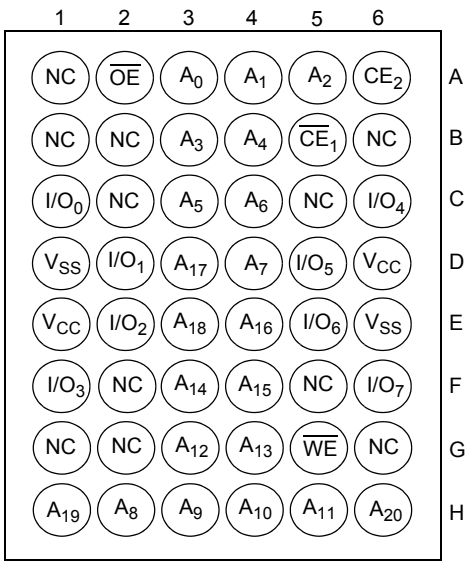



**Figure 2. 48-ball VFBGA pinout (Top View)** [1]




**Note**
1. NC pins are not connected on the die.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on $V_{CC}$ relative to GND [2] ..... –0.5 V to $V_{CC}$ + 0.5 V

DC voltage applied to outputs in High Z state [2] ..... –0.5 V to $V_{CC}$ + 0.5 V

DC input voltage [2] ..... –0.5 V to $V_{CC}$ + 0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, method 3015) ..... > 2001 V

Latch-up current ..... > 140 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Industrial | –40 °C to +85 °C | 3.3 V ± 0.3 V |

## DC Electrical Characteristics

Over the Operating Range

| Parameter | Description | | Test Conditions | -10ns | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ [3] | Max | |
| $V_{OH}$ | Output HIGH voltage | 2.2 V to 2.7 V | Min $V_{CC}$, $I_{OH}$ = –1.0 mA | 2.0 | – | – | V |
| | | 2.7 V to 3.0 V | Min $V_{CC}$, $I_{OH}$ = –4.0 mA | 2.2 | – | – | |
| | | 3.0 V to 3.6 V | Min $V_{CC}$, $I_{OH}$ = –4.0 mA | 2.4 | – | – | |
| $V_{OL}$ | Output LOW voltage | 2.2 V to 2.7 V | Min $V_{CC}$, $I_{OL}$ = 2.0 mA | – | – | 0.4 | V |
| | | 2.7 V to 3.6 V | Min $V_{CC}$, $I_{OL}$ = 8.0 mA | – | – | 0.4 | |
| $V_{IH}$ | Input HIGH voltage | 2.2 V to 2.7 V | – | 2.0 | – | $V_{CC}$ + 0.3 | V |
| | | 2.7 V to 3.6 V | – | 2.0 | – | $V_{CC}$ + 0.3 | |
| $V_{IL}$ | Input LOW voltage [2] | 2.2 V to 2.7 V | – | –0.3 | – | 0.6 | V |
| | | 2.7 V to 3.6 V | – | –0.3 | – | 0.8 | |
| $I_{IX}$ | Input leakage current | | GND ≤ $V_{IN}$ ≤ $V_{CC}$ | –1 | | +1 | µA |
| $I_{OZ}$ | Output leakage current | | GND ≤ $V_{OUT}$ ≤ $V_{CC}$, Output disabled | –1 | | +1 | µA |
| $I_{CC}$ | $V_{CC}$ operating supply current | | $V_{CC}$ = Max, f = $f_{MAX}$ = $1/t_{RC}$, $I_{OUT}$ = 0 mA, CMOS levels | – | 90 | 110 | mA |
| $I_{SB1}$ | Automatic CE power-down current – TTL inputs | | Max $V_{CC}$, $\overline{CE_1}$ ≥ $V_{IH}$, $CE_2$ ≤ $V_{IL}$, $V_{IN}$ ≥ $V_{IH}$ or $V_{IN}$ ≤ $V_{IL}$, f = $f_{MAX}$ | – | – | 40 | mA |
| $I_{SB2}$ | Automatic CE power-down current – CMOS inputs | | Max $V_{CC}$, $\overline{CE_1}$ ≥ $V_{CC}$ – 0.3 V, $CE_2$ ≤ 0.3 V, $V_{IN}$ ≥ $V_{CC}$ – 0.3 V or $V_{IN}$ ≤ 0.3 V, f = 0 | – | 20 | 30 | mA |

**Notes**

2. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = $V_{CC}$ + 2 V for pulse durations of less than 20 ns.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = 3 V (for $V_{CC}$ range of 2.2 V–3.6 V)

## Capacitance

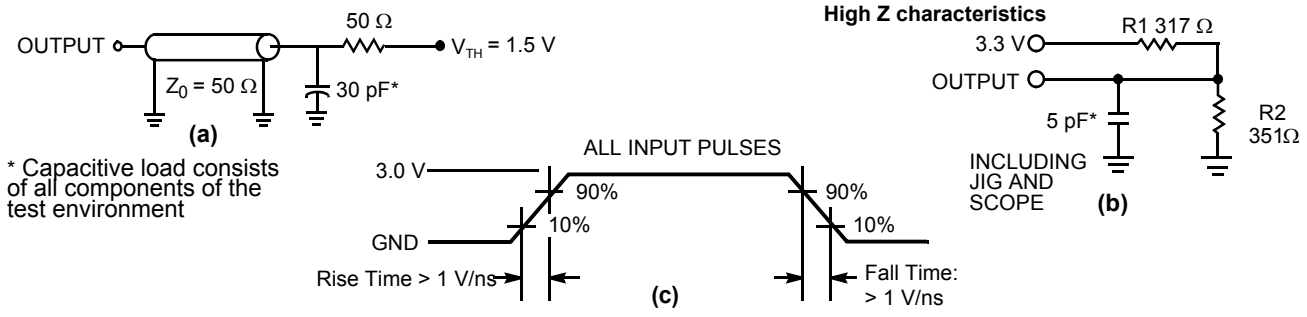
| Parameter [4] | Description | Test Conditions | TSOP II | VFBGA | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{CC}$ = 3.3 V | 10 | 10 | pF |
| $C_{OUT}$ | IO capacitance | | 10 | 10 | pF |

## Thermal Resistance

| Parameter [4] | Description | Test Conditions | TSOP II | VFBGA | Unit |
|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance (junction to ambient) | Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board | 93.63 | 31.50 | °C/W |
| $\Theta_{JC}$ | Thermal resistance (junction to case) | | 21.58 | 15.75 | °C/W |

## AC Test Loads and Waveforms

**Figure 3. AC Test Loads and Waveforms [5]**




**Notes**
4. Tested initially and after any design or process changes that may affect these parameters.
5. Full device AC operation assumes a 100-µs ramp time from 0 to $V_{CC(min)}$ and 100-µs wait time after $V_{CC}$ stabilization.

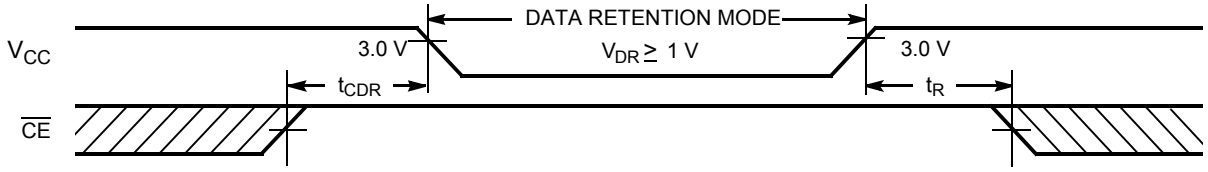
## Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for data retention | – | 1.0 | – | V |
| $I_{CCDR}$ | Data retention current | $V_{CC} = V_{DR}$, $\overline{CE}_1 \geq V_{CC} - 0.2$ V, $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V | _ | 30 | mA |
| $t_{CDR}$ [6] | Chip deselect to data retention time | – | 0 | – | ns |
| $t_R$ [7] | Operation recovery time | – | 10 | – | ns |

## Data Retention Waveform

**Figure 4. Data Retention Waveform**




**Notes**
6. Tested initially and after any design or process changes that may affect these parameters.
7. Full device operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min.)}$ > 100 µs or stable at $V_{CC(min.)}$ > 100 µs.

## AC Switching Characteristics

Over the Operating Range

| Parameter [8] | Description | -10 | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| **Read Cycle** | | | | |
| $t_{power}$ | $V_{CC}$(typical) to the first access [9, 10] | 100 | – | µs |
| $t_{RC}$ | Read cycle time | 10 | – | ns |
| $t_{AA}$ | Address to data valid | – | 10 | ns |
| $t_{OHA}$ | Data hold from address change | 3 | – | ns |
| $t_{ACE}$ | $\overline{CE}_1$ LOW/$CE_2$ HIGH to data valid | – | 10 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to data valid | – | 5 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to low Z [11, 12, 13] | 0 | – | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to high Z [11, 12, 13] | – | 5 | ns |
| $t_{LZCE}$ | $\overline{CE}_1$ LOW/$CE_2$ HIGH to low Z [11, 12, 13] | 3 | – | ns |
| $t_{HZCE}$ | $\overline{CE}_1$ HIGH/$CE_2$ LOW to high Z [11, 12, 13] | – | 5 | ns |
| $t_{PU}$ | $\overline{CE}_1$ LOW/$CE_2$ HIGH to power-up [10] | 0 | – | ns |
| $t_{PD}$ | $\overline{CE}_1$ HIGH/$CE_2$ LOW to power-down [10] | – | 10 | ns |
| **Write Cycle** [14, 15] | | | | |
| $t_{WC}$ | Write cycle time | 10 | – | ns |
| $t_{SCE}$ | $\overline{CE}_1$ LOW/$CE_2$ HIGH to write end | 7 | – | ns |
| $t_{AW}$ | Address setup to write end | 7 | – | ns |
| $t_{HA}$ | Address hold from write end | 0 | – | ns |
| $t_{SA}$ | Address setup to write start | 0 | – | ns |
| $t_{PWE}$ | $\overline{WE}$ pulse width | 7 | – | ns |
| $t_{SD}$ | Data setup to write end | 5 | – | ns |
| $t_{HD}$ | Data hold from write end | 0 | – | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to low Z [11, 12, 13] | 3 | – | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to high Z [11, 12, 13] | – | 5 | ns |

**Notes**

8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V. Test conditions for the read cycle use output loading shown in (a) of Figure 3 on page 5, unless specified otherwise.
9. $t_{POWER}$ gives the minimum amount of time that the power supply is at typical $V_{CC}$ values until the first memory access is performed.
10. These parameters are guaranteed by design and are not tested.
11. $t_{HZOE}$, $t_{HZCE}$, $t_{HZWE}$, $t_{LZOE}$, $t_{LZCE}$, and $t_{LZWE}$ are specified with a load capacitance of 5 pF as in (b) of Figure 3 on page 5. Transition is measured ±200 mV from steady state voltage.
12. At any temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZBE}$ is less than $t_{LZBE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any device. These parameters are guaranteed by design and are not tested.
13. Tested initially and after any design or process changes that may affect these parameters.
14. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1$ = $V_{IL}$, and $CE_2$ = $V_{IH}$. $\overline{CE}_1$ and $\overline{WE}$ are LOW along with $CE_2$ HIGH to initiate a write, and the transition of any of these signals can terminate. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
15. The minimum write cycle time for Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) is the sum of $t_{HZWE}$ and $t_{SD}$.

## Switching Waveforms

**Figure 5. Read Cycle No. 1 (Address Transition Controlled)** [16, 17]

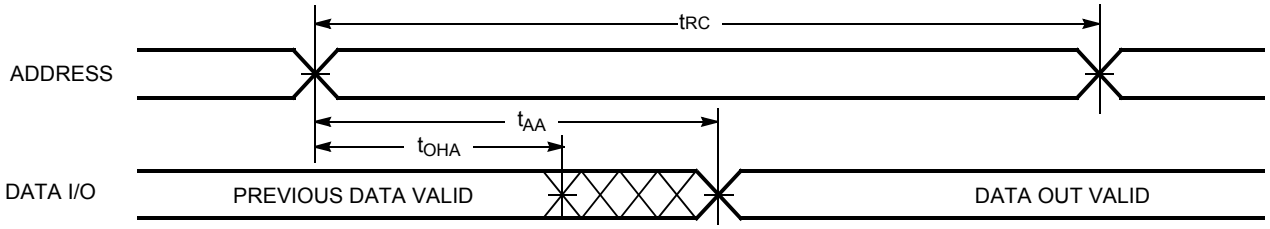
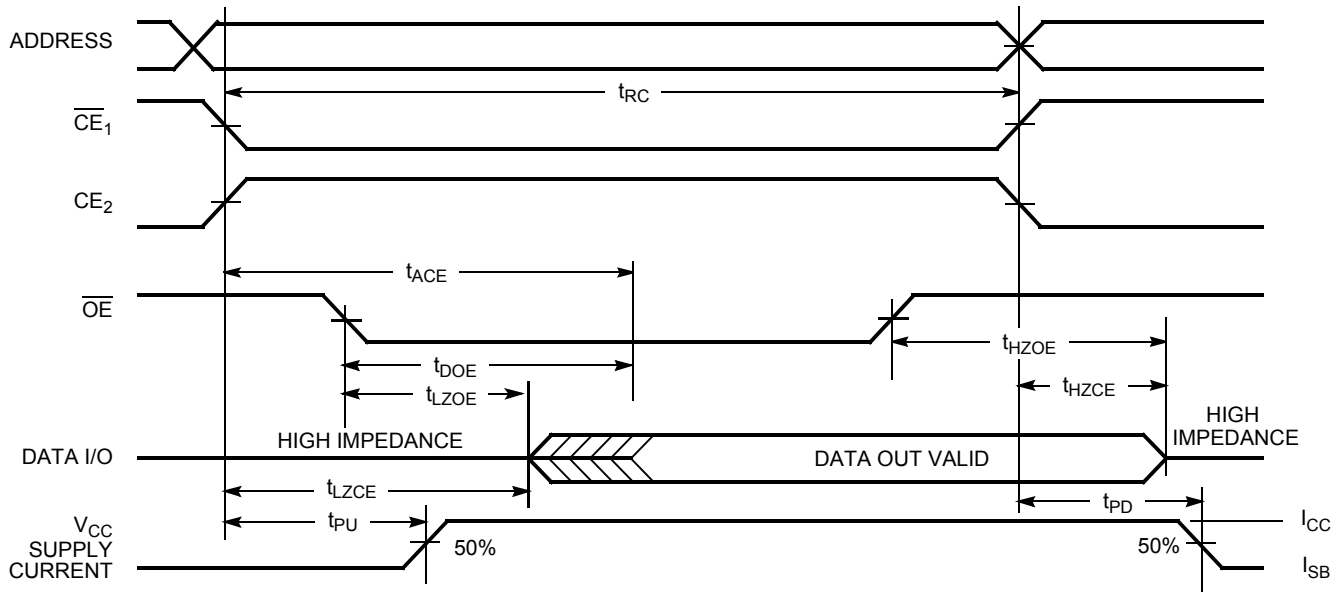



**Figure 6. Read Cycle No. 2 ($\overline{OE}$ Controlled)** [17, 18]




**Notes**
16. The device is continuously selected. $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$.
17. $\overline{WE}$ is HIGH for read cycle.
18. Address valid before or similar to $\overline{CE}_1$ transition LOW and $CE_2$ transition HIGH.

## Switching Waveforms (continued)

**Figure 7. Write Cycle No. 1 ($\overline{CE}$ Controlled)** [19, 20, 21, 22]

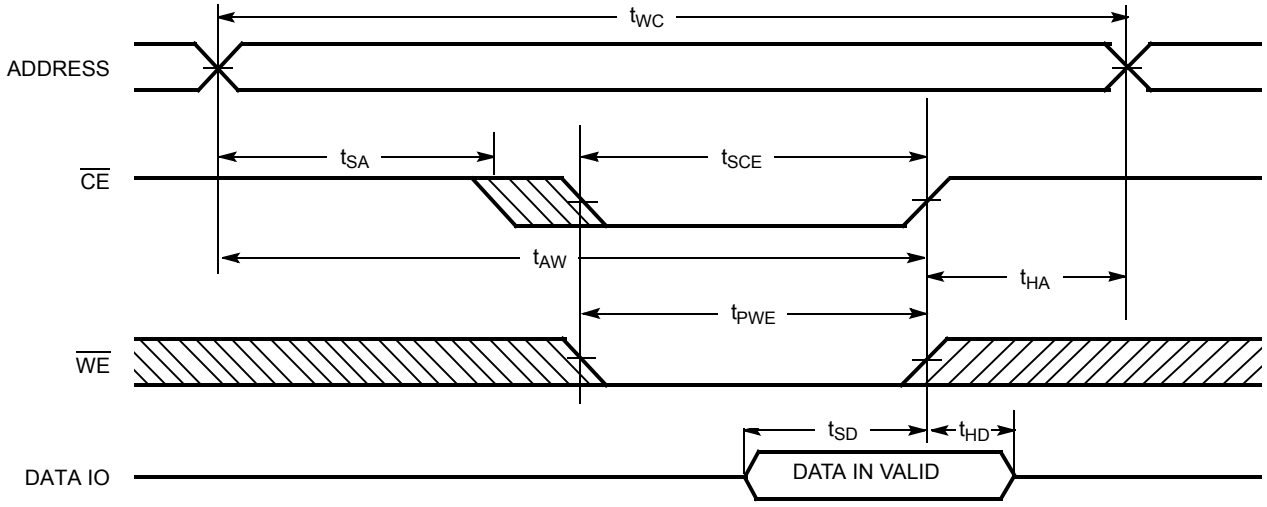
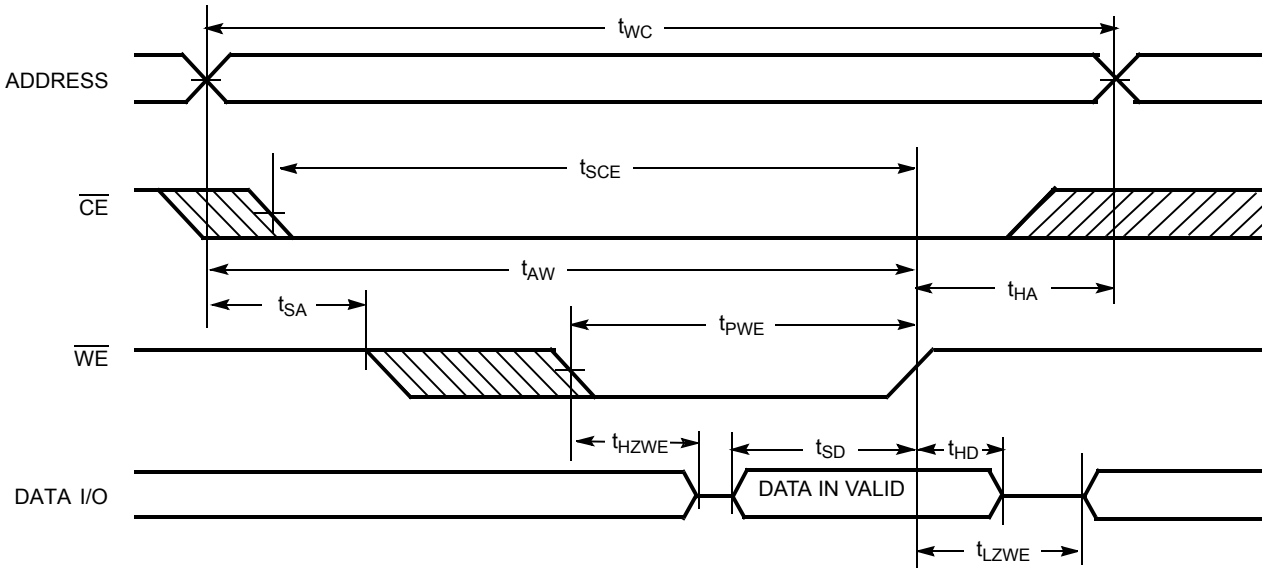



**Figure 8. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)** [19, 20, 21, 22]




**Notes**

19. $\overline{CE}$ is a shorthand combination of both $\overline{CE}_1$ and $CE_2$ combined. It is active LOW.
20. Data I/O is high impedance if $\overline{OE}$ = $V_{IH}$.
21. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.
22. The internal write time of the memory is defined by the overlap of WE = $V_{IL}$, CE = $V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

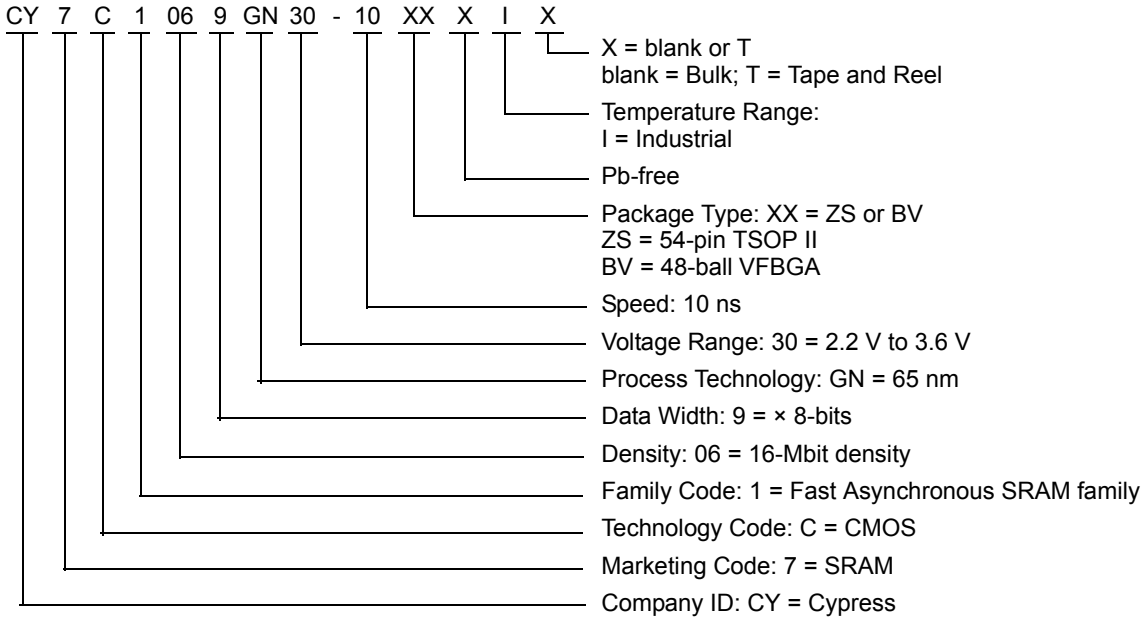
## Truth Table

| $\overline{CE}_1$ | $CE_2$ | $\overline{OE}$ | $\overline{WE}$ | $I/O_0$–$I/O_7$ | Mode | Power |
|---|---|---|---|---|---|---|
| H | X | X | X | High Z | Power-down | Standby ($I_{SB}$) |
| X | L | X | X | High Z | Power-down | Standby ($I_{SB}$) |
| L | H | L | H | Data out | Read all bits | Active ($I_{CC}$) |
| L | H | X | L | Data in | Write all bits | Active ($I_{CC}$) |
| L | H | H | H | High Z | Selected, outputs disabled | Active ($I_{CC}$) |

## Ordering Information

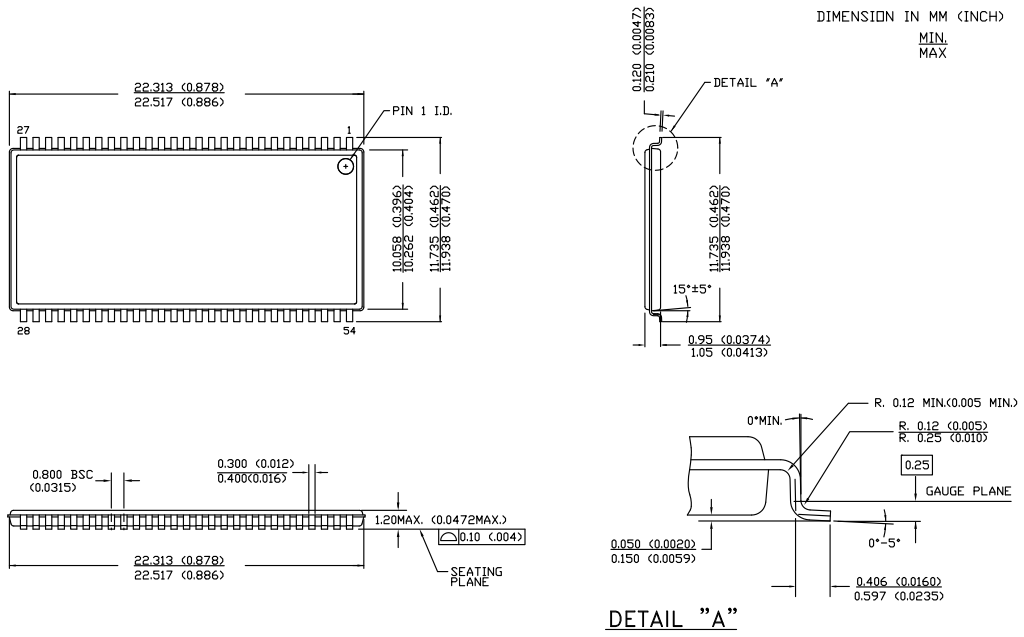
| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 10 | CY7C1069GN30-10ZSXI | 51-85160 | 54-pin TSOP II (Pb-free) | Industrial |
| | CY7C1069GN30-10ZSXIT | 51-85160 | 54-pin TSOP II (Pb-free), Tape and Reel | |
| | CY7C1069GN30-10BVXI | 51-85150 | 48-ball VFBGA (Pb-free) | |
| | CY7C1069GN30-10BVXIT | 51-85150 | 48-ball VFBGA (Pb-free), Tape and Reel | |

### Ordering Code Definitions



## Package Diagrams

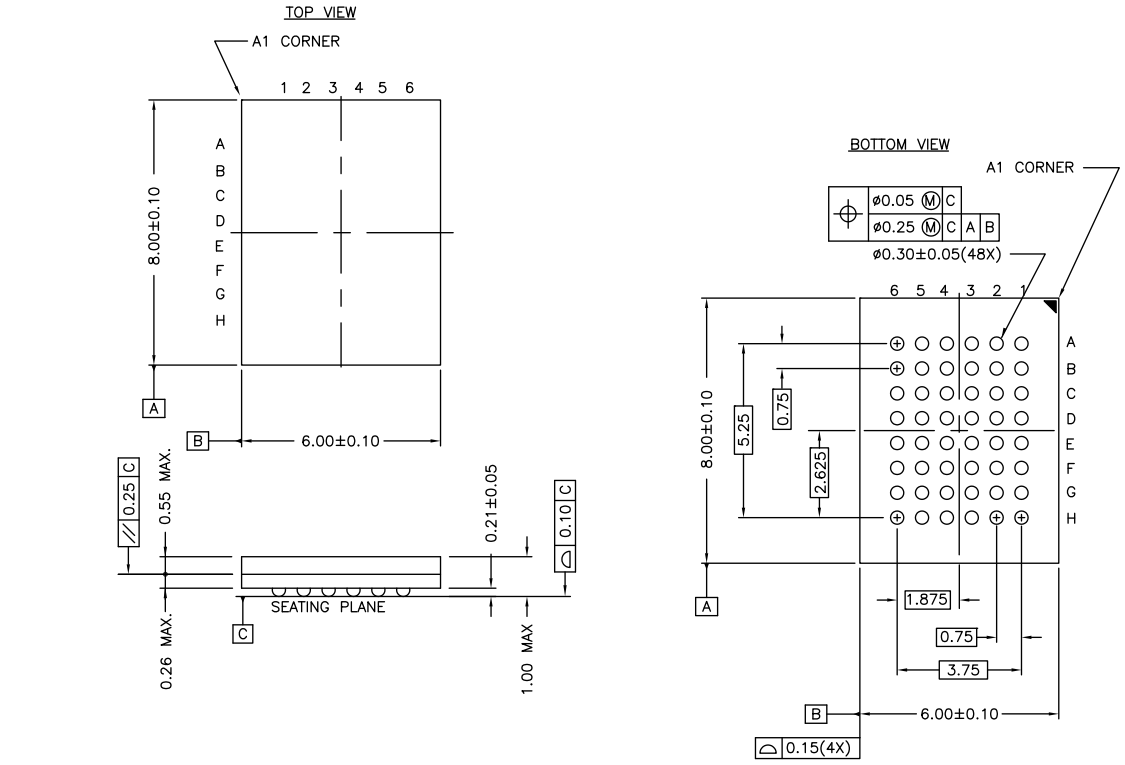
**Figure 9. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Z54-II Package Outline, 51-85160**




51-85160 *E

## Package Diagrams (continued)

**Figure 10. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150**




NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

## Acronyms

| Acronym | Description |
|---|---|
| $\overline{CE}$ | chip enable |
| CMOS | complementary metal oxide semiconductor |
| I/O | input/output |
| $\overline{OE}$ | output enable |
| SRAM | static random access memory |
| VFBGA | very fine-pitch ball grid array |
| TSOP | thin small outline package |
| TTL | transistor-transistor logic |
| $\overline{WE}$ | write enable |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| MHz | megahertz |
| µA | microampere |
| µs | microsecond |
| mA | milliampere |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

## Document History Page

| Document Title: CY7C1069GN, 16-Mbit (2M × 8) Static RAM<br>Document Number: 002-00046 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 4948206 | NILE | 10/13/2015 | New data sheet |
| *A | 5437942 | NILE | 09/15/2016 | Updated DC Electrical Characteristics:<br>Removed Operating Range “2.7 V to 3.6 V” and all values corresponding to $V_{OH}$ parameter.<br>Included Operating Ranges “2.7 V to 3.0 V” and “3.0 V to 3.6 V” and all values corresponding to $V_{OH}$ parameter.<br>Updated Ordering Information:<br>Updated part numbers.<br>Updated Ordering Code Definitions.<br>Updated to new template.<br>Completing Sunset Review. |
| *B | 5999403 | AESATMP8 | 12/19/2017 | Updated logo and Copyright. |

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