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9-Mbit (256K × 36/512K × 18) Flow-Through SRAM

Features

- Supports 100 MHz, 133 MHz bus operations
- Supports 100 MHz bus operations (Automotive)
- 256K × 36/512K × 18 common I/O
- 3.3 V – 5% and +10% core power supply (V_{DD})
- 2.5 V or 3.3 V I/O power supply (V_{DDQ})
- Fast clock-to-output times
  - 6.5 ns (133-MHz version)
- Provide high performance 2-1-1-1 access rate
- User-selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed write
- Asynchronous output enable
- Available in Pb-free 100-pin TQFP package, Pb-free 165-ball FBGA package and non Pb-free 119-ball BGA package
- TQFP available with 3-chip enable and 2-chip enable
- IEEE 1149.1 JTAG-compatible boundary scan
- “ZZ” sleep mode option

Functional Description

The CY7C1361C/CY7C1363C is a 3.3 V, 256K × 36/512K × 18 synchronous flow-through SRAMs, respectively designed to interface with high speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 6.5 ns (133 MHz version). A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access. All synchronous inputs are gated by registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining chip enable (CE_1), depth-expansion chip enables (CE_2 and CE_3[1]), burst control inputs (ADSC, ADSP, and ADV), write enables (BW_x, and BWE), and global write (GW). Asynchronous inputs include the output enable (OE) and the ZZ pin.

The CY7C1361C/CY7C1363C enables either interleaved or linear burst sequences, selected by the MODE input pin. A HIGH selects an interleaved burst sequence, while a LOW selects a linear burst sequence. Burst accesses can be initiated with the processor address strobe (ADSP) or the cache controller address strobe (ADSC) inputs. Address advancement is controlled by the address advancement (ADV) input.

Addresses and chip enables are registered at rising edge of clock when either address strobe processor (ADSP) or address strobe controller (ADSC) are active. Subsequent burst addresses can be internally generated as controlled by the advance pin (ADV).

The CY7C1361C/CY7C1363C operates from a +3.3 V core power supply while all outputs may operate with either a +2.5 or +3.3 V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

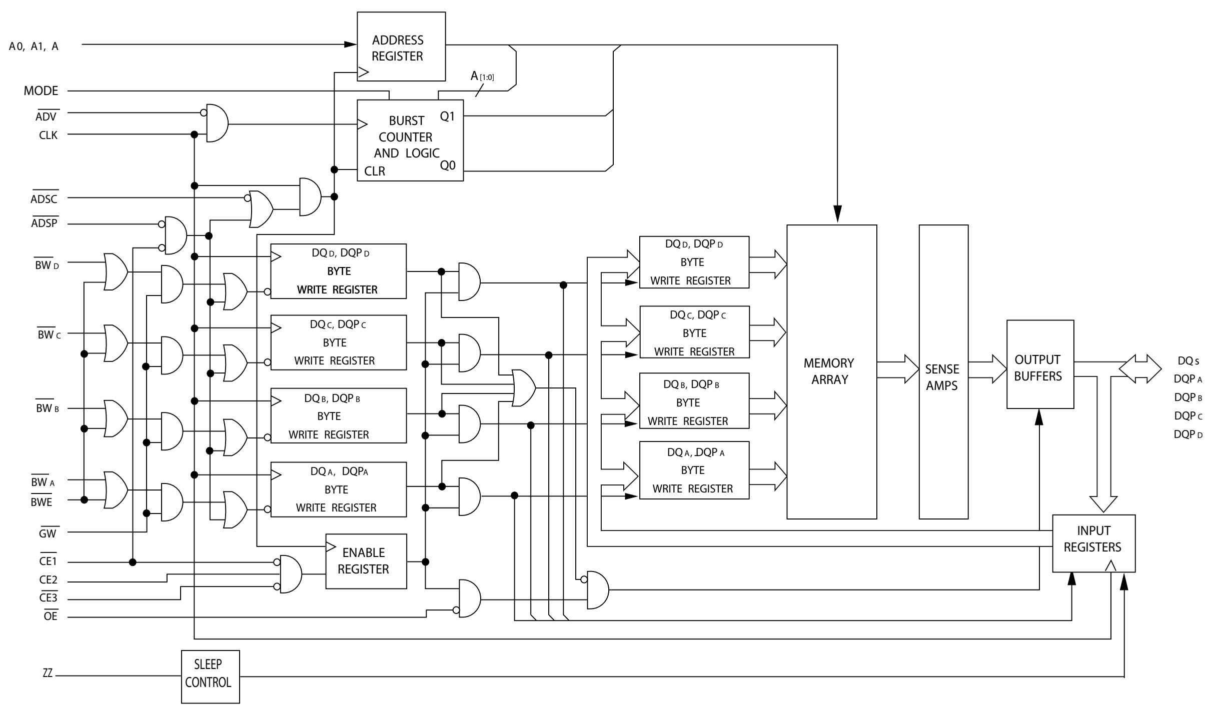
For a complete list of related documentation, click here.

Selection Guide

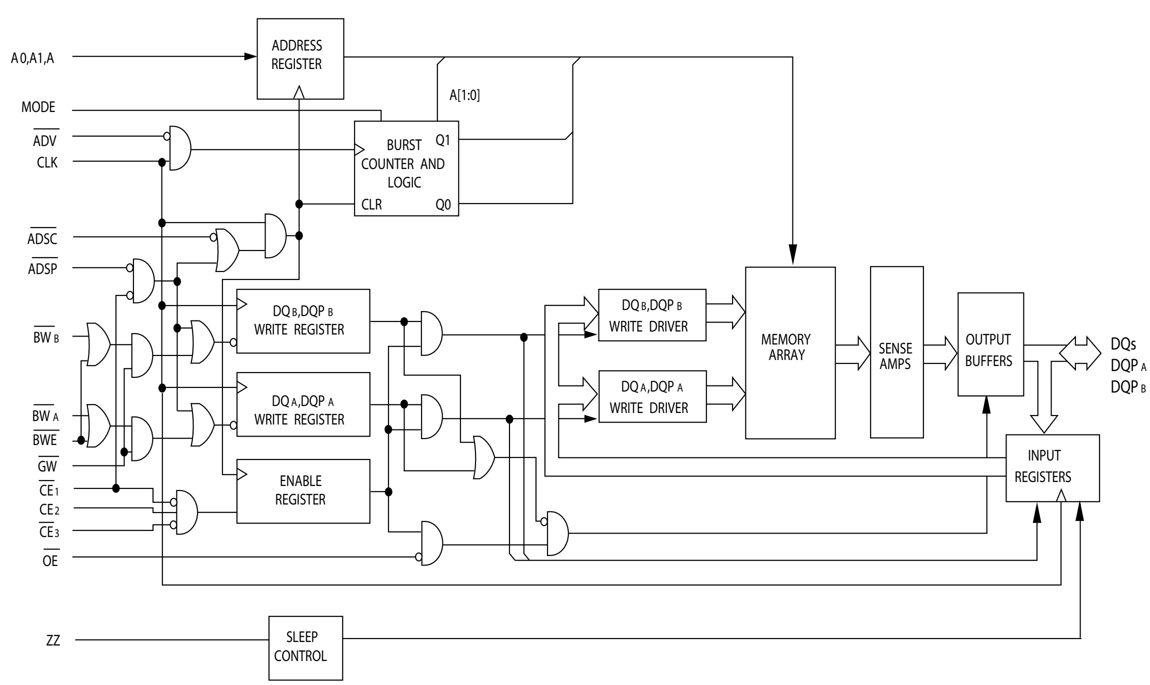
Description		133 MHz	100 MHz	Unit
Maximum access time		6.5	8.5	ns
Maximum operating current		250	180	mA
Maximum CMOS standby current	Commercial/Industrial	40	40	mA
	Automotive	–	60	mA

Note
1. CE_3 is for A version of 100-pin TQFP (3 Chip Enable Option). 119-ball BGA is offered only in 2 Chip Enable.

Logic Block Diagram – CY7C1361C



Logic Block Diagram – CY7C1363C



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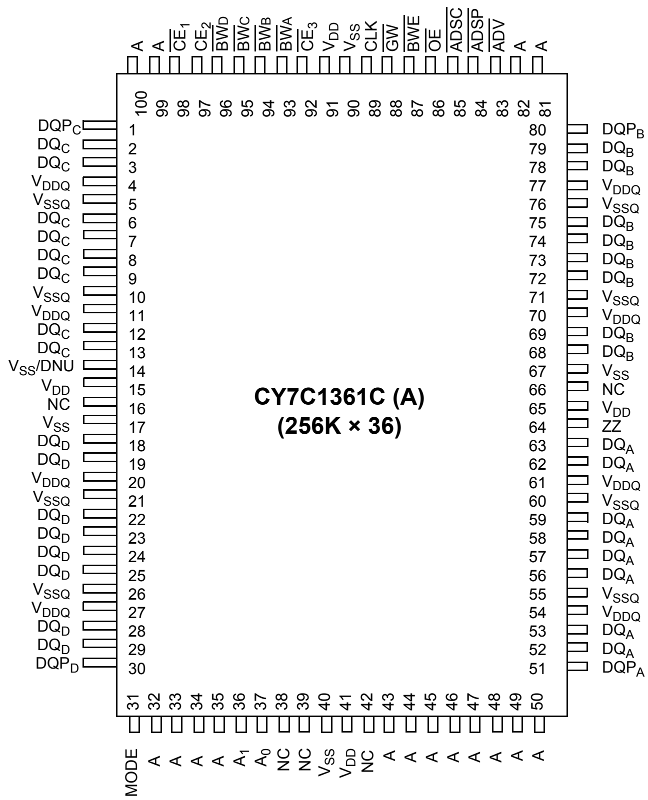
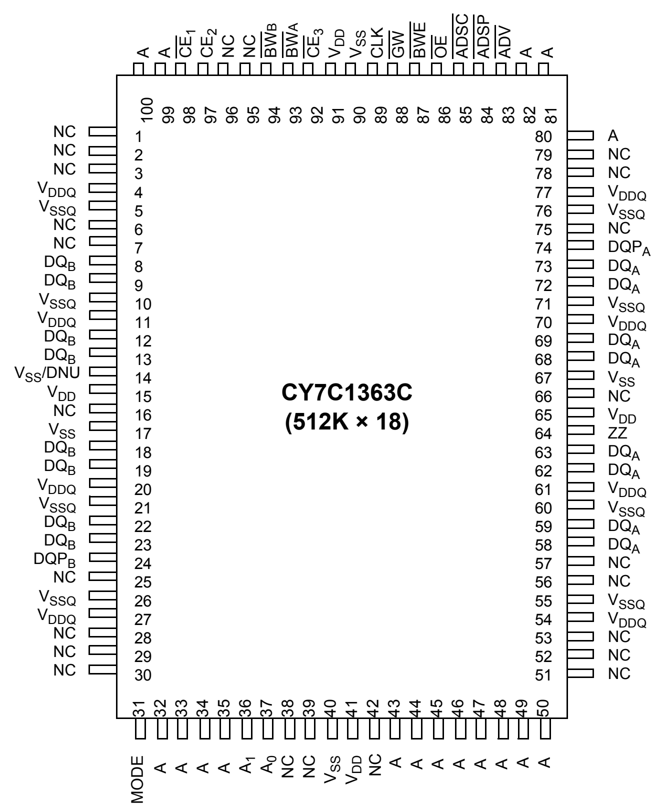
Pin Configurations

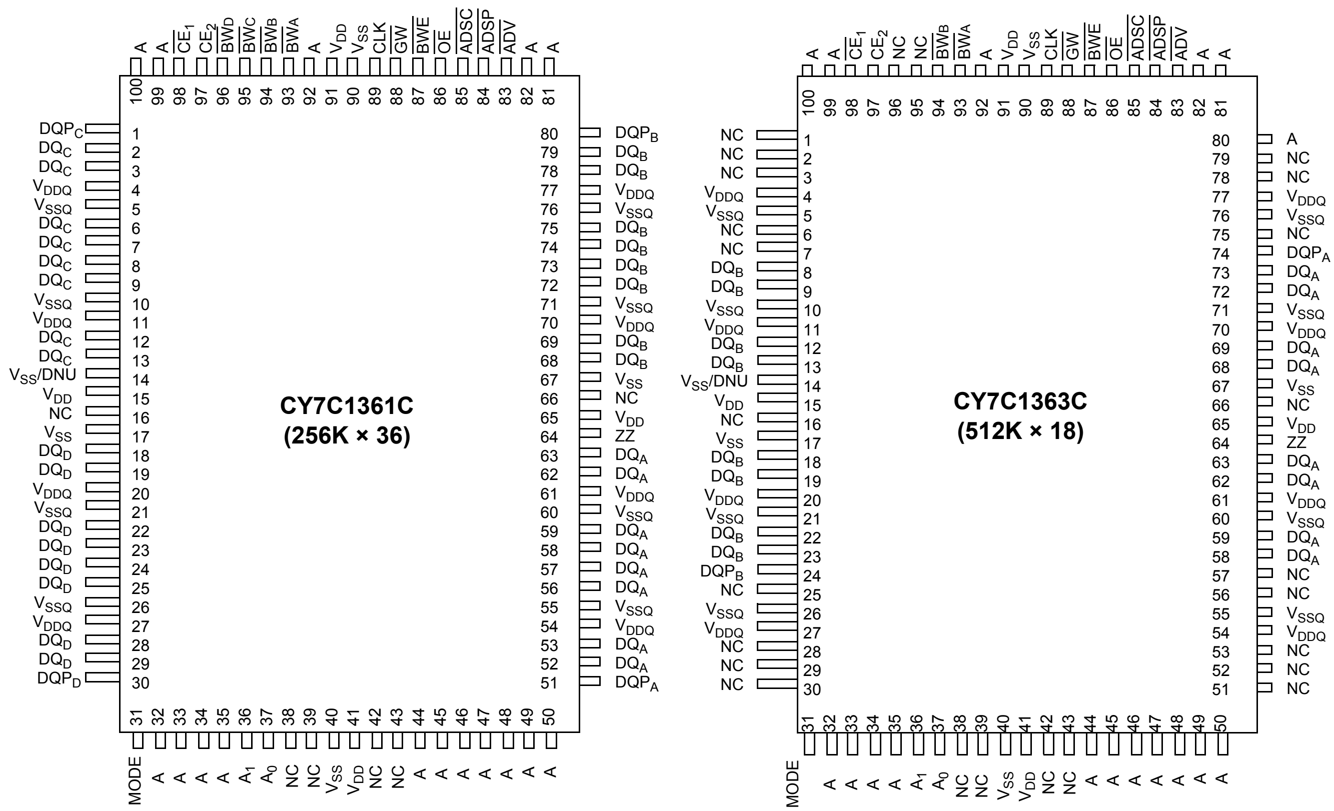
Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout (3 Chip Enables - A version)





Pin Configurations *(continued)*

Figure 2. 100-pin TQFP (14 × 20 × 1.4 mm) pinout (2 Chip Enables - AJ Version)



Pin Configurations *(continued)*

Figure 3. 119-ball BGA (14 × 22 × 2.4 mm) pinout (2 Chip Enables with JTAG)

CY7C1361C (256K × 36)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC/288M	CE_2	A	$\overline{ADSC}$	A	A	NC/512M
C	NC/144M	A	A	V_{DD}	A	A	NC/1G
D	DQ_C	DQP_C	V_{SS}	NC	V_{SS}	DQP_B	DQ_B
E	DQ_C	DQ_C	V_{SS}	$\overline{CE}_1$	V_{SS}	DQ_B	DQ_B
F	V_{DDQ}	DQ_C	V_{SS}	$\overline{OE}$	V_{SS}	DQ_B	V_{DDQ}
G	DQ_C	DQ_C	$\overline{BW}_C$	$\overline{ADV}$	$\overline{BW}_B$	DQ_B	DQ_B
H	DQ_C	DQ_C	V_{SS}	$\overline{GW}$	V_{SS}	DQ_B	DQ_B
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQ_D	DQ_D	V_{SS}	CLK	V_{SS}	DQ_A	DQ_A
L	DQ_D	DQ_D	$\overline{BW}_D$	NC	$\overline{BW}_A$	DQ_A	DQ_A
M	V_{DDQ}	DQ_D	V_{SS}	$\overline{BWE}$	V_{SS}	DQ_A	V_{DDQ}
N	DQ_D	DQ_D	V_{SS}	A1	V_{SS}	DQ_A	DQ_A
P	DQ_D	DQP_D	V_{SS}	A0	V_{SS}	DQP_A	DQ_A
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	NC/72M	A	A	A	NC/36M	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Pin Configurations *(continued)*

Figure 4. 165-ball FBGA pinout (3 Chip Enable)

CY7C1361C (256K × 36)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/288M	A	$\overline{CE}_1$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
B	NC/144M	A	CE_2	$\overline{BW}_D$	$\overline{BW}_A$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC/576M
C	DQP_C	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC/1G	DQP_B
D	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
E	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
F	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
G	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
K	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
L	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
M	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
N	DQP_D	NC	V_{DDQ}	V_{SS}	NC	NC/18M	NC	V_{SS}	V_{DDQ}	NC	DQP_A
P	NC	NC/72M	A	A	TDI	A1	TDO	A	A	A	A
R	MODE	NC/36M	A	A	TMS	A0	TCK	A	A	A	A

Pin Definitions

Name	I/O	Description
A_0, A_1, A	Input-synchronous	**Address inputs used to select one of the address locations**. Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and $\overline{CE}_1$, CE_2, and $\overline{CE}_3$[2] are sampled active. $A_{[1:0]}$ feed the 2-bit counter.
$\overline{BW}_A$,$\overline{BW}_B$, $\overline{BW}_C$,$\overline{BW}_D$	Input-synchronous	**Byte write select inputs, active LOW**. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input-synchronous	**Global write enable input, active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (all bytes are written, regardless of the values on $\overline{BW}_X$ and $\overline{BWE}$).
CLK	Input-clock	**Clock input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW, during a burst operation.
$\overline{CE}_1$	Input-synchronous	**Chip enable 1 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$[2] to select/deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH. $\overline{CE}_1$ is sampled only when a new external address is loaded.
CE_2	Input-synchronous	**Chip enable 2 input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$[2] to select/deselect the device. CE_2 is sampled only when a new external address is loaded.
$\overline{CE}_3$[2]	Input-synchronous	**Chip enable 3 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device. $\overline{CE}_3$ is sampled only when a new external address is loaded.
$\overline{OE}$	Input-asynchronous	**Output enable, asynchronous input, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	Input-synchronous	**Advance input signal, sampled on the rising edge of CLK**. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	Input-synchronous	**Address strobe from processor, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. $\overline{ASDP}$ is ignored when $\overline{CE}_1$ is deasserted HIGH.
$\overline{ADSC}$	Input-synchronous	**Address strobe from controller, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
$\overline{BWE}$	Input-synchronous	**Byte write enable input, active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
ZZ	Input-asynchronous	**ZZ "sleep" input, active HIGH**. When asserted HIGH places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull down.
DQ_s	I/O-synchronous	**Bidirectional data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQ_s and DQP_X are placed in a tristate condition.The outputs are automatically tristated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
DQP_X	I/O-synchronous	**Bidirectional data parity I/O lines**. Functionally, these signals are identical to DQ_s. During write sequences, DQP_X is controlled by $\overline{BW}_X$ correspondingly.
MODE	Input-static	**Selects burst order**. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode Pin has an internal pull-up.
V_{DD}	Power supply	**Power supply inputs to the core of the device**.

Note
2. $\overline{CE}_3$ is for A version of 100-pin TQFP (3 Chip Enable Option). 119-ball BGA is offered only in 2 Chip Enable.

Pin Definitions *(continued)*

Name	I/O	Description
V_{DDQ}	I/O power supply	**Power supply for the I/O circuitry**.
V_{SS}	Ground	**Ground for the core of the device**.
V_{SSQ}	I/O ground	**Ground for the I/O circuitry**.
TDO	JTAG serial output synchronous	**Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK. If the JTAG feature is not being used, this pin should be left unconnected. This pin is not available on TQFP packages.
TDI	JTAG serial input synchronous	**Serial data-in to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not being used, this pin can be left floating or connected to V_{DD} through a pull up resistor. This pin is not available on TQFP packages.
TMS	JTAG serial input synchronous	**Serial data-in to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not being used, this pin can be disconnected or connected to V_{DD}. This pin is not available on TQFP packages.
TCK	JTAG-clock	**Clock input to the JTAG circuitry**. If the JTAG feature is not being used, this pin must be connected to V_{SS}. This pin is not available on TQFP packages.
NC	–	**No connects**. Not internally connected to the die. 18M, 36M, 72M, 144M, 288M, 576M, and 1G are address expansion pins and are not internally connected to the die.
V_{SS}/DNU	Ground/DNU	This pin can be connected to ground or should be left floating.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CDV}) is 6.5 ns (133 MHz device).

The CY7C1361C/CY7C1363C supports secondary cache in systems using either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that use a linear burst sequence. The burst order is user-selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the processor address strobe (ADSP) or the controller address strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the byte write enable (BWE) and byte write select (BW_X) inputs. A global write enable (GW) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous chip selects ($\overline{CE}_1$, CE_2, $\overline{CE}_3$[3]) and an asynchronous output enable (OE) provide for easy bank selection and output tristate control. ADSP is ignored if $\overline{CE}_1$ is HIGH.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE}_1$, CE_2, and $\overline{CE}_3$[3] are all asserted active and (2) ADSP or ADSC is asserted LOW (if the access is initiated by ADSC, the write inputs must be deasserted during this first cycle). The address presented to the address inputs is latched into the address register and the burst counter/control logic and presented to the memory core. If the OE input is asserted LOW, the requested data will be available at the data outputs a maximum to t_{CDV} after clock rise. ADSP is ignored if $\overline{CE}_1$ is HIGH.

Single Write Accesses Initiated by ADSP

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE}_1$, CE_2, $\overline{CE}_3$[3] are all asserted active and (2) ADSP is asserted LOW. The addresses presented are loaded into the address register and the burst inputs (GW, BWE, and BW_X) are ignored during this first clock cycle. If the write inputs are asserted active (see Partial Truth Table for Read/Write on page 12 for appropriate states that indicate a write) on the next clock rise, the appropriate data will be latched and written into the device.Byte writes are allowed. All I/Os are tristated during a byte write. Since this is a common I/O device, the asynchronous OE input signal must be deasserted and the I/Os must be tristated prior to the presentation of data to DQs. As a safety precaution, the data lines are tristated once a write cycle is detected, regardless of the state of OE.

Note
3. $\overline{CE}_3$ is for A version of 100-pin TQFP (3 Chip Enable Option). 119-ball BGA is offered only in 2 Chip Enable.

Single Write Accesses Initiated by ADSC

This write access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$[4] are all asserted active, (2) $\overline{ADSC}$ is asserted LOW, (3) $\overline{ADSP}$ is deasserted HIGH, and (4) the write input signals ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW_X}$) indicate a write access. $\overline{ADSC}$ is ignored if $\overline{ADSP}$ is active LOW.

The addresses presented are loaded into the address register and the burst counter/control logic and delivered to the memory core. The information presented to $DQ_{[A:D]}$ is written into the specified address location. Byte writes are allowed. All I/Os are tristated when a write is detected, even a byte write. Since this is a common I/O device, the asynchronous $\overline{OE}$ input signal must be deasserted and the I/Os must be tristated prior to the presentation of data to DQ_s. As a safety precaution, the data lines are tristated once a write cycle is detected, regardless of the state of $\overline{OE}$.

Burst Sequences

The CY7C1361C/CY7C1363C provides an on-chip two-bit wraparound burst counter inside the SRAM. The burst counter is fed by $A_{[1:0]}$, and can follow either a linear or interleaved burst order. The burst order is determined by the state of the MODE input. A LOW on MODE will select a linear burst sequence. A HIGH on MODE selects an interleaved burst order. Leaving MODE unconnected causes the device to default to a interleaved burst sequence.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation 'sleep' mode. Two clock cycles are required to enter into or exit from this 'sleep' mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the 'sleep' mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the 'sleep' mode. $\overline{CE_1}$, CE_2, $\overline{CE_3}$[4], $\overline{ADSP}$, and $\overline{ADSC}$ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions		Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2$ V	Commercial/Industrial	–	50	mA
			Automotive	–	60	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2$ V		–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2$ V		$2t_{CYC}$	–	ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled		–	$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled		0	–	ns

Note
4. $\overline{CE_3}$ is for A version of 100-pin TQFP (3 Chip Enable Option). 119-ball BGA is offered only in 2 Chip Enable.

Truth Table

The Truth Table for CY7C1361C and CY7C1363C follows. [5, 6, 7, 8, 9]

Cycle Description	Address Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected cycle, power-down	None	H	X	X	L	X	L	X	X	X	L–H	Tri-state
Deselected cycle, power-down	None	L	L	X	L	L	X	X	X	X	L–H	Tri-state
Deselected cycle, power-down	None	L	X	H	L	L	X	X	X	X	L–H	Tri-state
Deselected cycle, power-down	None	L	L	X	L	H	L	X	X	X	L–H	Tri-state
Deselected cycle, power-down	None	X	X	H	L	H	L	X	X	X	L–H	Tri-state
Sleep mode, power-down	None	X	X	X	H	X	X	X	X	X	X	Tri-state
Read cycle, begin burst	External	L	H	L	L	L	X	X	X	L	L–H	Q
Read cycle, begin burst	External	L	H	L	L	L	X	X	X	H	L–H	Tri-state
Write cycle, begin burst	External	L	H	L	L	H	L	X	L	X	L–H	D
Read cycle, begin burst	External	L	H	L	L	H	L	X	H	L	L–H	Q
Read cycle, begin burst	External	L	H	L	L	H	L	X	H	H	L–H	Tri-state
Read cycle, continue burst	Next	X	X	X	L	H	H	L	H	L	L–H	Q
Read cycle, continue burst	Next	X	X	X	L	H	H	L	H	H	L–H	Tri-state
Read cycle, continue burst	Next	H	X	X	L	X	H	L	H	L	L–H	Q
Read cycle, continue burst	Next	H	X	X	L	X	H	L	H	H	L–H	Tri-state
Write cycle, continue burst	Next	X	X	X	L	H	H	L	L	X	L–H	D
Write cycle, continue burst	Next	H	X	X	L	X	H	L	L	X	L–H	D
Read cycle, suspend burst	Current	X	X	X	L	H	H	H	H	L	L–H	Q
Read cycle, suspend burst	Current	X	X	X	L	H	H	H	H	H	L–H	Tri-state
Read cycle, suspend burst	Current	H	X	X	L	X	H	H	H	L	L–H	Q
Read cycle, suspend burst	Current	H	X	X	L	X	H	H	H	H	L–H	Tri-state
Write cycle, suspend burst	Current	X	X	X	L	H	H	H	L	X	L–H	D
Write cycle, suspend burst	Current	H	X	X	L	X	H	H	L	X	L–H	D

Notes
5. X = "Don't Care." H = Logic HIGH, L = Logic LOW.
6. $\overline{WRITE}$ = L when any one or more byte write enable signals and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all byte write enable signals, $\overline{BWE}$, $\overline{GW}$ = H.
7. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
8. The SRAM always initiates a read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW_X}$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to tri-state. $\overline{OE}$ is a don't care for the remainder of the write cycle.
9. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tri-state when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

Partial Truth Table for Read/Write

The Partial Truth Table for Read/Write for CY7C1361C follows. [10, 11]

Function (CY7C1361C)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_D}$	$\overline{BW_C}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write byte (A, DQP_A)	H	L	H	H	H	L
Write byte (B, DQP_B)	H	L	H	H	L	H
Write bytes (B, A, DQP_A, DQP_B)	H	L	H	H	L	L
Write byte (C, DQP_C)	H	L	H	L	H	H
Write bytes (C, A, DQP_C, DQP_A)	H	L	H	L	H	L
Write bytes (C, B, DQP_C, DQP_B)	H	L	H	L	L	H
Write bytes (C, B, A, DQP_C, DQP_B, DQP_A)	H	L	H	L	L	L
Write byte (D, DQP_D)	H	L	L	H	H	H
Write bytes (D, A, DQP_D, DQP_A)	H	L	L	H	H	L
Write bytes (D, B, DQP_D, DQP_A)	H	L	L	H	L	H
Write bytes (D, B, A, DQP_D, DQP_B, DQP_A)	H	L	L	H	L	L
Write bytes (D, B, DQP_D, DQP_B)	H	L	L	L	H	H
Write bytes (D, B, A, DQP_D, DQP_C, DQP_A)	H	L	L	L	H	L
Write bytes (D, C, A, DQP_D, DQP_B, DQP_A)	H	L	L	L	L	H
Write all bytes	H	L	L	L	L	L
Write all bytes	L	X	X	X	X	X

Partial Truth Table for Read/Write

The Partial Truth Table for Read/Write for CY7C1363C follows. [10, 11]

Function (CY7C1363C)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X
Read	H	L	H	H
Write byte A – (DQ_A and DQP_A)	H	L	H	L
Write byte B – (DQ_B and DQP_B)	H	L	L	H
Write all bytes	H	L	L	L
Write all bytes	L	X	X	X

Notes
10. X = “Don't Care.” H = Logic HIGH, L = Logic LOW.
11. Table only lists a partial listing of the byte write combinations. Any Combination of $\overline{BW_X}$ is valid Appropriate write will be done based on which byte write is active.

IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1361C incorporates a serial boundary scan test access port (TAP) in the BGA package only. The TQFP package does not offer this functionality. This part operates in accordance with IEEE Standard 1149.1-1900, but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 3.3 V or 2.5 V I/O logic levels.

The CY7C1361C contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. Upon power up, the device comes up in a reset state which does not interfere with the operation of the device.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information about loading the instruction register, see the TAP Controller State Diagram on page 15. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register.

Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see Instruction Codes on page 19). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A RESET is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power up, the TAP is reset internally to ensure that TDO comes up in a high Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the TAP Controller Block Diagram on page 16. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary ‘01’ pattern to enable fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This enables data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order on page 20 show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in Identification Register Definitions on page 19.

TAP Instruction Set

Overview

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Codes on page 19. Three of these instructions are listed as

RESERVED and should not be used. The other five instructions are described in detail in this section.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented.

The TAP controller cannot be used to load address data or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this SRAM TAP controller, and therefore this device is not compliant to 1149.1. The TAP controller does recognize an all-0 instruction.

When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a high Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and enables the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a high Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1-mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergoes a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD enables an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required - that is, while data captured is shifted out, the preloaded data can be shifted in.

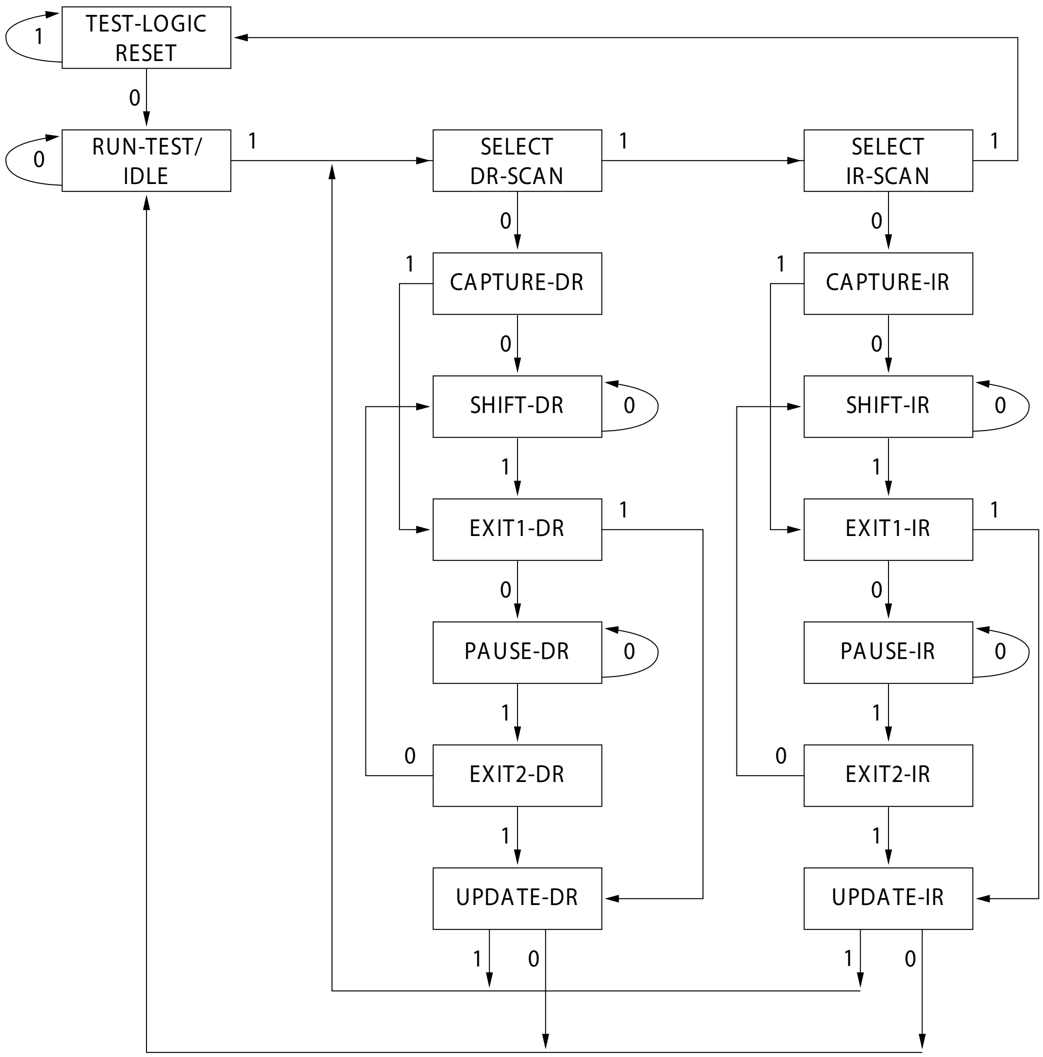
BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

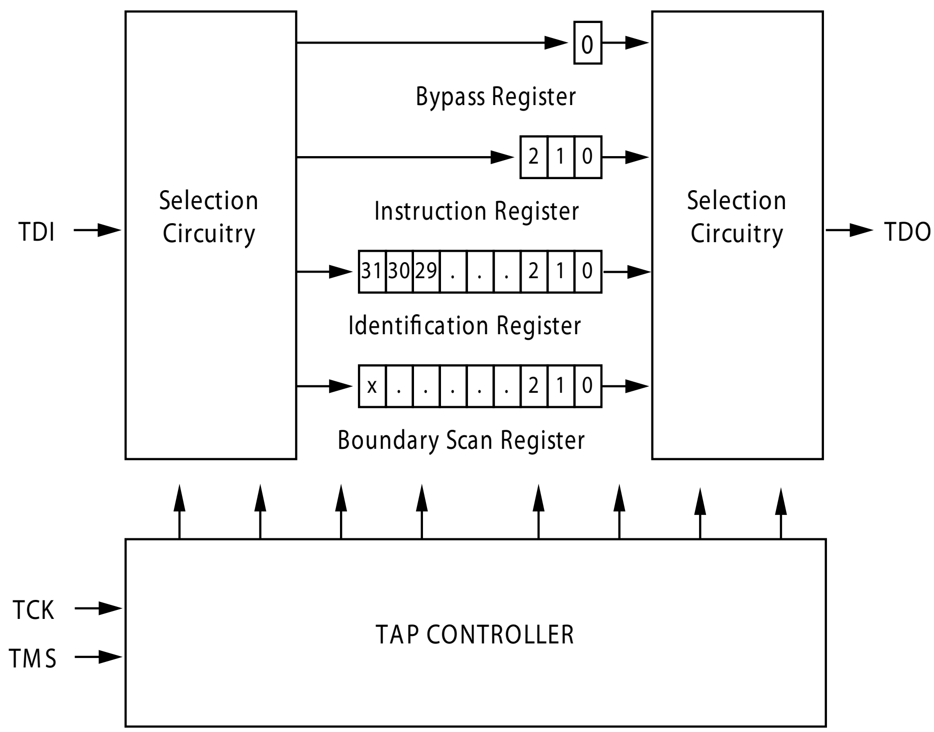
These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram

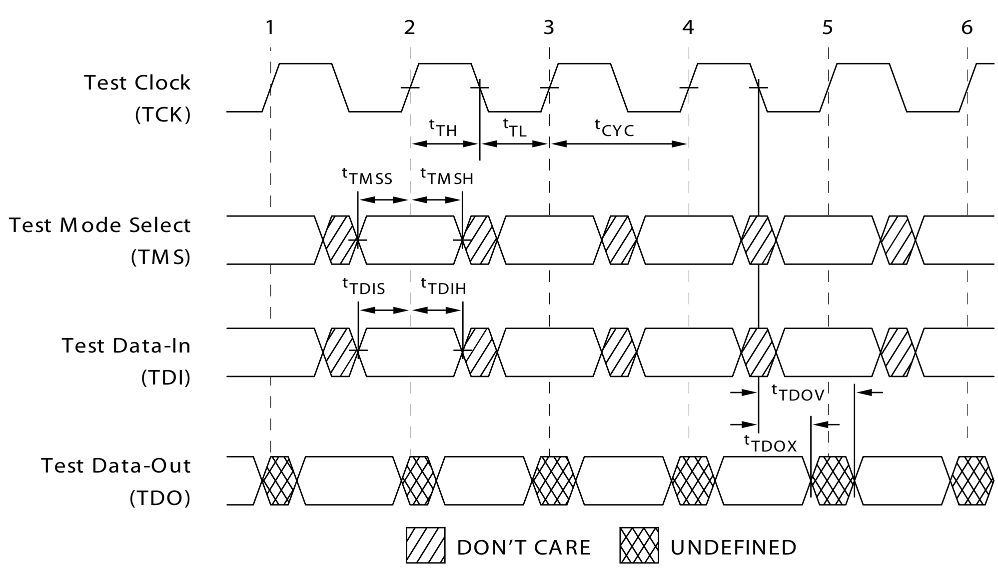


The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Timing



TAP AC Switching Characteristics

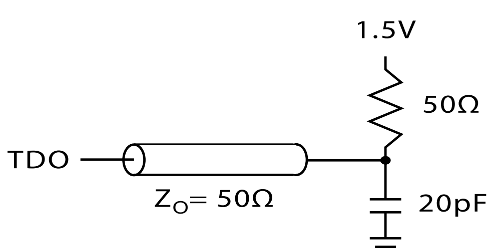
Over the Operating Range

Parameter [12, 13]	Parameter	Min	Max	Unit
Clock				
t_{TCYC}	TCK clock cycle time	50	–	ns
t_{TF}	TCK clock frequency	–	20	MHz
t_{TH}	TCK clock HIGH time	20	–	ns
t_{TL}	TCK clock LOW time	20	–	ns
Output Times				
t_{TDOV}	TCK clock LOW to TDO valid	–	10	ns
t_{TDOX}	TCK clock LOW to TDO invalid	0	–	ns
Set-up Times				
t_{TMSS}	TMS setup to TCK clock rise	5	–	ns
t_{TDIS}	TDI setup to TCK clock rise	5	–	ns
t_{CS}	Capture setup to TCK rise	5	–	ns
Hold Times				
t_{TMSH}	TMS hold after TCK clock rise	5	–	ns
t_{TDIH}	TDI hold after clock rise	5	–	ns
t_{CH}	Capture hold after clock rise	5	–	ns

3.3 V TAP AC Test Conditions

Input pulse levels .... V_{SS} to 3.3 V
Input rise and fall times ....1 ns
Input timing reference levels .... 1.5 V
Output reference levels .... 1.5 V
Test load termination supply voltage .... 1.5 V

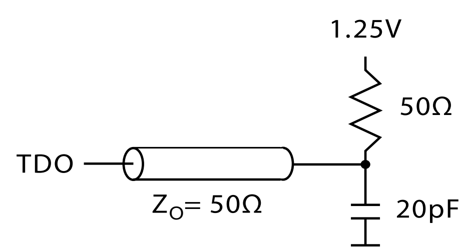
3.3 V TAP AC Output Load Equivalent



2.5 V TAP AC Test Conditions

Input pulse levels .... V_{SS} to 2.5 V
Input rise and fall time ....1 ns
Input timing reference levels .... 1.25 V
Output reference levels .... 1.25 V
Test load termination supply voltage .... 1.25 V

2.5 V TAP AC Output Load Equivalent



Notes
12. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
13. Test conditions are specified using the load in TAP AC test conditions. t_R/t_F = 1 ns.

TAP DC Electrical Characteristics and Operating Conditions

(0 °C < T_A < +70 °C; V_{DD} = 3.3 V ± 0.165 V unless otherwise noted)

Parameter [14]	Description	Test Conditions		Min	Max	Unit
V_{OH1}	Output HIGH voltage	I_{OH} = –4.0 mA	V_{DDQ} = 3.3 V	2.4	–	V
		I_{OH} = –1.0 mA	V_{DDQ} = 2.5 V	2.0	–	V
V_{OH2}	Output HIGH voltage	I_{OH} = –100 µA	V_{DDQ} = 3.3 V	2.9	–	V
			V_{DDQ} = 2.5 V	2.1	–	V
V_{OL1}	Output LOW voltage	I_{OL} = 8.0 mA	V_{DDQ} = 3.3 V	–	0.4	V
		I_{OL} = 8.0 mA	V_{DDQ} = 2.5 V	–	0.4	V
V_{OL2}	Output LOW voltage	I_{OL} = 100 µA	V_{DDQ} = 3.3 V	–	0.2	V
			V_{DDQ} = 2.5 V	–	0.2	V
V_{IH}	Input HIGH voltage		V_{DDQ} = 3.3 V	2.0	V_{DD} + 0.3	V
			V_{DDQ} = 2.5 V	1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW voltage		V_{DDQ} = 3.3 V	–0.5	0.7	V
			V_{DDQ} = 2.5 V	–0.3	0.7	V
I_X	Input load current	GND ≤ V_{IN} ≤ V_{DDQ}		–5	5	µA

Note
14. All voltages referenced to V_{SS} (GND).

Identification Register Definitions

Instruction Field	CY7C1361C (256K × 36)	Description
Revision number (31:29)	000	Describes the version number.
Device depth (28:24) [15]	01011	Reserved for Internal Use
Device width (23:18) 119-ball BGA	101001	Defines memory type and architecture
Cypress device ID (17:12)	100110	Defines width and density
Cypress JEDEC ID Code (11:1)	00000110100	Allows unique identification of SRAM vendor.
ID register presence indicator (0)	1	Indicates the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size (× 36)
Instruction	3
Bypass	1
ID	32
Boundary scan order (119-ball BGA package)	71

Instruction Codes

Instruction	Code	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to high Z state.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a high Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

Note
15. Bit #24 is “1” in the Register Definitions for both 2.5 V and 3.3 V versions of this device.

Boundary Scan Order

119-ball BGA

CY7C1361C (256 K × 36)

Bit #	Ball ID	Signal Name	Bit #	Ball ID	Signal Name
1	K4	CLK	37	P4	A0
2	H4	$\overline{GW}$	38	N4	A1
3	M4	$\overline{BWE}$	39	R6	A
4	F4	$\overline{OE}$	40	T5	A
5	B4	$\overline{ADSC}$	41	T3	A
6	A4	$\overline{ADSP}$	42	R2	A
7	G4	ADV	43	R3	MODE
8	C3	A	44	P2	DQP_D
9	B3	A	45	P1	DQ_D
10	D6	DQP_B	46	L2	DQ_D
11	H7	DQ_B	47	K1	DQ_D
12	G6	DQ_B	48	N2	DQ_D
13	E6	DQ_B	49	N1	DQ_D
14	D7	DQ_B	50	M2	DQ_D
15	E7	DQ_B	51	L1	DQ_D
16	F6	DQ_B	52	K2	DQ_D
17	G7	DQ_B	53	Internal	Internal
18	H6	DQ_B	54	H1	DQ_C
19	T7	ZZ	55	G2	DQ_C
20	K7	DQ_A	56	E2	DQ_C
21	L6	DQ_A	57	D1	DQ_C
22	N6	DQ_A	58	H2	DQ_C
23	P7	DQ_A	59	G1	DQ_C
24	N7	DQ_A	60	F2	DQ_C
25	M6	DQ_A	61	E1	DQ_C
26	L7	DQ_A	62	D2	DQP_C
27	K6	DQ_A	63	C2	A
28	P6	DQP_A	64	A2	A
29	T4	A	65	E4	$\overline{CE_1}$
30	A3	A	66	B2	CE_2
31	C5	A	67	L3	$\overline{BW_D}$
32	B5	A	68	G3	$\overline{BW_C}$
33	A5	A	69	G5	$\overline{BW_B}$
34	C6	A	70	L5	$\overline{BW_A}$
35	A6	A	71	Internal	Internal
36	B6	A			

Boundary Scan Order

165-ball FBGA

CY7C1361C (256 K × 36)

Bit #	ball ID	Signal Name
1	B6	CLK
2	B7	$\overline{GW}$
3	A7	$\overline{BWE}$
4	B8	$\overline{OE}$
5	A8	$\overline{ADSC}$
6	B9	$\overline{ADSP}$
7	A9	$\overline{ADV}$
8	B10	A
9	A10	A
10	C11	DQP_B
11	E10	DQ_B
12	F10	DQ_B
13	G10	DQ_B
14	D10	DQ_B
15	D11	DQ_B
16	E11	DQ_B
17	F11	DQ_B
18	G11	DQ_B
19	H11	ZZ
20	J10	DQ_A
21	K10	DQ_A
22	L10	DQ_A
23	M10	DQ_A
24	J11	DQ_A
25	K11	DQ_A
26	L11	DQ_A
27	M11	DQ_A
28	N11	DQP_A
29	R11	A
30	R10	A
31	P10	A
32	R9	A
33	P9	A
34	R8	A
35	P8	A
36	P11	A

Bit #	ball ID	Signal Name
37	R6	A0
38	P6	A1
39	R4	A
40	P4	A
41	R3	A
42	P3	A
43	R1	MODE
44	N1	DQP_D
45	L2	DQ_D
46	K2	DQ_D
47	J2	DQ_D
48	M2	DQ_D
49	M1	DQ_D
50	L1	DQ_D
51	K1	DQ_D
52	J1	DQ_D
53	Internal	Internal
54	G2	DQ_C
55	F2	DQ_C
56	E2	DQ_C
57	D2	DQ_C
58	G1	DQ_C
59	F1	DQ_C
60	E1	DQ_C
61	D1	DQ_C
62	C1	DQP_C
63	B2	A
64	A2	A
65	A3	CE_1
66	B3	CE_2
67	B4	$\overline{BW}_D$
68	A4	$\overline{BW}_C$
69	A5	$\overline{BW}_B$
70	B5	$\overline{BW}_A$
71	A6	$\overline{CE}_3$

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature .... –65 °C to + 150 °C

Ambient temperature with power applied .... –55 °C to + 125 °C

Supply voltage on V_{DD} relative to GND ......–0.5 V to + 4.6 V

Supply voltage on V_{DDQ} relative to GND ..... –0.5 V to + V_{DD}

DC voltage applied to outputs in tri-state ....–0.5 V to V_{DDQ} + 0.5 V

DC input voltage ....–0.5 V to V_{DD} + 0.5 V

Current into outputs (LOW) .... 20 mA

Static discharge voltage (per MIL-STD-883, method 3015) .... > 2001 V

Latch-up current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V_{DD}
Industrial	–40 °C to +85 °C		
Automotive	–40 °C to +125 °C		

Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU	Logical single-bit upsets	25 °C	361	394	FIT/ Mb
LMBU	Logical multi-bit upsets	25 °C	0	0.01	FIT/ Mb
SEL	Single event latch up	85 °C	0	0.1	FIT/ Dev

* *No LMBU or SEL events occurred during testing*; this column represents a statistical χ^2, 95% confidence limit calculation. For more details refer to Application Note AN54908 “Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates”

Electrical Characteristics

Over the Operating Range

Parameter [16, 17]	Description	Test Conditions	Min	Max	Unit
V_{DD}	Power supply voltage		3.135	3.6	V
V_{DDQ}	I/O supply voltage	for 3.3 V I/O	3.135	V_{DD}	V
		for 2.5 V I/O	2.375	2.625	V
V_{OH}	Output HIGH voltage	for 3.3 V I/O, I_{OH} = –4.0 mA	2.4	–	V
		for 2.5 V I/O, I_{OH} = –1.0 mA	2.0	–	V
V_{OL}	Output LOW voltage	for 3.3 V I/O, I_{OL} = 8.0 mA	–	0.4	V
		for 2.5 V I/O, I_{OL} = 1.0 mA	–	0.4	V
V_{IH}	Input HIGH voltage[16]	for 3.3 V I/O	2.0	V_{DD} + 0.3 V	V
		for 2.5 V I/O	1.7	V_{DD} + 0.3 V	V
V_{IL}	Input LOW voltage[16]	for 3.3 V I/O	–0.3	0.8	V
		for 2.5 V I/O	–0.3	0.7	V
I_X	Input leakage current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}	–5	5	µA
	Input current of MODE	Input = V_{SS}	–30	–	µA
		Input = V_{DD}	–	5	µA
	Input current of ZZ	Input = V_{SS}	–5	–	µA
		Input = V_{DD}	–	30	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ $V_{DDQ,}$ output disabled	–5	5	µA

Notes

16. Overshoot: $V_{IH(AC)} < V_{DD}$ + 1.5 V (Pulse width less than t_{CYC}/2), undershoot: $V_{IL(AC)}$ > –2 V (Pulse width less than t_{CYC}/2).
17. $T_{Power-up}$: Assumes a linear ramp from 0 V to $V_{DD(min)}$ within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \leq V_{DD}$.

Electrical Characteristics *(continued)*

Over the Operating Range

Parameter [16, 17]	Description	Test Conditions		Min	Max	Unit
I_{DD}	V_{DD} operating supply current	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	7.5 ns cycle, 133 MHz	–	250	mA
			10 ns cycle, 100 MHz	–	180	
I_{SB1}	Automatic CE power-down current – TTL inputs	Max V_{DD}, device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}, inputs switching	All speeds (Commercial /Industrial)	–	110	mA
			10 ns cycle, 100 MHz (Automotive)	–	150	mA
I_{SB2}	Automatic CE power-down current – CMOS inputs	Max V_{DD}, device deselected, $V_{IN} \geq V_{DD}$ – 0.3 V or $V_{IN} \leq$ 0.3 V, f = 0, inputs static	All speeds	–	40	mA
I_{SB3}	Automatic CE power-down current – CMOS inputs	Max V_{DD}, device deselected, $V_{IN} \geq V_{DDQ}$ – 0.3 V or $V_{IN} \leq$ 0.3 V, f = f_{MAX}, inputs switching	All speeds (Commercial /Industrial)	–	100	mA
			10 ns cycle, 100 MHz (Automotive)	–	120	mA
I_{SB4}	Automatic CE power-down current – TTL inputs	Max V_{DD}, device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = 0, inputs static	All speeds (Commercial /Industrial)	–	40	mA
			10 ns cycle, 100 MHz (Automotive)	–	60	mA

Capacitance

Parameter [18]	Description	Test Conditions	100-pin TQFP Max	119-ball BGA Max	165-ball FBGA Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V, V_{DDQ} = 2.5 V	5	5	5	pF
C_{CLK}	Clock input capacitance		5	5	5	pF
$C_{I/O}$	Input/output capacitance		5	7	7	pF

Thermal Resistance

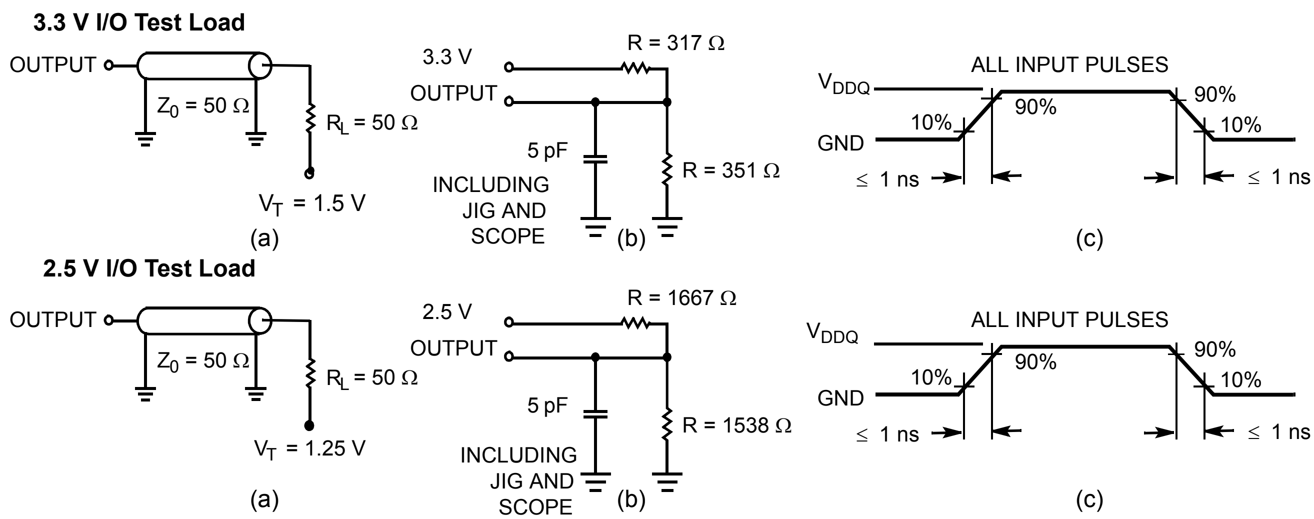
Parameter [18]	Description	Test Conditions	100-pin TQFP Package	119-ball BGA Package	165-ball FBGA Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, according to EIA/JESD51	29.41	34.1	16.8	°C/W
Θ_{JC}	Thermal resistance (junction to case)		6.31	14.0	3.0	°C/W

Note

18. Tested initially and after any design or process change that may affect these parameters.

AC Test Loads and Waveforms

Figure 5. AC Test Loads and Waveforms



Switching Characteristics

Over the Operating Range

Parameter [19, 20]	Description	-133		-100		Unit
		Min	Max	Min	Max	
t_{POWER}	V_{DD}(typical) to the first access [21]	1	–	1	–	ms
Clock						
t_{CYC}	Clock cycle time	7.5	–	10	–	ns
t_{CH}	Clock HIGH	3.0	–	4.0	–	ns
t_{CL}	Clock LOW	3.0	–	4.0	–	ns
Output Times						
t_{CDV}	Data output valid after CLK rise	–	6.5	–	8.5	ns
t_{DOH}	Data output hold after CLK rise	2.0	–	2.0	–	ns
t_{CLZ}	Clock to low Z [22, 23, 24]	0	–	0	–	ns
t_{CHZ}	Clock to high Z [22, 23, 24]	–	3.5	–	3.5	ns
t_{OEV}	$\overline{OE}$ LOW to output valid	–	3.5	–	3.5	ns
t_{OELZ}	$\overline{OE}$ LOW to output low Z [22, 23, 24]	0	–	0	–	ns
t_{OEHZ}	$\overline{OE}$ HIGH to output high Z [22, 23, 24]	–	3.5	–	3.5	ns
Set-up Times						
t_{AS}	Address setup before CLK rise	1.5	–	1.5	–	ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ setup before CLK rise	1.5	–	1.5	–	ns
t_{ADVS}	$\overline{ADV}$ setup before CLK rise	1.5	–	1.5	–	ns
t_{WES}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW}_{[A:D]}$ setup before CLK rise	1.5	–	1.5	–	ns
t_{DS}	Data input setup before CLK rise	1.5	–	1.5	–	ns
t_{CES}	Chip enable setup	1.5	–	1.5	–	ns
Hold Times						
t_{AH}	Address hold after CLK rise	0.5	–	0.5	–	ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ hold after CLK rise	0.5	–	0.5	–	ns
t_{WEH}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW}_{[A:D]}$ hold after CLK rise	0.5	–	0.5	–	ns
t_{ADVH}	$\overline{ADV}$ hold after CLK rise	0.5	–	0.5	–	ns
t_{DH}	Data input hold after CLK rise	0.5	–	0.5	–	ns
t_{CEH}	Chip enable hold after CLK rise	0.5	–	0.5	–	ns

Notes

19. Timing reference level is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.
20. Test conditions shown in (a) of Figure 5 on page 24 unless otherwise noted.
21. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above $V_{DD(minimum)}$ initially, before a read or write operation can be initiated.
22. t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of Figure 5 on page 24. Transition is measured ± 200 mV from steady-state voltage.
23. At any given voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve high Z prior to low Z under the same system conditions.
24. This parameter is sampled and not 100% tested.