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**256K (32K x 8) Static RAM**

**Features**

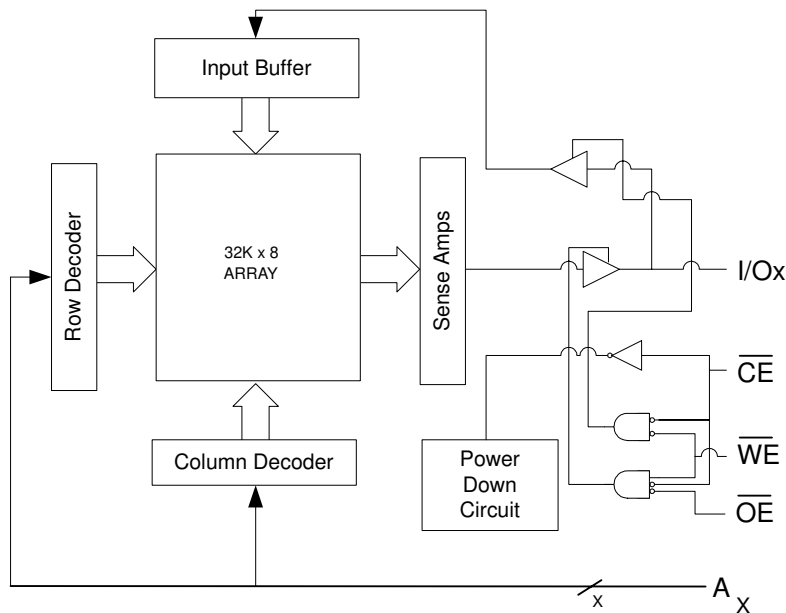
- **Fast access time: 12 ns**
- **Wide voltage range: 5.0V ± 10% (4.5V to 5.5V)**
- **CMOS for optimum speed/power**
- **TTL-compatible Inputs and Outputs**
- **2.0V Data Retention**
- **Low CMOS standby power**
- **Automated Power-down when deselected**
- **Available in Pb-free and non Pb-free 28-pin (300-Mil) Molded SOJ, 28-pin (300-Mil) DIP and 28-pin TSOP I packages**

**General Description**

The CY7C199C is a high-performance CMOS Asynchronous SRAM organized as 32K by 8 bits that supports an asynchronous memory interface. The device features an automatic power-down feature that significantly reduces power consumption when deselected.

See the Truth Table in this data sheet for a complete description of read and write modes

**Logic Block Diagram**



**Product Portfolio**

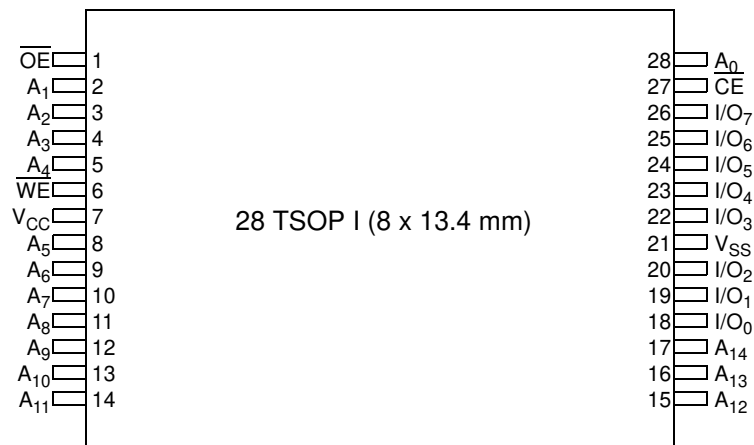
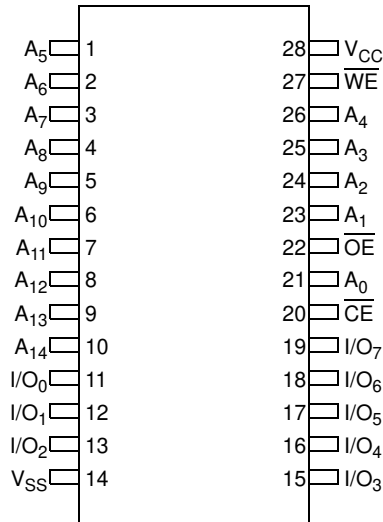
|                                  | <b>12 ns</b> | <b>15 ns</b> | <b>20 ns</b> | <b>Unit</b> |
|----------------------------------|--------------|--------------|--------------|-------------|
| Maximum Access Time              | 12           | 15           | 20           | ns          |
| Maximum Operating Current        | 85           | 80           | 75           | mA          |
| Maximum CMOS Standby Current (L) |              | 500          |              | μA          |

**Note:**

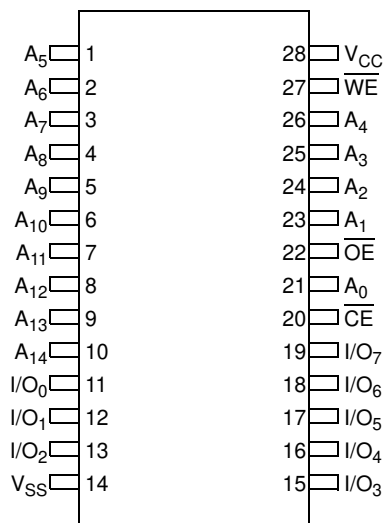
1. For best-practices recommendations, please refer to the Cypress application note *System Design Guidelines* on [www.cypress.com](http://www.cypress.com).

Pin Layout and Specifications

28 DIP (6.9 x 35.6 x 3.5 mm)



28 SOJ



**Pin Description**

| Pin              | Type            | Description        | DIP   | SOJ   | TSOP I   |
|------------------|-----------------|--------------------|---|---|--|
| A <sub>X</sub>   | Input           | Address Inputs     | 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 21, 23, 24, 25, 26 | 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 21, 23, 24, 25, 26 | 2, 3, 4, 5, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 28 |
| $\overline{CE}$  | Control         | Chip Enable        | 20  | 20  | 27   |
| I/O <sub>X</sub> | Input or Output | Data Input/Outputs | 11, 12, 13, 15, 16, 17, 18, 19                    | 11, 12, 13, 15, 16, 17, 18, 19                    | 18, 19, 20, 22, 23, 24, 25, 26                       |
| $\overline{OE}$  | Control         | Output Enable      | 22  | 22  | 1  |
| V <sub>CC</sub>  | Supply          | Power (5.0V)       | 28  | 28  | 7  |
| V <sub>SS</sub>  | Supply          | Ground             | 14  | 14  | 21   |
| $\overline{WE}$  | Control         | Write Enable       | 27  | 27  | 6  |

**Maximum Ratings** (Above which the useful life may be impaired. For user guidelines, not tested.)

| Parameter                          | Description   | Value                         | Unit |
|------------------------------------|---|-------------------------------|------|
| T <sub>STG</sub>                   | Storage Temperature   | -65 to +150                   | °C   |
| T <sub>AMB</sub>                   | Ambient Temperature with Power Applied (i.e., case temperature) | -55 to +125                   | °C   |
| V <sub>CC</sub>                    | Core Supply Voltage Relative to V <sub>SS</sub>                 | -0.5 to +7.0                  | V    |
| V <sub>IN</sub> , V <sub>OUT</sub> | DC Voltage Applied to any Pin Relative to V <sub>SS</sub>       | -0.5 to V <sub>CC</sub> + 0.5 | V    |
| I <sub>OUT</sub>                   | Output Short-Circuit Current                                    | 20                            | mA   |
| V <sub>ESD</sub>                   | Static Discharge Voltage (per MIL-STD-883, Method 3015)         | > 2001                        | V    |
| I <sub>LU</sub>                    | Latch-up Current  | > 200                         | mA   |

**Operating Range**

| Range      | Ambient Temperature (T <sub>A</sub> ) | Voltage Range (V <sub>CC</sub> ) |
|------------|---------------------------------------|----------------------------------|
| Commercial | 0°C to 70°C                           | 5.0V ± 10%                       |
| Industrial | -40°C to 85°C                         | 5.0V ± 10%                       |

**DC Electrical Characteristics** Over the Operating Range [2]

| Parameter        | Description  | Condition  | 12 ns |                       | 15 ns |                       | 20 ns |                       | Unit |
|------------------|--|--|-------|-----------------------|-------|-----------------------|-------|-----------------------|------|
|                  |  |  | Min.  | Max.                  | Min.  | Max.                  | Min.  | Max.                  |      |
| V <sub>IH</sub>  | Input HIGH Voltage                                       |  | 2.2   | V <sub>CC</sub> + 0.3 | 2.2   | V <sub>CC</sub> + 0.3 | 2.2   | V <sub>CC</sub> + 0.3 | V    |
| V <sub>IL</sub>  | Input LOW Voltage  |  | -0.5  | 0.8                   | -0.5  | 0.8                   | -0.5  | 0.8                   | V    |
| V <sub>OH</sub>  | Output HIGH Voltage                                      | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA  | 2.4   |                       | 2.4   |                       | 2.4   |                       | V    |
| V <sub>OL</sub>  | Output LOW Voltage                                       | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA   |       | 0.4                   |       | 0.4                   |       | 0.4                   | V    |
| I <sub>IX</sub>  | Input Leakage Current                                    | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -5    | +5                    | -5    | +5                    | -5    | +5                    | μA   |
| I <sub>OZ</sub>  | Output Leakage Current                                   | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled   | -5    | +5                    | -5    | +5                    | -5    | +5                    | μA   |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current                 | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = F <sub>MAX</sub> = 1/t <sub>RC</sub>  |       | 85                    |       | 80                    |       | 75                    | mA   |
| I <sub>SB1</sub> | Automatic $\overline{CE}$ Power-down Current TTL Inputs  | Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = F <sub>MAX</sub> |       | 30                    |       | 30                    |       | 30                    | mA   |
|                  |  |  | L     |                       |       | 10                    |       |                       | mA   |
| I <sub>SB2</sub> | Automatic $\overline{CE}$ Power-down Current CMOS Inputs | Max. V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0             |       | 10                    |       | 10                    |       | 10                    | mA   |
|                  |  |  | L     |                       |       | 500                   |       |                       | μA   |

**Note:**

 2. V<sub>IL</sub> (min) = -2.0V for pulse durations of less than 20 ns.

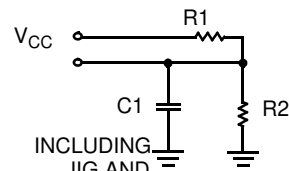
**Capacitance<sup>[3]</sup>**

| Parameter        | Description        | Conditions  | Max.           | Unit |
|------------------|--------------------|---|----------------|------|
|                  |                    |   | ALL – PACKAGES |      |
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz,<br>V <sub>CC</sub> = 5.0V | 8              | pF   |
| C <sub>OUT</sub> | Output Capacitance |   | 8              |      |

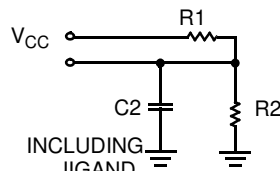
**Thermal Resistance<sup>[4]</sup>**

| Parameter       | Description                              | Conditions  | TSOP I | SOJ   | DIP   | Unit |
|-----------------|--|---|--------|-------|-------|------|
| Θ <sub>JA</sub> | Thermal Resistance (Junction to Ambient) | Still Air, soldered on a 3 × 4.5 square inch, two-layer printed circuit board | 88.6   | 79    | 69.33 | °C/W |
| Θ <sub>JC</sub> | Thermal Resistance (Junction to Case)    |   | 21.94  | 41.42 | 31.62 |      |

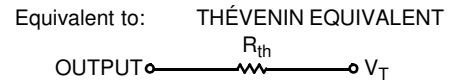
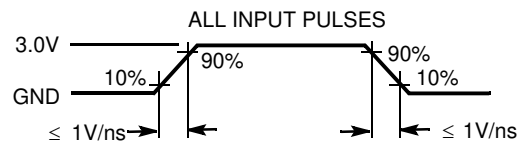
**AC Test Loads and Waveforms**



INCLUDING JIG AND SCOPE  
**(a)**  
output load



INCLUDING JIG AND SCOPE  
**(b)**  
output load for t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZWE</sub>



**Notes:**

3. Tested initially and after any design or process change that may affect these parameters.
4. Test Conditions assume a transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.

**AC Test Conditions**

| Parameter       | Description       | Nom. | Unit |
|-----------------|-------------------|------|------|
| C1              | Capacitor 1       | 30   | pF   |
| C2              | Capacitor 2       | 5    |      |
| R1              | Resistor 1        | 480  | Ω    |
| R2              | Resistor 2        | 255  |      |
| R <sub>TH</sub> | Resistor Thevenin | 167  |      |
| V <sub>TH</sub> | Voltage Thevenin  | 1.73 | V    |

**AC Electrical Characteristics**<sup>[5, 6, 7]</sup>

| Parameter         | Description                   | 12 ns |     | 15 ns |     | 20 ns |     | Unit |
|-------------------|-------------------------------|-------|-----|-------|-----|-------|-----|------|
|                   |                               | Min   | Max | Min   | Max | Min   | Max |      |
| t <sub>RC</sub>   | Read Cycle Time               | 12    |     | 15    |     | 20    |     | ns   |
| t <sub>AA</sub>   | Address to Data Valid         |       | 12  |       | 15  |       | 20  | ns   |
| t <sub>OHA</sub>  | Data Hold from Address Change | 3     |     | 3     |     | 3     |     | ns   |
| t <sub>ACE</sub>  | $\overline{CE}$ to Data Valid |       | 12  |       | 15  |       | 20  | ns   |
| t <sub>DOE</sub>  | $\overline{OE}$ to Data Valid |       | 5   |       | 7   |       | 9   | ns   |
| t <sub>LZOE</sub> | $\overline{OE}$ to Low Z      | 0     |     | 0     |     | 0     |     | ns   |
| t <sub>HZOE</sub> | $\overline{OE}$ to High Z     |       | 5   |       | 7   |       | 9   | ns   |
| t <sub>LZCE</sub> | $\overline{CE}$ to Low Z      | 3     |     | 3     |     | 3     |     | ns   |
| t <sub>HZCE</sub> | $\overline{CE}$ to High Z     |       | 5   |       | 7   |       | 9   | ns   |
| t <sub>PU</sub>   | $\overline{CE}$ to Power-up   | 0     |     | 0     |     | 0     |     | ns   |
| t <sub>PD</sub>   | $\overline{CE}$ to Power-down |       | 12  |       | 15  |       | 20  | ns   |
| t <sub>WC</sub>   | Write Cycle Time              | 12    |     | 15    |     | 20    |     | ns   |
| t <sub>SCE</sub>  | $\overline{CE}$ to Write End  | 9     |     | 10    |     | 15    |     | ns   |
| t <sub>AW</sub>   | Address Set-up to Write End   | 9     |     | 10    |     | 15    |     | ns   |
| t <sub>HA</sub>   | Address Hold from Write End   | 0     |     | 0     |     | 0     |     | ns   |
| t <sub>SA</sub>   | Address Set-up to Write Start | 0     |     | 0     |     | 0     |     | ns   |
| t <sub>PWE</sub>  | $\overline{WE}$ Pulse Width   | 8     |     | 9     |     | 15    |     | ns   |
| t <sub>SD</sub>   | Data Set-up to Write End      | 8     |     | 9     |     | 10    |     | ns   |
| t <sub>HD</sub>   | Data Hold from Write End      | 0     |     | 0     |     | 0     |     | ns   |
| t <sub>HZWE</sub> | $\overline{WE}$ LOW to High Z |       | 7   |       | 7   |       | 10  | ns   |
| t <sub>LZWE</sub> | $\overline{WE}$ HIGH to Low Z | 3     |     | 3     |     | 3     |     | ns   |

**Notes:**

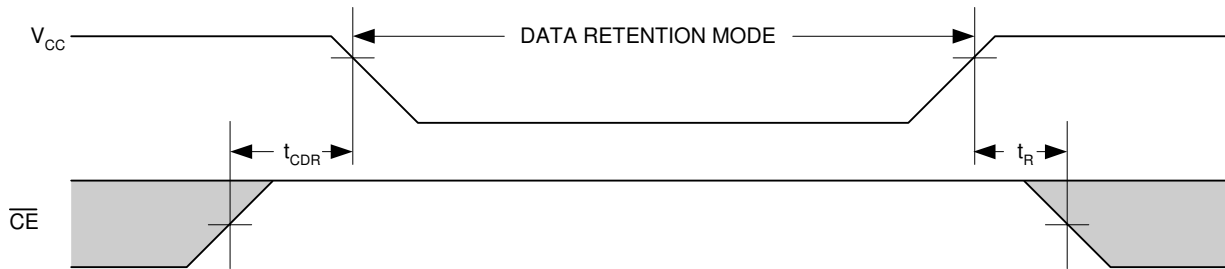
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZWE</sub> are specified as in part (b) of the A/C Test Loads. Transitions are measured ± 200 mV from steady state voltage.

**Data Retention Characteristics<sup>[8]</sup>**

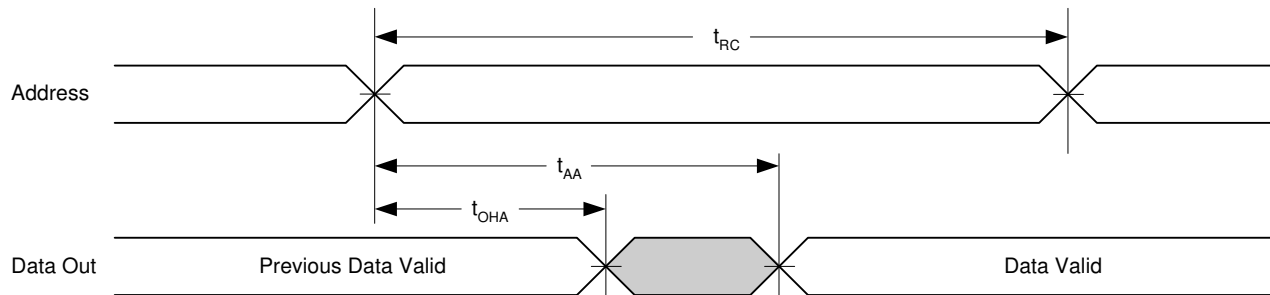
| Parameter         | Description                          | Condition  | ALL  |      | Unit |
|-------------------|--------------------------------------|--|------|------|------|
|                   |                                      |  | Min. | Max. |      |
| V <sub>DR</sub>   | V <sub>CC</sub> for Data Retention   |  | 2.0  | –    | V    |
| I <sub>CCDR</sub> | Data Retention Current               | V <sub>CC</sub> = V <sub>DR</sub> = 2.0V, CE ≥ V <sub>CC</sub> – 0.3V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.3V or V <sub>IN</sub> ≤ 0.3V | –    | 150  | μA   |
| t <sub>CDR</sub>  | Chip Deselect to Data Retention Time |  | 0    | –    | ns   |
| t <sub>R</sub>    | Operation Recovery Time              |  | 200  | –    | μs   |

**Timing Waveforms**

**Data Retention Waveform**

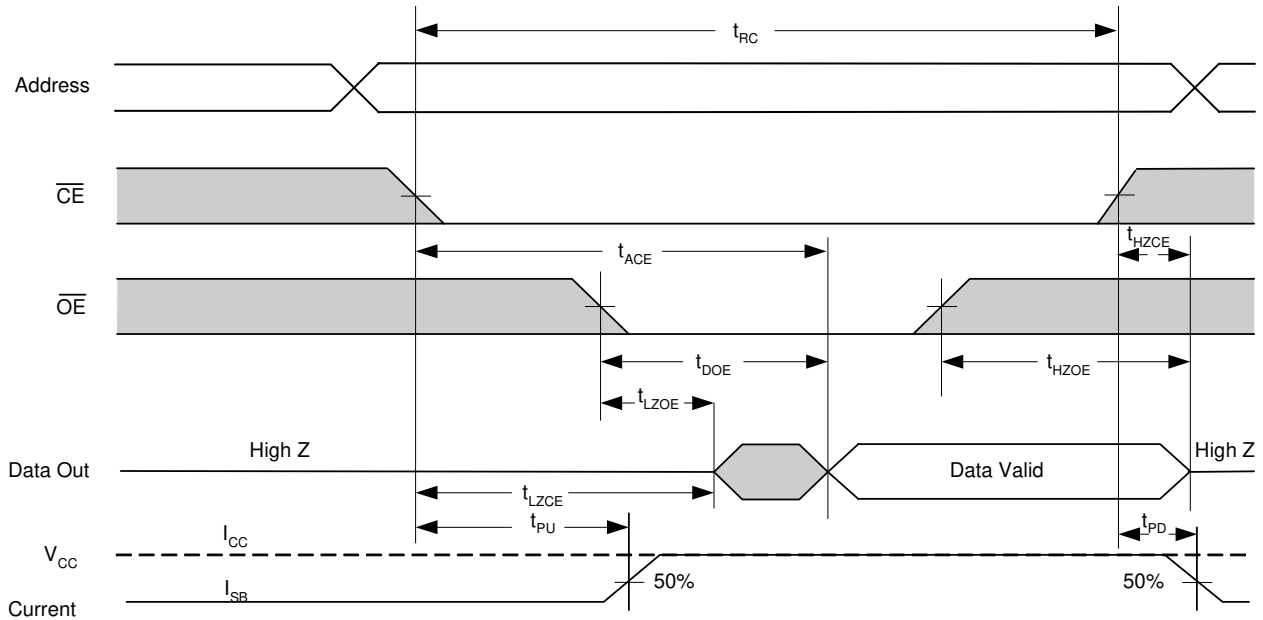
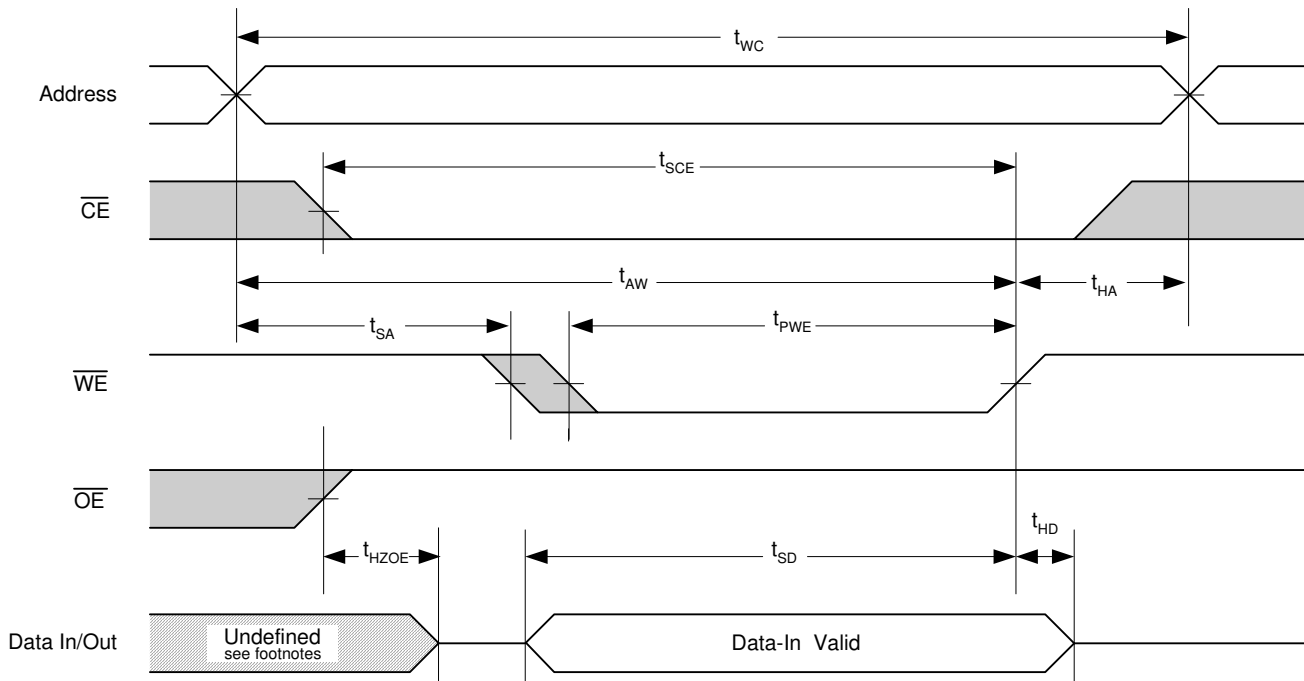


**Read Cycle No. 1<sup>[11, 10]</sup>**



**Notes:**

- 8. L-version only.
- 9. Device is continuously selected.  $\overline{OE} = V_{IL} = \overline{CE}$ .
- 10.  $\overline{WE}$  is HIGH for Read Cycle.

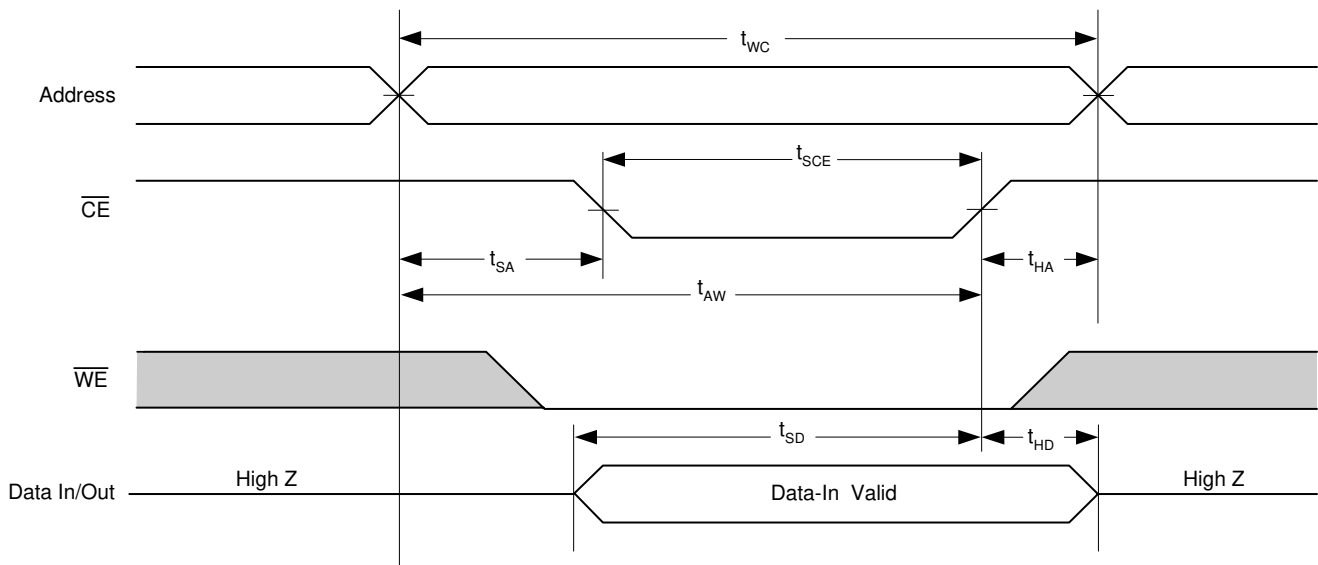
**Timing Waveforms (continued)**
**Read Cycle No. 2<sup>[11, 12]</sup>**

**Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[13, 14, 15]</sup>**

**Notes:**

11. This cycle is  $\overline{OE}$  Controlled and  $\overline{WE}$  is HIGH read cycle.
12. Address valid prior to or coincident with CE transition LOW.
13. This cycle is  $\overline{WE}$  controlled,  $\overline{OE}$  is HIGH during write.
14. Data In/Out is high impedance if  $\overline{OE} = V_{IH}$ .
15. During this period the I/Os are in output state and input signals should not be applied.

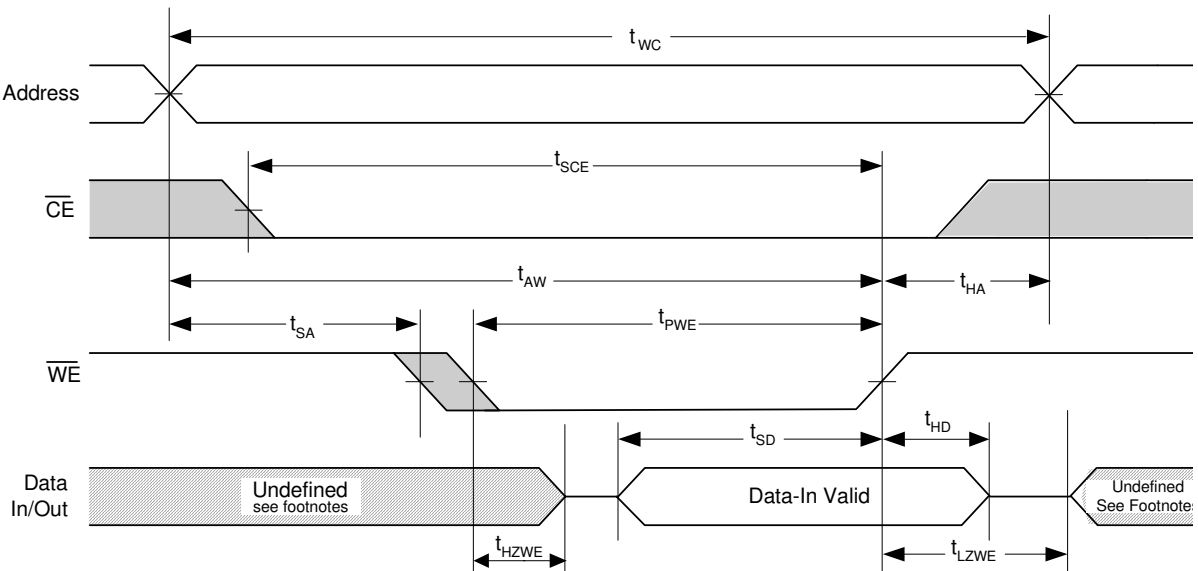


**Timing Waveforms** (continued)

**Write Cycle No. 2** ( $\overline{CE}$  Controlled)<sup>[14, 16, 17]</sup>



**Write Cycle No. 3** ( $\overline{WE}$  Controlled,  $\overline{OE}$  Low)<sup>[18]</sup>



**Notes:**

- 16. This cycle is  $\overline{CE}$  controlled.
- 17. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
- 18. The cycle is  $\overline{WE}$  controlled,  $\overline{OE}$  LOW. The minimum write cycle time is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Truth Table**

| CE | WE | OE | Input/Output | Mode                | Power                |
|----|----|----|--------------|---------------------|----------------------|
| H  | X  | X  | High Z       | Deselect/Power-Down | Standby ( $I_{SB}$ ) |
| L  | H  | L  | Data Out     | Read                | Active ( $I_{CC}$ )  |
| L  | L  | X  | Data In      | Write               | Active ( $I_{CC}$ )  |
| L  | H  | H  | High Z       | Deselect            | Active ( $I_{CC}$ )  |

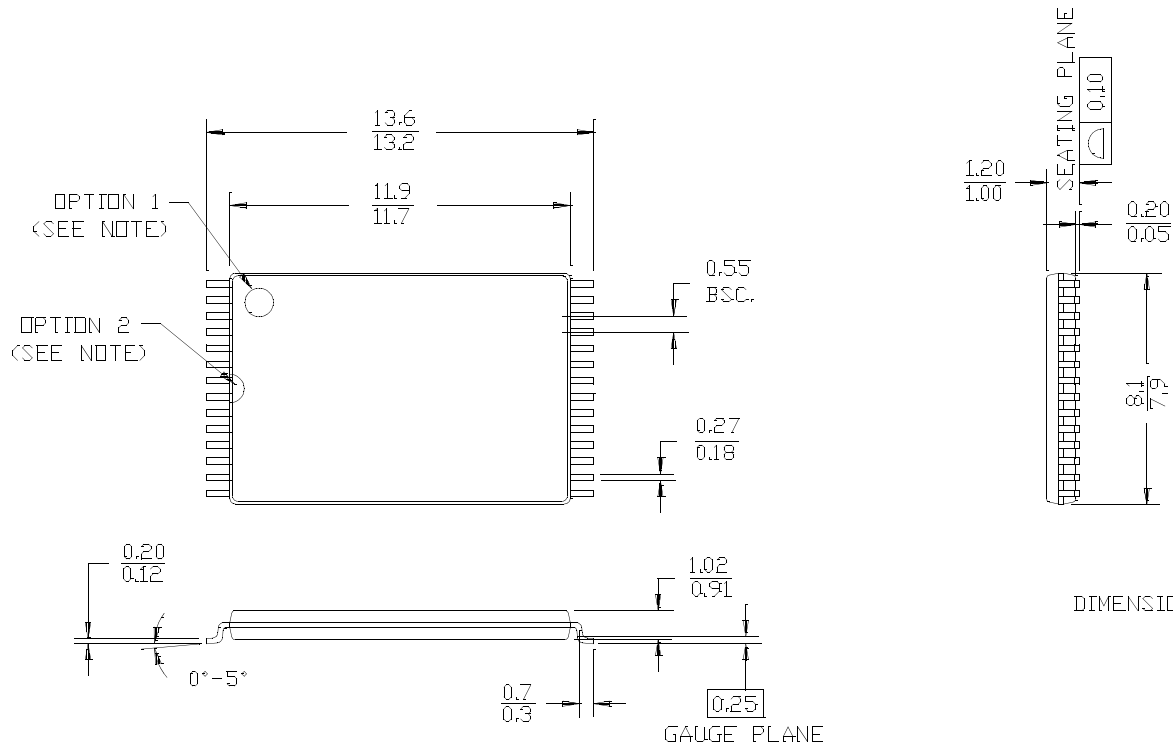
**Ordering Information**

| Speed         | Ordering Code   | Package Name                | Package Type                          | Operating Range |
|---------------|-----------------|-----------------------------|---------------------------------------|-----------------|
| 12            | CY7C199C-12VC   | 51-85031                    | 28-pin (300-Mil) Molded SOJ           | Commercial      |
|               | CY7C199C-12VXC  |                             | 28-pin (300-Mil) Molded SOJ (Pb-Free) |                 |
|               | CY7C199C-12ZXI  | 51-85071                    | 28-pin TSOP I (Pb-Free)               | Industrial      |
|               | CY7C199C-12VI   | 51-85031                    | 28-pin (300-Mil) Molded SOJ           |                 |
| 15            | CY7C199C-15PC   | 51-85014                    | 28-pin (300-Mil) DIP                  | Commercial      |
|               | CY7C199C-15PXC  |                             | 28-pin (300-Mil) DIP (Pb-Free)        |                 |
|               | CY7C199C-15ZC   | 51-85071                    | 28-pin TSOP I                         |                 |
|               | CY7C199C-15ZXI  |                             | 28-pin TSOP I (Pb-Free)               |                 |
|               | CY7C199C-15VC   | 51-85031                    | 28-pin (300-Mil) Molded SOJ           |                 |
|               | CY7C199C-15VXC  |                             | 28-pin (300-Mil) Molded SOJ (Pb-Free) |                 |
|               | CY7C199CL-15VC  |                             | 28-pin (300-Mil) Molded SOJ           |                 |
|               | CY7C199CL-15VXC |                             | 28-pin (300-Mil) Molded SOJ (Pb-Free) |                 |
| CY7C199C-15VI | 51-85031        | 28-pin (300-Mil) Molded SOJ | Industrial                            |                 |
| 20            | CY7C199C-20ZXI  | 51-85071                    | 28-pin TSOP I (Pb-Free)               | Industrial      |

**Package Diagrams**

**28-pin TSOP 1 (8 x 13.4 mm) (51-85071)**

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2



DIMENSION IN MM  
MAX.  
MIN.

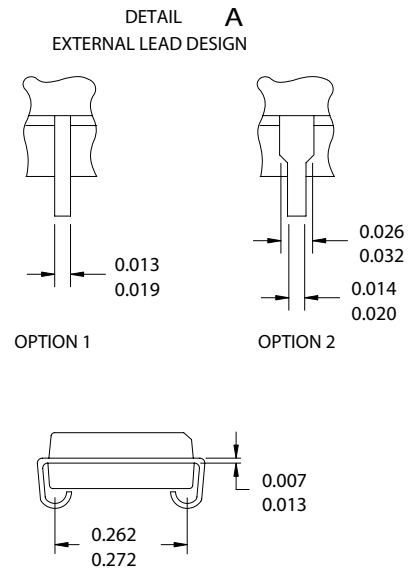
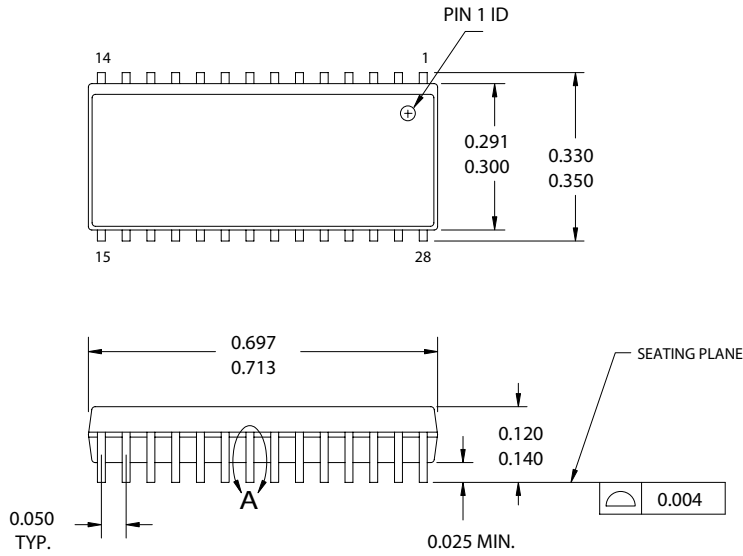
51-85071-\*G

**Package Diagrams** (continued)

**28-pin (300-Mil) Molded SOJ (51-85031)**

NOTE :

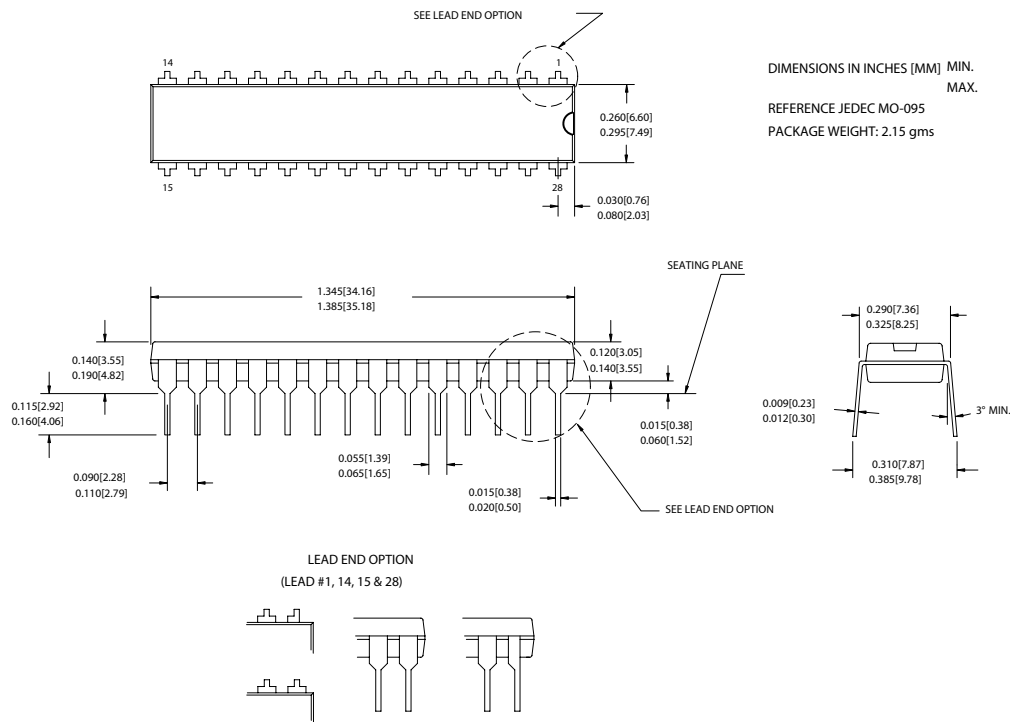
1. JEDEC STD REF MO088
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH  
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.006 in (0.152 mm) PER SIDE
3. DIMENSIONS IN INCHES  
MIN.  
MAX.



51-85031-°C

**Package Diagrams (continued)**

**28-pin (300-Mil) PDIP (51-85014)**



51-85014-\*D

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**Document History Page**

| Document Title: CY7C199C 256K (32K x 8) Static RAM<br>Document Number: 38-05408 |         |            |                 |   |
|---|---------|------------|-----------------|---|
| REV.  | ECN No. | Issue Date | Orig. of Change | Description of Change   |
| **  | 129233  | 09/11/03   | HGK             | New Data Sheet  |
| *A  | 129697  | 09/15/03   | KKV             | Minor change:<br>Move Product Portfolio from page 4 to page 1<br>Move Truth table from page 9 to page 3   |
| *B  | 341574  | See ECN    | PCI             | Added Lead-Free part to Ordering info on Page #10   |
| *C  | 492500  | See ECN    | NXR             | Removed 25 ns speed bin<br>Changed the description of $I_{IX}$ from Input Load Current to Input Leakage Current in DC Electrical Characteristics table<br>Removed $I_{OS}$ parameter from DC Electrical Characteristics table<br>Updated the ordering information table |