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256/512/1K/2K/4K x 9 Asynchronous FIFO

Features

- Asynchronous first-in first-out (FIFO) buffer memories
- 256 x 9 (CY7C419)
- 512 x 9 (CY7C421)
- 1K x 9 (CY7C425)
- 2K x 9 (CY7C429)
- 4K x 9 (CY7C433)
- Dual-ported RAM cell
- High speed 50 MHz read and write independent of depth and width
- Low operating power: I_{CC} = 35 mA
- Empty and full flags (Half Full flag in standalone)
- TTL compatible
- Retransmit in standalone
- Expandable in width
- PLCC, 7x7 TQFP, SOJ, 300-mil, and 600-mil DIP
- Pb-free packages available
- Pin compatible and functionally equivalent to IDT7200, IDT7201, IDT7202, IDT7203, IDT7204, AM7200, AM7201, AM7202, AM7203, and AM7204

Functional Description

The CY7C419, CY7C420/1, CY7C424/5, CY7C428/9, and CY7C432/3 are first-in first-out (FIFO) memories offered in 600-mil wide and 300-mil wide packages. There are 256, 512, 1,024, 2,048, and 4,096 words respectively by 9 bits wide. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and empty flags are provided to prevent overrun and underrun. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel. This eliminates the serial addition of propagation delays, so that throughput is not reduced. Data is steered in a similar manner.
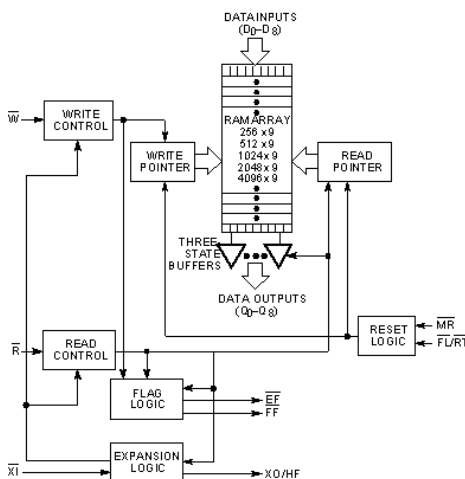
The read and write operations may be asynchronous; each can occur at a rate of 50 MHz. The write operation occurs when the write (W) signal is LOW. Read occurs when read (R) goes LOW. The nine data outputs go to the high impedance state when R is HIGH.

A Half Full (HF) output flag that is valid in the standalone and width expansion configurations is provided. In the depth expansion configuration, this pin provides the expansion out (XO) information that is used to tell the next FIFO that it is activated.

In the standalone and width expansion configurations, a LOW on the retransmit (RT) input causes the FIFOs to retransmit the data. Read enable (R) and write enable (W) must both be HIGH during retransmit, and then R is used to access the data.

The CY7C419, CY7C420, CY7C421, CY7C424, CY7C425, CY7C428, CY7C429, CY7C432, and CY7C433 are fabricated using an advanced 0.65-micron P-well CMOS technology. Input ESD protection is greater than 2000V and latch-up is prevented by careful layout and guard rings.

Logic Block Diagram
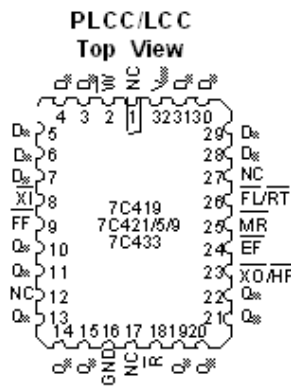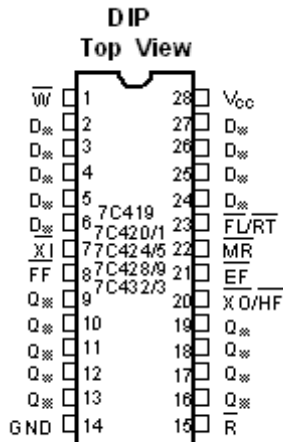
Pin Configurations

Figure 1. 32-Pin PLCC/LCC

PLCC/LCC
Top View

7C419
7C421/5/9
7C433

Figure 3. 32-Pln TQFP

TQFP
Top View

7C419
7C421/5/9
7C433

Figure 2. 28-Pin DIP

DIP
Top View

7C419
7C420/1
7C424/5
7C428/9
7C432/3
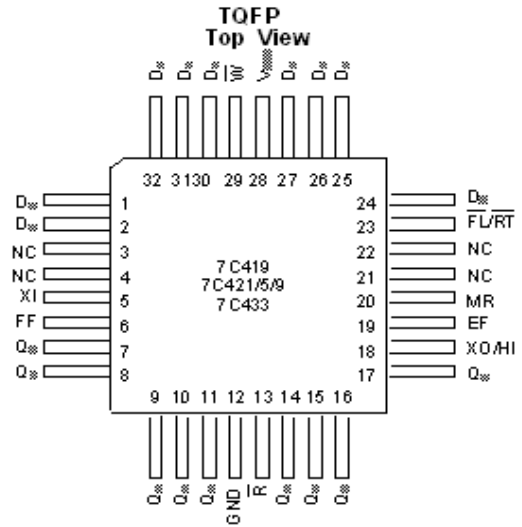
Table 1. Selection Guide

4K x 9	−10	−15	−20	−25	−30	−40	−65
Frequency (MHz)	50	40	33.3	28.5	25	20	12.5
Maximum Access Time (ns)	10	15	20	25	30	40	65
I_{CC1} (mA)	35	35	35	35	35	35	35

Maximum Rating

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.[1]

Storage Temperature .... –65°C to +150°C

Ambient Temperature with Power Applied.. –55°C to +125°C

Supply Voltage to Ground Potential................ –0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State .... –0.5V to +7.0V

DC Input Voltage .... –0.5V to +7.0V

Power Dissipation... 1.0W

Output Current, into Outputs (LOW)........................... 20 mA

Static Discharge Voltage... >2000V
(per MIL–STD–883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		All Speed Grades		Unit
				Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage		Commercial	2.0	V_{CC}	V
			Industrial	2.2	V_{CC}	
V_{IL}	Input LOW Voltage			[4]	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–10	+10	μA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		–10	+10	μA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			–90	mA

Notes
1. Single Power Supply: The voltage on any input or I/O pin can not exceed the power pin during power-up.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. V_{IL} (Min.) = –2.0V for pulse durations of less than 20 ns.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		−10		−15		−20		−25		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA f = f_{MAX}	Commercial		85		65		55		50	mA
			Industrial				100		90		80	
I_{CC1}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA F = 20 MHz	Commercial		35		35		35		35	mA
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Commercial		10		10		10		10	mA
			Industrial				15		15		15	
I_{SB2}	Power-Down Current	All Inputs ≥ V_{CC} −0.2V	Commercial		5		5		5		5	mA
			Industrial				8		8		8	

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		−30		−40		−65		Unit
				Min	Max	Min	Max	Min	Max	
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA f = f_{MAX}	Commercial		40		35		35	mA
			Industrial		75		70		65	
I_{CC1}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA F = 20 MHz	Commercial		35		35		35	mA
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Commercial		10		10		10	mA
			Industrial		15		15		15	
I_{SB2}	Power-Down Current	All Inputs ≥ V_{CC} −0.2V	Commercial		5		5		5	mA
			Industrial		8		8		8	

Capacitance[6]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	6	pF
C_{OUT}	Output Capacitance		6	pF

Note
6. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[7, 8]

Parameter	Description	−10 Min	−10 Max	−15 Min	−15 Max	−20 Min	−20 Max	−25 Min	−25 Max	Unit
t_{RC}	Read Cycle Time	20		25		30		35		ns
t_A	Access Time		10		15		20		25	ns
t_{RR}	Read Recovery Time	10		10		10		10		ns
t_{PR}	Read Pulse Width	10		15		20		25		ns
t_{LZR}[6,9]	Read LOW to Low Z	3		3		3		3		ns
t_{DVR}[9,10]	Data Valid After Read HIGH	5		5		5		5		ns
t_{HZR}[6,9,10]	Read HIGH to High Z		15		15		15		18	ns
t_{WC}	Write Cycle Time	20		25		30		35		ns
t_{PW}	Write Pulse Width	10		15		20		25		ns
t_{HWZ}[6,9]	Write HIGH to Low Z	5		5		5		5		ns
t_{WR}	Write Recovery Time	10		10		10		10		ns
t_{SD}	Data Set-Up Time	6		8		12		15		ns
t_{HD}	Data Hold Time	0		0		0		0		ns
t_{MRSC}	MR Cycle Time	20		25		30		35		ns
t_{PMR}	MR Pulse Width	10		15		20		25		ns
t_{RMR}	MR Recovery Time	10		10		10		10		ns
t_{RPW}	Read HIGH to MR HIGH	10		15		20		25		ns
t_{WPW}	Write HIGH to MR HIGH	10		15		20		25		ns
t_{RTC}	Retransmit Cycle Time	20		25		30		35		ns
t_{PRT}	Retransmit Pulse Width	10		15		20		25		ns
t_{RTR}	Retransmit Recovery Time	10		10		10		10		ns
t_{EFL}	MR to EF LOW		20		25		30		35	ns
t_{HFH}	MR to HF HIGH		20		25		30		35	ns
t_{FFH}	MR to FF HIGH		20		25		30		35	ns
t_{REF}	Read LOW to EF LOW		10		15		20		25	ns
t_{RFF}	Read HIGH to FF HIGH		10		15		20		25	ns
t_{WEF}	Write HIGH to EF HIGH		10		15		20		25	ns
t_{WFF}	Write LOW to FF LOW		10		15		20		25	ns
t_{WHF}	Write LOW to HF LOW		10		15		20		25	ns
t_{RHF}	Read HIGH to HF HIGH		10		15		20		25	ns
t_{RAE}	Effective Read from Write HIGH		10		15		20		25	ns
t_{RPE}	Effective Read Pulse Width After EF HIGH	10		15		20		25		ns
t_{WAF}	Effective Write from Read HIGH		10		15		20		25	ns
t_{WPF}	Effective Write Pulse Width After FF HIGH	10		15		20		25		ns
t_{XOL}	Expansion Out LOW Delay from Clock		10		15		20		25	ns
t_{XOH}	Expansion Out HIGH Delay from Clock		10		15		20		25	ns

Notes
7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance, as in part (a) of AC Test Load and Waveforms, unless otherwise specified.
8. See the last page of this specification for Group A subgroup testing information.
9. t_{HZR} transition is measured at +200 mV from V_{OL} and −200 mV from V_{OH}. t_{DVR} transition is measured at the 1.5V level. t_{HWZ} and t_{LZR} transition is measured at ±100 mV from the steady state.
10. t_{HZR} and t_{DVR} use capacitance loading as in part (b) of AC Test Load and Waveforms.

[+] Feedback

Switching Characteristics Over the Operating Range[7, 8] (continued)

Parameter	Description	−30 Min	−30 Max	−40 Min	−40 Max	−65 Min	−65 Max	Unit
t_{RC}	Read Cycle Time	40		50		80		ns
t_A	Access Time		30		40		65	ns
t_{RR}	Read Recovery Time	10		10		15		ns
t_{PR}	Read Pulse Width	30		40		65		ns
t_{LZR}[6,9]	Read LOW to Low Z	3		3		3		ns
t_{DVR}[9,10]	Data Valid After Read HIGH	5		5		5		ns
t_{HZR}[6,9,10]	Read HIGH to High Z		20		20		20	ns
t_{WC}	Write Cycle Time	40		50		80		ns
t_{PW}	Write Pulse Width	30		40		65		ns
t_{HWZ}[6,9]	Write HIGH to Low Z	5		5		5		ns
t_{WR}	Write Recovery Time	10		10		15		ns
t_{SD}	Data Set-Up Time	18		20		30		ns
t_{HD}	Data Hold Time	0		0		0		ns
t_{MRSC}	MR Cycle Time	40		50		80		ns
t_{PMR}	MR Pulse Width	30		40		65		ns
t_{RMR}	MR Recovery Time	10		10		15		ns
t_{RPW}	Read HIGH to MR HIGH	30		40		65		ns
t_{WPW}	Write HIGH to MR HIGH	30		40		65		ns
t_{RTC}	Retransmit Cycle Time	40		50		80		ns
t_{PRT}	Retransmit Pulse Width	30		40		65		ns
t_{RTR}	Retransmit Recovery Time	10		10		15		ns
t_{EFL}	MR to EF LOW		40		50		80	ns
t_{HFH}	MR to HF HIGH		40		50		80	ns
t_{FFH}	MR to FF HIGH		40		50		80	ns
t_{REF}	Read LOW to EF LOW		30		35		60	ns
t_{RFF}	Read HIGH to FF HIGH		30		35		60	ns
t_{WEF}	Write HIGH to EF HIGH		30		35		60	ns
t_{WFF}	Write LOW to FF LOW		30		35		60	ns
t_{WHF}	Write LOW to HF LOW		30		35		60	ns
t_{RHF}	Read HIGH to HF HIGH		30		35		60	ns
t_{RAE}	Effective Read from Write HIGH		30		35		60	ns
t_{RPE}	Effective Read Pulse Width After EF HIGH	30		40		65		ns
t_{WAF}	Effective Write from Read HIGH		30		35		60	ns
t_{WPF}	Effective Write Pulse Width After FF HIGH	30		40		65		ns
t_{XOL}	Expansion Out LOW Delay from Clock		30		40		65	ns
t_{XOH}	Expansion Out HIGH Delay from Clock		30		40		65	ns

Switching Waveforms

Figure 4. Asynchronous Read and Write
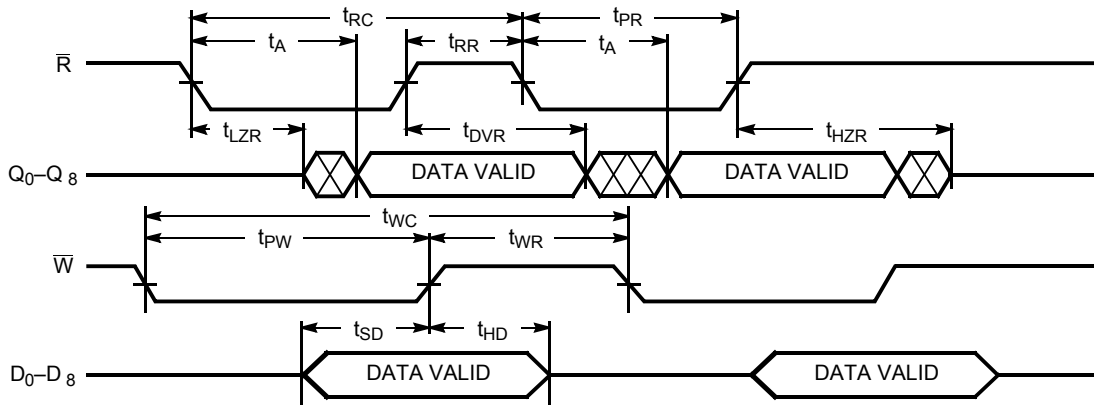
Figure 5. Master Reset
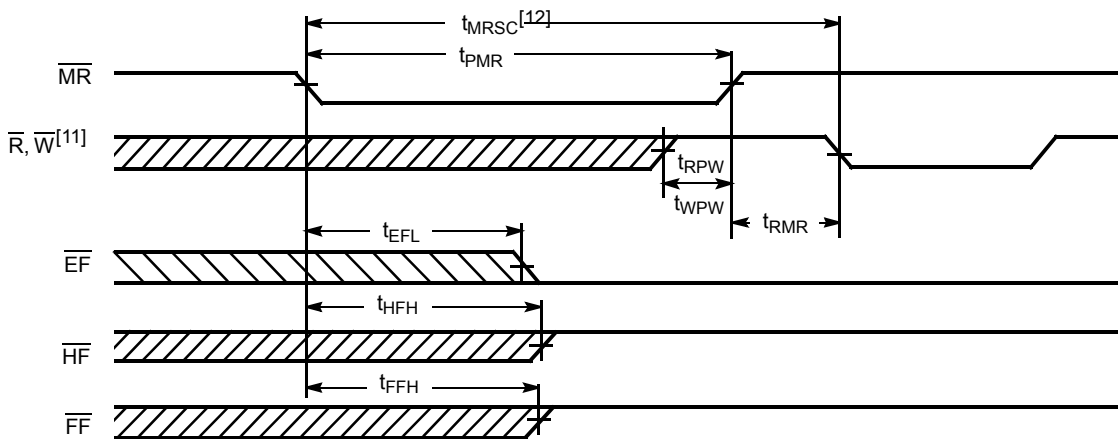
Figure 6. Half-full Flag
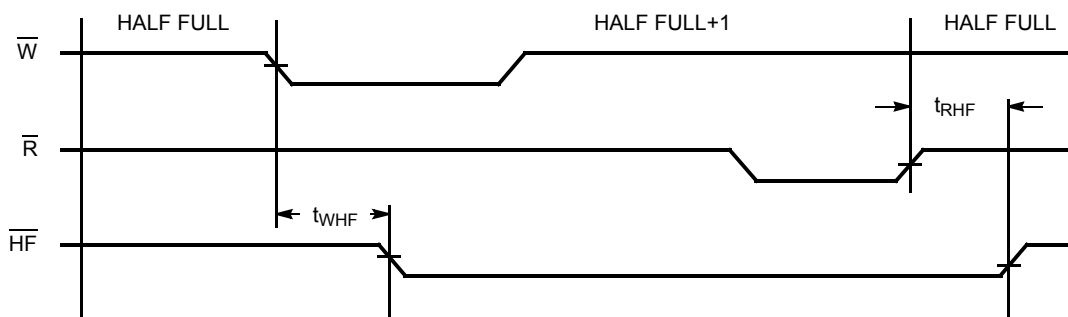
Notes
11. $\overline{W}$ and $\overline{R} \geq V_{IH}$ around the rising edge of $\overline{MR}$
12. $t_{MRSC} = t_{PMR} + t_{RMR}$.

[+] Feedback

Switching Waveforms (continued)

Figure 7. Last Write to First Read Full Flag

$\overline{R}$
$\overline{W}$
$\overline{FF}$

LAST WRITE   FIRST READ   ADDITIONAL READS   FIRST WRITE

t_{WFF} t_{RFF}
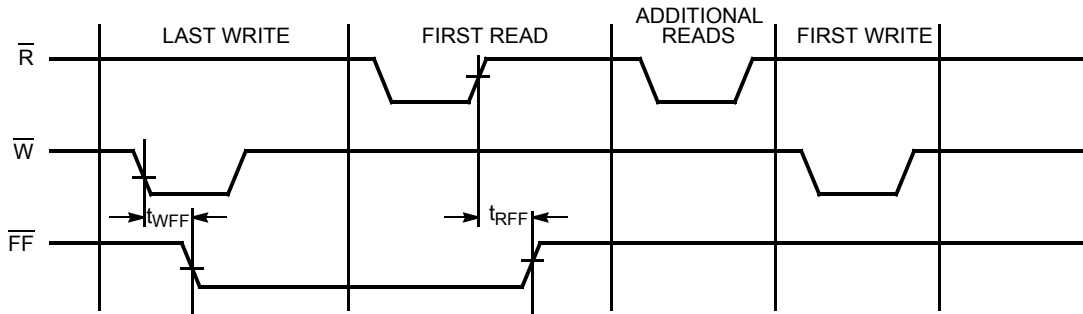
Figure 8. Last Read to First Write Empty Flag

$\overline{W}$
$\overline{R}$
$\overline{EF}$
DATA OUT

LAST READ   FIRST WRITE   ADDITIONAL WRITES   FIRST READ

t_{REF} t_{WEF}
t_A
VALID   VALID
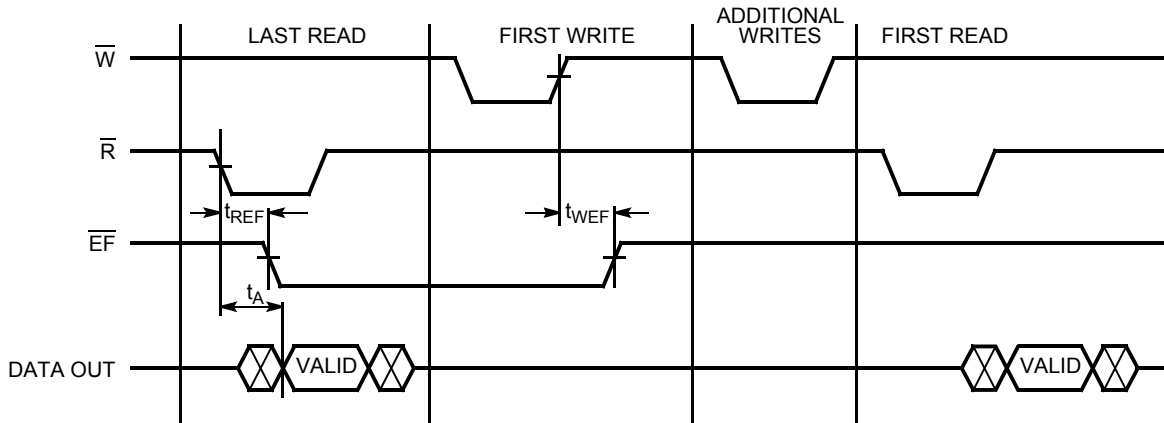
Figure 9. Retransmit[13]

$\overline{FL}/\overline{RT}$
$\overline{R},\overline{W}$
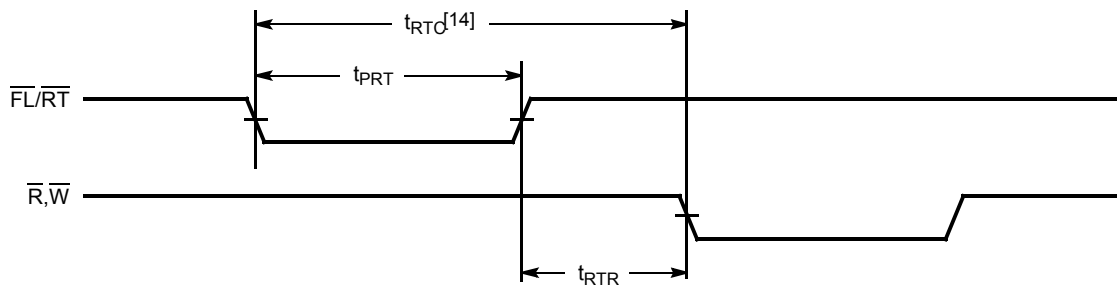
t_{RTC}[14]
t_{PRT}
t_{RTR}

Notes
13. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.
14. $t_{RTC} = t_{PRT} + t_{RTR}$.

[+] Feedback

Switching Waveforms (continued)

Figure 10. Empty Flag and Read Data Flow-through Mode
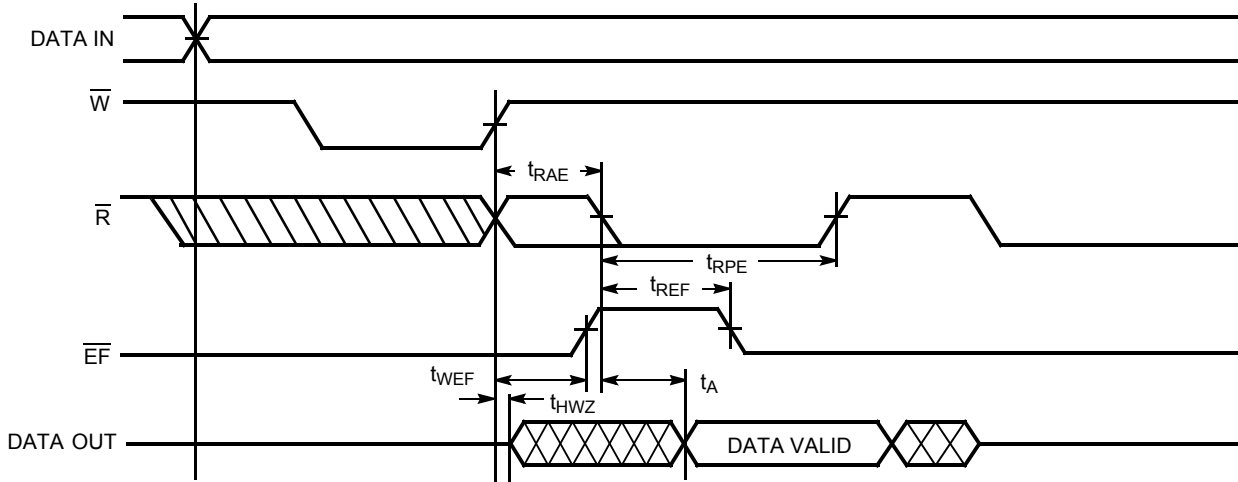
Figure 11. Full Flag and Write Data Flow-through Mode
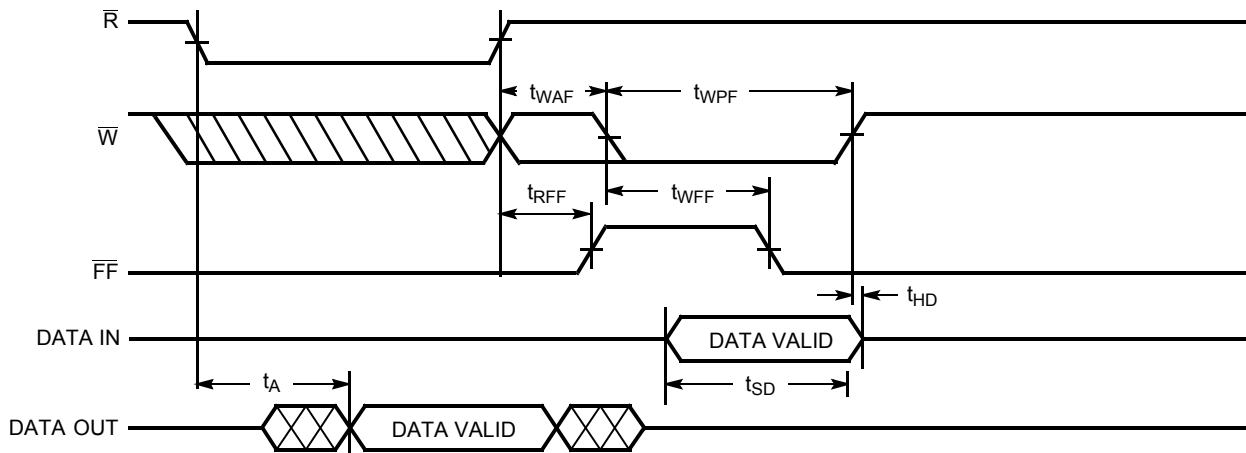
Switching Waveforms (continued)

Figure 12. Expansion Timing Diagrams

WRITE TO LAST PHYSICAL LOCATION OF DEVICE 1

WRITE TO FIRST PHYSICAL LOCATION OF DEVICE 2

$\overline{W}$

t_{WR}

$\overline{XO}_1(\overline{XI}_2)^{[15]}$

t_{XOL}

t_{XOH}

t_{SD} t_{HD} t_{SD} t_{HD}

$D_0 – D_8$ DATA VALID   DATA VALID

READ FROM LAST PHYSICAL LOCATION OF DEVICE 1

READ FROM FIRST PHYSICAL LOCATION OF DEVICE 2

$\overline{R}$

t_{RR}

$\overline{XO}_1(\overline{XI}_2)^{[15]}$

t_{XOL}

t_{XOH}

t_{HZR}

t_{LZR} t_{DVR} t_{DVR}

$Q_0 – Q_8$ DATA VALID   DATA VALID

t_A t_A
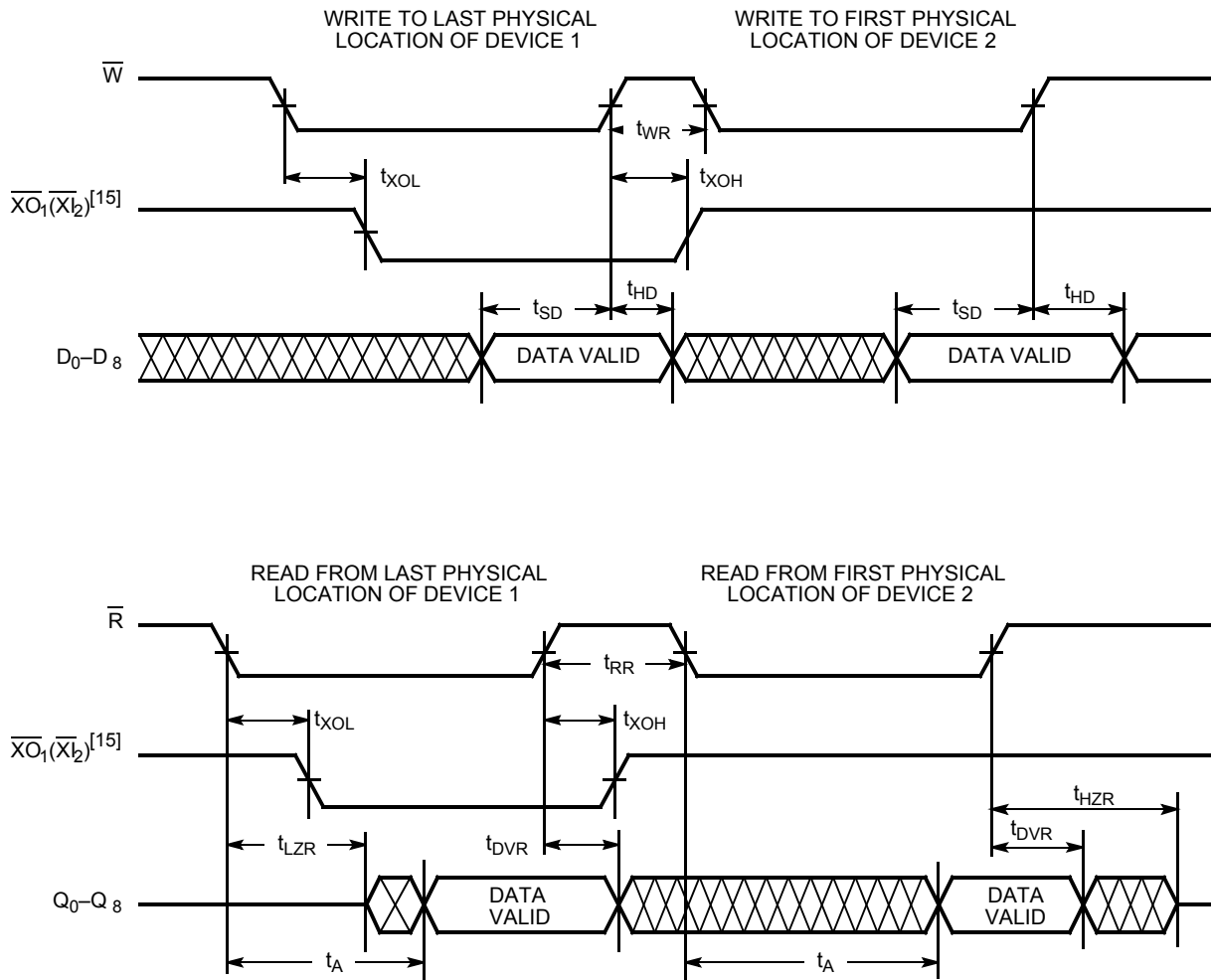
Note
15. Expansion Out of device 1 ($\overline{XO}_1$) is connected to Expansion In of device 2 ($\overline{XI}_2$).

Architecture

The CY7C419, CY7C420/1, CY7C424/5, CY7C428/9, CY7C432/3 FIFOs consist of an array of 256, 512, 1024, 2048, 4096 words of 9 bits each (implemented by an array of dual-port RAM cells), a read pointer, a write pointer, control signals (W, R, XI, XO, FL, RT, MR), and Full, Half Full, and Empty flags.

Dual-Port RAM

The dual-port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time required for data propagation through the memory, which is the case if memory is implemented using the conventional register array architecture.

Resetting the FIFO

Upon power up, the FIFO must be reset with a Master Reset (MR) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag (EF) being LOW, and both the Half Full (HF) and Full flags (FF) being HIGH. Read (R) and write (W) must be HIGH t_{RPW}/t_{WPW} before and t_{RMR} after the rising edge of MR for a valid reset cycle. If reading from the FIFO after a reset cycle is attempted, the outputs are in the high impedance state.

Writing Data to the FIFO

The availability of at least one empty location is indicated by a HIGH FF. The falling edge of W initiates a write cycle. Data appearing at the inputs (D_0–D_8) t_{SD} before and t_{HD} after the rising edge of W will be stored sequentially in the FIFO.

The EF LOW-to-HIGH transition occurs t_{WEF} after the first LOW-to-HIGH transition of W for an empty FIFO. HF goes LOW t_{WHF} after the falling edge of W following the FIFO actually being Half Full. Therefore, the HF is active once the FIFO is filled to half its capacity plus one word. HF will remain LOW while less than one half of total memory is available for writing. The LOW-to-HIGH transition of HF occurs t_{RHF} after the rising edge of R when the FIFO goes from half full +1 to half full. HF is available in standalone and width expansion modes. FF goes LOW t_{WFF} after the falling edge of W, during the cycle in which the last available location is filled. Internal logic prevents overrunning a full FIFO. Writes to a full FIFO are ignored and the write pointer is not incremented. FF goes HIGH tRFF after a read from a full FIFO.

Reading Data from the FIFO

The falling edge of R initiates a read cycle if the EF is not LOW. Data outputs (Q_0 to Q_8) are in a high impedance condition between read operations (R HIGH), when the FIFO is empty, or when the FIFO is not the active device in the depth expansion mode.

When one word is in the FIFO, the falling edge of R initiates a HIGH-to-LOW transition of EF. The rising edge of R causes the data outputs to go to the high impedance state and remain such until a write is performed. Reads to an empty FIFO are ignored and do not increment the read pointer. From the empty condition, the FIFO can be read t_{WEF} after a valid write.

The retransmit feature is beneficial when transferring packets of data. It enables the receiver to acknowledge receipt of data and retransmit, if necessary.

The Retransmit (RT) input is active in the standalone and width expansion modes. The retransmit feature is intended for use when a number of writes equal to or less than the depth of the FIFO have occurred since the last MR cycle. A LOW pulse on RT resets the internal read pointer to the first physical location of the FIFO. R and W must both be HIGH while and t_{RTR} after retransmit is LOW. With every read cycle after retransmit, previously accessed data and not previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Full, Half Full, and Empty flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of RT are also transmitted. FIFO, up to the full depth, can be repeatedly retransmitted.

Standalone/Width Expansion Modes

Standalone and width expansion modes are set by grounding Expansion In (XI) and tying First Load (FL) to V_{CC}. FIFOs can be expanded in width to provide word widths greater than nine in increments of nine. During width expansion mode, all control line inputs are common to all devices, and flag outputs from any device can be monitored.

Depth Expansion Mode

Depth expansion mode (see Figure 13 on page 12) is entered when, during a MR cycle, Expansion Out (XO) of one device is connected to Expansion In (XI) of the next device, with XO of the last device connected to XI of the first device. In the depth expansion mode the First Load (FL) input, when grounded, indicates that this part is the first to be loaded. All other devices must have this pin HIGH. To enable the correct FIFO, XO is pulsed LOW when the last physical location of the previous FIFO is written to and pulsed LOW again when the last physical location is read. Only one FIFO is enabled for read and one for write at any given time. All other devices are in standby.

FIFOs can also be expanded simultaneously in depth and width. Consequently, any depth or width FIFO can be created of word widths in increments of 9. When expanding in depth, a composite FF must be created by ORing the FFs together. Likewise, a composite EF is created by ORing the EFs together. HF and RT functions are not available in depth expansion mode.

Use of the Empty and Full Flags

To achieve maximum frequency, the flags must be valid at the beginning of the next cycle. However, because they can be updated by either edge of the read or write signal, they must be valid by one-half of a cycle. Cypress FIFOs meet this requirement; some competitors' FIFOs do not.

The reason for why the flags should be valid by the next cycle is complex. The "effective pulse width violation" phenomenon can occur at the full and empty boundary conditions, if the flags are not properly used. The empty flag must be used to prevent reading from an empty FIFO and the full flag must be used to prevent writing into a full FIFO.

For example, consider an empty FIFO that is receiving read pulses. Because the FIFO is empty, the read pulses are ignored by the FIFO, and nothing happens. Next, a single word is written

into the FIFO, with a signal that is asynchronous to the read signal. The (internal) state machine in the FIFO goes from empty to empty+1. However, it does this asynchronously with respect to the read signal, so that the effective pulse width of the read signal cannot be determined, because the state machine does not look at the read signal until it goes to the empty+1 state.

Similarly, the minimum write pulse width may be violated by trying to write into a full FIFO, and asynchronously performing a read. The empty and full flags are used to avoid these effective pulse width violations, but to do this and operate at the maximum frequency, the flag must be valid at the beginning of the next cycle.

Figure 13. Depth Expansion

* FIRST DEVICE

Ordering Information

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
10	CY7C421–10AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C421–10JC	J65	32-Pin Plastic Leaded Chip Carrier	
	CY7C421–10JXC	J65	32-Pin Pb-Free Plastic Leaded Chip Carriers	
	CY7C421–10PC	P21	28-Pin (300-Mil) Molded DIP	
	CY7C421–10VC	V21	28-Pin (300-Mil) Molded SOJ	
15	CY7C421–15AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C421–15AXC	A32	32-Pin Pb-Free Thin Plastic Quad Flatpack	
	CY7C421–15JC	J65	32-Pin Plastic Leaded Chip Carrier	
	CY7C421–15JI	J65	32-Pin Plastic Leaded Chip Carrier	Industrial
	CY7C421–15VI	V21	28-Pin (300-Mil) Molded SOJ	
20	CY7C421–20JC	J65	32-Pin Plastic Leaded Chip Carrier	Commercial
	CY7C421–20JXC	J65	32-Pin Pb-Free Plastic Leaded Chip Carriers	
	CY7C421–20PC	P21	28-Pin (300-Mil) Molded DIP	
	CY7C421–20VC	V21	28-Pin (300-Mil) Molded SOJ	
	CY7C421–20VXC	V21	28-Pin (300-Mil) Pb-Free Molded SOJ	
	CY7C421–20JI	J65	32-Pin Plastic Leaded Chip Carrier	Industrial
	CY7C421–20JXI	J65	32-Pin Plastic Leaded Chip Carrier	
25	CY7C421–25JC	J65	32-Pin Plastic Leaded Chip Carrier	Commercial
	CY7C421–25PC	P21	28-Pin (300-Mil) Molded DIP	
	CY7C421–25VC	V21	28-Pin (300-Mil) Molded SOJ	
	CY7C421–25JI	J65	32-Pin Plastic Leaded Chip Carrier	Industrial
	CY7C421–25PI	P21	28-Pin (300-Mil) Molded DIP	
30	CY7C421–30JC	J65	32-Pin Plastic Leaded Chip Carrier	Commercial
	CY7C421–30PC	P21	28-Pin (300-Mil) Molded DIP	
	CY7C421–30JI	J65	32-Pin Plastic Leaded Chip Carrier	Industrial
40	CY7C421–40JC	J65	32-Pin Plastic Leaded Chip Carrier	Commercial
	CY7C421–40PC	P21	28-Pin (300-Mil) Molded DIP	
	CY7C421–40VC	V21	28-Pin (300-Mil) Molded SOJ	
	CY7C421–40JI	J65	32-Pin Plastic Leaded Chip Carrier	Industrial
65	CY7C421–65JC	J65	32-Pin Plastic Leaded Chip Carrier	Commercial
	CY7C421–65PC	P21	28-Pin (300-Mil) Molded DIP	
	CY7C421–65VC	V21	28-Pin (300-Mil) Molded SOJ	
	CY7C421–65JI	J65	32-Pin Plastic Leaded Chip Carrier	Industrial

[+] Feedback

Package Diagrams

Figure 14. 32-Pin Thin Plastic Quad Flat Pack A32 (51-85063)

DIMENSIONS IN MILLIMETERS
LEAD COPLANARITY 0.080 MAX.

DIM. A	DIM. A1
1.60 MAX.	1.40±0.05 PKG. THICK
1.20 MAX.	1.00±0.05 PKG. THICK

51-85063-*B
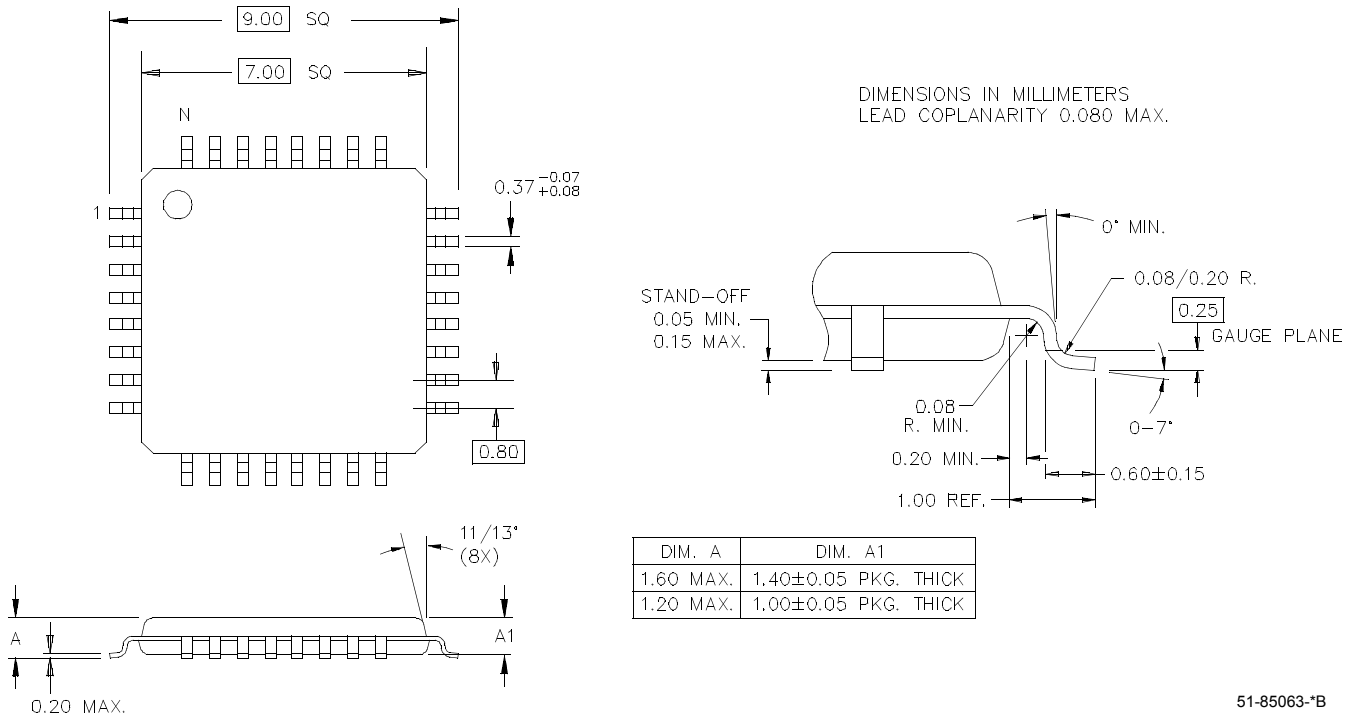
Figure 15. 32-Pin Plastic Leaded Chip Carrier J65 (51-85002)

DIMENSIONS IN INCHES $\frac{MIN.}{MAX.}$

51-85002-*B
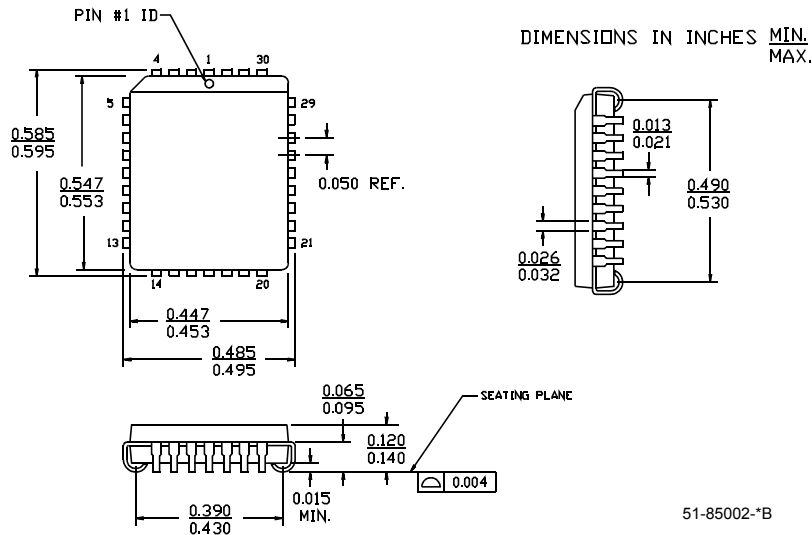
Package Diagrams (continued)

Figure 16. 28-Pin (300-Mil) PDIP P21 (51-85014)

DIMENSIONS IN INCHES [MM] MIN.
                             MAX.

REFERENCE JEDEC MO-095
PACKAGE WEIGHT: 2.15 gms

SEE LEAD END OPTION

0.260[6.60]
0.295[7.49]

0.030[0.76]
0.080[2.03]

1.345[34.16]
1.385[35.18]

SEATING PLANE

0.140[3.55]
0.190[4.82]

0.120[3.05]
0.140[3.55]

0.115[2.92]
0.160[4.06]

0.290[7.36]
0.325[8.25]

0.015[0.38]
0.060[1.52]

0.009[0.23]
0.012[0.30]

3° MIN.

0.055[1.39]
0.065[1.65]

0.090[2.28]
0.110[2.79]

0.015[0.38]
0.020[0.50]

0.310[7.87]
0.385[9.78]

SEE LEAD END OPTION

LEAD END OPTION
(LEAD #1, 14, 15 & 28)

51-85014-*D

Package Diagrams (continued)

Figure 17. 28-Pin (300-Mil) Molded SOJ V21(51-85031)

NOTE :
1. JEDEC STD REF MO088
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.006 In (0.152 mm) PER SIDE
3. DIMENSIONS IN INCHES MIN.
                          MAX.

51-85031-*C

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