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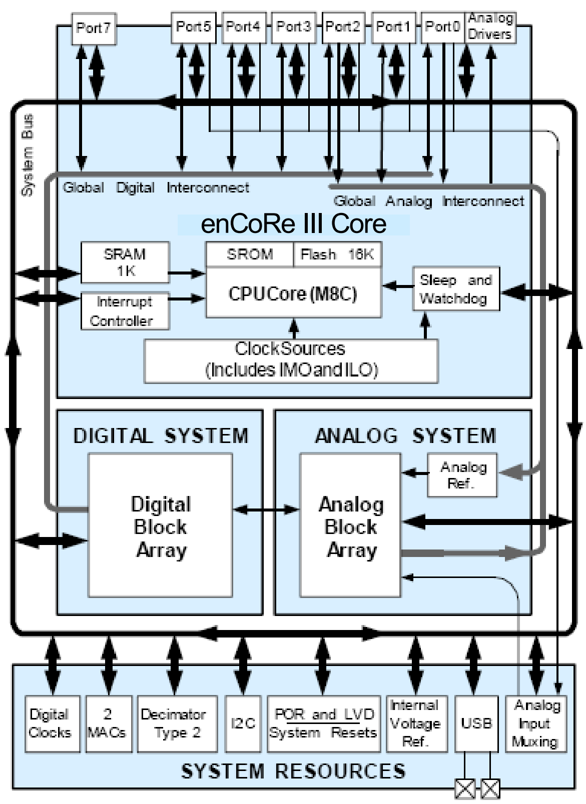
CY7C64215

enCoRe™ III Full-Speed USB Controller

Features

- Powerful Harvard-architecture processor
  - M8C processor speeds up to 24 MHz
  - Two 8 × 8 multiply, 32-bit accumulate
  - 3.15 to 5.25-V operating voltage
  - USB 2.0 USB-IF certified. TID# 40000110
  - Commercial operating temperature range: 0 °C to +70 °C
  - Industrial operating temperature range: –40 °C to +85 °C
- Advanced peripherals (enCoRe™ III blocks)
  - Six analog enCoRe III blocks provide:
    - Up to 14-bit incremental and delta sigma analog-to-digital converters (ADCs)
  - Programmable threshold comparator
  - Four digital enCoRe III blocks provide:
    - 8-bit and 16-bit pulse width modulators (PWMs), timers, and counters
    - I^2C master
    - SPI master or slave
    - Full-duplex universal asynchronous receiver-transmitter (UART)
    - CYFISNP modules to talk to Cypress CYFI™ radio
- Complex peripherals by combining blocks
- Full-speed USB (12 Mbps)
  - Four unidirectional endpoints
  - One bidirectional control endpoint
  - Dedicated 256-byte buffer
  - No external crystal required
  - Operational at 3.15 V to 3.5 V or 4.35 V to 5.25 V
- Flexible on-chip memory
  - 16 KB flash program storage 50,000 erase/write cycles
  - 1 KB SRAM data storage
  - In-system serial programming (ISSP)
  - Partial flash updates
  - Flexible protection modes
  - EEPROM emulation in flash
- Programmable pin configurations
  - 25 mA sink on all general purpose I/Os (GPIOs)
  - Pull-up, Pull-down, high Z, strong, or open drain drive modes on all GPIOs
  - Configurable interrupt on all GPIOs
- Precision, programmable clocking
  - Internal ±4% 24- and 48-MHz oscillator with support for external clock oscillator
  - Internal oscillator for watchdog and sleep
  - .25% accuracy for USB with no external components
- Additional system resources
  - Inter-integrated circuit (I^2C) slave, master, and multimaster to 400 kHz
  - Watchdog and sleep timers
  - User-configurable low-voltage detection (LVD)
  - Integrated supervisory circuit
  - On-chip precision voltage reference
- Complete development tools
  - Free development software (PSoC® Designer™)
  - Full-featured, in-circuit emulator and programmer
  - Full-speed emulation
  - Complex breakpoint structure
  - 128 KB trace memory

Block Diagram



Errata: For information on silicon errata, see "Errata" on page 40. Details include trigger conditions, devices affected, and proposed workaround.

Contents

Applications

- PC human interface devices
  - Mouse (optomechanical, optical, trackball)
  - Keyboards
  - Joysticks
- Gaming
  - Game pads
  - Console keyboards
- General purpose
  - Barcode scanners
  - POS terminal
  - Consumer electronics
  - Toys
  - Remote controls
  - USB to serial

enCoRe III Functional Overview

The enCoRe III is based on the flexible PSoC architecture and is a full-featured, full-speed (12-Mbps) USB part. Configurable analog, digital, and interconnect circuitry enable a high level of integration in a host of consumer, and communication applications.

This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in both 28-pin SSOP and 56-pin QFN packages.

enCoRe III architecture, as illustrated in the "Block Diagram" on page 1, is comprised of four main areas: enCoRe III core, digital system, analog system, and system resources including a full-speed USB port. Configurable global busing enables all the device resources to combine into a complete custom system. The enCoRe III CY7C64215 can have up to seven I/O ports that connect to the global digital and analog interconnects, providing access to four digital blocks and six analog blocks.

enCoRe III Core

The enCoRe III Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIOs.

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four-million instructions per second (MIPS) 8-bit Harvard-architecture microprocessor. The CPU uses an interrupt controller with up to 20 vectors, to simplify programming of real-time embedded events. Program execution is timed and protected using the included sleep and watchdog timers (WDT).

Memory encompasses 16 KB of flash for program storage, 1 KB of SRAM for data storage, and up to 2 KB of EEPROM emulated using the flash. Program flash uses four protection levels on blocks of 64 bytes, enabling customized software IP protection.

enCoRe III incorporates flexible internal clock generators, including a 24-MHz internal main oscillator (IMO) accurate to 8% over temperature and voltage as well as an option for an external clock oscillator (ECO). USB operation requires the OSC LOCK bit of the USB_CR0 register to be set to obtain IMO accuracy to.25%.

The 24-MHz IMO is doubled to 48 MHz for use by the digital system, if needed. The 48-MHz clock is required to clock the USB block and must be enabled for communication. A low-power 32-kHz internal low-speed oscillator (ILO) is provided for the sleep timer and WDT. The clocks, together with programmable clock dividers (system resource), provide flexibility to integrate almost any timing requirement into enCoRe III. In USB systems, the IMO self-tunes to ±0.25% accuracy for USB communication.

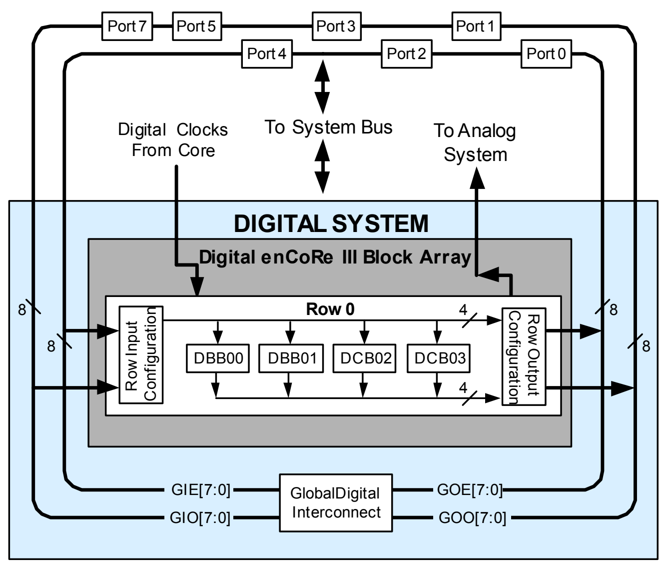
The extended temperature range for the industrial operating range (–40 °C to +85 °C) requires the use of an ECO, which is only available on the 56-pin QFN package.

enCoRe III GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, enabling great flexibility in external interfacing. Every pin also has capability to generate a system interrupt on high-level, low-level, and change from last read.

The Digital System

The digital system is composed of four digital enCoRe III blocks. Each block is an 8-bit resource that is used alone or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals, which are called user module references.

Figure 1. Digital System Block Diagram



The following digital configurations can be built from the blocks:

- PWMs, timers, and counters (8-bit and 16-bit)
- UART 8-bit with selectable parity
- SPI master and slave
- I^2C master
- RF interface: Interface to Cypress CYFI radio

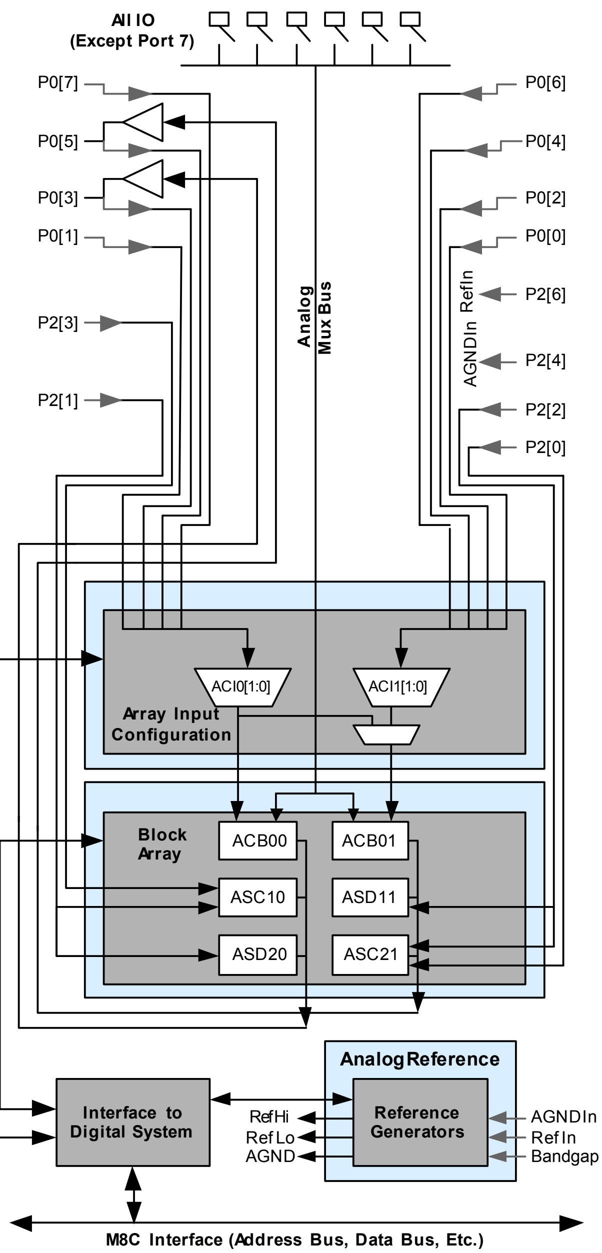
The digital blocks are connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also enable signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

The Analog System

The analog system is composed of six configurable blocks, comprised of an opamp circuit enabling the creation of complex analog signal flows. Analog peripherals are very flexible and are customized to support specific application requirements. enCoRe III analog function supports the Analog-to-digital converters (with 6- to 14-bit resolution, selectable as incremental, and delta-sigma) and programmable threshold comparator).

Analog blocks are arranged in two columns of three, with each column comprising one continuous time (CT) - AC B00 or AC B01 - and two switched capacitor (SC) - ASC10 and ASD20 or ASD11 and ASC21 - blocks, as shown in Figure 2.

Figure 2. Analog System Block Diagram



The Analog Multiplexer System

The analog mux bus can connect to every GPIO pin in ports 0 to 5. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters. It is split into two sections for simultaneous dual-channel processing. An additional 8:1 analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Additional System Resources

System resources provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power-on reset. Brief statements describing the merits of each resource follow.

- Full-speed USB (12 Mbps) with five configurable endpoints and 256 bytes of RAM. No external components required except two series resistors. Industrial temperature operating range for USB requires an external clock oscillator.
- Two multiply accumulates (MACs) provide fast 8-bit multipliers with 32-bit accumulate, to assist in both general math and digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of delta-sigma ADCs.
- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks are routed to both the digital and analog systems.
- The I^2C module provides 100- and 400-kHz communication over two wires. Slave, master, and multimaster modes are all supported.
- LVD interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.

enCoRe III Device Characteristics

enCoRe III devices have four digital blocks and six analog blocks. The following table lists the resources available for specific enCoRe III devices.

Table 1. enCoRe III Device Characteristics

Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY7C64215 28 Pin	up to 22	1	4	22	2	2	6	1K	16K
CY7C64215 56 Pin	up to 50	1	4	48	2	2	6	1K	16K

Getting Started

The quickest path to understanding the enCoRe III silicon is by reading this datasheet and using the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the enCoRe V integrated circuit and presents specific pin, register, and electrical specifications.

For in-depth information, along with detailed programming details, see the *PSoC® Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are ADCs, DACs, amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and are linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select User Modules
2. Configure User Modules
3. Organize and Connect
4. Generate, Verify, and Debug

Select Components

PSoC Designer provides a library of pre-built, pre-tested hardware peripheral components called “user modules”. User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure Components

Each of the User Modules you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more

digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the User Module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the "Generate Configuration Files" step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition

to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Pin Information

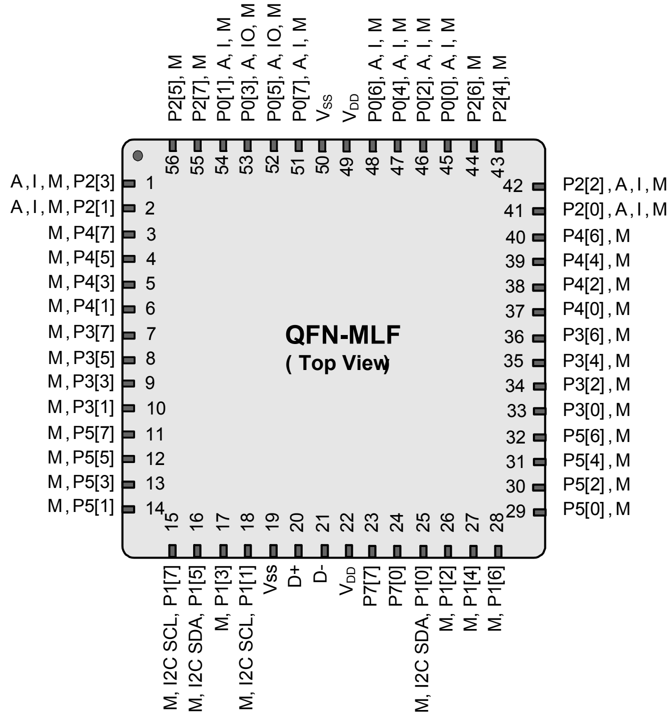
56-Pin Part Pinout

The CY7C64215 enCoRe III device is available in a 56-pin package which is listed and illustrated in the following table. Every port pin (labeled "P") is capable of digital I/O. However, V_{SS} and V_{DD} are not capable of digital I/O.

Table 2. 56-Pin Part Pinout (QFN-MLF SAWN)[1]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P2[3]	Direct switched capacitor block input.
2	I/O	I, M	P2[1]	Direct switched capacitor block input.
3	I/O	M	P4[7]	
4	I/O	M	P4[5]	
5	I/O	M	P4[3]	
6	I/O	M	P4[1]	
7	I/O	M	P3[7]	
8	I/O	M	P3[5]	
9	I/O	M	P3[3]	
10	I/O	M	P3[1]	
11	I/O	M	P5[7]	
12	I/O	M	P5[5]	
13	I/O	M	P5[3]	
14	I/O	M	P5[1]	
15	I/O	M	P1[7]	I2C serial clock (SCL).
16	I/O	M	P1[5]	I2C serial data (SDA).
17	I/O	M	P1[3]	
18	I/O	M	P1[1]	I2C SCL, ISSP-SCLK.
19	Power		V_{SS}	Ground connection.
20	USB		D+	
21	USB		D-	
22	Power		V_{DD}	Supply voltage.
23	I/O		P7[7]	
24	I/O		P7[0]	
25	I/O	M	P1[0]	I2C SDA, ISSP-SDATA.
26	I/O	M	P1[2]	
27	I/O	M	P1[4]	Optional external clock input EXTCLK.
28	I/O	M	P1[6]	
29	I/O	M	P5[0]	
30	I/O	M	P5[2]	
31	I/O	M	P5[4]	
32	I/O	M	P5[6]	
33	I/O	M	P3[0]	
34	I/O	M	P3[2]	
35	I/O	M	P3[4]	
36	I/O	M	P3[6]	
37	I/O	M	P4[0]	
38	I/O	M	P4[2]	
39	I/O	M	P4[4]	
40	I/O	M	P4[6]	
41	I/O	I, M	P2[0]	Direct switched capacitor block input.
42	I/O	I, M	P2[2]	Direct switched capacitor block input.
43	I/O	M	P2[4]	External analog ground (AGND) input.
44	I/O	M	P2[6]	External voltage reference (VREF) input.
45	I/O	I, M	P0[0]	Analog column mux input.
46	I/O	I, M	P0[2]	Analog column mux input and column output.
47	I/O	I, M	P0[4]	Analog column mux input and column output.
48	I/O	I, M	P0[6]	Analog column mux input.
49	Power		V_{DD}	Supply voltage.
50	Power		V_{SS}	Ground connection.
51	I/O	I, M	P0[7]	Analog column mux input.
52	I/O	I/O, M	P0[5]	Analog column mux input and column output
53	I/O	I/O, M	P0[3]	Analog column mux input and column output.
54	I/O	I, M	P0[1]	Analog column mux input.
55	I/O	M	P2[7]	
56	I/O	M	P2[5]	

Figure 3. CY7C64215 56-Pin enCoRe III Device



LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.

Note
1. The center pad on the QFN-MLF package should be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

28-Pin Part Pinout

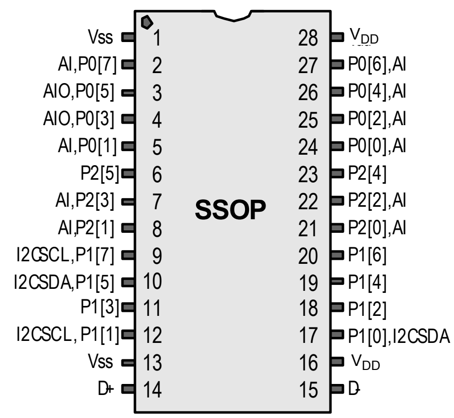
The CY7C64215 enCoRe III device is available in a 28-pin package which is listed and illustrated in the following table. Every port pin (labeled with a “P”) is capable of digital I/O. However, V_{SS} and V_{DD} are not capable of digital I/O.

Table 3. 28-Pin Part Pinout (SSOP)

Pin No.	Type		Name	Description
	Digital	Analog		
1	Power		GND	Ground connection.
2	I/O	I, M	P0[7]	Analog column mux input.
3	I/O	I/O,M	P0[5]	Analog column mux input and column output.
4	I/O	I/O,M	P0[3]	Analog column mux input and column output.
5	I/O	I,M	P0[1]	Analog column mux input.
6	I/O	M	P2[5]	
7	I/O	M	P2[3]	Direct switched capacitor block input.
8	I/O	M	P2[1]	Direct switched capacitor block input.
9	I/O	M	P1[7]	I^2C SCL
10	I/O	M	P1[5]	I^2C SDA
11	I/O	M	P1[3]	
12	I/O	M	P1[1]	I^2C SCL, ISSP-SCLK.
13	Power		GND	Ground connection.
14	USB		D+	
15	USB		D-	
16	Power		V_{DD}	Supply voltage.
17	I/O	M	P1[0]	I^2C SCL, ISSP-SDATA.
18	I/O	M	P1[2]	
19	I/O	M	P1[4]	
20	I/O	M	P1[6]	
21	I/O	M	P2[0]	Direct switched capacitor block input.
22	I/O	M	P2[2]	Direct switched capacitor block input.
23	I/O	M	P2[4]	External analog ground (AGND) input.
24	I/O	M	P0[0]	Analog column mux input.
25	I/O	M	P0[2]	Analog column mux input and column output.
26	I/O	M	P0[4]	Analog column mux input and column output.
27	I/O	M	P0[6]	Analog column mux input.
28	Power		V_{DD}	Supply voltage.

LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.

Figure 4. CY7C64215 28-Pin enCoRe III Device



Register Reference

The register conventions specific to this section are listed in the following table.

Table 4. Register Conventions

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The enCoRe III device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, bank 0 and bank 1. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set to '1', the user is in bank 1.

Note In the following register mapping tables, blank fields are reserved and should not be accessed.

Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	PMA0_DR	40	RW	ASC10CR0	80	RW		C0	
PRT0IE	01	RW	PMA1_DR	41	RW	ASC10CR1	81	RW		C1	
PRT0GS	02	RW	PMA2_DR	42	RW	ASC10CR2	82	RW		C2	
PRT0DM2	03	RW	PMA3_DR	43	RW	ASC10CR3	83	RW		C3	
PRT1DR	04	RW	PMA4_DR	44	RW	ASD11CR0	84	RW		C4	
PRT1IE	05	RW	PMA5_DR	45	RW	ASD11CR1	85	RW		C5	
PRT1GS	06	RW	PMA6_DR	46	RW	ASD11CR2	86	RW		C6	
PRT1DM2	07	RW	PMA7_DR	47	RW	ASD11CR3	87	RW		C7	
PRT2DR	08	RW	USB_SOF0	48	R		88			C8	
PRT2IE	09	RW	USB_SOF1	49	R		89			C9	
PRT2GS	0A	RW	USB_CR0	4A	RW		8A			CA	
PRT2DM2	0B	RW	USBIO_CR0	4B	#		8B			CB	
PRT3DR	0C	RW	USBIO_CR1	4C	RW		8C			CC	
PRT3IE	0D	RW		4D			8D			CD	
PRT3GS	0E	RW	EP1_CNT1	4E	#		8E			CE	
PRT3DM2	0F	RW	EP1_CNT	4F	RW		8F			CF	
PRT4DR	10	RW	EP2_CNT1	50	#	ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW	EP2_CNT	51	RW	ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW	EP3_CNT1	52	#	ASD20CR2	92	RW		D2	
PRT4DM2	13	RW	EP3_CNT	53	RW	ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW	EP4_CNT1	54	#	ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW	EP4_CNT	55	RW	ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW	EP0_CR	56	#	ASC21CR2	96	RW	I2C_CFG	D6	RW
PRT5DM2	17	RW	EP0_CNT	57	#	ASC21CR3	97	RW	I2C_SCR	D7	#
	18		EP0_DR0	58	RW		98		I2C_DR	D8	RW
	19		EP0_DR1	59	RW		99		I2C_MSCR	D9	#
	1A		EP0_DR2	5A	RW		9A		INT_CLR0	DA	RW
	1B		EP0_DR3	5B	RW		9B		INT_CLR1	DB	RW
PRT7DR	1C	RW	EP0_DR4	5C	RW		9C		INT_CLR2	DC	RW
PRT7IE	1D	RW	EP0_DR5	5D	RW		9D		INT_CLR3	DD	RW
PRT7GS	1E	RW	EP0_DR6	5E	RW		9E		INT_MSK3	DE	RW
PRT7DM2	1F	RW	EP0_DR7	5F	RW		9F		INT_MSK2	DF	RW
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W	AMUXCFG	61	RW		A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCB02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCB02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCB02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCB03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_D	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	PMA0_WA	40	RW	ASC10CR0	80	RW	USBIO_CR2	C0	RW
PRT0DM1	01	RW	PMA1_WA	41	RW	ASC10CR1	81	RW	USB_CR1	C1	#
PRT0IC0	02	RW	PMA2_WA	42	RW	ASC10CR2	82	RW			
PRT0IC1	03	RW	PMA3_WA	43	RW	ASC10CR3	83	RW			
PRT1DM0	04	RW	PMA4_WA	44	RW	ASD11CR0	84	RW	EP1_CR0	C4	#
PRT1DM1	05	RW	PMA5_WA	45	RW	ASD11CR1	85	RW	EP2_CR0	C5	#
PRT1IC0	06	RW	PMA6_WA	46	RW	ASD11CR2	86	RW	EP3_CR0	C6	#
PRT1IC1	07	RW	PMA7_WA	47	RW	ASD11CR3	87	RW	EP4_CR0	C7	#
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D			8D			CD	
PRT3IC0	0E	RW		4E			8E			CE	
PRT3IC1	0F	RW		4F			8F			CF	
PRT4DM0	10	RW	PMA0_RA	50	RW		90		GDI_O_IN	D0	RW
PRT4DM1	11	RW	PMA1_RA	51	RW	ASD20CR1	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW	PMA2_RA	52	RW	ASD20CR2	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW	PMA3_RA	53	RW	ASD20CR3	93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW	PMA4_RA	54	RW	ASC21CR0	94	RW		D4	
PRT5DM1	15	RW	PMA5_RA	55	RW	ASC21CR1	95	RW		D5	
PRT5IC0	16	RW	PMA6_RA	56	RW	ASC21CR2	96	RW		D6	
PRT5IC1	17	RW	PMA7_RA	57	RW	ASC21CR3	97	RW		D7	
	18			58			98		MUX_CR0	D8	RW
	19			59			99		MUX_CR1	D9	RW
	1A			5A			9A		MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
PRT7DM0	1C	RW		5C			9C			DC	
PRT7DM1	1D	RW		5D			9D		OSC_GO_EN	DD	RW
PRT7IC0	1E	RW		5E			9E		OSC_CR4	DE	RW
PRT7IC1	1F	RW		5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW	CMP_GO_EN	64	RW		A4		VLT_CMP	E4	R
DBB01IN	25	RW		65	RW		A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC		MUX_CR4	EC	RW
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD		MUX_CR5	ED	RW
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_CR	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

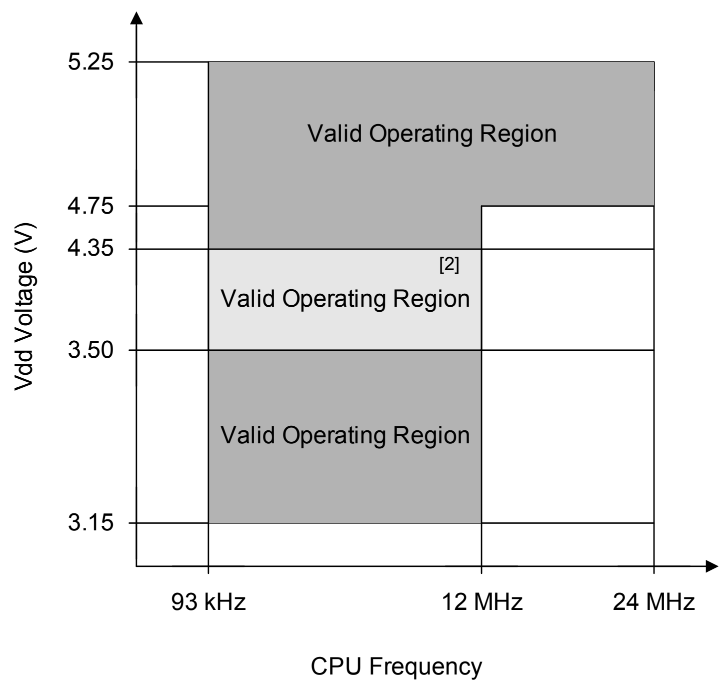
Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY7C64215 enCoRe III. For the most up-to-date electrical specifications, confirm that you have the most recent datasheet by going to the web at http://www.cypress.com/go/usb.

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications for devices running at greater than 12 MHz are valid for –40 °C ≤ T_A ≤ 70°C and T_J ≤ 82 °C.

Figure 5. Voltage versus CPU Frequency



Note

2. This is a valid operating region for the CPU, but USB hardware is non functional in the voltage range from 3.50 V to 4.35 V.

Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{STG}	Storage temperature	–55	–	+100	°C	Higher storage temperatures reduces data retention time.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	–
$T_{BAKETIME}$	Bake time	See package label	–	72	Hours	–
T_A	Ambient temperature with power applied	0	–	+70	°C	–
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	–
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	–
V_{IO2}	DC voltage applied to tristate	V_{SS} – 0.5	–	V_{DD} + 0.5	V	–
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	–
I_{MAIO}	Maximum current into any port pin configured as an analog driver	–50	–	+50	mA	–
ESD	Electrostatic discharge voltage	2000	–	–	V	Human body model ESD.
LU	Latch up current	–	–	200	mA	–

Operating Temperature

Table 6. Operating Temperature

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{AC}	Commercial ambient temperature	0	–	+70	°C	–
T_{AI}	Industrial ambient temperature	–40	–	+85	°C	USB operation requires the use of an external clock oscillator and the 56-pin QFN package.
T_J	Junction temperature	–40	–	+100	°C	The temperature rise from ambient to junction is package specific. See “Thermal Impedance” on page 32. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 7. DC Chip-Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{DD}	Supply voltage	3.0	–	5.25	V	See DC POR and LVD specifications, Table 15 on page 22. USB hardware is not functional when V_{DD} is between 3.5 V to 4.35 V.
I_{DD5}	Supply current, IMO = 24 MHz (5 V)	–	14	27	mA	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off.
I_{DD3}	Supply current, IMO = 24 MHz (3.3 V)	–	8	14	mA	Conditions are V_{DD} = 3.3 V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.367 kHz, analog power = off.
I_{SB}	Sleep [3] (mode) current with POR, LVD, sleep timer, and WDT [4].	–	3	6.5	μA	Conditions are with internal slow speed oscillator, V_{DD} = 3.3 V, 0 °C ≤ T_A ≤ 55 °C, analog power = off.
I_{SBH}	Sleep (mode) current with POR, LVD, sleep timer, and WDT at high temperature [4] .	–	4	25	μA	Conditions are with internal slow speed oscillator, V_{DD} = 3.3 V, 55 °C < T_A ≤ 70 °C, analog power = off.

Notes

3. Errata: When the device operates at4.75 V to 5.25 V and the 3.3-V regulator is enabled, a short low pulse may be created on the DP signal line during device wakeup. The 15- to 20-μs low pulse of the DP line may be interpreted by the host computer as a deattach or the beginning of a wakeup. For more details refer to Errata on page 40.
4. Standby current includes all functions (POR, LVD, WDT, sleep time) needed for reliable system operation. This should be compared with devices that have similar functions enabled.

DC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 8. DC GPIO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	–
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	–
V_{OH}	High output level	V_{DD} – 1.0	–	–	V	I_{OH} = 10 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I_{OH} budget.
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 25 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined I_{OL} budget.
I_{OH}	High-level source current	10	–	–	mA	–
I_{OL}	Low-level sink current	25	–	–	mA	–
V_{IL}	Input low level	–	–	0.8	V	V_{DD} = 3.15 to 5.25.
V_{IH}	Input high level	2.1	–		V	V_{DD} = 3.15 to 5.25.
V_H	Input hysteresis	–	60	–	mV	–
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.

DC Full-Speed USB Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges when the IMO is selected as system clock: 4.75 V to 5.25 V and 0 °C ≤ T_A ≤ 70 °C, or 3.15 V to 3.5 V and 0 °C ≤ T_A ≤ 70 °C, respectively.

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges when an external clock is selected as the system clock: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C.

Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 9. DC Full Speed (12 Mbps) USB Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
USB Interface						
V_{DI}	Differential input sensitivity	0.2	–	–	V	| (D+) – (D–) |
V_{CM}	Differential input common mode range	0.8	–	2.5	V	–
V_{SE}	Single-ended receiver threshold	0.8	–	2.0	V	–
C_{IN}	Transceiver capacitance	–	–	20	pF	–
I_{IO}	High Z state data line leakage	–10	–	10	μA	0 V < V_{IN} < 3.3 V.
R_{EXT}	External USB series resistor	23	–	25	Ω	In series with each USB pin.
V_{UOH}	Static output high, driven	2.8	–	3.6	V	15 kΩ ± 5% to ground. Internal pull-up enabled.
V_{UOHI}	Static output high, idle	2.7	–	3.6	V	15 kΩ ± 5% to ground. Internal pull-up enabled.
V_{UOL}	Static output low	–	–	0.3	V	15 kΩ ± 5% to ground. Internal pull-up enabled.
Z_O	USB driver output impedance	28	–	44	Ω	Including R_{EXT} resistor.
V_{CRS}	D+/D– crossover voltage	1.3	–	2.0	V	–

DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 10. 5 V DC Analog Output Buffer Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
C_L	Load Capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (absolute value)	–	3	12	mV	–
TCV_{OSOB}	Average input offset voltage drift	–	+6	–	μV/°C	–
V_{CMOB}	Common mode input voltage range	0.5	–	V_{DD} – 1.0	V	–
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 0.6 0.6	 – –	 W W	–
$V_{OHIGHOB}$	High output voltage swing (Load = 32 ohms to V_{DD}/2) Power = low Power = high	 0.5 × V_{DD} + 1.1 0.5 × V_{DD} + 1.1	 – –	 – –	 V V	–
V_{OLOWOB}	Low output voltage swing (Load = 32 ohms to V_{DD}/2) Power = low Power = high	 – –	 – –	 0.5 × V_{DD} – 1.3 0.5 × V_{DD} – 1.3	 V V	–
I_{SOB}	Supply current including bias cell (no load) Power = low Power = high	 – –	 1.1 2.6	 5.1 8.8	 mA mA	–
$PSRR_{OB}$	Supply voltage rejection ratio	53	64	–	dB	(0.5 × V_{DD} – 1.3) ≤ V_{OUT} ≤ (V_{DD} – 2.3).

Table 11. 3.3 V DC Analog Output Buffer Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
C_L	Load Capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (absolute value)	–	3	12	mV	–
TCV_{OSOB}	Average input offset voltage drift	–	+6	–	μV/°C	–
V_{CMOB}	Common mode input voltage range	0.5	-	V_{DD} – 1.0	V	–
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 1 1	 – –	 W W	–
$V_{OHIGHOB}$	High output voltage swing (Load = 1 KΩ to V_{DD}/2) Power = low Power = high	 0.5 × V_{DD} + 1.0 0.5 × V_{DD} + 1.0	 – –	 – –	 V V	–
V_{OLOWOB}	Low output voltage swing (Load = 1 KΩ to V_{DD}/2) Power = low Power = high	 – –	 – –	 0.5 × V_{DD} – 1.0 0.5 × V_{DD} – 1.0	 V V	–
I_{SOB}	Supply current including bias cell (no load) Power = low Power = high	 –	 0.8 2.0	 2.0 4.3	 mA mA	–
$PSRR_{OB}$	Supply voltage rejection ratio	34	64	–	dB	(0.5 × V_{DD} – 1.0) ≤ V_{OUT} ≤ (0.5 × V_{DD} + 0.9).

DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The guaranteed specifications are measured through the analog continuous time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Table 12. 5-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	V_{DD}/2 + Bandgap	V_{DD}/2 + 1.229	V_{DD}/2 + 1.290	V_{DD}/2 + 1.346	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.038	V_{DD}/2	V_{DD}/2 + 0.040	V
		V_{REFLO}	Ref Low	V_{DD}/2 – Bandgap	V_{DD}/2 – 1.356	V_{DD}/2 – 1.295	V_{DD}/2 – 1.218	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	V_{DD}/2 + Bandgap	V_{DD}/2 + 1.220	V_{DD}/2 + 1.292	V_{DD}/2 + 1.348	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.036	V_{DD}/2	V_{DD}/2 + 0.036	V
		V_{REFLO}	Ref Low	V_{DD}/2 – Bandgap	V_{DD}/2 – 1.357	V_{DD}/2 – 1.297	V_{DD}/2 – 1.225	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	V_{DD}/2 + Bandgap	V_{DD}/2 + 1.221	V_{DD}/2 + 1.293	V_{DD}/2 + 1.351	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.036	V_{DD}/2	V_{DD}/2 + 0.036	V
		V_{REFLO}	Ref Low	V_{DD}/2 – Bandgap	V_{DD}/2 – 1.357	V_{DD}/2 – 1.298	V_{DD}/2 – 1.228	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	V_{DD}/2 + Bandgap	V_{DD}/2 + 1.219	V_{DD}/2 + 1.293	V_{DD}/2 + 1.353	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.037	V_{DD}/2 – 0.001	V_{DD}/2 + 0.036	V
		V_{REFLO}	Ref Low	V_{DD}/2 – Bandgap	V_{DD}/2 – 1.359	V_{DD}/2 – 1.299	V_{DD}/2 – 1.229	V
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.092	P2[4] + P2[6] – 0.011	P2[4] + P2[6] + 0.064	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.031	P2[4] – P2[6] + 0.007	P2[4] – P2[6] + 0.056	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.078	P2[4] + P2[6] – 0.008	P2[4] + P2[6] + 0.063	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.031	P2[4] – P2[6] + 0.004	P2[4] – P2[6] + 0.043	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.006	P2[4] + P2[6] + 0.062	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.032	P2[4] – P2[6] + 0.003	P2[4] – P2[6] + 0.038	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.006	P2[4] + P2[6] + 0.062	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.034	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.037	V

Table 12. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b010	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.037	V_{DD} – 0.007	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.036	V_{DD}/2 – 0.001	V_{DD}/2 + 0.036	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.029	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.034	V_{DD} – 0.006	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.036	V_{DD}/2 – 0.001	V_{DD}/2 + 0.035	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.024	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.032	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.036	V_{DD}/2 – 0.001	V_{DD}/2 + 0.035	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.022	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.031	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.037	V_{DD}/2 – 0.001	V_{DD}/2 + 0.035	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.020	V
0b011	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	3 × Bandgap	3.760	3.884	4.006	V
		V_{AGND}	AGND	2 × Bandgap	2.522	2.593	2.669	V
		V_{REFLO}	Ref Low	Bandgap	1.252	1.299	1.342	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	3 × Bandgap	3.766	3.887	4.010	V
		V_{AGND}	AGND	2 × Bandgap	2.523	2.594	2.670	V
		V_{REFLO}	Ref Low	Bandgap	1.252	1.297	1.342	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	3 × Bandgap	3.769	3.888	4.013	V
		V_{AGND}	AGND	2 × Bandgap	2.523	2.594	2.671	V
		V_{REFLO}	Ref Low	Bandgap	1.251	1.296	1.343	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	3 × Bandgap	3.769	3.889	4.015	V
		V_{AGND}	AGND	2 × Bandgap	2.523	2.595	2.671	V
		V_{REFLO}	Ref Low	Bandgap	1.251	1.296	1.344	V
0b100	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.483 – P2[6]	2.582 – P2[6]	2.674 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.522	2.593	2.669	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.524 – P2[6]	2.600 – P2[6]	2.676 – P2[6]	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.490 – P2[6]	2.586 – P2[6]	2.679 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.523	2.594	2.669	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.523 – P2[6]	2.598 – P2[6]	2.675 – P2[6]	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.493 – P2[6]	2.588 – P2[6]	2.682 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.523	2.594	2.670	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.523 – P2[6]	2.597 – P2[6]	2.675 – P2[6]	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.494 – P2[6]	2.589 – P2[6]	2.685 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.523	2.595	2.671	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.522 – P2[6]	2.596 – P2[6]	2.676 – P2[6]	V

Table 12. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b101	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.218	P2[4] + 1.291	P2[4] + 1.354	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.335	P2[4] – 1.294	P2[4] – 1.237	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.221	P2[4] + 1.293	P2[4] + 1.358	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.337	P2[4] – 1.297	P2[4] – 1.243	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.222	P2[4] + 1.294	P2[4] + 1.360	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.338	P2[4] – 1.298	P2[4] – 1.245	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.221	P2[4] + 1.294	P2[4] + 1.362	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.340	P2[4] – 1.298	P2[4] – 1.245	V
0b110	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.513	2.593	2.672	V
		V_{AGND}	AGND	Bandgap	1.264	1.302	1.340	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.008	V_{SS} + 0.038	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.514	2.593	2.674	V
		V_{AGND}	AGND	Bandgap	1.264	1.301	1.340	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.028	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.514	2.593	2.676	V
		V_{AGND}	AGND	Bandgap	1.264	1.301	1.340	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.024	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.514	2.593	2.677	V
		V_{AGND}	AGND	Bandgap	1.264	1.300	1.340	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.021	V
0b111	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	3.2 × Bandgap	4.028	4.144	4.242	V
		V_{AGND}	AGND	1.6 × Bandgap	2.028	2.076	2.125	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.008	V_{SS} + 0.034	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	3.2 × Bandgap	4.032	4.142	4.245	V
		V_{AGND}	AGND	1.6 × Bandgap	2.029	2.076	2.126	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.025	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	3.2 × Bandgap	4.034	4.143	4.247	V
		V_{AGND}	AGND	1.6 × Bandgap	2.029	2.076	2.126	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.021	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	3.2 × Bandgap	4.036	4.144	4.249	V
		V_{AGND}	AGND	1.6 × Bandgap	2.029	2.076	2.126	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.019	V

Table 13. 3.3-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.200	$V_{DD}/2$ + 1.290	$V_{DD}/2$ + 1.365	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.030	$V_{DD}/2$	$V_{DD}/2$ + 0.034	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.346	$V_{DD}/2$ – 1.292	$V_{DD}/2$ – 1.208	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.196	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.374	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.029	$V_{DD}/2$	$V_{DD}/2$ + 0.031	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.349	$V_{DD}/2$ – 1.295	$V_{DD}/2$ – 1.227	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.204	$V_{DD}/2$ + 1.293	$V_{DD}/2$ + 1.369	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.030	$V_{DD}/2$	$V_{DD}/2$ + 0.030	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.351	$V_{DD}/2$ – 1.297	$V_{DD}/2$ – 1.229	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.189	$V_{DD}/2$ + 1.294	$V_{DD}/2$ + 1.384	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.032	$V_{DD}/2$	$V_{DD}/2$ + 0.029	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.353	$V_{DD}/2$ – 1.297	$V_{DD}/2$ – 1.230	V
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.105	P2[4] + P2[6] – 0.008	P2[4] + P2[6] + 0.095	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.035	P2[4] – P2[6] + 0.006	P2[4] – P2[6] + 0.053	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.094	P2[4] + P2[6] – 0.005	P2[4] + P2[6] + 0.073	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.033	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.042	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.094	P2[4] + P2[6] – 0.003	P2[4] + P2[6] + 0.075	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.035	P2[4] – P2[6]	P2[4] – P2[6] + 0.038	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.095	P2[4] + P2[6] – 0.003	P2[4] + P2[6] + 0.080	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.038	P2[4] – P2[6]	P2[4] – P2[6] + 0.038	V
0b010	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.119	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.028	$V_{DD}/2$	$V_{DD}/2$ + 0.029	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.022	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.131	V_{DD} – 0.004	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.028	$V_{DD}/2$	$V_{DD}/2$ + 0.028	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.021	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.111	V_{DD} – 0.003	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.029	$V_{DD}/2$	$V_{DD}/2$ + 0.028	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.017	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.128	V_{DD} – 0.003	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.029	$V_{DD}/2$	$V_{DD}/2$ + 0.029	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.019	V
0b011	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–

Table 13. 3.3-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b100	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–
0b101	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.214	P2[4] + 1.291	P2[4] + 1.359	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.335	P2[4] – 1.292	P2[4] – 1.200	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.219	P2[4] + 1.293	P2[4] + 1.357	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.335	P2[4] – 1.295	P2[4] – 1.243	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.222	P2[4] + 1.294	P2[4] + 1.356	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.337	P2[4] – 1.296	P2[4] – 1.244	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.224	P2[4] + 1.295	P2[4] + 1.355	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.339	P2[4] – 1.297	P2[4] – 1.244	V
0b110	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.510	2.595	2.655	V
		V_{AGND}	AGND	Bandgap	1.276	1.301	1.332	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.031	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.513	2.594	2.656	V
		V_{AGND}	AGND	Bandgap	1.275	1.301	1.331	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.021	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.516	2.595	2.657	V
		V_{AGND}	AGND	Bandgap	1.275	1.301	1.331	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.017	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.520	2.595	2.658	V
		V_{AGND}	AGND	Bandgap	1.275	1.300	1.331	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.015	V
0b111	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–

DC Analog enCoRe III Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C $\leq T_A \leq$ 85 °C, or 3.15 V to 3.5 V and –40 °C $\leq T_A \leq$ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 14. DC Analog enCoRe III Block Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
R_{CT}	Resistor unit value (CT)	–	12.2	–	kΩ	–
C_{SC}	Capacitor unit value (SC)	–	80	–	fF	–

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the *PSoC®* *Technical Reference Manual* for more information on the VLT_CR register.

Table 15. DC POR and LVD Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
 V_{PPOR0R} [5] V_{PPOR1R} [5] V_{PPOR2R} [5]	V_{DD} value for PPOR trip (positive ramp) PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	–	 2.91 4.39 4.55	–	 V V V	–
 V_{PPOR0} V_{PPOR1} V_{PPOR2}	V_{DD} value for PPOR trip (negative ramp) PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	–	 2.82 4.39 4.55	–	 V V V	–
 V_{PH0} V_{PH1} V_{PH2}	PPOR hysteresis PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	 – – –	 92 0 0	 – – –	 mV mV mV	–
 V_{LVD0} V_{LVD1} V_{LVD2} V_{LVD3} V_{LVD4} V_{LVD5} V_{LVD6} V_{LVD7}	V_{DD} value for LVD trip VM[2:0] = 000b VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b	 2.86 2.96 3.07 3.92 4.39 4.55 4.63 4.72	 2.92 3.02 3.13 4.00 4.48 4.64 4.73 4.81	 2.98[6] 3.08 3.20 4.08 4.57 4.74[7] 4.82 4.91	 V V V V V V V V	–

Notes

5. Errata: When VDD of the device is pulled below ground just before power on, the first read from each 8K Flash page may be corrupted. This issue does not affect Flash page 0 because it is the selected page upon reset. For more details in Errata on page 40.
6. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
7. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C $\leq T_A \leq$ 85 °C, or 3.15 V to 3.5 V and –40 °C $\leq T_A \leq$ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 16. DC Programming Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5.0	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	3.0	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation	3.15	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	15	30	mA	–
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	–
V_{IHP}	Input high voltage during programming or Verify	2.1	–	–	V	–
I_{ILP}	Input current when applying Vilp to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input current when applying Vihp to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	–
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	–
$Flash_{ENPB}$	Flash endurance (per block)	50,000[8]	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total)[9]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention	10	–	–	Years	–

DC I^2C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C $\leq T_A \leq$ 85 °C, or 3.15 V to 3.5 V and –40 °C $\leq T_A \leq$ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 17. DC I^2C Specifications [10]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	3.15 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	3.15 V ≤ V_{DD} ≤ 5.25 V

Notes

8. The 50,000 cycle Flash endurance per block will only be guaranteed if the Flash is operating within one voltage range. Voltage ranges are 3.0V to 3.6V and 4.75V to 5.25V.
9. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs application note AN2015 for more information.
10. All GPIOs meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I^2C GPIO pins also meet the mentioned specifications.

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 18. AC Chip-Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
$F_{IMO245V}$	IMO frequency for 24 MHz (5 V)	23.04	24	24.96[11, 12]	MHz	Trimmed for 5 V operation using factory trim values.
$F_{IMO243V}$	IMO frequency for 24 MHz (3.3 V)	22.08	24	25.92[11,13]	MHz	Trimmed for 3.3 V operation using factory trim values.
F_{IMOUSB}	IMO frequency with USB frequency locking enabled and USB traffic present	23.94	24	24.06[12]	MHz	USB operation for system clock source from the IMO is limited to 0°C ≤ T_A ≤ 70°C.
F_{CPU1}	CPU frequency (5 V nominal)	0.090	24	24.96[11,12]	MHz	SLIMO mode = 0.
F_{CPU2}	CPU frequency (3.3 V nominal)	0.086	12	12.96[12,13]	MHz	SLIMO mode = 0.
F_{BLK5}	Digital PSoC block frequency (5 V nominal)	0	48	49.92[11,12,14]	MHz	Refer to the AC Digital Block Specifications on page 26.
F_{BLK3}	Digital PSoC block frequency (3.3 V nominal)	0	24	25.92[12,14]	MHz	–
F_{32K1}	ILO frequency	15	32	64	kHz	–
F_{32K_U}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing.
DC_{ILO}	ILO duty cycle	20	50	80	%	–
DC_{24M}	24-MHz duty cycle	40	50	60	%	–
Step24M	24-MH trim step size	–	50	–	kHz	–
Fout48M	48-MHz output frequency	46.08	48.0	49.92[11,13]	MHz	Trimmed. Utilizing factory trim values.
F_{MAX}	Maximum frequency of signal on row input or row output	–	–	12.96	MHz	–
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	–
$T_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	–
T_{jit_IMO}[15]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	1200	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	900	6000	ps	N = 32.
	24 MHz IMO period jitter (RMS)	–	200	900	ps	

Notes
11. 4.75 V < V_{DD} < 5.25 V.
12. Accuracy derived from Internal Main Oscillator with appropriate trim for V_{DD} range.
13. 3.0 V < V_{DD} < 3.6 V. See application note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3 V.
14. See the individual user module data sheets for information on maximum frequencies for user modules.
15. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

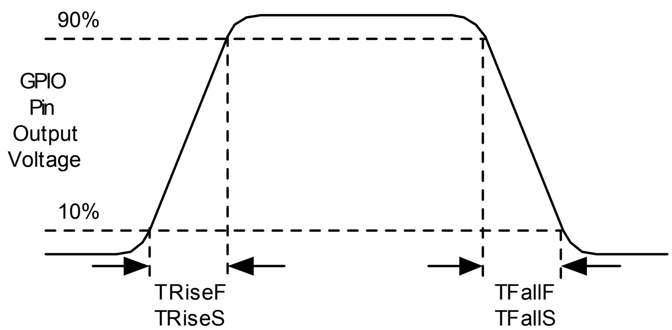
AC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 19. AC GPIO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
F_{GPIO}	GPIO operating frequency	0	–	12	MHz	Normal Strong Mode
TRiseF	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10%–90%
TFallF	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10%–90%
TRiseS	Rise time, slow strong mode, Cload = 50 pF	10	27	–	ns	V_{DD} = 3 to 5.25 V, 10%–90%
TFallS	Fall time, slow strong mode, Cload = 50 pF	10	22	–	ns	V_{DD} = 3 to 5.25 V, 10%–90%

Figure 6. GPIO Timing Diagram



AC Full Speed USB Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 20. AC Full-Speed (12 Mbps) USB Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{RFS}	Transition rise time	4	–	20	ns	For 50-pF load.
T_{FSS}	Transition fall time	4	–	20	ns	For 50-pF load.
T_{RFMFS}	Rise/fall time matching: (T_R/T_F)	90	–	111	%	For 50-pF load.
$T_{DRATEFS}$	Full-speed data rate	12 – 0.25%	12	12 + 0.25%	Mbps	–