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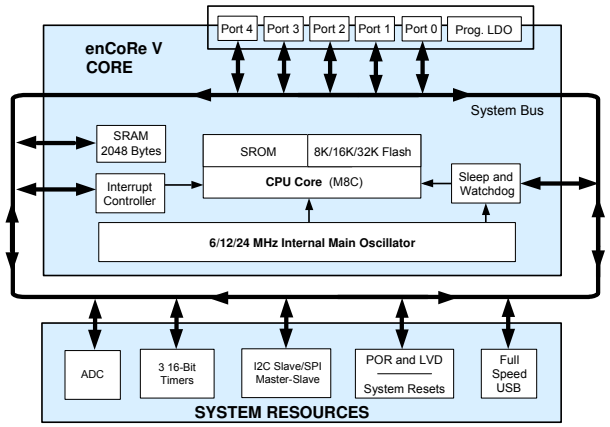
CY7C6431x
CY7C6434x
CY7C6435x

enCoRe™ V Full Speed USB Controller

Features

- Powerful Harvard-architecture processor
  - M8C processor speeds running up to 24 MHz
  - Low power at high processing speeds
  - Interrupt controller
  - 3.0 V to 5.5 V operating voltage without USB
  - Operating voltage with USB enabled:
    - 3.15 V to 3.45 V when supply voltage is around 3.3 V
    - 4.35 V to 5.25 V when supply voltage is around 5.0 V
  - Commercial temperature range: 0 °C to +70 °C
  - Industrial temperature range: –40 °C to +85 °C
- Flexible on-chip memory
  - Up to 32 KB flash program storage:
    - 50,000 erase and write cycles
    - Flexible protection modes
  - Up to 2048 bytes SRAM data storage
  - In-system serial programming (ISSP)
- Complete development tools
  - Free development tool PSoC Designer™
  - Full-featured, in-circuit emulator and programmer
  - Full-speed emulation
  - Complex breakpoint structure
  - 128-KB trace memory
- Precision, programmable clocking
  - Crystal-less oscillator with support for an external crystal or resonator
  - Internal ±5.0% 6, 12, or 24 MHz main oscillator (IMO):
    - 0.25% accuracy with oscillator lock to USB data, no external components required
    - Internal low-speed oscillator (ILO) at 32 kHz for watchdog and sleep. The frequency range is 19 to 50 kHz with a 32-kHz typical value
- Programmable pin configurations
  - Up to 36 general purpose I/O (GPIO) depending on package.
  - 25 mA sink current on all GPIO
    - 60mA total sink current on Even port pins and 60 mA total sink current on Odd port pins
    - 120 mA total sink current on all GPIOs
  - Pull-up, High Z, open drain, CMOS drive modes on all GPIO
  - CMOS drive mode A -5 mA source current on ports 0 and 1 and 1 mA on ports 2, 3, and 4
    - 20 mA total source current on all GPIOs
  - Low dropout voltage regulator for Port 1 pins:
    - Programmable to output 3.0, 2.5, or 1.8 V
  - Selectable, regulated digital I/O on Port 1
  - Configurable input threshold for Port 1
  - Hot-swappable Capability on Port 1
- Full-Speed USB (12 Mbps)
  - Eight unidirectional endpoints
  - One bidirectional control endpoint
  - USB 2.0-compliant: TID# 40000893
  - Dedicated 512 bytes buffer
  - No external crystal required
- Additional system resources
  - Configurable communication speeds
  - I^2C slave:
    - Selectable to 50 kHz, 100 kHz, or 400 kHz
    - Implementation requires no clock stretching
    - Implementation during sleep modes with less than 100 µA
    - Hardware address detection
  - SPI master and SPI slave:
    - Configurable between 46.9 kHz and 12 MHz
  - Three 16-bit timers
  - 10-bit ADC used to monitor battery voltage or other signals with external components
  - Watchdog and sleep timers
  - Integrated supervisory circuit

enCoRe V Block Diagram



Errata: For information on silicon errata, see "Errata" on page 35. Details include trigger conditions, devices affected, and proposed workaround.

Contents

Functional Overview

The enCoRe V family of devices are designed to replace multiple traditional full-speed USB microcontroller system components with one, low cost single-chip programmable component. Communication peripherals (I^2C/SPI), a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as illustrated in the enCoRe V Block Diagram on page 1, consists of two main areas: the CPU core and the system resources. Depending on the enCoRe V package, up to 36 GPIO are also included.

This product is an enhanced version of Cypress's successful full speed-USB peripheral controllers. Enhancements include faster CPU at lower voltage operation, lower current consumption, twice the RAM and Flash, hot-swappable I/Os, I^2C hardware address recognition, new very low current sleep mode, and new package options.

The enCoRe V Core

The enCoRe V Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO and ILO. The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a four-MIPS, 8-bit Harvard architecture microprocessor.

During USB operation, the CPU speed can be set to any setting. Be aware that USB throughput decreases with a decrease in CPU speed. For maximum throughput, the CPU clock should be made equal to the system clock. The system clock must be 24 MHz for USB operation.

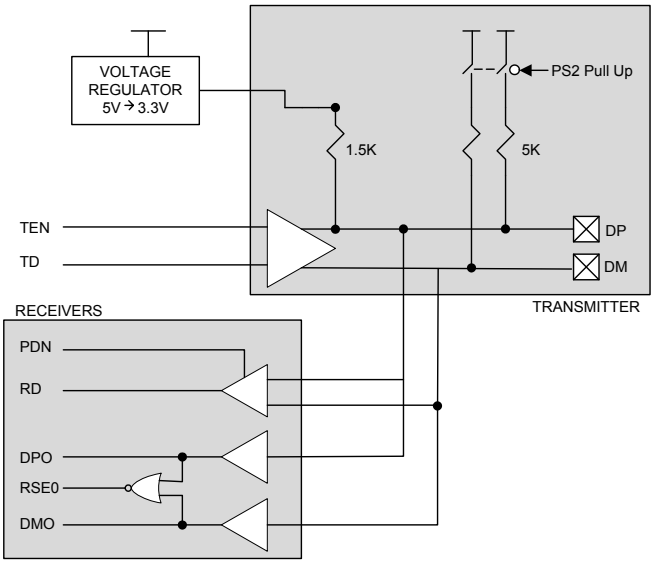
System resources provide additional capability, such as a configurable I^2C slave and SPI master-slave communication interface and various system resets supported by the M8C.

Full-Speed USB

The enCoRe V USB system resource adheres to the USB 2.0 Specification for full speed devices operating at 12 Mb/second with one upstream port and one USB address. enCoRe V USB consists of these components:

- Serial interface engine (SIE) block.
- PSoC memory arbiter (PMA) block.
- 512 bytes of dedicated SRAM.
- A full-speed USB Transceiver with internal regulator and two dedicated USB pins.

Figure 1. USB Transceiver Regulator



At the enCoRe V system level, the full-speed USB system resource interfaces to the rest of the enCoRe V by way of the M8C's register access instructions and to the outside world by way of the two USB pins. The SIE supports nine endpoints including a bidirectional control endpoint (endpoint 0) and eight unidirectional data endpoints (endpoints 1 to 8). The unidirectional data endpoints are individually configurable as either IN or OUT.

Low value series resistors R_{EXT} (22 Ω) must be added externally to the D+ and D– lines to meet the driving impedance requirement for full-speed USB.

The USB Serial Interface Engine (SIE) allows the enCoRe V device to communicate with the USB host at full speed data rates (12 Mb/s). The SIE simplifies the interface to USB traffic by automatically handling the following USB processing tasks without firmware intervention:

- Translates the encoded received data and formats the data to be transmitted on the bus.
- Generates and checks cyclical redundancy checks (CRCs). Incoming packets failing checksum verification are ignored.
- Checks addresses. Ignores all transactions not addressed to the device.
- Sends appropriate ACK/NAK/Stall handshakes.
- Identifies token type (SETUP, IN, OUT) and sets the appropriate token bit once a valid token in received.
- Identifies Start-of-Frame (SOF) and saves the frame count.
- Sends data to or retrieves data from the USB SRAM, by way of the PSoC Memory Arbiter (PMA).

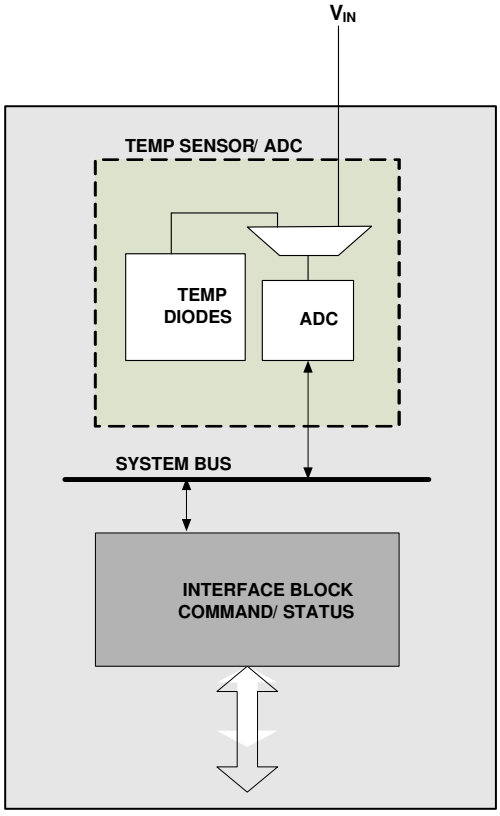
Firmware is required to handle various parts of the USB interface. The SIE issues interrupts after key USB events to direct firmware to appropriate tasks:

- Fill and empty the USB data buffers in USB SRAM.
- Enable PMA channels appropriately.
- Coordinate enumeration by decoding USB device requests.
- Suspend and resume coordination.
- Verify and select data toggle values.

10-bit ADC

The ADC on enCoRe V device is an independent block with a state machine interface to control accesses to the block. The ADC is housed together with the temperature sensor core and can be connected to this or the Analog mux bus. As a default operation, the ADC is connected to the temperature sensor diodes to give digital values of the temperature.

Figure 2. ADC System Performance Block Diagram



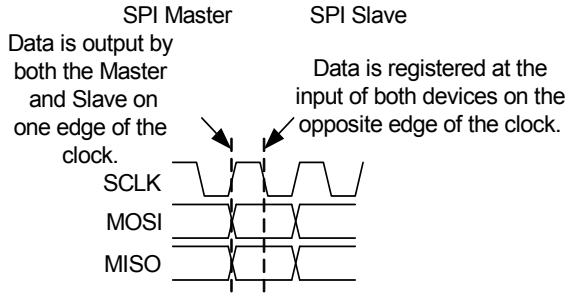
The ADC User Module contains an integrator block and one comparator with positive and negative input set by the MUXes. The input to the integrator stage comes from the analog global input mux or the temperature sensor with an input voltage range of 0 V to V_{REFADC}.

In the ADC only configuration (the ADC MUX selects the Analog mux bus, not the default temperature sensor connection), an external voltage can be connected to the input of the modulator for voltage conversion. The ADC is run for a number of cycles set by the timer, depending upon the desired resolution of the ADC. A counter counts the number of trips by the comparator, which is proportional to the input voltage. The Temp Sensor block clock speed is 36 MHz and is divided down to 1 to 12 MHz for ADC operation.

SPI

The serial peripheral interconnect (SPI) 3-wire protocol uses both edges of the clock to enable synchronous communication without the need for stringent setup and hold requirements.

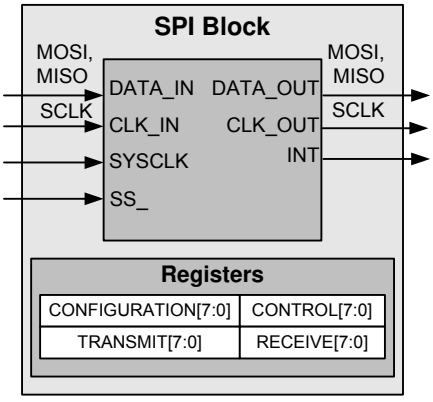
Figure 3. Basic SPI Configuration



A device can be a master or slave. A master outputs clock and data to the slave device and inputs slave data. A slave device inputs clock and data from the master device and outputs data for input to the master. Together, the master and slave are essentially a circular Shift register, where the master generates the clocking and initiates data transfers.

A basic data transfer occurs when the master sends eight bits of data, along with eight clocks. In any transfer, both master and slave transmit and receive simultaneously. If the master only sends data, the received data from the slave is ignored. If the master wishes to receive data from the slave, the master must send dummy bytes to generate the clocking for the slave to send data back.

Figure 4. SPI Block Diagram



SPI configuration register (SPI_CFG) sets master/slave functionality, clock speed, and interrupt select. SPI control register (SPI_CR) provides four control bits and four status bits for device interfacing and synchronization.

The SPIM hardware has no support for driving the Slave Select (SS_) signal. The behavior and use of this signal is dependent on the application and enCoRe V device and, if required, must be implemented in firmware.

There is an additional data input in the SPIS, Slave Select (SS_), which is an active low signal. SS_ must be asserted to enable the SPIS to receive and transmit. SS_ has two high level functions:

- To allow for the selection of a given slave in a multi-slave environment.
- To provide additional clocking for TX data queuing in SPI modes 0 and 1.

I²C Slave

The I²C slave enhanced communications block is a serial-to-parallel processor, designed to interface the enCoRe V device to a two-wire I²C serial communications bus. To eliminate the need for excessive CPU intervention and overhead, the block provides I²C-specific support for status detection and generation of framing bits. By default, the I²C slave enhanced module is firmware compatible with the previous generation of I²C slave functionality. However, this module provides new features that are configurable to implement significant flexibility for both internal and external interfacing. The basic I²C features include:

- Slave, transmitter, and receiver operation.
- Byte processing for low CPU overhead.
- Interrupt or polling CPU interface.
- Support for clock rates of up to 400 kHz.
- 7- or 10-bit addressing (through firmware support).
- SMBus operation (through firmware support).

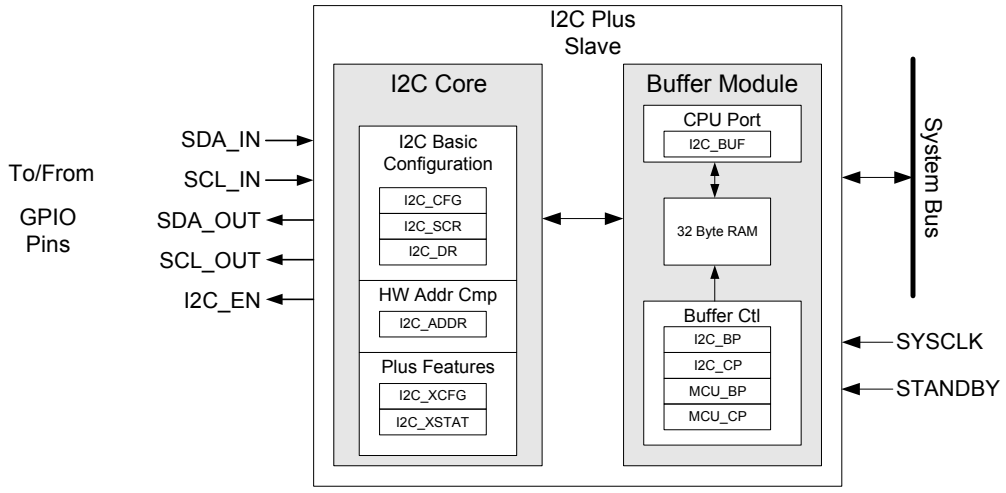
Enhanced features of the I²C Slave Enhanced Module include:

- Support for 7-bit hardware address compare.
- Flexible data buffering schemes.
- A “no bus stalling” operating mode.
- A low power bus monitoring mode.

The I²C block controls the data (SDA) and the clock (SCL) to the external I²C interface through direct connections to two dedicated GPIO pins. When I²C is enabled, these GPIO pins are not available for general purpose use. The enCoRe V CPU firmware interacts with the block through I/O register reads and writes, and firmware synchronization is implemented through polling and/or interrupts.

In the default operating mode, which is firmware compatible with previous versions of I²C slave modules, the I²C bus is stalled upon every received address or byte, and the CPU is required to read the data or supply data as required before the I²C bus continues. However, this I²C Slave Enhanced module provides new data buffering capability as an enhanced feature. In the EZI²C buffering mode, the I²C slave interface appears as a 32-byte RAM buffer to the external I²C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave never stalls the bus. In this protocol, the data available in the RAM (this is managed by the CPU) is valid.

Figure 5. I²C Block Diagram



Additional System Resources

System resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The following statements describe the merits of each system resource.

- Low voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (power on reset) circuit eliminates the need for a system supervisor.
- The 5 V maximum input, 1.8, 2.5, or 3 V selectable output, LDO regulator provides regulation for I/Os. A register controlled bypass mode enables the user to disable the LDO.
- Standard Cypress PSoC IDE tools are available for debugging the enCoRe V family of parts.

Getting Started

The quickest path to understanding the enCoRe V silicon is by reading this data sheet and using the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications. For in-depth information, along with detailed programming information, see the *enCoRe™ V CY7C643xx, enCoRe™ V LV CY7C604xx Technical Reference Manual (TRM)* for this PSoC device.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device data sheets on the web at http://www.cypress.com.

Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs and are available at http://www.cypress.com.

Development Kits

PSoC development kits are available online from Cypress at http://www.cypress.com and through a growing number of regional and global distributors, including Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops) is available online at http://www.cypress.com. The training covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant, go to http://www.cypress.com and look for CYPros Consultants.

Solutions Library

Visit our growing library of solution-focused designs at http://www.cypress.com. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at http://www.cypress.com. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary Integrated Design Environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for a given application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality In-Circuit Emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24-MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select user modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called user modules. User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a Pulse width modulator (PWM) user module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module data sheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

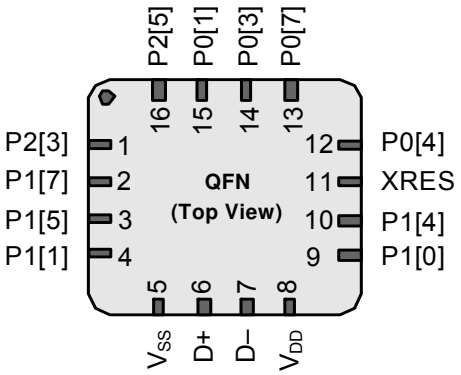
The last step in the development process takes place inside PSoC Designer’s Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

Pin Information

The enCoRe V USB device is available in a variety of packages which are listed and illustrated in the subsequent tables.

16-pin part pinout

Figure 6. CY7C64315/CY7C64316 16-pin enCoRe V USB Device



Pin Definitions

16-pin part pinout (QFN)

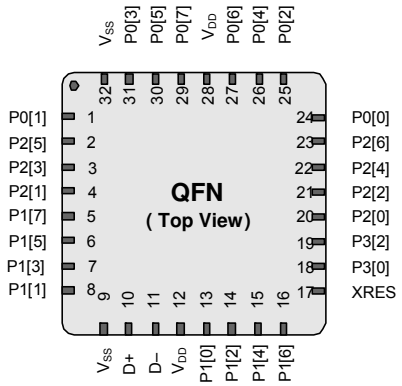
Pin No.	Type	Name	Description
1	I/O	P2[3]	Digital I/O, crystal input (Xin)
2	I/OHR	P1[7]	Digital I/O, SPI SS, I^2C SCL
3	I/OHR	P1[5]	Digital I/O, SPI MISO, I^2C SDA
4	I/OHR	P1[1][1, 2]	Digital I/O, ISSP CLK, I^2C SCL, SPI MOSI
5	Power	V_{SS}	Ground connection
6	USB line	D+	USB PHY
7	USB line	D–	USB PHY
8	Power	V_{DD}	Supply
9	I/OHR	P1[0][1, 2]	Digital I/O, ISSP DATA, I^2C SDA, SPI CLK
10	I/OHR	P1[4]	Digital I/O, optional external clock input (EXTCLK)
11	Input	XRES	Active high external reset with internal pull-down
12	I/OH	P0[4]	Digital I/O
13	I/OH	P0[7]	Digital I/O
14	I/OH	P0[3]	Digital I/O
15	I/OH	P0[1]	Digital I/O
16	I/O	P2[5]	Digital I/O, crystal output (Xout)

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Notes
1. During power up or reset event, device P1[0] and P1[1] may disturb the I^2C bus. Use alternate pins if issues are encountered.
2. These are the in-system serial programming (ISSP) pins that are not High Z at power on reset (POR).

32-pin part pinout

Figure 7. CY7C64343/CY7C64345/CY7C64346 32-pin enCoRe V USB Device



Pin Definitions

32-pin part pinout (QFN)

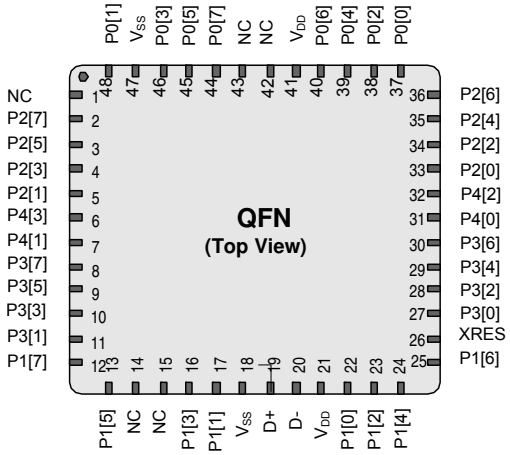
Pin No.	Type	Name	Description
1	I/OH	P0[1]	Digital I/O
2	I/O	P2[5]	Digital I/O, crystal output (Xout)
3	I/O	P2[3]	Digital I/O, crystal Input (Xin)
4	I/O	P2[1]	Digital I/O
5	I/OHR	P1[7]	Digital I/O, I^2C SCL, SPI SS
6	I/OHR	P1[5]	Digital I/O, I^2C SDA, SPI MISO
7	I/OHR	P1[3]	Digital I/O, SPI CLK
8	I/OHR	P1[1][3, 4]	Digital I/O, ISSP CLK, I^2C SCL, SPI MOSI
9	Power	V_{SS}	Ground
10	I/O	D+	USB PHY
11	I/O	D–	USB PHY
12	Power	V_{DD}	Supply voltage
13	I/OHR	P1[0][3, 4]	Digital I/O, ISSP DATA, I^2C SDA, SPI CLK
14	I/OHR	P1[2]	Digital I/O
15	I/OHR	P1[4]	Digital I/O, optional external clock input (EXTCLK)
16	I/OHR	P1[6]	Digital I/O
17	Reset	XRES	Active high external reset with internal pull down
18	I/O	P3[0]	Digital I/O
19	I/O	P3[2]	Digital I/O
20	I/O	P2[0]	Digital I/O
21	I/O	P2[2]	Digital I/O
22	I/O	P2[4]	Digital I/O
23	I/O	P2[6]	Digital I/O
24	I/OH	P0[0]	Digital I/O
25	I/OH	P0[2]	Digital I/O
26	I/OH	P0[4]	Digital I/O
27	I/OH	P0[6]	Digital I/O
28	Power	V_{DD}	Supply voltage
29	I/OH	P0[7]	Digital I/O
30	I/OH	P0[5]	Digital I/O
31	I/OH	P0[3]	Digital I/O
32	Power	V_{SS}	Ground
CP	Power	V_{SS}	Ensure the center pad is connected to ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Notes
3. During power up or reset event, device P1[0] and P1[1] may disturb the I^2C bus. Use alternate pins if issues are encountered.
4. These are the in-system serial programming (ISSP) pins that are not High Z at power on reset (POR).

48-pin Part Pinout

Figure 8. CY7C64355/CY7C64356 48-pin enCoRe V USB Device



Pin Definitions

48-pin Part Pinout (QFN)

Pin No.	Type	Pin Name	Description
1	NC	NC	No connection
2	I/O	P2[7]	Digital I/O
3	I/O	P2[5]	Digital I/O, crystal out (Xout)
4	I/O	P2[3]	Digital I/O, crystal in (Xin)
5	I/O	P2[1]	Digital I/O
6	I/O	P4[3]	Digital I/O
7	I/O	P4[1]	Digital I/O
8	I/O	P3[7]	Digital I/O
9	I/O	P3[5]	Digital I/O
10	I/O	P3[3]	Digital I/O
11	I/O	P3[1]	Digital I/O
12	I/OHR	P1[7]	Digital I/O, I^2C SCL, SPI SS
13	I/OHR	P1[5]	Digital I/O, I^2C SDA, SPI MISO
14	NC	NC	No connection
15	NC	NC	No connection
16	I/OHR	P1[3]	Digital I/O, SPI CLK
17	I/OHR	P1[1][5, 6]	Digital I/O, ISSP CLK, I^2C SCL, SPI MOSI
18	Power	V_{SS}	Supply ground
19	I/O	D+	USB
20	I/O	D–	USB
21	Power	V_{DD}	Supply voltage
22	I/OHR	P1[0][5, 6]	Digital I/O, ISSP DATA, I^2C SDA, SPI CLK
23	I/OHR	P1[2]	Digital I/O

Notes
5. During power up or reset event, device P1[0] and P1[1] may disturb the I^2C bus. Use alternate pins if issues are encountered.
6. These are the in-system serial programming (ISSP) pins that are not High Z at power on reset (POR).

Pin Definitions

48-pin Part Pinout (QFN)

Pin No.	Type	Pin Name	Description
24	I/OHR	P1[4]	Digital I/O, optional external clock input (EXTCLK)
25	I/OHR	P1[6]	Digital I/O
26	XRES	Ext Reset	Active high external reset with internal pull down
27	I/O	P3[0]	Digital I/O
28	I/O	P3[2]	Digital I/O
29	I/O	P3[4]	Digital I/O
30	I/O	P3[6]	Digital I/O
31	I/O	P4[0]	Digital I/O
32	I/O	P4[2]	Digital I/O
33	I/O	P2[0]	Digital I/O
34	I/O	P2[2]	Digital I/O
35	I/O	P2[4]	Digital I/O
36	I/O	P2[6]	Digital I/O
37	I/OH	P0[0]	Digital I/O
38	I/OH	P0[2]	Digital I/O
39	I/OH	P0[4]	Digital I/O
40	I/OH	P0[6]	Digital I/O
41	Power	V_{DD}	Supply voltage
42	NC	NC	No connection
43	NC	NC	No connection
44	I/OH	P0[7]	Digital I/O
45	I/OH	P0[5]	Digital I/O
46	I/OH	P0[3]	Digital I/O
47	Power	V_{SS}	Supply ground
48	I/OH	P0[1]	Digital I/O
CP	Power	V_{SS}	Ensure the center pad is connected to ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Register Reference

The section discusses the registers of the enCoRe V device. It lists all the registers in mapping tables, in address order.

Register Conventions

The register conventions specific to this section are listed in the following table.

Table 1. Register Conventions

Convention	Description
R	Read register or bits
W	Write register or bits
L	Logical register or bits
C	Clearable register or bits
#	Access is bit specific

Register Mapping Tables

The enCoRe V device has a total register address space of 512 bytes. The register space is also referred to as I/O space and is broken into two parts: Bank 0 (user space) and Bank 1 (configuration space). The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set, the user is said to be in the “extended” address space or the “configuration” registers.

Table 2. Register Map Bank 0 Table: User Space

Name	Addr (0, Hex)	Access	Name	Addr (0, Hex)	Access	Name	Addr (0, Hex)	Access	Name	Addr (0, Hex)	Access
PRT0DR	00	RW	EP1_CNT0	40	#		80			C0	
PRT0IE	01	RW	EP1_CNT1	41	RW		81			C1	
	02		EP2_CNT0	42	#		82			C2	
	03		EP2_CNT1	43	RW		83			C3	
PRT1DR	04	RW	EP3_CNT0	44	#		84			C4	
PRT1IE	05	RW	EP3_CNT1	45	RW		85			C5	
	06		EP4_CNT0	46	#		86			C6	
	07		EP4_CNT1	47	RW		87			C7	
PRT2DR	08	RW	EP5_CNT0	48	#		88		I2C_XCFG	C8	RW
PRT2IE	09	RW	EP5_CNT1	49	RW		89		I2C_XSTAT	C9	R
	0A		EP6_CNT0	4A	#		8A		I2C_ADDR	CA	RW
	0B		EP6_CNT1	4B	RW		8B		I2C_BP	CB	R
PRT3DR	0C	RW	EP7_CNT0	4C	#		8C		I2C_CP	CC	R
PRT3IE	0D	RW	EP7_CNT1	4D	RW		8D		CPU_BP	CD	RW
	0E		EP8_CNT0	4E	#		8E		CPU_CP	CE	R
	0F		EP8_CNT1	4F	RW		8F		I2C_BUF	CF	RW
PRT4DR	10	RW		50			90		CUR_PP	D0	RW
PRT4IE	11	RW		51			91		STK_PP	D1	RW
	12			52			92			D2	
	13			53			93		IDX_PP	D3	RW
	14			54			94		MVR_PP	D4	RW
	15			55			95		MVW_PP	D5	RW
	16			56			96		I2C_CFG	D6	RW
	17			57			97		I2C_SCR	D7	#
	18		PMA0_DR	58	RW		98		I2C_DR	D8	RW
	19		PMA1_DR	59	RW		99			D9	
	1A		PMA2_DR	5A	RW		9A		INT_CLR0	DA	RW
	1B		PMA3_DR	5B	RW		9B		INT_CLR1	DB	RW
	1C		PMA4_DR	5C	RW		9C		INT_CLR2	DC	RW
	1D		PMA5_DR	5D	RW		9D			DD	
	1E		PMA6_DR	5E	RW		9E		INT_MSK2	DE	RW
	1F		PMA7_DR	5F	RW		9F		INT_MSK1	DF	RW
	20			60			A0		INT_MSK0	E0	RW
	21			61			A1		INT_SW_EN	E1	RW
	22			62			A2		INT_VC	E2	RC
	23			63			A3		RES_WDT	E3	W
	24		PMA8_DR	64	RW		A4			E4	
	25		PMA9_DR	65	RW		A5			E5	
	26		PMA10_DR	66	RW		A6			E6	
	27		PMA11_DR	67	RW		A7			E7	
	28		PMA12_DR	68	RW		A8			E8	
SPI_TXR	29	W	PMA13_DR	69	RW		A9			E9	
SPI_RXR	2A	R	PMA14_DR	6A	RW		AA			EA	
SPI_CR	2B	#	PMA15_DR	6B	RW		AB			EB	
	2C		TMP_DR0	6C	RW		AC			EC	
	2D		TMP_DR1	6D	RW		AD			ED	
	2E		TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30			70		PT0_CFG	B0	RW		F0	
USB_SOF0	31	R		71		PT0_DATA1	B1	RW		F1	
USB_SOF1	32	R		72		PT0_DATA0	B2	RW		F2	
USB_CR0	33	RW		73		PT1_CFG	B3	RW		F3	
USBIO_CR0	34	#		74		PT1_DATA1	B4	RW		F4	
USBIO_CR1	35	#		75		PT1_DATA0	B5	RW		F5	
EP0_CR	36	#		76		PT2_CFG	B6	RW		F6	
EP0_CNT0	37	#		77		PT2_DATA1	B7	RW	CPU_F	F7	RL
EP0_DR0	38	RW		78		PT2_DATA0	B8	RW		F8	
EP0_DR1	39	RW		79			B9			F9	
EP0_DR2	3A	RW		7A			BA			FA	
EP0_DR3	3B	RW		7B			BB			FB	
EP0_DR4	3C	RW		7C			BC			FC	
EP0_DR5	3D	RW		7D			BD			FD	
EP0_DR6	3E	RW		7E			BE		CPU_SCR1	FE	#
EP0_DR7	3F	RW		7F			BF		CPU_SCR0	FF	#

Gray fields are reserved; do not access these fields. # Access is bit specific.

Table 3. Register Map Bank 1 Table: Configuration Space

Name	Addr (1, Hex)	Access	Name	Addr (1, Hex)	Access	Name	Addr (1, Hex)	Access	Name	Addr (1, Hex)	Access
PRT0DM0	00	RW	PMA4_RA	40	RW		80			C0	
PRT0DM1	01	RW	PMA5_RA	41	RW		81			C1	
	02		PMA6_RA	42	RW		82			C2	
	03		PMA7_RA	43	RW		83			C3	
PRT1DM0	04	RW	PMA8_WA	44	RW		84			C4	
PRT1DM1	05	RW	PMA9_WA	45	RW		85			C5	
	06		PMA10_WA	46	RW		86			C6	
	07		PMA11_WA	47	RW		87			C7	
PRT2DM0	08	RW	PMA12_WA	48	RW		88			C8	
PRT2DM1	09	RW	PMA13_WA	49	RW		89			C9	
	0A		PMA14_WA	4A	RW		8A			CA	
	0B		PMA15_WA	4B	RW		8B			CB	
PRT3DM0	0C	RW	PMA8_RA	4C	RW		8C			CC	
PRT3DM1	0D	RW	PMA9_RA	4D	RW		8D			CD	
	0E		PMA10_RA	4E	RW		8E			CE	
	0F		PMA11_RA	4F	RW		8F			CF	
PRT4DM0	10	RW	PMA12_RA	50	RW		90			D0	
PRT4DM1	11	RW	PMA13_RA	51	RW		91			D1	
	12		PMA14_RA	52	RW		92		ECO_ENBUS	D2	RW
	13		PMA15_RA	53	RW		93		ECO_TRIM	D3	RW
	14		EP1_CR0	54	#		94			D4	
	15		EP2_CR0	55	#		95			D5	
	16		EP3_CR0	56	#		96			D6	
	17		EP4_CR0	57	#		97			D7	
	18		EP5_CR0	58	#		98		MUX_CR0	D8	RW
	19		EP6_CRO	59	#		99		MUX_CR1	D9	RW
	1A		EP7_CR0	5A	#		9A		MUX_CR2	DA	RW
	1B		EP8_CR0	5B	#		9B		MUX_CR3	DB	RW
	1C			5C			9C		IO_CFG1	DC	RW
	1D			5D			9D		OUT_P1	DD	RW
	1E			5E			9E		IO_CFG2	DE	RW
	1F			5F			9F		MUX_CR4	DF	RW
	20			60			A0		OSC_CR0	E0	RW
	21			61			A1		ECO_CFG	E1	#
	22			62			A2		OSC_CR2	E2	RW
	23			63			A3		VLT_CR	E3	RW
	24			64			A4		VLT_CMP	E4	R
	25			65			A5			E5	
	26			66			A6			E6	
	27			67			A7			E7	
	28			68			A8		IMO_TR	E8	W
SPI_CFG	29	RW		69			A9		ILO_TR	E9	W
	2A			6A			AA			EA	
	2B			6B			AB		SLP_CFG	EB	RW
	2C		TMP_DR0	6C	RW		AC		SLP_CFG2	EC	RW
	2D		TMP_DR1	6D	RW		AD		SLP_CFG3	ED	RW
	2E		TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
USB_CR1	30	#		70			B0			F0	
	31			71			B1			F1	
	32			72			B2			F2	
	33			73			B3			F3	
PMA0_WA	34	RW		74			B4			F4	
PMA1_WA	35	RW		75			B5			F5	
PMA2_WA	36	RW		76			B6			F6	
PMA3_WA	37	RW		77			B7		CPU_F	F7	RL
PMA4_WA	38	RW		78			B8			F8	
PMA5_WA	39	RW		79			B9			F9	
PMA6_WA	3A	RW		7A			BA		IMO_TR1	FA	RW
PMA7_WA	3B	RW		7B			BB			FB	
PMA0_RA	3C	RW		7C			BC			FC	
PMA1_RA	3D	RW		7D		USB_MISC_CR	BD	RW		FD	
PMA2_RA	3E	RW		7E			BE			FE	
PMA3_RA	3F	RW		7F			BF			FF	

Gray fields are reserved; do not access these fields. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the enCoRe V USB devices. For the most up-to-date electrical specifications, verify that you have the most recent data sheet available by visiting the company web site at http://www.cypress.com

Figure 9. Voltage versus CPU Frequency

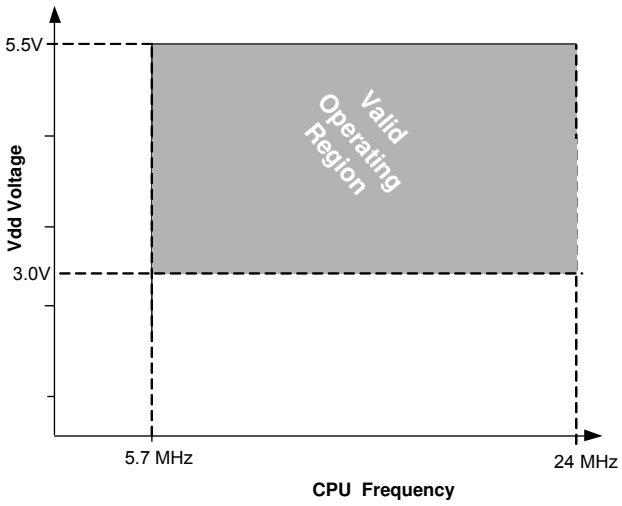
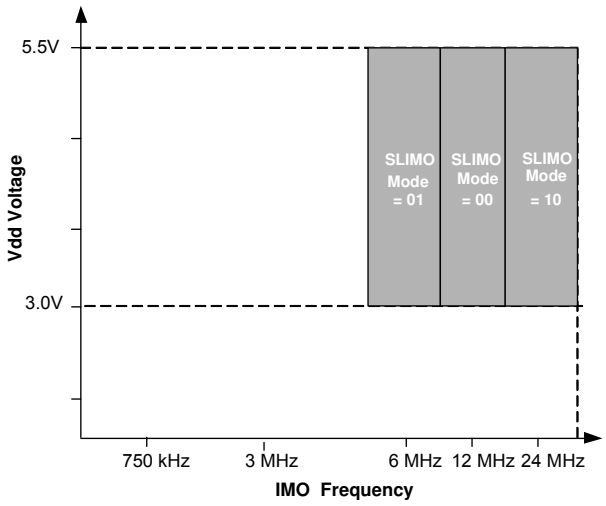


Figure 10. IMO Frequency Trim Options



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 4. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{STG}	Storage temperature[10]	Higher storage temperatures reduces data retention time. Recommended Storage Temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85°C degrades reliability.	–55	+25	+125	°C
V_{DD}	Supply voltage relative to V_{SS}		–0.5	–	+6.0	V
V_{IO}	DC input voltage		V_{SS} – 0.5	–	V_{DD} + 0.5	V
V_{IOZ}	DC voltage applied to tristate		V_{SS} – 0.5	–	V_{DD} + 0.5	V
I_{MIO}	Maximum current into any port pin		–25	–	+50	mA
ESD	Electrostatic discharge voltage	Human body model ESD	2000	–	–	V
LU [8]	Latch up current	In accordance with JESD78 standard	–	–	200	mA

Operating Temperature

Table 5. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{AI}	Ambient industrial temperature		–40	–	+85	°C
T_{AC}	Ambient commercial temperature		0	–	+70	°C
T_{JI}	Operational industrial die temperature [11]	The temperature rise from ambient to junction is package specific. Refer the table Thermal Impedances per Package on page 31. The user must limit the power consumption to comply with this requirement.	–40	–	+100	°C
T_{JC}	Operational commercial die temperature	The temperature rise from ambient to junction is package specific. Refer the table Thermal Impedances per Package on page 31. The user must limit the power consumption to comply with this requirement.	0	–	+85	°C

Notes

7. When V_{DD} remains in the range from 1.71 V to 1.9 V for more than 50 µsec, the slew rate when moving from the 1.71 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 µsec to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the SRPOWER_UP parameter.
8. Errata: For Port 1 pins P1[1], P1[4], and P1[5] 300 Ohm external resistor is needed to meet this spec. Refer to "Errata" on page 35 for more details.
9. If powering down in standby sleep mode, to properly detect and recover from a V_{DD} brown out condition any of the following actions must be taken:
   - Bring the device out of sleep before powering down.
   - Assure that V_{DD} falls below 100 mV before powering back up.
   - Set the No Buzz bit in the OSC_CR0 register to keep the voltage monitoring circuit powered during sleep.
   - Increase the buzz rate to assure that the falling edge of V_{DD} is captured. The rate is configured through the PSSDC bits in the SLP_CFG register. For the referenced registers, refer to the enCoRe V Technical Reference Manual. In deep sleep mode, additional low power voltage monitoring circuitry allows V_{DD} brown out conditions to be detected for edge rates slower than 1 V/ms.

DC Electrical Characteristics

DC Chip Level Specifications

Table 6 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 6. DC Chip Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{DD}	Operating voltage [7, 9]	No USB activity.	3.0	–	5.5	V
$I_{DD24,3}$	Supply current, CPU = 24 MHz	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 24 MHz, No USB/I^2C/SPI.	–	2.9	4.0	mA
$I_{DD12,3}$	Supply current, CPU = 12 MHz	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 12 MHz, No USB/I^2C/SPI.	–	1.7	2.6	mA
$I_{DD6,3}$	Supply current, CPU = 6 MHz	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 6 MHz, No USB/I^2C/SPI.	–	1.2	1.8	mA
$I_{SB1,3}$	Standby current with POR, LVD, and sleep timer	V_{DD} = 3.0 V, T_A = 25 °C, I/O regulator turned off.	–	1.1	1.5	µA
$I_{SB0,3}$	Deep sleep current	V_{DD} = 3.0 V, T_A = 25 °C, I/O regulator turned off.	–	0.1	–	µA
V_{DDUSB}	Operating voltage	USB activity, USB regulator enabled	4.35	–	5.25	V
$I_{DD24,5}$	Supply current, CPU = 24 MHz	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 24 MHz, IMO = 24 MHz USB Active, No I^2C/SPI.	–	7.1	–	mA
$I_{DD12,5}$	Supply current, CPU = 12 MHz	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 12 MHz, IMO = 24 MHz USB Active, No I^2C/SPI.	–	6.2	–	mA
$I_{DD6,5}$	Supply current, CPU = 6 MHz	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 6 MHz, IMO = 24 MHz USB Active, No I^2C/SPI	–	5.8	–	mA
$I_{SB1,5}$	Standby current with POR, LVD, and sleep timer	V_{DD} = 5.0 V, T_A = 25 °C, I/O regulator turned off.	–	1.1	–	µA
$I_{SB0,5}$	Deep sleep current	V_{DD} = 5.0 V, T_A = 25 °C, I/O regulator turned off.	–	0.1	–	µA
V_{DDUSB}	Operating voltage	USB activity, USB regulator bypassed	3.15	3.3	3.60	V

Notes

10. Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrade reliability.
11. The temperature rise from ambient to junction is package specific. See Package Handling on page 31. The user must limit the power consumption to comply with this requirement.

Table 7. DC Characteristics – USB Interface

Symbol	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ pull-up resistance	With idle bus	0.900	–	1.575	kΩ
Rusba	USB D+ pull-up resistance	While receiving traffic	1.425	–	3.090	kΩ
Vohusb	Static output high		2.8	–	3.6	V
Volusb	Static output low		–	–	0.3	V
Vdi	Differential input sensitivity		0.2	–	–	V
Vcm	Differential input common mode range		0.8	–	2.5	V
Vse	Single-ended receiver threshold		0.8	–	2.0	V
Cin	Transceiver capacitance			–	50	pF
Iio	High Z state data Line Leakage	On D+ or D– line	–10	–	+10	µA
Rps2	PS/2 Pull Up Resistance		3	5	7	kΩ
Rext	External USB Series Resistor	In series with each USB pin	21.78	22.0	22.22	Ω

ADC Electrical Specifications

Table 8. ADC User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Input						
V_{IN}	Input voltage range		0	–	VREFADC	V
C_{IIN}	Input capacitance		–	–	5	pF
R_{IN}	Input resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution	1/(500fF* Data Clock)	1/(400fF* Data Clock)	1/(300fF* Data Clock)	Ω
Reference						
V_{REFADC}	ADC reference voltage		1.14	–	1.26	V
Conversion Rate						
F_{CLK}	Data clock	Source is chip's internal main oscillator. See AC Chip-Level Specifications for accuracy	2.25	–	6	MHz
S8	8-bit sample rate	Data Clock set to 6 MHz. Sample Rate = 0.001/ (2^Resolution/Data Clock)	–	23.4375	–	ksps
S10	10-bit sample rate	Data Clock set to 6 MHz. Sample Rate = 0.001/ (2^Resolution/Data Clock)	–	5.859	–	ksps
DC Accuracy						
RES	Resolution	Can be set to 8-, 9-, or 10-bit	8	–	10	bits
DNL	Differential nonlinearity		–1	–	+2	LSB
INL	Integral nonlinearity		–2	–	+2	LSB
E_{Offset}	Offset error	8-bit resolution	0	3.2	19.2	LSB
		10-bit resolution	0	12.8	76.8	LSB
E_{gain}	Gain error	For any resolution	–5	–	+5	%FSR
Power						
I_{ADC}	Operating current		–	2.1	2.6	mA
PSRR	Power supply rejection ratio	PSRR (V_{DD} > 3.0 V)	–	24	–	dB
		PSRR (V_{DD} < 3.0 V)	–	30	–	dB

DC General Purpose I/O Specifications

Table 9 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and package specific temperature range. Typical parameters apply to 5 V and 3.3 V at 25 °C. These are for design guidance only.

Table 9. 3.0 V and 5.5 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor		4	5.6	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 pins	$I_{OH} \leq 10$ µA, maximum of 10 mA source current in all I/Os.	$V_{DD} - 0.2$	–	–	V
V_{OH2}	High output voltage Port 2 or 3 Pins	I_{OH} = 1 mA, maximum of 20 mA source current in all I/Os.	$V_{DD} - 0.9$	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator disabled	$I_{OH} < 10$ µA, maximum of 10 mA source current in all I/Os.	$V_{DD} - 0.2$	–	–	V
V_{OH4}	High output voltage Port 0 or 1 pins with LDO regulator disabled	I_{OH} = 5 mA, maximum of 20 mA source current in all I/Os.	$V_{DD} - 0.9$	–	–	V
V_{OH5}	High output voltage Port 1 pins with LDO regulator enabled for 3 V Out	$I_{OH} < 10$ µA, $V_{DD} > 3.1$ V, maximum of 4 I/Os all sourcing 5 mA	2.85	3.00	3.3	V
V_{OH6}	High output voltage Port 1 pins with LDO regulator enabled for 3 V out	I_{OH} = 5 mA, $V_{DD} > 3.1$ V, maximum of 20 mA source current in all I/Os	2.20	–	–	V
V_{OH7}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	$I_{OH} < 10$ µA, $V_{DD} > 3.0$ V, maximum of 20 mA source current in all I/Os	2.35	2.50	2.75	V
V_{OH8}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	I_{OH} = 2 mA, $V_{DD} > 3.0$ V, maximum of 20 mA source current in all I/Os	1.90	–	–	V
V_{OH9}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	$I_{OH} < 10$ µA, $V_{DD} > 3.0$ V, maximum of 20 mA source current in all I/Os	1.60	1.80	2.1	V
V_{OH10}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} = 1 mA, $V_{DD} > 3.0$ V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V_{OL}	Low output voltage	I_{OL} = 25 mA, $V_{DD} > 3.3$ V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]).	–	–	0.75	V
V_{IL}	Input low voltage		–	–	0.8	V
V_{IH}	Input high voltage		2.0	–	–	V
V_H	Input hysteresis voltage		–	80	–	mV
I_{IL}	Input leakage (absolute value)		–	0.001	1	µA
C_{PIN}	Pin capacitance	Package and pin dependent. Temp = 25 °C.	0.5	1.7	5	pF

DC POR and LVD Specifications

Table 10 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 10. DC POR and LVD Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{PPOR}	V_{DD} value for PPOR trip[12] PORLEV[1:0] = 10b		–	2.82	2.95	V
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b		–	–	–	V
V_{LVD1}	VM[2:0] = 001b		–	–	–	V
V_{LVD2}	VM[2:0] = 010b		2.85	2.92	2.99	V
V_{LVD3}	VM[2:0] = 011b		2.95	3.02	3.09	V
V_{LVD4}	VM[2:0] = 100b		3.06	3.13	3.20	V
V_{LVD5}	VM[2:0] = 101b		–-	–	–	V
V_{LVD6}	VM[2:0] = 110b		–	–	–	V
V_{LVD7}	VM[2:0] = 111b		4.62	4.73	4.83	V

DC Programming Specifications

Table 11 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 11. DC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
$V_{DDIWRITE}$	Supply voltage for flash write operations		1.71	–	5.25	V
I_{DDP}	Supply current during programming or verify		–	5	25	mA
V_{ILP}	Input low voltage during programming or verify	See appropriate DC General Purpose I/O Specifications table	–	–	V_{IL}	V
V_{IHP}	Input high voltage during programming or verify		1.71	–	$V_{DDIWRITE}$ + 0.3	V
I_{ILP}	Input current when applying Vilp to P1[0] or P1[1] during programming or verify[13]		–	–	0.2	mA
I_{IHP}	Input current when applying Vihp to P1[0] or P1[1] during programming or verify[13]		–	–	1.5	mA
V_{OLP}	Output low voltage during programming or verify		–	–	V_{SS} + 0.75	V
V_{OHP}	Output high voltage during programming or verify		$V_{DDIWRITE}$ – 0.9	–	$V_{DDIWRITE}$	V
$Flash_{ENPB}$	Flash write endurance[14]		50,000	–	–	Cycles
$Flash_{DR}$	Flash data retention[15]		10	20	–	Years

Notes
12. Always greater than 50 mV above V_{PPOR} (PORLEV = 10) for falling supply.
13. Driving internal pull down resistor.
14. Erase/write cycles per block.
15. Following maximum Flash write cycles at Tamb = 55 °C and Tj = 70 °C.

AC Electrical Characteristics

AC Chip Level Specifications

The following tables list guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 12. AC Chip Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{CPU}	Processing frequency[16]		5.7	–	25.2	MHz
F_{32K1}	Internal low-speed oscillator (ILO) frequency	Trimmed[17]	19	32	50	kHz
F_{32K_U}	ILO untrimmed frequency)		13	32	82	kHz
F_{32K2}	ILO frequency	Untrimmed	13	32	82	kHz
F_{IMO24}	Internal main oscillator (IMO) stability for 24 MHz ± 5%(12)		22.8	24	25.2	MHz
F_{IMO12}	IMO stability for 12 MHz[17]		11.4	12	12.6	MHz
F_{IMO6}	IMO stability for 6 MHz[17]		5.7	6.0	6.3	MHz
DC_{IMO}	Duty cycle of IMO		40	50	60	%
DC_{ILO}	ILO duty cycle		40	50	60	%
SR_{POWER_UP}	Power supply slew rate		–	–	250	V/ms
T_{XRST}	External reset pulse width at power-up	After supply voltage is valid	1	–	–	ms
T_{XRST2}	External reset pulse width after power-up[18]	Applies after part has booted	10	–	–	µs

Table 13. AC Characteristics – USB Data Timings

Symbol	Description	Conditions	Min	Typ	Max	Units
Tdrate	Full speed data rate	Average bit rate	11.97	12	12.03	MHz
Tdjr1	Receiver data jitter tolerance	To next transition	–18.5	–	18.5	ns
Tdjr2	Receiver data jitter tolerance	To pair transition	–9	–	9	ns
Tudj1	Driver differential jitter	To next transition	–3.5	–	3.5	ns
Tudj2	Driver differential jitter	To pair transition	–4.0	–	4.0	ns
Tfdeop	Source jitter for differential transition	To SE0 transition	–2	–	5	ns
Tfeopt	Source SE0 interval of EOP		160	–	175	ns
Tfeopr	Receiver SE0 interval of EOP		82	–	–	ns
Tfst	Width of SE0 interval during differential transition		–	–	14	ns

Table 14. AC Characteristics – USB Driver

Symbol	Description	Conditions	Min	Typ	Max	Units
Tr	Transition rise time	50 pF	4	–	20	ns
Tf	Transition fall time	50 pF	4	–	20	ns
TR [19]	Rise/fall time matching		90.00	–	111.1	%
Vcrs	Output signal crossover voltage		1.3	–	2.0	V

Notes

16. V_{DD} = 3.0 V and T_J = 85 °C, CPU speed.
17. Trimmed for 3.3 V operation using factory trim values.
18. The minimum required XRES pulse length is longer when programming the device (see Table 17 on page 24).
19. Errata: Rising to falling rate matching of the USB D+ and D- lines has a corner case issue when operating voltage is below 3.3 V. Refer to "Errata" on page 35 for more details.

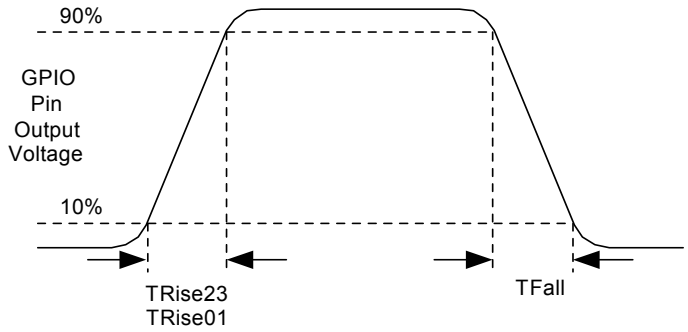
AC General Purpose I/O Specifications

Table 15 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 15. AC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO operating frequency	Normal strong mode, Ports 0, 1	–	–	12	MHz
TRise23	Rise time, strong mode Ports 2, 3	V_{DD} = 3.0 to 3.6 V, 10% - 90%	15	–	80	ns
TRise01	Rise time, strong mode Ports 0, 1	V_{DD} = 3.0 to 3.6 V, 10% - 90%	10	–	50	ns
TFall	Fall time, strong mode All Ports	V_{DD} = 3.0 to 3.6 V, 10% - 90%	10	–	50	ns

Figure 11. GPIO Timing Diagram



AC External Clock Specifications

Table 16 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 16. AC External Clock Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{OSCEXT}	Frequency		0.750	–	25.2	MHz
–	High period		20.6	–	5300	ns
–	Low period		20.6	–	–	ns
–	Power-up IMO to switch		150	–	–	µs

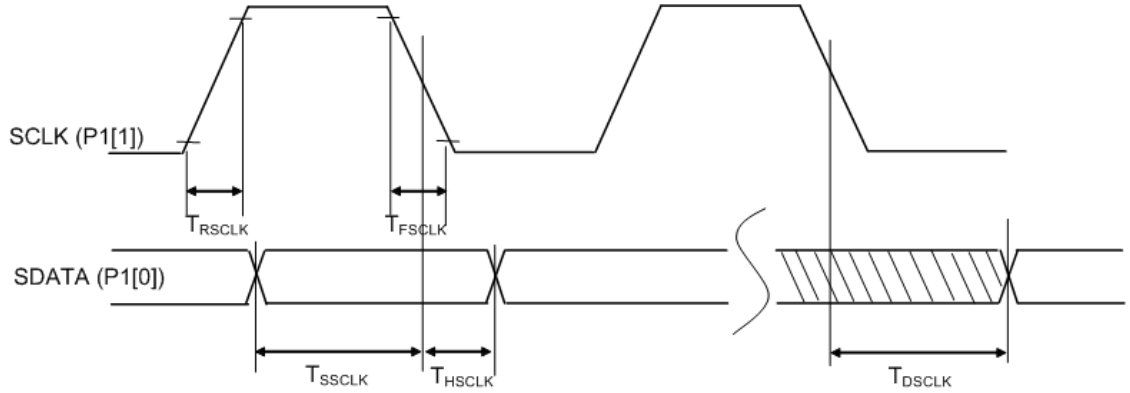
AC Programming Specifications

Table 17 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 17. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{RSCLK}	Rise time of SCLK		1	–	20	ns
T_{FSCLK}	Fall time of SCLK		1	–	20	ns
T_{SSCLK}	Data setup time to falling edge of SCLK		40	–	–	ns
T_{HSCLK}	Data hold time from falling edge of SCLK		40	–	–	ns
F_{SCLK}	Frequency of SCLK		0	–	8	MHz
T_{ERASEB}	Flash erase time (Block)		–	–	18	ms
T_{WRITE}	Flash block write time		–	–	25	ms
T_{DSCLK1}	Data out delay from falling edge of SCLK,	V_{DD} > 3.6 V	–	–	60	ns
T_{DSCLK2}	Data out delay from falling edge of SCLK	3.0 V < V_{DD} < 3.6 V	–	–	85	ns
T_{XRST3}	External reset pulse width after power-up	Required to enter programming mode when coming out of sleep	263	–	–	µs

Figure 12. Timing Diagram - AC Programming Cycle



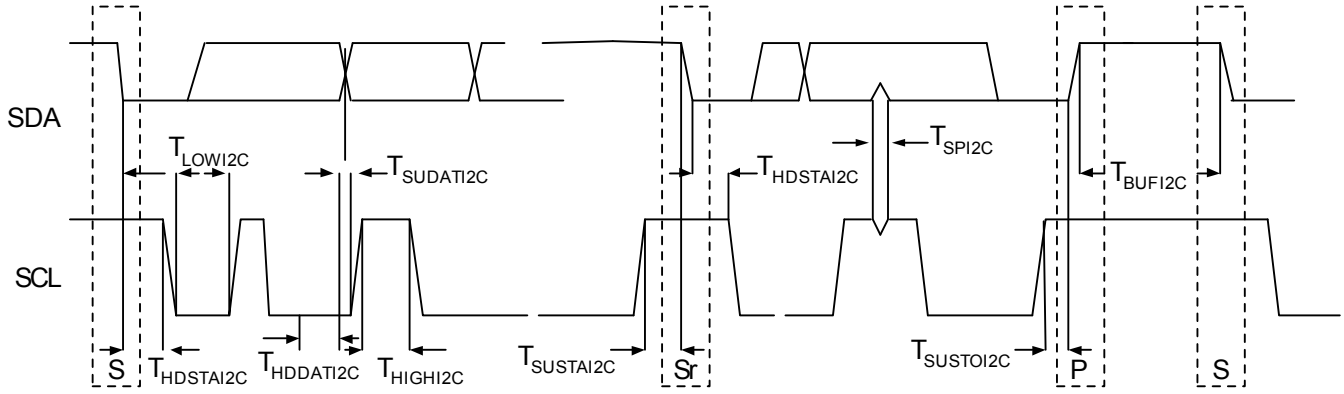
AC I²C Specifications

Table 18 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	µs
T_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs
$T_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs
$T_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs
$T_{HDDATI2C}$	Data hold time	0	–	0	–	µs
$T_{SUDATI2C}$	Data setup time	250	–	100[20]	–	ns
$T_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs
T_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs
T_{SPI2C}	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns

Figure 13. Definition of Timing for Fast/Standard Mode on the I²C Bus



Note

20. A Fast mode I²C bus device can be used in a standard mode I²C bus system, but the requirement $t_{SUDAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SUDAT} = 1000 + 250 = 1250$ ns (according to the standard mode I²C bus specification) before the SCL line is released.