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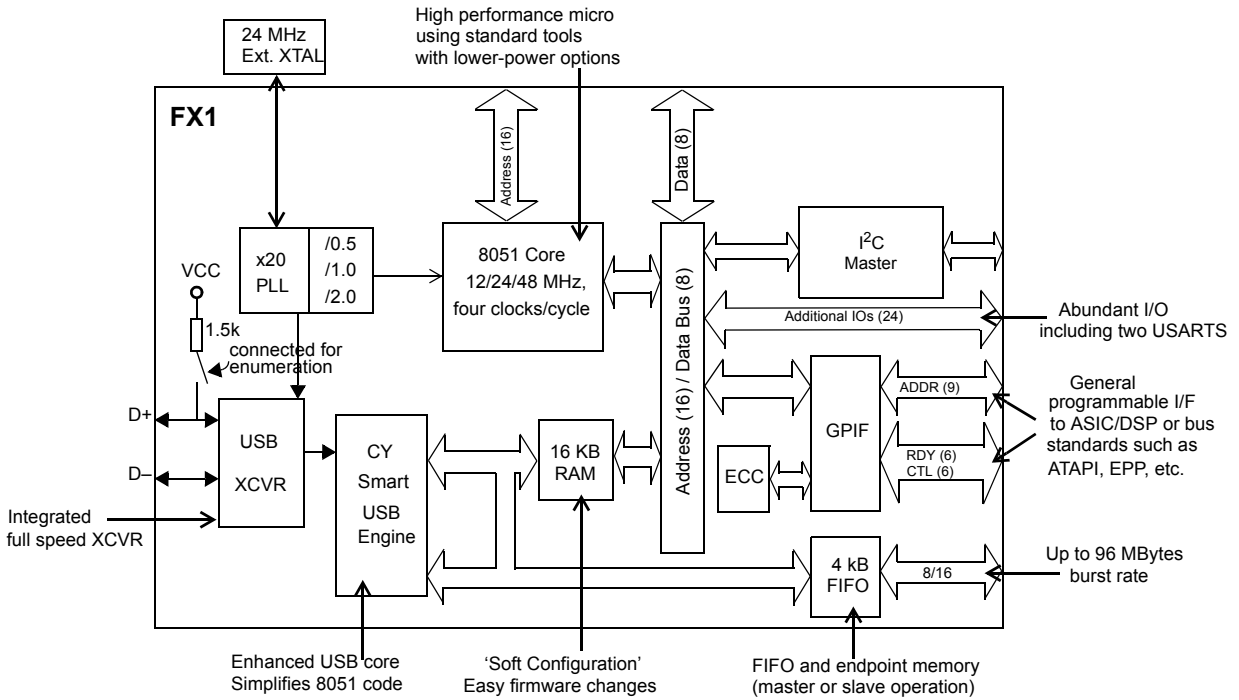
CY7C64713

EZ-USB FX1™ USB Microcontroller Full Speed USB Peripheral Controller

Features

- Single Chip Integrated USB Transceiver, SIE, and Enhanced 8051 Microprocessor
- Fit, Form, and Function Upgradable to the FX2LP (CY7C68013A)
 - Pin compatible
 - Object code compatible
 - Functionally compatible (FX1 functionality is a Subset of the FX2LP)
- Draws No More than 65 mA in Any Mode, Making the FX1 Suitable for Bus Powered Applications
- Software: 8051 Runs from Internal RAM, which is:
 - Downloaded using USB
 - Loaded from EEPROM
 - External memory device (128 pin configuration only)
- 16 KBytes of On-Chip Code/Data RAM
- Four Programmable BULK/INTERRUPT/ISOCHRONOUS Endpoints
 - Buffering options: double, triple, and quad
- Additional Programmable (BULK/INTERRUPT) 64-byte Endpoint
- 8- or 16-bit External Data Interface
- Smart Media Standard ECC Generation
- GPIF
 - Allows direct connection to most parallel interfaces; 8- and 16-bit
 - Programmable waveform descriptors and configuration registers to define waveforms
 - Supports multiple Ready (RDY) inputs and Control (CTL) outputs
- Integrated, Industry Standard 8051 with Enhanced Features:
 - Up to 48 MHz clock rate
 - Four clocks for each instruction cycle
 - Two USARTS
 - Three counters or timers
 - Expanded interrupt system
 - Two data pointers
- 3.3V Operation with 5V Tolerant Inputs
- Smart SIE
- Vectored USB Interrupts
- Separate Data Buffers for the Setup and DATA Portions of a CONTROL Transfer
- Integrated I²C Controller, Running at 100 or 400 KHz
- 48 MHz, 24 MHz, or 12 MHz 8051 Operation
- Four Integrated FIFOs
 - Brings glue and FIFOs inside for lower system cost
 - Automatic conversion to and from 16-bit buses
 - Master or slave operation
 - FIFOs can use externally supplied clock or asynchronous strobes
 - Easy interface to ASIC and DSP ICs
- Vectored for FIFO and GPIF Interrupts
- Up to 40 General Purpose IOs (GPIO)
- Four Package Options:
 - 128 pin TQFP
 - 100 pin TQFP
 - 56 pin SSOP
 - 56 pin QFN Pb-free

Logic Block Diagram



Functional Description

EZ-USB FX1™ (CY7C64713) is a full speed, highly integrated, USB microcontroller. By integrating the USB transceiver, Serial Interface Engine (SIE), enhanced 8051 microcontroller, and a programmable peripheral interface in a single chip, Cypress has created a very cost effective solution that provides superior time-to-market advantages.

The EZ-USB FX1 is more economical, because it incorporates the USB transceiver and provides a smaller footprint solution than the USB SIE or external transceiver implementations. With EZ-USB FX1, the Cypress Smart SIE handles most of the USB protocol in hardware, freeing the embedded microcontroller for application specific functions and decreasing the development time to ensure USB compatibility.

The General Programmable Interface (GPIF) and Master/Slave Endpoint FIFO (8 or 16-bit data bus) provide an easy and glueless interface to popular interfaces such as ATA, UTOPIA, EPP, PCMCIA, and most DSP/processors.

Four Pb-free packages are defined for the family: 56 SSOP, 56 QFN, 100 TQFP, and 128 TQFP.

Applications

- DSL modems
- ATA interface
- Memory card readers
- Legacy conversion devices
- Home PNA
- Wireless LAN
- MP3 players
- Networking

The [Reference Designs](#) section of the cypress website provides additional tools for typical USB applications. Each reference design comes complete with firmware source and object code, schematics, and documentation. Please visit <http://www.cypress.com> for more information.

Functional Overview

USB Signaling Speed

FX1 operates at one of the three rates defined in the USB Specification Revision 2.0, dated April 27, 2000:

Full speed, with a signaling bit rate of 12 Mbps.

FX1 does not support the low speed signaling mode of 1.5 Mbps or the high speed mode of 480 Mbps.

8051 Microprocessor

The 8051 microprocessor embedded in the FX1 family has 256 bytes of register RAM, an expanded interrupt system, three timer/counters, and two USARTs.

8051 Clock Frequency

FX1 has an on-chip oscillator circuit that uses an external 24 MHz (± 100 ppm) crystal with the following characteristics:

- Parallel resonant
- Fundamental mode
- 500 μ W drive level
- 12 pF (5% tolerance) load capacitors.

An on-chip PLL multiplies the 24 MHz oscillator up to 480 MHz, as required by the transceiver/PHY, and the internal counters divide it down for use as the 8051 clock. The default 8051 clock frequency is 12 MHz. The clock frequency of the 8051 is dynamically changed by the 8051 through the CPUCS register.

The CLKOUT pin, which is three-stated and inverted using the internal control bits, outputs the 50% duty cycle 8051 clock at the selected 8051 clock frequency which is 48, 24, or 12 MHz.

USARTS

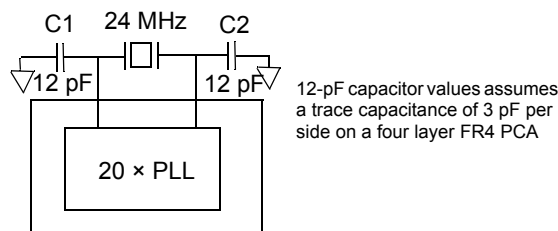
FX1 contains two standard 8051 USARTs, addressed by Special Function Register (SFR) bits. The USART interface pins are available on separate I/O pins, and are not multiplexed with port pins.

UART0 and UART1 can operate using an internal clock at 230 Kbaud with no more than 1% baud rate error. 230 Kbaud operation is achieved by an internally derived clock source that generates overflow pulses at the appropriate time. The internal clock adjusts for the 8051 clock rate (48, 24, 12 MHz) such that it always presents the correct frequency for 230-Kbaud operation.^[1]

Special Function Registers

Certain 8051 SFR addresses are populated to provide fast access to critical FX1 functions. These SFR additions are shown in [Table 1](#) on page 4. Bold type indicates non-standard, enhanced 8051 registers. The two SFR rows that end with '0' and '8' contain bit addressable registers. The four I/O ports A–D use the SFR addresses used in the standard 8051 for ports 0–3, which are not implemented in the FX1. Because of the faster and more efficient SFR addressing, the FX1 I/O ports are not addressable in the external RAM space (using the MOVX instruction).

Figure 1. Crystal Configuration



Note

1. 115-Kbaud operation is also possible by programming the 8051 SMOD0 or SMOD1 bits to a '1' for UART0 and UART1, respectively.

Table 1. Special Function Registers

x	8x	9x	Ax	Bx	Cx	Dx	Ex	Fx
0	IOA	IOB	IOC	IOD	SCON1	PSW	ACC	B
1	SP	EXIF	INT2CLR	IOE	SBUF1			
2	DPL0	MPAGE	INT4CLR	OEA				
3	DPH0			OEB				
4	DPL1			OEC				
5	DPH1			OED				
6	DPS			OEE				
7	PCON							
8	TCON	SCON0	IE	IP	T2CON	EICON	EIE	EIP
9	TMOD	SBUF0						
A	TL0	AUTOPTRH1	EP2468STAT	EP01STAT	RCAP2L			
B	TL1	AUTOPTRL1	EP24FIFOFLGS	GPIFTRIG	RCAP2H			
C	TH0	reserved	EP68FIFOFLGS		TL2			
D	TH1	AUTOPTRH2		GPIFSGLDATH	TH2			
E	CKCON	AUTOPTRL2		GPIFSGLDATLX				
F		reserved	AUTOPTRSETUP	GPIFSGLDATLNOX				

I²C Bus

FX1 supports the I²C bus as a master only at 100/400 KHz. SCL and SDA pins have open drain outputs and hysteresis inputs. These signals must be pulled up to 3.3V, even if no I²C device is connected.

Buses

All packages: 8 or 16-bit 'FIFO' bidirectional data bus, multiplexed on I/O ports B and D. 128 pin package: adds 16-bit output only 8051 address bus, 8-bit bidirectional data bus.

USB Boot Methods

During the power up sequence, internal logic checks the I²C port for the connection of an EEPROM whose first byte is either 0xC0 or 0xC2. If found, it uses the VID/PID/DID values in the EEPROM in place of the internally stored values (0xC0). Alternatively, it boot-loads the EEPROM contents into an internal RAM (0xC2). If no EEPROM is detected, FX1 enumerates using internally stored descriptors. The default ID values for FX1 are VID/PID/DID (0x04B4, 0x6473, 0xAxxx where xxx=Chip revision).^[2]

Table 2. Default ID Values for FX1

Default VID/PID/DID		
Vendor ID	0x04B4	Cypress Semiconductor
Product ID	0x6473	EZ-USB FX1
Device release	0xAxxx	Depends on chip revision (nnn = chip revision where first silicon = 001)

Note

2. The I²C bus SCL and SDA pins must be pulled up, even if an EEPROM is not connected. Otherwise this detection method does not work properly.

ReNumeration™

Because the FX1's configuration is soft, one chip can take on the identities of multiple distinct USB devices.

When first plugged into the USB, the FX1 enumerates automatically and downloads firmware and the USB descriptor tables over the USB cable. Next, the FX1 enumerates again, this time as a device defined by the downloaded information. This patented two step process, called ReNumeration, happens instantly when the device is plugged in, with no indication that the initial download step has occurred.

Two control bits in the USBCS (USB Control and Status) register control the ReNumeration process: DISCON and RENUM. To simulate a USB disconnect, the firmware sets DISCON to 1. To reconnect, the firmware clears DISCON to 0.

Before reconnecting, the firmware sets or clears the RENUM bit to indicate if the firmware or the Default USB Device handles device requests over endpoint zero:

- RENUM = 0, the Default USB Device handles device requests
- RENUM = 1, the firmware handles device requests

Bus-powered Applications

The FX1 fully supports bus powered designs by enumerating with less than 100 mA as required by the USB specification.

Interrupt System

INT2 Interrupt Request and Enable Registers

FX1 implements an autovector feature for INT2 and INT4. There are 27 INT2 (USB) vectors, and 14 INT4 (FIFO/GPIF) vectors. See [EZ-USB Technical Reference Manual \(TRM\)](#) for more details.

USB-Interrupt Autovectors

The main USB interrupt is shared by 27 interrupt sources. The FX1 provides a second level of interrupt vectoring, called Autovectoring, to save code and processing time that is normally required to identify the individual USB interrupt source. When a USB interrupt is asserted, the FX1 pushes the program counter on to its stack and then jumps to address 0x0043, where it expects to find a “jump” instruction to the USB Interrupt service routine.

The FX1 jump instruction is encoded as shown in [Table 3](#).

If Autovectoring is enabled (AV2EN = 1 in the INTSETUP register), the FX1 substitutes its INT2VEC byte. Therefore, if the

high byte (“page”) of a jump table address is preloaded at location 0x0044, the automatically inserted INT2VEC byte at 0x0045 directs the jump to the correct address out of the 27 addresses within the page.

FIFO/GPIF Interrupt (INT4)

Just as the USB Interrupt is shared among 27 individual USB-interrupt sources, the FIFO/GPIF interrupt is shared among 14 individual FIFO/GPIF sources. The FIFO/GPIF Interrupt, such as the USB Interrupt, can employ autovectoring. [Table 4](#) on page 6 shows the priority and INT4VEC values for the 14 FIFO/GPIF interrupt sources.

Table 3. INT2 USB Interrupts

USB INTERRUPT TABLE FOR INT2			
Priority	INT2VEC Value	Source	Notes
1	00	SUDAV	Setup Data Available
2	04	SOF	Start of Frame
3	08	SUTOK	Setup Token Received
4	0C	SUSPEND	USB Suspend request
5	10	USB RESET	Bus reset
6	14		Reserved
7	18	EP0ACK	FX1 ACK'd the CONTROL Handshake
8	1C		Reserved
9	20	EP0-IN	EP0-IN ready to be loaded with data
10	24	EP0-OUT	EP0-OUT has USB data
11	28	EP1-IN	EP1-IN ready to be loaded with data
12	2C	EP1-OUT	EP1-OUT has USB data
13	30	EP2	IN: buffer available. OUT: buffer has data
14	34	EP4	IN: buffer available. OUT: buffer has data
15	38	EP6	IN: buffer available. OUT: buffer has data
16	3C	EP8	IN: buffer available. OUT: buffer has data
17	40	IBN	IN-Bulk-NAK (any IN endpoint)
18	44		Reserved
19	48	EP0PING	EP0 OUT was Pinged and it NAK'd
20	4C	EP1PING	EP1 OUT was Pinged and it NAK'd
21	50	EP2PING	EP2 OUT was Pinged and it NAK'd
22	54	EP4PING	EP4 OUT was Pinged and it NAK'd
23	58	EP6PING	EP6 OUT was Pinged and it NAK'd
24	5C	EP8PING	EP8 OUT was Pinged and it NAK'd
25	60	ERRLIMIT	Bus errors exceeded the programmed limit
26	64		
27	68		Reserved
28	6C		Reserved
29	70	EP2ISOERR	ISO EP2 OUT PID sequence error
30	74	EP4ISOERR	ISO EP4 OUT PID sequence error
31	78	EP6ISOERR	ISO EP6 OUT PID sequence error
32	7C	EP8ISOERR	ISO EP8 OUT PID sequence error

Table 4. Individual FIFO/GPIF Interrupt Sources

Priority	INT4VEC Value	Source	Notes
1	80	EP2PF	Endpoint 2 Programmable Flag
2	84	EP4PF	Endpoint 4 Programmable Flag
3	88	EP6PF	Endpoint 6 Programmable Flag
4	8C	EP8PF	Endpoint 8 Programmable Flag
5	90	EP2EF	Endpoint 2 Empty Flag
6	94	EP4EF	Endpoint 4 Empty Flag
7	98	EP6EF	Endpoint 6 Empty Flag
8	9C	EP8EF	Endpoint 8 Empty Flag
9	A0	EP2FF	Endpoint 2 Full Flag
10	A4	EP4FF	Endpoint 4 Full Flag
11	A8	EP6FF	Endpoint 6 Full Flag
12	AC	EP8FF	Endpoint 8 Full Flag
13	B0	GPIFDONE	GPIF Operation Complete
14	B4	GPIFWF	GPIF Waveform

If Autovectoring is enabled (AV4EN = 1 in the INTSETUP register), the FX1 substitutes its INT4VEC byte. Therefore, if the high byte (“page”) of a jump-table address is preloaded at location 0x0054, the automatically inserted INT4VEC byte at 0x0055 directs the jump to the correct address out of the 14 addresses within the page. When the ISR occurs, the FX1 pushes the program counter onto its stack and then jumps to address 0x0053, where it expects to find a “jump” instruction to the ISR Interrupt service routine.

Reset and Wakeup

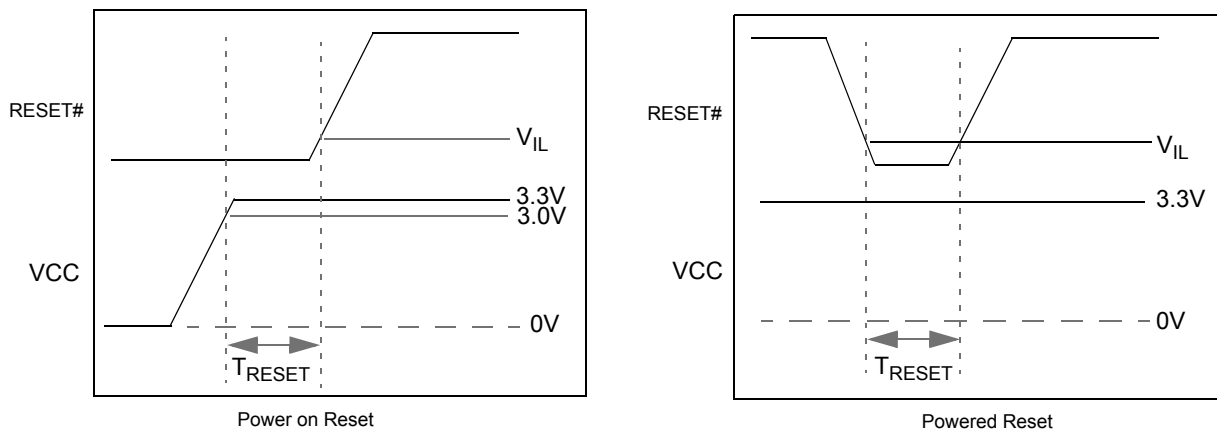
Reset Pin

The input pin, RESET#, resets the FX1 when asserted. This pin has hysteresis and is active LOW. When a crystal is used with the CY7C64713, the reset period must allow for the stabilization

of the crystal and the PLL. This reset period must be approximately 5 ms after VCC has reached 3.0 Volts. If the crystal input pin is driven by a clock signal the internal PLL stabilizes in 200 μs after VCC has reached 3.0V^[3]. Figure 2 shows a power on reset condition and a reset applied during operation. A power on reset is defined as the time a reset is asserted when power is being applied to the circuit. A powered reset is defined to be when the FX1 has been previously powered on and operating and the RESET# pin is asserted.

Cypress provides an application note which describes and recommends power on reset implementation and is found on the Cypress web site. While the application note discusses the FX2, the information provided applies also to the FX1. For more information on reset implementation for the FX2 family of products visit <http://www.cypress.com>.

Figure 2. Reset Timing Plots



Note

3. If the external clock is powered at the same time as the CY7C64713 and has a stabilization wait period. It must be added to the 200 μs.

Table 5. Reset Timing Values

Condition	T _{RESET}
Power On Reset with crystal	5 ms
Power On Reset with external clock	200 μs + Clock stability time
Powered Reset	200 μs

Wakeup Pins

The 8051 puts itself and the rest of the chip into a power down mode by setting PCON.0 = 1. This stops the oscillator and PLL. When WAKEUP is asserted by external logic, the oscillator restarts, after the PLL stabilizes, and then the 8051 receives a wakeup interrupt. This applies irrespective of whether the FX1 is connected to the USB or not.

The FX1 exits the power down (USB suspend) state using one of the following methods:

- USB bus activity (if D+/D- lines are left floating, noise on these lines may indicate activity to the FX1 and initiate a wakeup).
- External logic asserts the WAKEUP pin.
- External logic asserts the PA3/WU2 pin.

The second wakeup pin, WU2, can also be configured as a general purpose I/O pin. This allows a simple external R-C network to be used as a periodic wakeup source. Note that WAKEUP is by default active LOW.

Program/Data RAM

Size

The FX1 has 16 KBytes of internal program/data RAM, where PSEN#/RD# signals are internally ORed to allow the 8051 to access it as both program and data memory. No USB control registers appear in this space.

Two memory maps are shown in the following diagrams:

- **Figure 3** Internal Code Memory, EA = 0
- **Figure 4** External Code Memory, EA = 1.

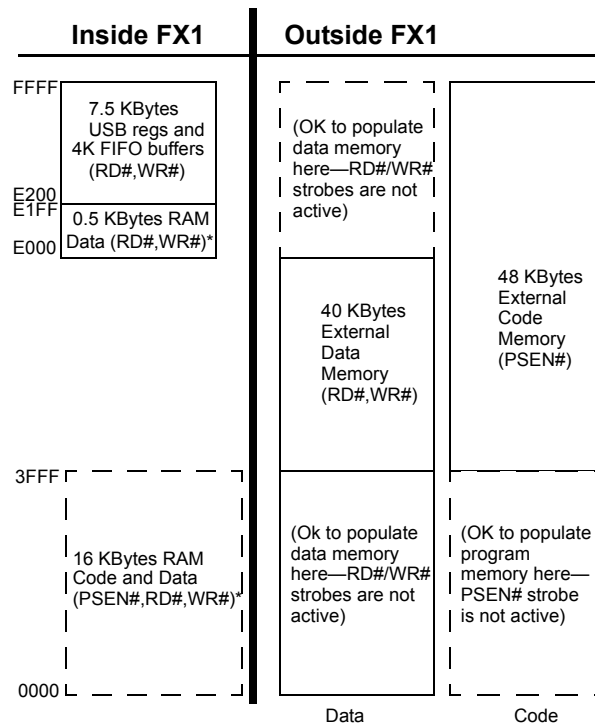
Internal Code Memory, EA = 0

This mode implements the internal 16 KByte block of RAM (starting at 0) as combined code and data memory. When the external RAM or ROM is added, the external read and write strobes are suppressed for memory spaces that exist inside the chip. This allows the user to connect a 64 KByte memory without requiring the address decodes to keep clear of internal memory spaces.

Only the **internal** 16 KBytes and **scratch pad** 0.5 KBytes RAM spaces have the following access:

- USB download
- USB upload
- Setup data pointer
- I²C interface boot load

Figure 3. Internal Code Memory, EA = 0.

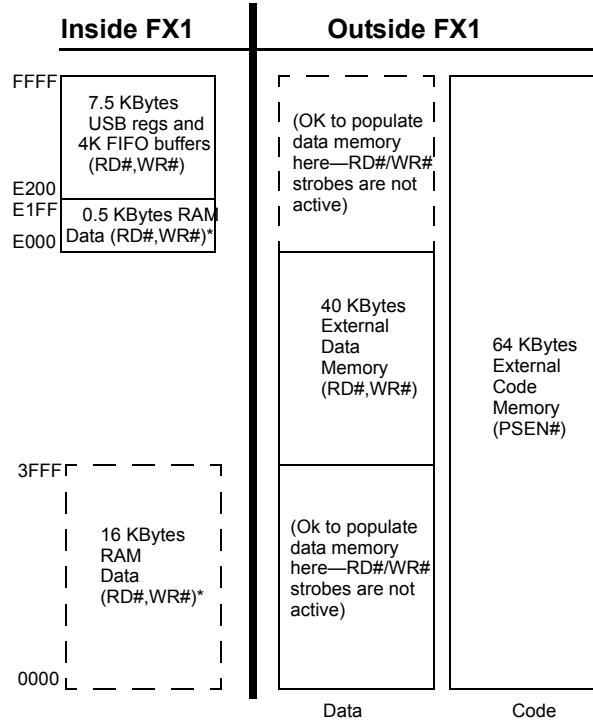


*SUDPTR, USB upload/download, I²C interface boot access

External Code Memory, EA = 1

The bottom 16 KBytes of program memory is external, and therefore the bottom 16 KBytes of internal RAM is accessible only as data memory.

Figure 4. External Code Memory, EA = 1



*SUDPTR, USB upload/download, I²C interface boot access

Figure 5. Register Addresses

FFFF	4 KBytes EP2-EP8 buffers (8 x 512) Not all Space is available for all transfer types
F000 - EFFF	2 KBytes RESERVED
E800 - E7FF	64 Bytes EP1IN
E7C0 - E7BF	64 Bytes EP1OUT
E780 - E77F	64 Bytes EP0 IN/OUT
E740 - E73F	64 Bytes RESERVED
E700 - E6FF	8051 Addressable Registers (512)
E500 - E4FF	Reserved (128)
E480 - E47F	128 bytes GPIF Waveforms
E400 - E3FF	Reserved (512)
E200 - E1FF	512 bytes 8051 xdata RAM
E000	

Endpoint RAM

Size

- 3 × 64 bytes (Endpoints 0 and 1)
- 8 × 512 bytes (Endpoints 2, 4, 6, 8)

Organization

- EP0—Bidirectional endpoint zero, 64 byte buffer
- EP1IN, EP1OUT—64 byte buffers, bulk or interrupt
- EP2, 4, 6, 8—Eight 512-byte buffers, bulk, interrupt, or isochronous, of which only the transfer size is available. EP4 and EP8 are double buffered, while EP2 and 6 are either double, triple, or quad buffered. Regardless of the physical size of the buffer, each endpoint buffer accommodates only one full speed packet. For bulk endpoints, the maximum number of bytes it can accommodate is 64, even though the physical buffer size is 512 or 1024. For an ISOCHRONOUS endpoint the maximum number of bytes it can accommodate is 1023. For endpoint configuration options, see [Figure 6](#).

Setup Data Buffer

A separate 8-byte buffer at 0xE6B8-0xE6BF holds the Setup data from a CONTROL transfer.

Default Alternate Settings

In the following table, '0' means "not implemented", and '2x' means "double buffered".

Table 6. Default Alternate Settings

Alternate Setting	0	1	2	3
ep0	64	64	64	64
ep1out	0	64 bulk	64 int	64 int
ep1in	0	64 bulk	64 int	64 int
ep2	0	64 bulk out (2x)	64 int out (2x)	64 iso out (2x)
ep4	0	64 bulk out (2x)	64 bulk out (2x)	64 bulk out (2x)
ep6	0	64 bulk in (2x)	64 int in (2x)	64 iso in (2x)
ep8	0	64 bulk in (2x)	64 bulk in (2x)	64 bulk in (2x)

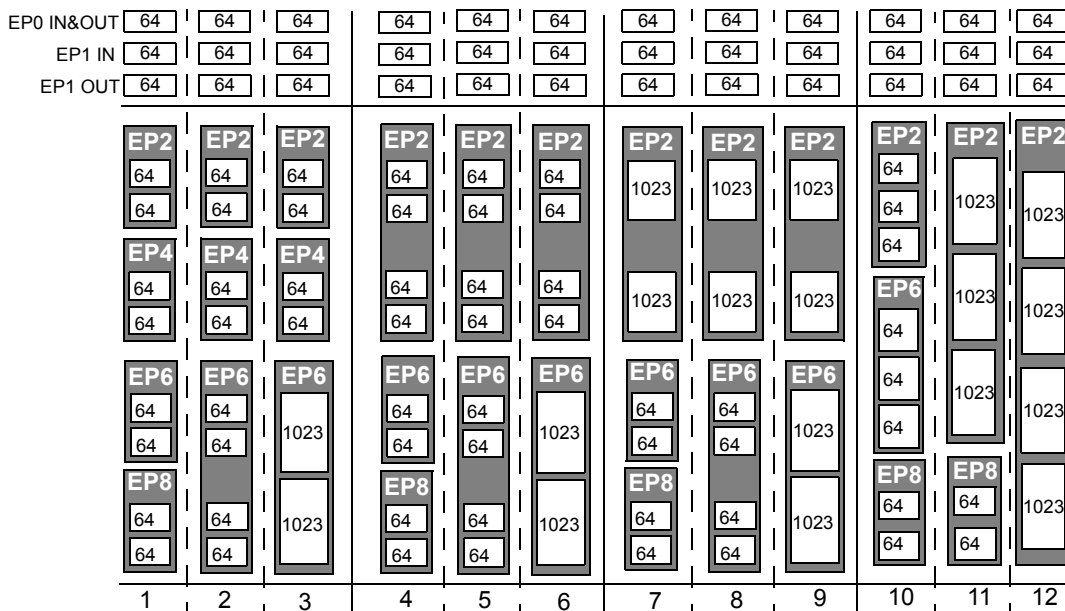
External FIFO Interface

Architecture

The FX1 slave FIFO architecture has eight 512-byte blocks in the endpoint RAM that directly serve as FIFO memories, and are controlled by FIFO control signals (such as IFCLK, SLCS#, SLRD, SLWR, SLOE, PKTEND, and flags). The usable size of these buffers depend on the USB transfer mode as described in the section [Organization](#) on page 9.

In operation, some of the eight RAM blocks fill or empty from the SIE, while the others are connected to the I/O transfer logic. The transfer logic takes two forms: the GPIF for internally generated control signals or the slave FIFO interface for externally controlled transfers.

Figure 6. Endpoint Configuration



Master/Slave Control Signals

The FX1 endpoint FIFOS are implemented as eight physically distinct 256x16 RAM blocks. The 8051/SIE can switch any of the RAM blocks between two domains: the USB (SIE) domain and the 8051-I/O Unit domain. This switching is done instantaneously, giving essentially zero transfer time between “USB FIFOS” and “Slave FIFOS.” While they are physically the same memory, no bytes are actually transferred between buffers.

At any time, some RAM blocks fill or empty with USB data under SIE control, while other RAM blocks are available to the 8051 and the I/O control unit. The RAM blocks operate as a single-port in the USB domain, and dual port in the 8051-I/O domain. The blocks are configured as single, double, triple, or quad buffered.

The I/O control unit implements either an internal master (M for master) or external master (S for Slave) interface.

In Master (M) mode, the GPIF internally controls FIFOADR[1..0] to select a FIFO. The RDY pins (two in the 56 pin package, six in the 100 pin and 128 pin packages) are used as flag inputs from an external FIFO or other logic if desired. The GPIF is run from either an internally derived clock or an externally supplied clock (IFCLK), at a rate that transfers data up to 96 Megabytes/s (48 MHz IFCLK with 16-bit interface).

In Slave (S) mode, the FX1 accepts either an internally derived clock or an externally supplied clock (IFCLK with a maximum frequency of 48 MHz) and SLCS#, SLRD, SLWR, SLOE, PKTEND signals from external logic. When using an external IFCLK, the external clock must be present before switching to the external clock with the IFCLKSRC bit. Each endpoint can individually be selected for byte or word operation by an internal configuration bit, and a Slave FIFO Output Enable signal SLOE enables data of the selected width. External logic must ensure that the output enable signal is inactive when writing data to a slave FIFO. The slave interface can also operate asynchronously, where the SLRD and SLWR signals act directly as strobes, rather than a clock qualifier as in the synchronous mode. The signals SLRD, SLWR, SLOE, and PKTEND are gated by the signal SLCS#.

GPIF and FIFO Clock Rates

An 8051 register bit selects one of two frequencies for the internally supplied interface clock: 30 MHz and 48 MHz. Alternatively, an externally supplied clock of 5 to 48 MHz feeding the IFCLK pin is used as the interface clock. IFCLK is configured to function as an output clock when the GPIF and FIFOs are internally clocked. An output enable bit in the IFCONFIG register turns this clock output off, if desired. Another bit within the IFCONFIG register inverts the IFCLK signal whether internally or externally sourced.

GPIF

The GPIF is a flexible 8 or 16-bit parallel interface driven by a user programmable finite state machine. It allows the CY7C64713 to perform local bus mastering, and can implement a wide variety of protocols such as ATA interface, printer parallel port, and Utopia.

The GPIF has six programmable control outputs (CTL), nine address outputs (GPIFADR_x), and six general purpose Ready inputs (RDY). The data bus width is 8 or 16 bits. Each GPIF vector defines the state of the control outputs, and determines

what state a Ready input (or multiple inputs) must be before proceeding. The GPIF vector is programmed to advance a FIFO to the next data value, advance an address, and so on. A sequence of the GPIF vectors create a single waveform that executes to perform the data move between the FX1 and the external device.

Six Control OUT Signals

The 100 and 128 pin packages bring out all six Control Output pins (CTL0-CTL5). The 8051 programs the GPIF unit to define the CTL waveforms. The 56 pin package brings out three of these signals: CTL0 - CTL2. CTL_x waveform edges are programmed to make transitions as fast as once per clock (20.8 ns using a 48 MHz clock).

Six Ready IN Signals

The 100 and 128 pin packages bring out all six Ready inputs (RDY0-RDY5). The 8051 programs the GPIF unit to test the RDY pins for GPIF branching. The 56 pin package brings out two of these signals, RDY0-1.

Nine GPIF Address OUT Signals

Nine GPIF address lines are available in the 100 and 128 pin packages: GPIFADR[8..0]. The GPIF address lines allow indexing through up to a 512 byte block of RAM. If more address lines are needed, I/O port pins are used.

Long Transfer Mode

In Master mode, the 8051 appropriately sets the GPIF transaction count registers (GPIFTCB3, GPIFTCB2, GPIFTCB1, or GPIFTCB0) for unattended transfers of up to 2³² transactions. The GPIF automatically throttles data flow to prevent under or overflow until the full number of requested transactions are complete. The GPIF decrements the value in these registers to represent the current status of the transaction.

ECC Generation

The EZ-USB FX1 can calculate ECCs (Error Correcting Codes) on data that pass across its GPIF or Slave FIFO interfaces. There are two ECC configurations: Two ECCs, each calculated over 256 bytes (SmartMedia™ Standard); and one ECC calculated over 512 bytes.

The ECC can correct any one-bit error or detect any two-bit error.

Note To use the ECC logic, the GPIF or Slave FIFO interface must be configured for byte-wide operation.

ECC Implementation

The two ECC configurations are selected by the ECCM bit:

0.0.0.1 ECCM = 0

Two 3-byte ECCs, each calculated over a 256-byte block of data. This configuration conforms to the SmartMedia Standard.

Write any value to ECCRESET, then pass data across the GPIF or Slave FIFO interface. The ECC for the first 256 bytes of data is calculated and stored in ECC1. The ECC for the next 256 bytes is stored in ECC2. After the second ECC is calculated, the values in the ECC_x registers do not change until the ECCRESET is written again, even if more data is subsequently passed across the interface.

0.0.0.2 ECCM = 1

One 3-byte ECC calculated over a 512-byte block of data.

Write any value to ECCRESET, then pass data across the GPIF or Slave FIFO interface. The ECC for the first 512 bytes of data is calculated and stored in ECC1; ECC2 is not used. After the ECC is calculated, the value in ECC1 does not change until the ECCRESET is written again, even if more data is subsequently passed across the interface

USB Uploads and Downloads

The core has the ability to directly edit the data contents of the internal 16 KByte RAM and of the internal 512 byte scratch pad RAM via a vendor specific command. This capability is normally used when 'soft' downloading user code and is available only to and from the internal RAM, only when the 8051 is held in reset. The available RAM spaces are 16 KBytes from 0x0000–0x3FFF (code/data) and 512 bytes from 0xE000–0xE1FF (scratch pad data RAM).^[4]

Autopointer Access

FX1 provides two identical autopointers. They are similar to the internal 8051 data pointers, but with an additional feature: they can optionally increment after every memory access. This capability is available to and from both internal and external RAM. The autopointers are available in external FX1 registers, under the control of a mode bit (AUTOPTRSETUP.0). Using the external FX1 autopointer access (at 0xE67B – 0xE67C) allows the autopointer to access all RAM, internal and external, to the part. Also, the autopointers can point to any FX1 register or endpoint buffer space. When autopointer access to external memory is enabled, the location 0xE67B and 0xE67C in XDATA and the code space cannot be used.

I²C Controller

FX1 has one I²C port that is driven by two internal controllers: one that automatically operates at boot time to load VID/PID/DID and configuration information; and another that the 8051, once running, uses to control external I²C devices. The I²C port operates in master mode only.

I²C Port Pins

The I²C pins SCL and SDA must have external 2.2 kΩ pull up resistors even if no EEPROM is connected to the FX1. External EEPROM device address pins must be configured properly. See Table 7 for configuring the device address pins.

Table 7. Strap Boot EEPROM Address Lines to These Values

Bytes	Example EEPROM	A2	A1	A0
16	24LC00 ^[5]	N/A	N/A	N/A
128	24LC01	0	0	0
256	24LC02	0	0	0
4K	24LC32	0	0	1
8K	24LC64	0	0	1
16K	24LC128	0	0	1

Notes

- 4. After the data is downloaded from the host, a 'loader' executes from the internal RAM to transfer downloaded data to the external memory.
- 5. This EEPROM has no address pins.

I²C Interface Boot Load Access

At power on reset the I²C interface boot loader loads the VID/PID/DID configuration bytes and up to 16 KBytes of program/data. The available RAM spaces are 16 KBytes from 0x0000–0x3FFF and 512 bytes from 0xE000–0xE1FF. The 8051 is in reset. I²C interface boot loads only occur after power on reset.

I²C Interface General Purpose Access

The 8051 can control peripherals connected to the I²C bus using the I2CTL and I2DAT registers. FX1 provides I²C master control only, because it is never an I²C slave.

Compatible with Previous Generation EZ-USB FX2

The EZ-USB FX1 is fit, form, and function upgradable to the EZ-USB FX2LP. This makes for an easy transition for designers wanting to upgrade their systems from full speed to high speed designs. The pinout and package selection are identical, and all firmware developed for the FX1 function in the FX2LP with proper addition of high speed descriptors and speed switching code.

Pin Assignments

Figure 7 on page 12 identifies all signals for the three package types. The following pages illustrate the individual pin diagrams, plus a combination diagram showing which of the full set of signals are available in the 128, 100, and 56 pin packages.

The signals on the left edge of the 56 pin package in Figure 7 on page 12 are common to all versions in the FX1 family. Three modes are available in all package versions: Port, GPIF master, and Slave FIFO. These modes define the signals on the right edge of the diagram. The 8051 selects the interface mode using the IFCONFIG[1:0] register bits. Port mode is the power on default configuration.

The 100-pin package adds functionality to the 56 pin package by adding these pins:

- PORTC or alternate GPIFADR[7:0] address signals
- PORTE or alternate GPIFADR[8] address signal and seven additional 8051 signals
- Three GPIF Control signals
- Four GPIF Ready signals
- Nine 8051 signals (two USARTs, three timer inputs, INT4, and INT5#)
- BKPT, RD#, WR#.

The 128 pin package adds the 8051 address and data buses plus control signals. Note that two of the required signals, RD# and WR#, are present in the 100 pin version. In the 100 pin and 128 pin versions, an 8051 control bit is set to pulse the RD# and WR# pins when the 8051 reads from and writes to the PORTC.

Figure 7. Signals

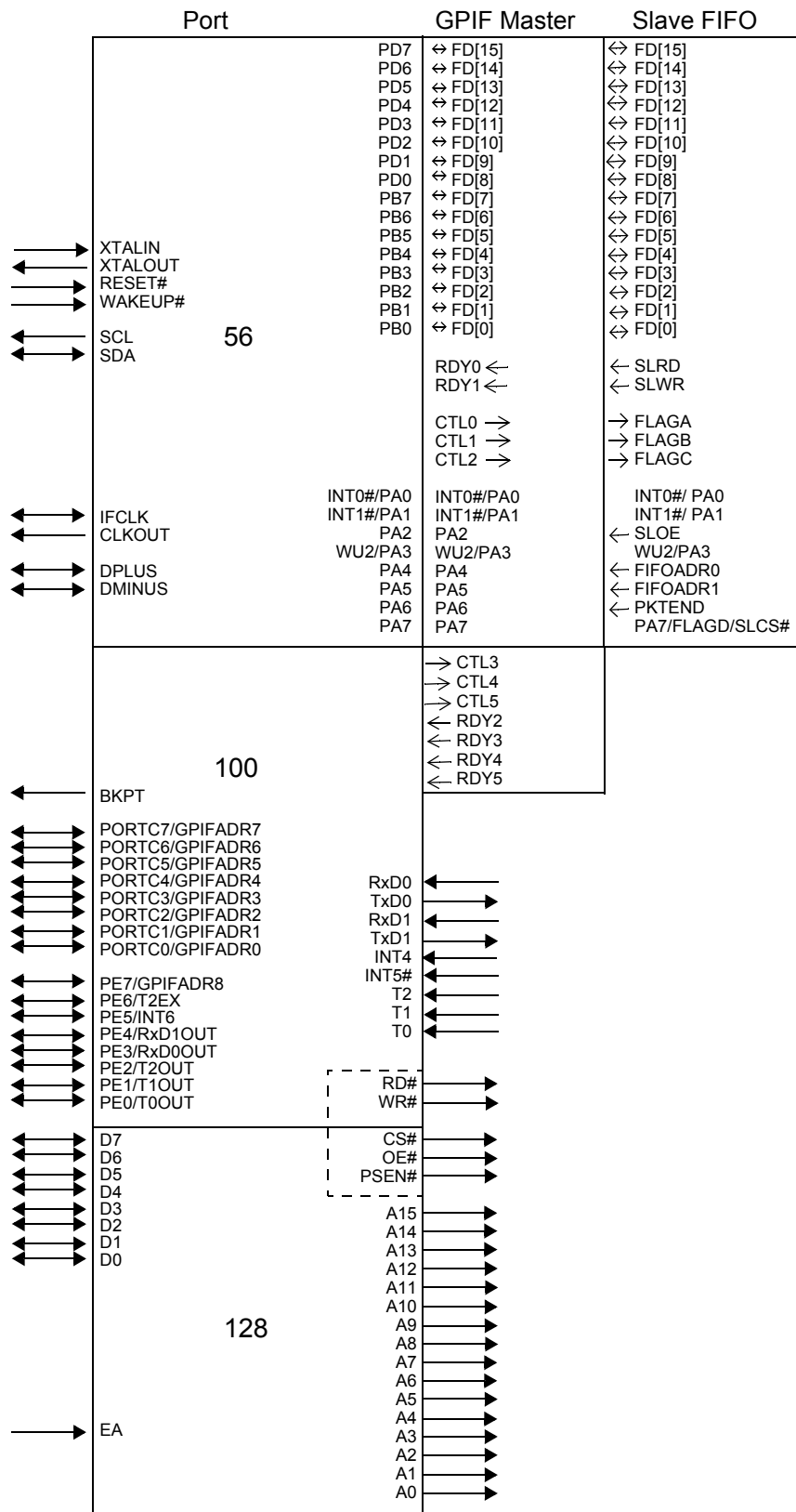
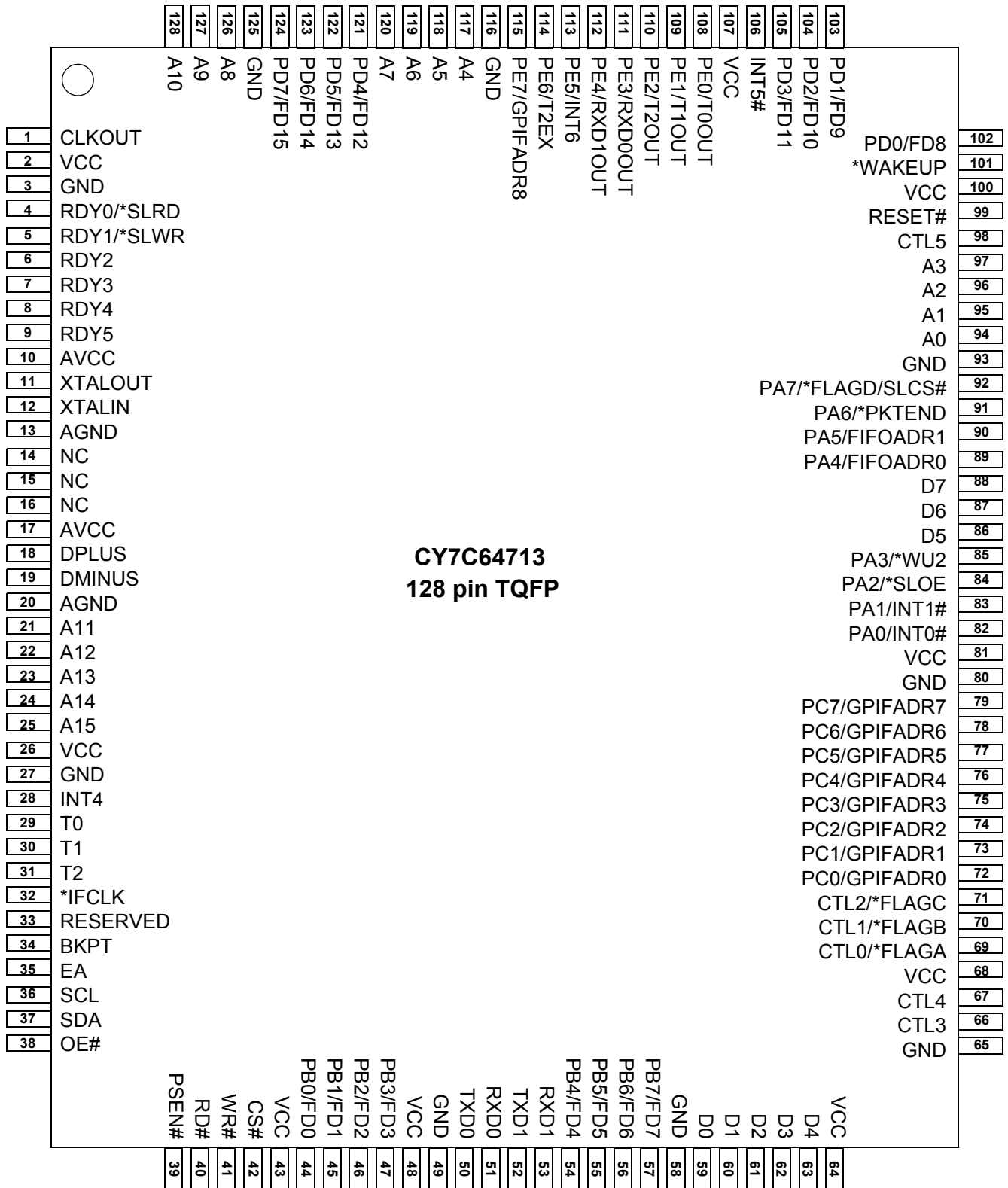
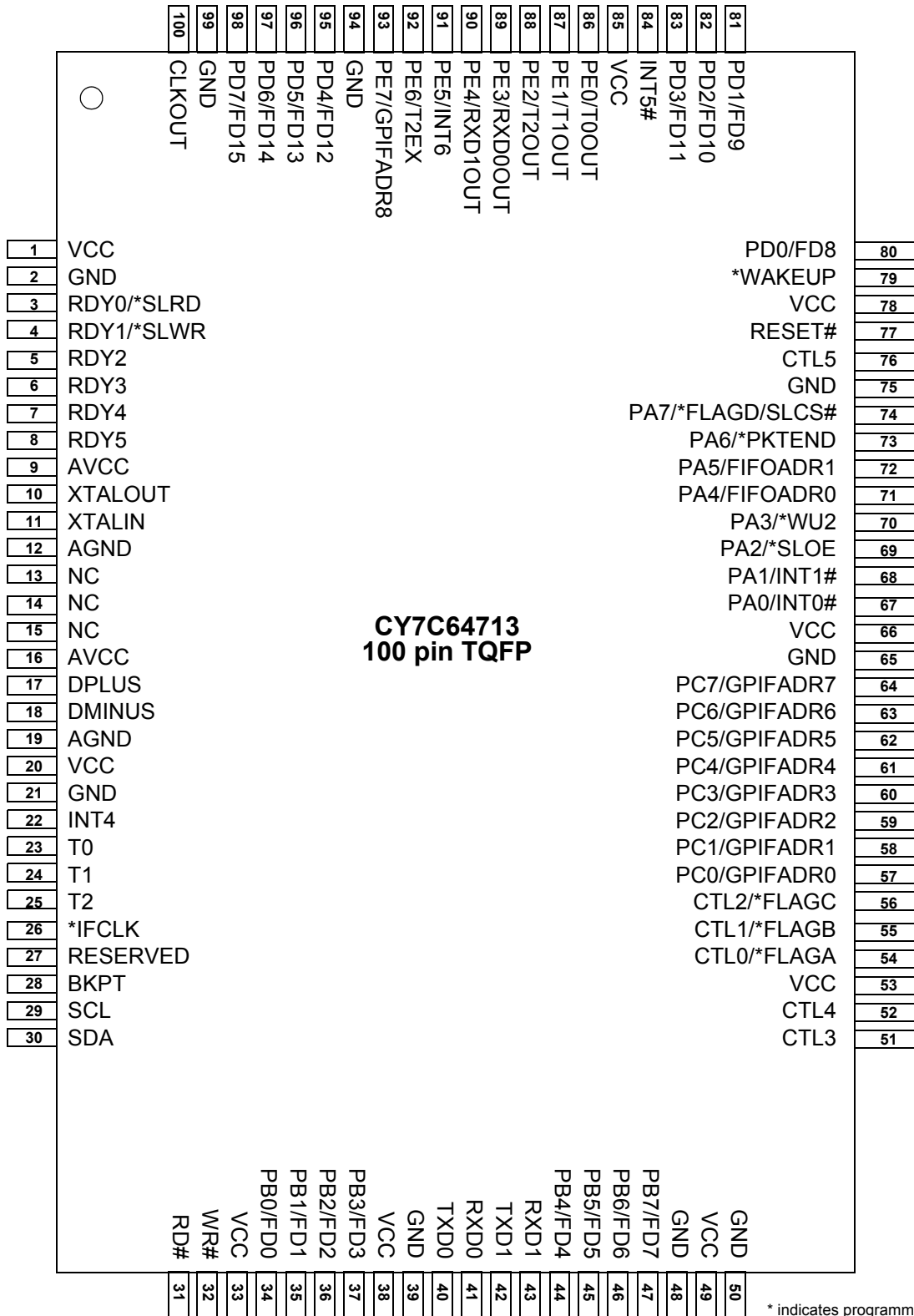


Figure 8. CY7C64713 128 pin TQFP Pin Assignment



* indicates programmable polarity

Figure 9. CY7C64713 100 pin TQFP Pin Assignment



* indicates programmable polarity

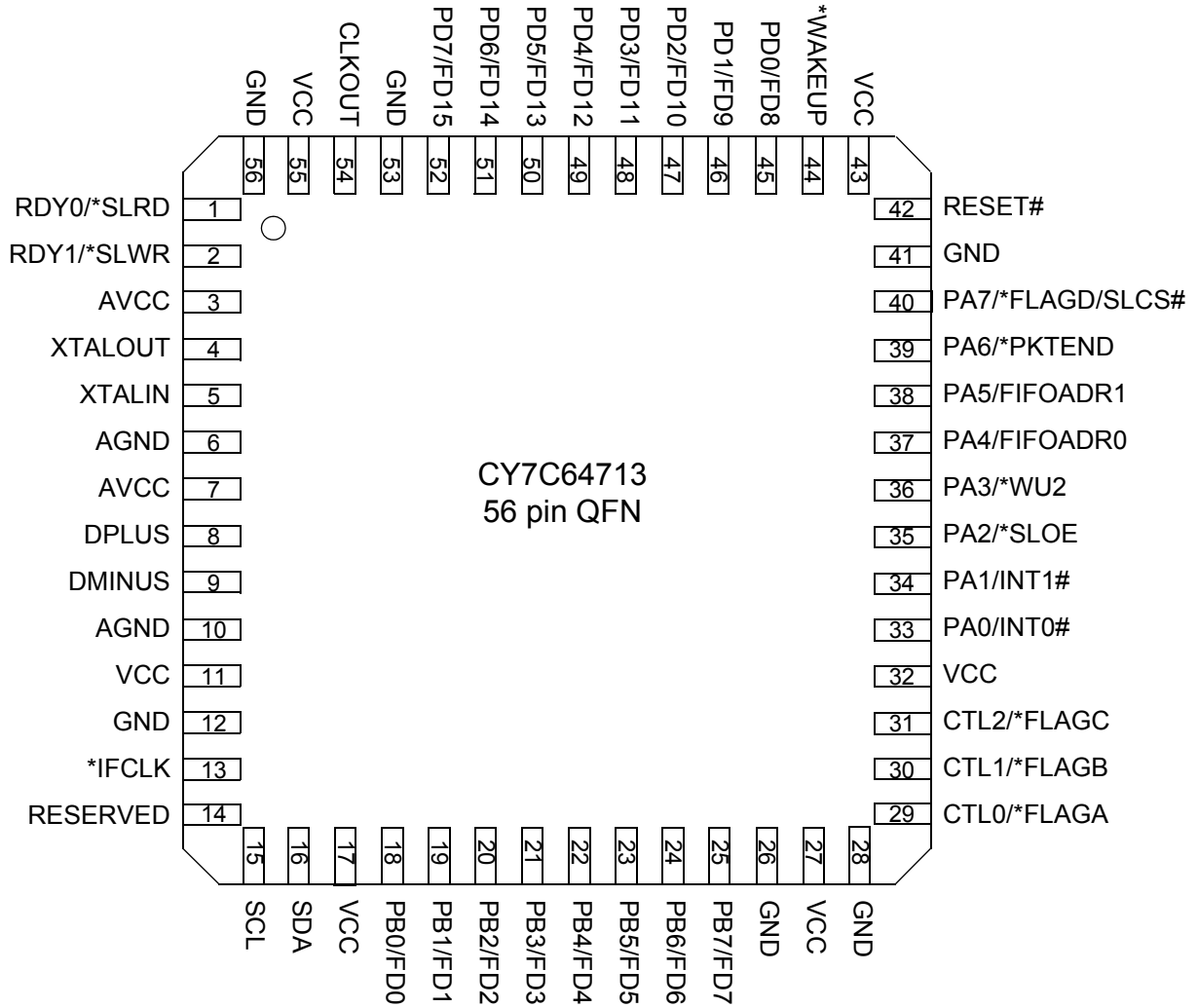
Figure 10. CY7C64713 56 pin SSOP Pin Assignment

**CY7C64713
56 pin SSOP**

1	PD5/FD13	PD4/FD12	56
2	PD6/FD14	PD3/FD11	55
3	PD7/FD15	PD2/FD10	54
4	GND	PD1/FD9	53
5	CLKOUT	PD0/FD8	52
6	VCC	*WAKEUP	51
7	GND	VCC	50
8	RDY0/*SLRD	RESET#	49
9	RDY1/*SLWR	GND	48
10	AVCC	PA7/*FLAGD/SLCS#	47
11	XTALOUT	PA6/PKTEND	46
12	XTALIN	PA5/FIFOADR1	45
13	AGND	PA4/FIFOADR0	44
14	AVCC	PA3/*WU2	43
15	DPLUS	PA2/*SLOE	42
16	DMINUS	PA1/INT1#	41
17	AGND	PA0/INT0#	40
18	VCC	VCC	39
19	GND	CTL2/*FLAGC	38
20	*IFCLK	CTL1/*FLAGB	37
21	RESERVED	CTL0/*FLAGA	36
22	SCL	GND	35
23	SDA	VCC	34
24	VCC	GND	33
25	PB0/FD0	PB7/FD7	32
26	PB1/FD1	PB6/FD6	31
27	PB2/FD2	PB5/FD5	30
28	PB3/FD3	PB4/FD4	29

* indicates programmable polarity

Figure 11. CY7C64713 56 pin QFN Pin Assignment



* indicates programmable polarity

CY7C64713 Pin Definitions

The FX1 Pin Definitions for CY7C64713 follow.^[6]

Table 8. FX1 Pin Definitions

128 TQFP	100 TQFP	56 SSOP	56 QFN	Name	Type	Default	Description
10	9	10	3	AVCC	Power	N/A	Analog VCC. Connect this pin to 3.3V power source. This signal provides power to the analog section of the chip.
17	16	14	7	AVCC	Power	N/A	Analog VCC. Connect this pin to 3.3V power source. This signal provides power to the analog section of the chip.
13	12	13	6	AGND	Ground	N/A	Analog Ground. Connect to ground with as short a path as possible.
20	19	17	10	AGND	Ground	N/A	Analog Ground. Connect to ground with as short a path as possible.
19	18	16	9	DMINUS	I/O/Z	Z	USB D- Signal. Connect to the USB D- signal.
18	17	15	8	DPLUS	I/O/Z	Z	USB D+ Signal. Connect to the USB D+ signal.
94				A0	Output	L	8051 Address Bus. This bus is driven at all times. When the 8051 is addressing the internal RAM it reflects the internal address.
95				A1	Output	L	
96				A2	Output	L	
97				A3	Output	L	
117				A4	Output	L	
118				A5	Output	L	
119				A6	Output	L	
120				A7	Output	L	
126				A8	Output	L	
127				A9	Output	L	
128				A10	Output	L	
21				A11	Output	L	
22				A12	Output	L	
23				A13	Output	L	
24				A14	Output	L	
25				A15	Output	L	
59				D0	I/O/Z	Z	8051 Data Bus. This bidirectional bus is high impedance when inactive, input for bus reads, and output for bus writes. The data bus is used for external 8051 program and data memory. The data bus is active only for external bus accesses, and is driven LOW in suspend.
60				D1	I/O/Z	Z	
61				D2	I/O/Z	Z	
62				D3	I/O/Z	Z	
63				D4	I/O/Z	Z	
86				D5	I/O/Z	Z	
87				D6	I/O/Z	Z	
88				D7	I/O/Z	Z	
39				PSEN#	Output	H	Program Store Enable. This active LOW signal indicates an 8051 code fetch from external memory. It is active for program memory fetches from 0x4000–0xFFFF when the EA pin is LOW, or from 0x0000–0xFFFF when the EA pin is HIGH.
34	28			BKPT	Output	L	Breakpoint. This pin goes active (HIGH) when the 8051 address bus matches the BPADDRH/L registers and breakpoints are enabled in the BREAKPT register (BPEN = 1). If the BPPULSE bit in the BREAKPT register is HIGH, this signal pulses HIGH for eight 12-/24-/48 MHz clocks. If the BPPULSE bit is LOW, the signal remains HIGH until the 8051 clears the BREAK bit (by writing '1' to it) in the BREAKPT register.

Note

6. Do not leave unused inputs floating. Tie either HIGH or LOW as appropriate. Pull outputs up or down to ensure signals at power up and in standby. Note that no pins must be driven when the device is powered down.

Table 8. FX1 Pin Definitions (continued)

128 TQFP	100 TQFP	56 SSOP	56 QFN	Name	Type	Default	Description
99	77	49	42	RESET#	Input	N/A	Active LOW Reset. Resets the entire chip. See the section “Reset and Wakeup” on page 6 for more details.
35				EA	Input	N/A	External Access. This pin determines where the 8051 fetches code between addresses 0x0000 and 0x3FFF. If EA = 0 the 8051 fetches this code from its internal RAM. IF EA = 1 the 8051 fetches this code from external memory.
12	11	12	5	XTALIN	Input	N/A	Crystal Input. Connect this signal to a 24 MHz parallel-resonant, fundamental mode crystal and load capacitor to GND. It is also correct to drive the XTALIN with an external 24 MHz square wave derived from another clock source. When driving from an external source, the driving signal must be a 3.3V square wave.
11	10	11	4	XTALOUT	Output	N/A	Crystal Output. Connect this signal to a 24 MHz parallel-resonant, fundamental mode crystal and load capacitor to GND. If an external clock is used to drive XTALIN, leave this pin open.
1	100	5	54	CLKOUT	O/Z	12 MHz	CLKOUT: 12, 24 or 48 MHz clock, phase locked to the 24 MHz input clock. The 8051 defaults to 12 MHz operation. The 8051 may three-state this output by setting CPUCS.1 = 1.
Port A							
82	67	40	33	PA0 or INT0#	I/O/Z	I (PA0)	Multiplexed pin whose function is selected by PORTACFG.0 PA0 is a bidirectional I/O port pin. INT0# is the active-LOW 8051 INT0 interrupt input signal, which is either edge triggered (IT0 = 1) or level triggered (IT0 = 0).
83	68	41	34	PA1 or INT1#	I/O/Z	I (PA1)	Multiplexed pin whose function is selected by: PORTACFG.1 PA1 is a bidirectional I/O port pin. INT1# is the active-LOW 8051 INT1 interrupt input signal, which is either edge triggered (IT1 = 1) or level triggered (IT1 = 0).
84	69	42	35	PA2 or SLOE	I/O/Z	I (PA2)	Multiplexed pin whose function is selected by two bits: IFCONFIG[1:0]. PA2 is a bidirectional I/O port pin. SLOE is an input-only output enable with programmable polarity (FIFOPINPOLAR.4) for the slave FIFOs connected to FD[7..0] or FD[15..0].
85	70	43	36	PA3 or WU2	I/O/Z	I (PA3)	Multiplexed pin whose function is selected by: WAKEUP.7 and OEA.3 PA3 is a bidirectional I/O port pin. WU2 is an alternate source for USB Wakeup , enabled by WU2EN bit (WAKEUP.1) and polarity set by WU2POL (WAKEUP.4). If the 8051 is in suspend and WU2EN = 1, a transition on this pin starts up the oscillator and interrupts the 8051 to allow it to exit the suspend mode. Asserting this pin inhibits the chip from suspending, if WU2EN = 1.
89	71	44	37	PA4 or FIFOADR0	I/O/Z	I (PA4)	Multiplexed pin whose function is selected by: IFCONFIG[1..0]. PA4 is a bidirectional I/O port pin. FIFOADR0 is an input-only address select for the slave FIFOs connected to FD[7..0] or FD[15..0].
90	72	45	38	PA5 or FIFOADR1	I/O/Z	I (PA5)	Multiplexed pin whose function is selected by: IFCONFIG[1..0]. PA5 is a bidirectional I/O port pin. FIFOADR1 is an input-only address select for the slave FIFOs connected to FD[7..0] or FD[15..0].

Table 8. FX1 Pin Definitions (continued)

128 TQFP	100 TQFP	56 SSOP	56 QFN	Name	Type	Default	Description
91	73	46	39	PA6 or PKTEND	I/O/Z	I (PA6)	Multiplexed pin whose function is selected by the IFCONFIG[1:0] bits. PA6 is a bidirectional I/O port pin. PKTEND is an input used to commit the FIFO packet data to the endpoint and whose polarity is programmable via FIFOPINPOLAR.5.
92	74	47	40	PA7 or FLAGD or SLCS#	I/O/Z	I (PA7)	Multiplexed pin whose function is selected by the IFCONFIG[1:0] and PORTACFG.7 bits. PA7 is a bidirectional I/O port pin. FLAGD is a programmable slave-FIFO output status flag signal. SLCS# gates all other slave FIFO enable/strobes
Port B							
44	34	25	18	PB0 or FD[0]	I/O/Z	I (PB0)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. PB0 is a bidirectional I/O port pin. FD[0] is the bidirectional FIFO/GPIF data bus.
45	35	26	19	PB1 or FD[1]	I/O/Z	I (PB1)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. PB1 is a bidirectional I/O port pin. FD[1] is the bidirectional FIFO/GPIF data bus.
46	36	27	20	PB2 or FD[2]	I/O/Z	I (PB2)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. PB2 is a bidirectional I/O port pin. FD[2] is the bidirectional FIFO/GPIF data bus.
47	37	28	21	PB3 or FD[3]	I/O/Z	I (PB3)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. PB3 is a bidirectional I/O port pin. FD[3] is the bidirectional FIFO/GPIF data bus.
54	44	29	22	PB4 or FD[4]	I/O/Z	I (PB4)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. PB4 is a bidirectional I/O port pin. FD[4] is the bidirectional FIFO/GPIF data bus.
55	45	30	23	PB5 or FD[5]	I/O/Z	I (PB5)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. PB5 is a bidirectional I/O port pin. FD[5] is the bidirectional FIFO/GPIF data bus.
56	46	31	24	PB6 or FD[6]	I/O/Z	I (PB6)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. PB6 is a bidirectional I/O port pin. FD[6] is the bidirectional FIFO/GPIF data bus.
57	47	32	25	PB7 or FD[7]	I/O/Z	I (PB7)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. PB7 is a bidirectional I/O port pin. FD[7] is the bidirectional FIFO/GPIF data bus.
PORT C							
72	57			PC0 or GPIFADR0	I/O/Z	I (PC0)	Multiplexed pin whose function is selected by PORTCCFG.0 PC0 is a bidirectional I/O port pin. GPIFADR0 is a GPIF address output pin.
73	58			PC1 or GPIFADR1	I/O/Z	I (PC1)	Multiplexed pin whose function is selected by PORTCCFG.1 PC1 is a bidirectional I/O port pin. GPIFADR1 is a GPIF address output pin.
74	59			PC2 or GPIFADR2	I/O/Z	I (PC2)	Multiplexed pin whose function is selected by PORTCCFG.2 PC2 is a bidirectional I/O port pin. GPIFADR2 is a GPIF address output pin.

Table 8. FX1 Pin Definitions (continued)

128 TQFP	100 TQFP	56 SSOP	56 QFN	Name	Type	Default	Description
75	60			PC3 or GPIFADR3	I/O/Z	1 (PC3)	Multiplexed pin whose function is selected by PORTCCFG.3 PC3 is a bidirectional I/O port pin. GPIFADR3 is a GPIF address output pin.
76	61			PC4 or GPIFADR4	I/O/Z	1 (PC4)	Multiplexed pin whose function is selected by PORTCCFG.4 PC4 is a bidirectional I/O port pin. GPIFADR4 is a GPIF address output pin.
77	62			PC5 or GPIFADR5	I/O/Z	1 (PC5)	Multiplexed pin whose function is selected by PORTCCFG.5 PC5 is a bidirectional I/O port pin. GPIFADR5 is a GPIF address output pin.
78	63			PC6 or GPIFADR6	I/O/Z	1 (PC6)	Multiplexed pin whose function is selected by PORTCCFG.6 PC6 is a bidirectional I/O port pin. GPIFADR6 is a GPIF address output pin.
79	64			PC7 or GPIFADR7	I/O/Z	1 (PC7)	Multiplexed pin whose function is selected by PORTCCFG.7 PC7 is a bidirectional I/O port pin. GPIFADR7 is a GPIF address output pin.
PORT D							
102	80	52	45	PD0 or FD[8]	I/O/Z	1 (PD0)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. FD[8] is the bidirectional FIFO/GPIF data bus.
103	81	53	46	PD1 or FD[9]	I/O/Z	1 (PD1)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. FD[9] is the bidirectional FIFO/GPIF data bus.
104	82	54	47	PD2 or FD[10]	I/O/Z	1 (PD2)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. FD[10] is the bidirectional FIFO/GPIF data bus.
105	83	55	48	PD3 or FD[11]	I/O/Z	1 (PD3)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. FD[11] is the bidirectional FIFO/GPIF data bus.
121	95	56	49	PD4 or FD[12]	I/O/Z	1 (PD4)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. FD[12] is the bidirectional FIFO/GPIF data bus.
122	96	1	50	PD5 or FD[13]	I/O/Z	1 (PD5)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. FD[13] is the bidirectional FIFO/GPIF data bus.
123	97	2	51	PD6 or FD[14]	I/O/Z	1 (PD6)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. FD[14] is the bidirectional FIFO/GPIF data bus.
124	98	3	52	PD7 or FD[15]	I/O/Z	1 (PD7)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. FD[15] is the bidirectional FIFO/GPIF data bus.
Port E							
108	86			PE0 or T0OUT	I/O/Z	1 (PE0)	Multiplexed pin whose function is selected by the PORTECFG.0 bit. PE0 is a bidirectional I/O port pin. T0OUT is an active HIGH signal from 8051 Timer-counter0. T0OUT outputs a high level for one CLKOUT clock cycle when Timer0 overflows. If Timer0 is operated in Mode 3 (two separate timer/counters), T0OUT is active when the low byte timer/counter overflows.

Table 8. FX1 Pin Definitions (continued)

128 TQFP	100 TQFP	56 SSOP	56 QFN	Name	Type	Default	Description
109	87			PE1 or T1OUT	I/O/Z	1 (PE1)	Multiplexed pin whose function is selected by the PORTECFG.1 bit. PE1 is a bidirectional I/O port pin. T1OUT is an active HIGH signal from 8051 Timer-counter1. T1OUT outputs a high level for one CLKOUT clock cycle when Timer1 overflows. If Timer1 is operated in Mode 3 (two separate timer/counters), T1OUT is active when the low byte timer/counter overflows.
110	88			PE2 or T2OUT	I/O/Z	1 (PE2)	Multiplexed pin whose function is selected by the PORTECFG.2 bit. PE2 is a bidirectional I/O port pin. T2OUT is the active HIGH output signal from 8051 Timer2. T2OUT is active (HIGH) for one clock cycle when Timer/Counter 2 overflows.
111	89			PE3 or RXD0OUT	I/O/Z	1 (PE3)	Multiplexed pin whose function is selected by the PORTECFG.3 bit. PE3 is a bidirectional I/O port pin. RXD0OUT is an active HIGH signal from 8051 UART0. If RXD0OUT is selected and UART0 is in Mode 0, this pin provides the output data for UART0 only when it is in sync mode. Otherwise it is a 1.
112	90			PE4 or RXD1OUT	I/O/Z	1 (PE4)	Multiplexed pin whose function is selected by the PORTECFG.4 bit. PE4 is a bidirectional I/O port pin. RXD1OUT is an active HIGH output from 8051 UART1. When the RXD1OUT is selected and UART1 is in Mode 0, this pin provides the output data for UART1 only when it is in sync mode. In Modes 1, 2, and 3, this pin is HIGH.
113	91			PE5 or INT6	I/O/Z	1 (PE5)	Multiplexed pin whose function is selected by the PORTECFG.5 bit. PE5 is a bidirectional I/O port pin. INT6 is the 8051 INT6 interrupt request input signal. The INT6 pin is edge-sensitive, active HIGH.
114	92			PE6 or T2EX	I/O/Z	1 (PE6)	Multiplexed pin whose function is selected by the PORTECFG.6 bit. PE6 is a bidirectional I/O port pin. T2EX is an active HIGH input signal to the 8051 Timer2. T2EX reloads timer 2 on its falling edge. T2EX is active only if the EXEN2 bit is set in T2CON.
115	93			PE7 or GPIFADR8	I/O/Z	1 (PE7)	Multiplexed pin whose function is selected by the PORTECFG.7 bit. PE7 is a bidirectional I/O port pin. GPIFADR8 is a GPIF address output pin.
4	3	8	1	RDY0 or SLRD	Input	N/A	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. RDY0 is a GPIF input signal. SLRD is the input-only read strobe with programmable polarity (FIFOPINPOLAR.3) for the slave FIFOs connected to FD[7..0] or FD[15..0].
5	4	9	2	RDY1 or SLWR	Input	N/A	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. RDY1 is a GPIF input signal. SLWR is the input-only write strobe with programmable polarity (FIFOPINPOLAR.2) for the slave FIFOs connected to FD[7..0] or FD[15..0].
6	5			RDY2	Input	N/A	RDY2 is a GPIF input signal.
7	6			RDY3	Input	N/A	RDY3 is a GPIF input signal.
8	7			RDY4	Input	N/A	RDY4 is a GPIF input signal.
9	8			RDY5	Input	N/A	RDY5 is a GPIF input signal.

Table 8. FX1 Pin Definitions (continued)

128 TQFP	100 TQFP	56 SSOP	56 QFN	Name	Type	Default	Description
69	54	36	29	CTL0 or FLAGA	O/Z	H	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. CTL0 is a GPIF control output. FLAGA is a programmable slave-FIFO output status flag signal. Defaults to programmable for the FIFO selected by the FIFOADR[1:0] pins.
70	55	37	30	CTL1 or FLAGB	O/Z	H	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. CTL1 is a GPIF control output. FLAGB is a programmable slave-FIFO output status flag signal. Defaults to FULL for the FIFO selected by the FIFOADR[1:0] pins.
71	56	38	31	CTL2 or FLAGC	O/Z	H	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. CTL2 is a GPIF control output. FLAGC is a programmable slave-FIFO output status flag signal. Defaults to EMPTY for the FIFO selected by the FIFOADR[1:0] pins.
66	51			CTL3	O/Z	H	CTL3 is a GPIF control output.
67	52			CTL4	Output	H	CTL4 is a GPIF control output.
98	76			CTL5	Output	H	CTL5 is a GPIF control output.
32	26	20	13	IFCLK	I/O/Z	Z	Interface Clock, used for synchronously clocking data into or out of the slave FIFOs. IFCLK also serves as a timing reference for all slave FIFO control signals and GPIF. When internal clocking is used (IFCONFIG.7 = 1) the IFCLK pin is configured to output 30/48 MHz by bits IFCONFIG.5 and IFCONFIG.6. IFCLK may be inverted, whether internally or externally sourced, by setting the bit IFCONFIG.4 = 1.
28	22			INT4	Input	N/A	INT4 is the 8051 INT4 interrupt request input signal. The INT4 pin is edge-sensitive, active HIGH.
106	84			INT5#	Input	N/A	INT5# is the 8051 INT5 interrupt request input signal. The INT5 pin is edge-sensitive, active LOW.
31	25			T2	Input	N/A	T2 is the active-HIGH T2 input signal to 8051 Timer2, which provides the input to Timer2 when C/T2 = 1. When C/T2 = 0, Timer2 does not use this pin.
30	24			T1	Input	N/A	T1 is the active-HIGH T1 signal for 8051 Timer1, which provides the input to Timer1 when C/T1 is 1. When C/T1 is 0, Timer1 does not use this bit.
29	23			T0	Input	N/A	T0 is the active-HIGH T0 signal for 8051 Timer0, which provides the input to Timer0 when C/T0 is 1. When C/T0 is 0, Timer0 does not use this bit.
53	43			RXD1	Input	N/A	RXD1 is an active-HIGH input signal for 8051 UART1, which provides data to the UART in all modes.
52	42			TXD1	Output	H	TXD1 is an active-HIGH output pin from 8051 UART1, which provides the output clock in sync mode, and the output data in async mode.
51	41			RXD0	Input	N/A	RXD0 is the active-HIGH RXD0 input to 8051 UART0, which provides data to the UART in all modes.
50	40			TXD0	Output	H	TXD0 is the active-HIGH TXD0 output from 8051 UART0, which provides the output clock in sync mode, and the output data in async mode.
42				CS#	Output	H	CS# is the active-LOW chip select for external memory.
41	32			WR#	Output	H	WR# is the active-LOW write strobe output for external memory.
40	31			RD#	Output	H	RD# is the active-LOW read strobe output for external memory.
38				OE#	Output	H	OE# is the active LOW output enable for external memory.

Table 8. FX1 Pin Definitions (continued)

128 TQFP	100 TQFP	56 SSOP	56 QFN	Name	Type	Default	Description
33	27	21	14	Reserved	Input	N/A	Reserved. Connect to ground.
101	79	51	44	WAKEUP	Input	N/A	USB Wakeup. If the 8051 is in suspend, asserting this pin starts up the oscillator and interrupts the 8051 to allow it to exit the suspend mode. Holding WAKEUP asserted inhibits the EZ-USB FX1 chip from suspending. This pin has programmable polarity (WAKEUP.4).
36	29	22	15	SCL	OD	Z	Clock for the I ² C interface. Connect to VCC with a 2.2K resistor, even if no I ² C peripheral is attached.
37	30	23	16	SDA	OD	Z	Data for I ² C interface. Connect to VCC with a 2.2K resistor, even if no I²C peripheral is attached.
2	1	6	55	VCC	Power	N/A	VCC. Connect to 3.3V power source.
26	20	18	11	VCC	Power	N/A	VCC. Connect to 3.3V power source.
43	33	24	17	VCC	Power	N/A	VCC. Connect to 3.3V power source.
48	38			VCC	Power	N/A	VCC. Connect to 3.3V power source.
64	49	34	27	VCC	Power	N/A	VCC. Connect to 3.3V power source.
68	53			VCC	Power	N/A	VCC. Connect to 3.3V power source.
81	66	39	32	VCC	Power	N/A	VCC. Connect to 3.3V power source.
100	78	50	43	VCC	Power	N/A	VCC. Connect to 3.3V power source.
107	85			VCC	Power	N/A	VCC. Connect to 3.3V power source.
3	2	7	56	GND	Ground	N/A	Ground.
27	21	19	12	GND	Ground	N/A	Ground.
49	39			GND	Ground	N/A	Ground.
58	48	33	26	GND	Ground	N/A	Ground.
65	50	35	28	GND	Ground	N/A	Ground.
80	65			GND	Ground	N/A	Ground.
93	75	48	41	GND	Ground	N/A	Ground.
116	94			GND	Ground	N/A	Ground.
125	99	4	53	GND	Ground	N/A	Ground.
14	13			NC	N/A	N/A	No Connect. This pin must be left open.
15	14			NC	N/A	N/A	No Connect. This pin must be left open.
16	15			NC	N/A	N/A	No Connect. This pin must be left open.

Register Summary

FX1 register bit definitions are described in the [EZ-USB TRM](#) in greater detail.

Table 9. FX1 Register Summary

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
GPIF Waveform Memories													
E400	128	WAVEDATA	GPIF Waveform Descriptor 0, 1, 2, 3 data	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
E480	128	reserved											
GENERAL CONFIGURATION													
E600	1	CPUCS	CPU Control & Status	0	0	PORTCSTB	CLKSPD1	CLKSPD0	CLKINV	CLKOE	8051RES	00000010	rrbbbbr
E601	1	IFCONFIG	Interface Configuration (Ports, GPIF, slave FIFOs)	IFCLKSRC	3048MHZ	IFCLKOE	IFCLKPOL	ASYN	GSTATE	IFCFG1	IFCFG0	10000000	RW
E602	1	PINFLAGSAB ^[7]	Slave FIFO FLAGA and FLAGB Pin Configuration	FLAGB3	FLAGB2	FLAGB1	FLAGB0	FLAGA3	FLAGA2	FLAGA1	FLAGA0	00000000	RW
E603	1	PINFLAGSCD ^[7]	Slave FIFO FLAGC and FLAGD Pin Configuration	FLAGD3	FLAGD2	FLAGD1	FLAGD0	FLAGC3	FLAGC2	FLAGC1	FLAGC0	00000000	RW
E604	1	FIFORESET ^[7]	Restore FIFOs to default state	NAKALL	0	0	0	EP3	EP2	EP1	EP0	xxxxxxxx	W
E605	1	BREAKPT	Breakpoint Control	0	0	0	0	BREAK	BPPULSE	BPEN	0	00000000	rrrrbbbr
E606	1	BPADDRH	Breakpoint Address H	A15	A14	A13	A12	A11	A10	A9	A8	xxxxxxxx	RW
E607	1	BPADDRL	Breakpoint Address L	A7	A6	A5	A4	A3	A2	A1	A0	xxxxxxxx	RW
E608	1	UART230	230 Kbaud internally generated ref. clock	0	0	0	0	0	0	230UART1	230UART0	00000000	rrrrrb
E609	1	FIFOPINPOLAR ^[7]	Slave FIFO Interface pins polarity	0	0	PKTEND	SLOE	SLRD	SLWR	EF	FF	00000000	rrbbbbbb
E60A	1	REVID	Chip Revision	rv7	rv6	rv5	rv4	rv3	rv2	rv1	rv0	RevA 00000001	R
E60B	1	REVCTL ^[7]	Chip Revision Control	0	0	0	0	0	0	dyn_out	enh_pkt	00000000	rrrrrb
UDMA													
E60C	1	GPIFHOLDAMOUNT	MSTB Hold Time (for UDMA)	0	0	0	0	0	0	HOLDTIME1	HOLDTIME0	00000000	rrrrrb
	3	reserved											
ENDPOINT CONFIGURATION													
E610	1	EP1OUTCFG	Endpoint 1-OUT Configuration	VALID	0	TYPE1	TYPE0	0	0	0	0	10100000	rbbrrrr
E611	1	EP1INCFG	Endpoint 1-IN Configuration	VALID	0	TYPE1	TYPE0	0	0	0	0	10100000	rbbrrrr
E612	1	EP2CFG	Endpoint 2 Configuration	VALID	DIR	TYPE1	TYPE0	SIZE	0	BUF1	BUF0	10100010	bbbbrbbr
E613	1	EP4CFG	Endpoint 4 Configuration	VALID	DIR	TYPE1	TYPE0	0	0	0	0	10100000	bbbbrrr
E614	1	EP6CFG	Endpoint 6 Configuration	VALID	DIR	TYPE1	TYPE0	SIZE	0	BUF1	BUF0	11100010	bbbbrbbr
E615	1	EP8CFG	Endpoint 8 Configuration	VALID	DIR	TYPE1	TYPE0	0	0	0	0	11100000	bbbbrrr
	2	reserved											
E618	1	EP2FIFOCFG ^[7]	Endpoint 2 / slave FIFO configuration	0	INFM1	OEP1	AUTOOUT	AUTOIN	ZEROLENIN	0	WORDWIDE	00000101	rbbbbbrb
E619	1	EP4FIFOCFG ^[7]	Endpoint 4 / slave FIFO configuration	0	INFM1	OEP1	AUTOOUT	AUTOIN	ZEROLENIN	0	WORDWIDE	00000101	rbbbbbrb
E61A	1	EP6FIFOCFG ^[7]	Endpoint 6 / slave FIFO configuration	0	INFM1	OEP1	AUTOOUT	AUTOIN	ZEROLENIN	0	WORDWIDE	00000101	rbbbbbrb
E61B	1	EP8FIFOCFG ^[7]	Endpoint 8 / slave FIFO configuration	0	INFM1	OEP1	AUTOOUT	AUTOIN	ZEROLENIN	0	WORDWIDE	00000101	rbbbbbrb
E61C	4	reserved											
E620	1	EP2AUTOINLENH ^[7]	Endpoint 2 AUTOIN Packet Length H	0	0	0	0	0	PL10	PL9	PL8	00000010	rrrrrb
E621	1	EP2AUTOINLENL ^[7]	Endpoint 2 AUTOIN Packet Length L	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	00000000	RW
E622	1	EP4AUTOINLENH ^[7]	Endpoint 4 AUTOIN Packet Length H	0	0	0	0	0	PL9	PL8	PL7	00000010	rrrrrb
E623	1	EP4AUTOINLENL ^[7]	Endpoint 4 AUTOIN Packet Length L	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	00000000	RW
E624	1	EP6AUTOINLENH ^[7]	Endpoint 6 AUTOIN Packet Length H	0	0	0	0	0	PL10	PL9	PL8	00000010	rrrrrb
E625	1	EP6AUTOINLENL ^[7]	Endpoint 6 AUTOIN Packet Length L	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	00000000	RW
E626	1	EP8AUTOINLENH ^[7]	Endpoint 8 AUTOIN Packet Length H	0	0	0	0	0	PL9	PL8	PL7	00000010	rrrrrb
E627	1	EP8AUTOINLENL ^[7]	Endpoint 8 AUTOIN Packet Length L	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	00000000	RW
E628	1	ECCCFG	ECC Configuration	0	0	0	0	0	0	0	ECCM	00000000	rrrrrb
E629	1	ECCRESET	ECC Reset	x	x	x	x	x	x	x	x	00000000	W
E62A	1	ECC1B0	ECC1 Byte 0 Address	LINE15	LINE14	LINE13	LINE12	LINE11	LINE10	LINE9	LINE8	11111111	R
E62B	1	ECC1B1	ECC1 Byte 1 Address	LINE7	LINE6	LINE5	LINE4	LINE3	LINE2	LINE1	LINE0	11111111	R
E62C	1	ECC1B2	ECC1 Byte 2 Address	COL5	COL4	COL3	COL2	COL1	COL0	LINE17	LINE16	11111111	R
E62D	1	ECC2B0	ECC2 Byte 0 Address	LINE15	LINE14	LINE13	LINE12	LINE11	LINE10	LINE9	LINE8	11111111	R
E62E	1	ECC2B1	ECC2 Byte 1 Address	LINE7	LINE6	LINE5	LINE4	LINE3	LINE2	LINE1	LINE0	11111111	R

Note

7. Read and writes to these register may require synchronization delay, see the section "Synchronization Delay" in the [EZ-USB TRM](#).

Table 9. FX1 Register Summary (continued)

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
E62F	1	ECC2B2	ECC2 Byte 2 Address	COL5	COL4	COL3	COL2	COL1	COL0	0	0	11111111	R
E630	1	EP2FIFOPFH ^[7]	Endpoint 2 / slave FIFO Programmable Flag H ISO Mode	DECIS	PKTSTAT	IN: PKTS[2] OUT:PFC12	IN: PKTS[1] OUT:PFC11	IN: PKTS[0] OUT:PFC10	0	PFC9	PFC8	10001000	bbbbrb
E630	1	EP2FIFOPFH ^[7]	Endpoint 2 / slave FIFO Programmable Flag H Non-ISO Mode	DECIS	PKTSTAT	OUT:PFC12	OUT:PFC11	OUT:PFC10	0	PFC9	IN:PKTS[2] OUT:PFC8	10001000	bbbbrb
E631	1	EP2FIFOPFL ^[7]	Endpoint 2 / slave FIFO Programmable Flag L	IN:PKTS[1] OUT:PFC7	IN:PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E632	1	EP4FIFOPFH ^[7]	Endpoint 4 / slave FIFO Programmable Flag H ISO Mode	DECIS	PKTSTAT	0	IN: PKTS[1] OUT:PFC10	IN: PKTS[0] OUT:PFC9	0	0	PFC8	10001000	bbrbrr
E632	1	EP4FIFOPFH ^[7]	Endpoint 4 / slave FIFO Programmable Flag H Non-ISO Mode	DECIS	PKTSTAT	0	OUT:PFC10	OUT:PFC9	0	0	PFC8	10001000	bbrbrr
E633	1	EP4FIFOPFL ^[7]	Endpoint 4 / slave FIFO Programmable Flag L	IN: PKTS[1] OUT:PFC7	IN: PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E634	1	EP6FIFOPFH ^[7]	Endpoint 6 / slave FIFO Programmable Flag H ISO Mode	DECIS	PKTSTAT	INPKTS[2] OUT:PFC12	IN: PKTS[1] OUT:PFC11	IN: PKTS[0] OUT:PFC10	0	PFC9	PFC8	00001000	bbbbrb
E634	1	EP6FIFOPFH ^[7]	Endpoint 6 / slave FIFO Programmable Flag H Non-ISO Mode	DECIS	PKTSTAT	OUT:PFC12	OUT:PFC11	OUT:PFC10	0	PFC9	IN:PKTS[2] OUT:PFC8	00001000	bbbbrb
E635	1	EP6FIFOPFL ^[7]	Endpoint 6 / slave FIFO Programmable Flag L	IN:PKTS[1] OUT:PFC7	IN:PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E636	1	EP8FIFOPFH ^[7]	Endpoint 8 / slave FIFO Programmable Flag H ISO Mode	DECIS	PKTSTAT	0	IN: PKTS[1] OUT:PFC10	IN: PKTS[0] OUT:PFC9	0	0	PFC8	00001000	bbrbrr
E636	1	EP8FIFOPFH ^[7]	Endpoint 8 / slave FIFO Programmable Flag H Non-ISO Mode	DECIS	PKTSTAT	0	OUT:PFC10	OUT:PFC9	0	0	PFC8	00001000	bbrbrr
E637	1	EP8FIFOPFL ^[7]	Endpoint 8 / slave FIFO Programmable Flag L	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E637	1	EP8FIFOPFL ^[7]	Endpoint 8 / slave FIFO Programmable Flag L Non-ISO Mode	IN: PKTS[1] OUT:PFC7	IN: PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
	8	reserved											
E640	1	reserved											
E641	1	reserved											
E642	1	reserved											
E643	1	reserved											
E644	4	reserved											
E648	1	INPKTEND ^[7]	Force IN Packet End	Skip	0	0	0	EP3	EP2	EP1	EP0	xxxxxxx	W
E649	7	OUTPKTEND ^[7]	Force OUT Packet End	Skip	0	0	0	EP3	EP2	EP1	EP0	xxxxxxx	W
		INTERRUPTS											
E650	1	EP2FIFOIE ^[7]	Endpoint 2 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGE PF	PF	EF	FF	00000000	RW
E651	1	EP2FIFOIRQ ^[7,8]	Endpoint 2 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00001111	rrrrbb
E652	1	EP4FIFOIE ^[7]	Endpoint 4 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGE PF	PF	EF	FF	00000000	RW
E653	1	EP4FIFOIRQ ^[7,8]	Endpoint 4 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00001111	rrrrbb
E654	1	EP6FIFOIE ^[7]	Endpoint 6 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGE PF	PF	EF	FF	00000000	RW
E655	1	EP6FIFOIRQ ^[7,8]	Endpoint 6 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00001110	rrrrbb
E656	1	EP8FIFOIE ^[7]	Endpoint 8 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGE PF	PF	EF	FF	00000000	RW
E657	1	EP8FIFOIRQ ^[7,8]	Endpoint 8 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00001110	rrrrbb
E658	1	IBNIE	IN-BULK-NAK Interrupt Enable	0	0	EP8	EP6	EP4	EP2	EP1	EP0	00000000	RW

Note

- 8. SFRs not part of the standard 8051 architecture.
- 9. The register can only be reset. It cannot be set.