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CY7C67300

EZ-Host™ Programmable Embedded USB Host and Peripheral Controller with Automotive AEC Grade Support

EZ-Host Features

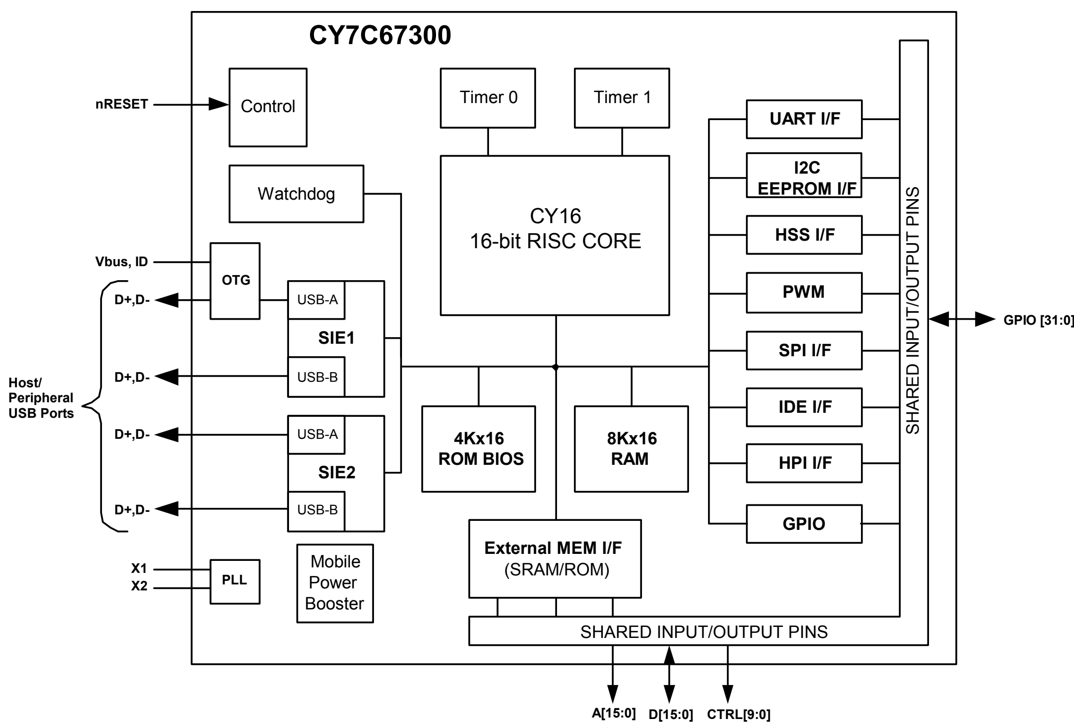
- Single chip programmable USB dual-role (Host/Peripheral) controller with two configurable Serial Interface Engines (SIEs) and four USB ports
- Support for USB On-The-Go (OTG) protocol
- On-chip 48 MHz 16-bit processor with dynamically switchable clock speed
- Configurable IO block supporting a variety of IO options or up to 32 bits of General Purpose IO (GPIO)
- 4K x 16 internal masked ROM containing built in BIOS that supports a communication ready state with access to I^2C™ EEPROM Interface, external ROM, UART, or USB
- 8K x 16 internal RAM for code and data buffering
- Extended memory interface port for external SRAM and ROM
- 16-bit parallel Host Port Interface (HPI) with a DMA/mailbox data path for an external processor to directly access all of the on-chip memory and control on-chip SIEs
- Fast serial port supports from 9600 baud to 2.0M baud
- SPI support in both master and slave
- On-chip 16-bit DMA/mailbox data path interface
- Supports 12 MHz external crystal or clock
- 3.3V operation
- Automotive AEC grade option (–40°C to 85°C)
- Package option—100-pin TQFP

Typical Applications

EZ-Host is a very powerful and flexible dual role USB controller that supports a wide variety of applications. It is primarily intended to enable host capability in applications such as:

- Set top boxes
- Printers
- KVM switches
- Kiosks
- Automotive applications
- Wireless access points

Block Diagram



Errata: For information on silicon errata, see "Errata" on page 107. Details include trigger conditions, devices affected, and proposed workaround.

Contents

Introduction

EZ-Host™ (CY7C67300) is Cypress Semiconductor's first full-speed, low cost multiport host/peripheral controller. EZ-Host is designed to easily interface to most high performance CPUs to add USB host functionality. EZ-Host has its own 16-bit RISC processor to act as a coprocessor or operate in standalone mode. EZ-Host also has a programmable IO interface block allowing a wide range of interface options.

Functional Overview

An overview of the processor core components are presented in this section.

Processor Core

EZ-Host has a general purpose 16-bit embedded RISC processor that runs at 48 MHz.

Clocking

EZ-Host requires a 12 MHz source for clocking. Either an external crystal or TTL level oscillator may be used. EZ-Host has an internal PLL that produces a 48 MHz internal clock from the 12 MHz source.

Memory

EZ-Host has a built in 4K × 16 masked ROM and an 8K × 16 internal RAM. The masked ROM contains the EZ-Host BIOS. The internal RAM can be used for program code or data.

Interrupts

EZ-Host provides 128 interrupt vectors. The first 48 vectors are hardware interrupts and the following 80 vectors are software interrupts.

General Timers and Watchdog Timer

EZ-Host has two built in programmable timers and a Watchdog timer. All three timers can generate an interrupt to the EZ-Host.

Power Management

EZ-Host has one main power saving mode, Sleep. Sleep mode pauses all operations and provides the lowest power state.

Interface Descriptions

EZ-Host has a wide variety of interface options for connectivity. With several interface options available, EZ-Host can act as a seamless data transport between many different types of devices.

See Table 1 and Table 2 on page 4 to understand how the interfaces share pins and which can coexist. Note that some interfaces have more then one possible port location selectable through the GPIO control register [0xC006]. General guidelines for interfaces are as follows:

- HPI and IDE interfaces are mutually exclusive.
- If 16-bit external memory is required, then HSS and SPI default locations must be used.
- I^2C EEPROM and OTG do not conflict with any interfaces.

Table 1. Interface Options for GPIO Pins

GPIO Pins	HPI	IDE	PWM	HSS	SPI	UART	I2C	OTG
GPIO31							SCL/SDA	
GPIO30							SCL/SDA	
GPIO29								OTGID
GPIO28						TX		
GPIO27						RX		
GPIO26			PWM3	CTS[1]				
GPIO25								
GPIO24	INT	IOREADY						
GPIO23	nRD	IOR						
GPIO22	nWR	IOW						
GPIO21	nCS							
GPIO20	A1	CS1						
GPIO19	A0	CS0						
GPIO18		A2	PWM2	RTS[1]				
GPIO17		A1	PWM1	RXD[1]				
GPIO16		A0	PWM0	TXD[1]				
GPIO15	D15	D15						
GPIO14	D14	D14						
GPIO13	D13	D13						
GPIO12	D12	D12						
GPIO11	D11	D11			MOSI[1]			
GPIO10	D10	D10			SCK[1]			
GPIO9	D9	D9			nSSI[1]			
GPIO8	D8	D8			MISO[1]			
GPIO7	D7	D7						
GPIO6	D6	D6						
GPIO5	D5	D5						
GPIO4	D4	D4						
GPIO3	D3	D3						
GPIO2	D2	D2						
GPIO1	D1	D1						
GPIO0	D0	D0						

Table 2. Interface Options for External Memory Bus Pins

MEM Pins	HPI	IDE	PWM	HSS	SPI	UART	I2C	OTG
D15				CTS[2]				
D14				RTS[2]				
D13				RXD[2]				
D12				TXD[2]				
D11					MOSI[2]			
D10					SCK[2]			
D9					nSSI[2]			
D8					MISO[2]			
D[7:0]								
A[18:0]								
CONTROL								

Notes
1. Default interface location.
2. Alternate interface location.

USB Interface

EZ-Host has two built in Host/Peripheral SIEs and four USB transceivers that meet the USB 2.0 specification requirements for full and low speed (high speed is not supported). In Host mode, EZ-Host supports four downstream ports, each support control, interrupt, bulk, and isochronous transfers. In Peripheral mode, EZ-Host supports one peripheral port with eight endpoints for each of the two SIEs. Endpoint 0 is dedicated as the control endpoint and only supports control transfers. Endpoints 1 though 7 support interrupt, bulk (up to 64 bytes/packet), or isochronous transfers (up to 1023 Bytes/packet size). EZ-Host also supports a combination of Host and Peripheral ports simultaneously as shown in Table 3 on page 5.

Table 3. USB Port Configuration Options

Port Configurations	Port 1A	Port 1B	Port 2A	Port 2B
OTG	OTG	–	–	–
OTG + 2 Hosts	OTG	–	Host	Host
OTG + 1 Host	OTG	–	Host	–
OTG + 1 Host	OTG	–	–	Host
OTG + 1 Peripheral	OTG	–	Peripheral	–
OTG + 1 Peripheral	OTG	–	–	Peripheral
4 Hosts	Host	Host	Host	Host
3 Hosts	Any Combination of Ports			
2 Hosts	Any Combination of Ports			
1 Host	Any Port			
2 Hosts + 1 Peripheral	Host	Host	Peripheral	–
2 Hosts + 1 Peripheral	Host	Host	–	Peripheral
2 Hosts + 1 Peripheral	Peripheral	–	Host	Host
2 Hosts + 1 Peripheral	–	Peripheral	Host	Host
1 Host + 1 Peripheral	Host	–	Peripheral	–
1 Host + 1 Peripheral	Host	–	–	Peripheral
1 Host + 1 Peripheral	–	Host	–	Peripheral
1 Host + 1 Peripheral	–	Host	Peripheral	–
1 Host + 1 Peripheral	Peripheral	–	Host	–
1 Host + 1 Peripheral	Peripheral	–	–	Host
1 Host + 1 Peripheral	–	Peripheral	–	Host
1 Host + 1 Peripheral	–	Peripheral	Host	–
2 Peripherals	Peripheral	–	Peripheral	–
2 Peripherals	Peripheral	–	–	Peripheral
2 Peripherals	–	Peripheral	–	Peripheral
2 Peripherals	–	Peripheral	Peripheral	–
1 Peripheral	Any Port			

USB Features

- USB 2.0-compliant for full and low speed
- Up to four downstream USB host ports
- Up to two upstream USB peripheral ports
- Configurable endpoint buffers (pointer and length), must reside in internal RAM
- Up to eight available peripheral endpoints (one control endpoint)
- Supports control, interrupt, bulk, and isochronous transfers
- Internal DMA channels for each endpoint
- Internal pull up and pull down resistors
- Internal series termination resistors on USB data lines

USB Pins

Table 4. USB Interface Pins

Pin Name	Pin Number
DM1A	22
DP1A	23
DM1B	18
DP1B	19
DM2A	9
DP2A	10
DM2B	4
DP2B	5

OTG Interface

EZ-Host has one USB port that is compatible with the USB On-The-Go supplement to the USB 2.0 specification. The USB OTG port has a various hardware features to support Session Request Protocol (SRP) and Host Negotiation Protocol (HNP). OTG is only supported on USB PORT 1A.

OTG Features

- Internal charge pump to supply and control VBUS
- VBUS valid status (above 4.4V)
- VBUS status for 2.4V< VBUS <0.8V
- ID pin status
- Switchable 2K ohm internal discharge resistor on VBUS
- Switchable 500 ohm internal pull up resistor on VBUS
- Individually switchable internal pull up and pull down resistors on the USB data lines

OTG Pins

Table 5. OTG Interface Pins

Pin Name	Pin Number
DM1A	22
DP1A	23
OTGVBUS	11
OTGID	41
CSwitchA	13
CSwitchB	12

External Memory Interface

EZ-Host provides a robust interface to a wide variety of external memory arrays. All available external memory array locations can contain either code or data. The CY16 RISC processor directly addresses a flat memory space from 0x0000 to 0xFFFF.

External Memory Interface Features

- Supports 8-bit or 16-bit SRAM or ROM
- SRAM or ROM can be used for code or data space
- Direct addressing of SRAM or ROM
- Two external memory mapped page registers

External Memory Access Strobes

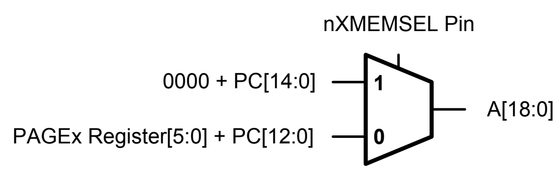
Access to external memory is sampled asynchronously on the rising edge of strobes with a minimum of one wait state cycle. Up to seven wait state cycles may be inserted for external memory access. Each additional wait state cycle stretches the external memory access time by 21 ns (you must be running in internal memory when changing wait states). An external memory device with 12 ns access time is necessary to support 48 MHz code execution.

Page Registers

EZ-Host allows extended data or program code to be stored in external SRAM, or ROM. The total size of extended memory can be up to 512K bytes. The CY16 processor can access extended memory via two address regions of 0x8000-0x9FFF and 0xA000-0xBFFF. The page register 0xC018 can be used to control the address region 0x8000-0x9FFF and the page register 0xC01A controls the address region of 0xA000-0xBFFF.

Figure 1 illustrates that when the nXMEMSEL pin is asserted the upper CPU address pins are driven by the contents of the Page x registers.

Figure 1. Page n Registers External Address Pins Logic



Where:
x = 1 or 2
PC = Program Counter
A = CPU Address Bus

Note:
PAGE 1 Register Active Range = 8000h to 9FFFh
PAGE 2 Register Active Range = A000h to BFFFh
nXMEMSEL Pin Active Range = 8000h to BFFFh

Merge Mode

Merge modes enabled through the External Memory Control register [0xC03A] allow combining of external memory regions in accordance with the following:

- nXMEMSEL is active from 0x8000 to 0xBFFF
- nXRAMSEL is active from 0x4000 to 0x7FFF when RAM Merge is disabled; nXRAMSEL is active from 0x4000 to 0xBFFF when RAM Merge is enabled
- nXROMSEL is active from 0xC100 to 0xDFFF when ROM Merge is disabled; nXROMSEL is active from 0x8000 to 0xDFFF (excluding the 0xC000 to 0xC0FF area) when ROM Merge is enabled

Program Memory Hole Description

Code residing in the 0xC000-0xC0FF address space is not accessible by the CPU.

DMA to External Memory Prohibited

EZ-Host supports an internal DMA engine to rapidly move data between different functional blocks within the chip. This DMA engine is used for SIE1, SIE2, HPI, SPI, HSS, and IDE but it can only transfer data between the specified block and internal RAM or ROM. Setting up the DMA engine to transfer to or from an external memory space might result in internal RAM data corruption because the hardware (for example, HSS/HPI/SIE1/SIE2/IDE) does not explicitly check the address range. For example, setting up a DMA transfer to external address 0x8000 might result in a DMA transfer into address 0x0000.

External Memory Related Resource Considerations:

- By default A[18:15] are not available for general addressing and are driven high on power up. The Upper Address Enable register must be written appropriately to enable A[18:15] for general addressing purposes.
- 47K ohm external pull up on pin A15 for 12 MHz crystal operation.
- During the 3 ms BIOS boot procedure the CPU external memory bus is active.
- ROM boot load value 0xC3B6 located at 0xC100.
- HPI, HSS, SPI, SIE1, SIE2, and IDE cannot DMA to external memory arrays.
- Page 1 banking is always enabled and is in effect from 0x8000 to 0x9FFF.
- Page 2 banking is always enabled and is in effect from 0xA000 to 0xBFFF.
- CPU memory bus strobes may wiggle when chip selects are inactive.

External Memory Interface Pins

Table 6. External Memory Interface Pins

Pin Name	Pin Number
nWR	64
nRD	62
nXMEMSEL (optional nCS)	34
nXROMSEL (ROM nCS)	35
nXRAMSEL (RAM nCS)	36
A18	95
A17	96
A16	97
A15	38
A14	33
A13	32
A12	31
A11	30
A10	27
A9	25
A8	24
A7	20
A6	17
A5	8
A4	7
A3	3
A2	2
A1	1
nBEL/A0	99
nBEH	98
D15	67
D14	68
D13	69
D12	70
D11	71
D10	72
D9	73
D8	74
D7	76
D6	77
D5	78
D4	79
D3	80
D2	81
D1	82
D0	83

External Memory Interface Block Diagrams

Figure 2 illustrates how to connect a 64k × 8 memory array (SRAM/ROM) to the EZ-Host external memory interface.

Figure 2. Interfacing to 64k × 8 Memory Array

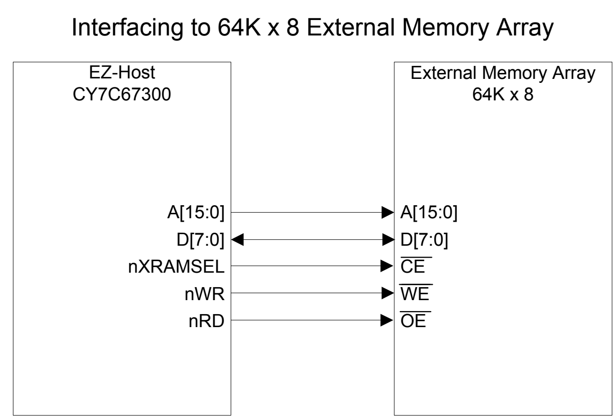


Figure 3 illustrates the interface for connecting a 16-bit ROM or 16-bit RAM to the EZ-Host external memory interface. In 16-bit mode, up to 256K words of external ROM or RAM are supported. Note that the address lines do not map directly.

Figure 3. Interfacing up to 256k × 16 for External Code/Data

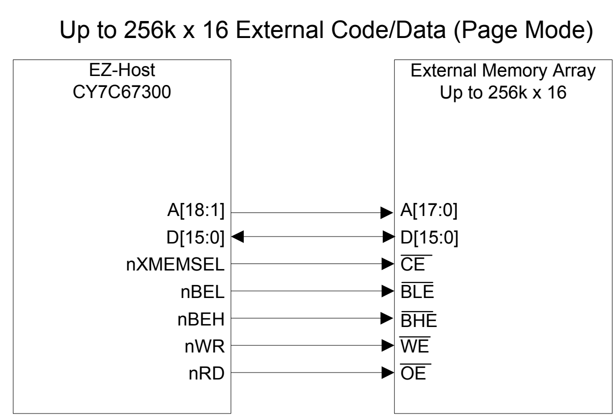
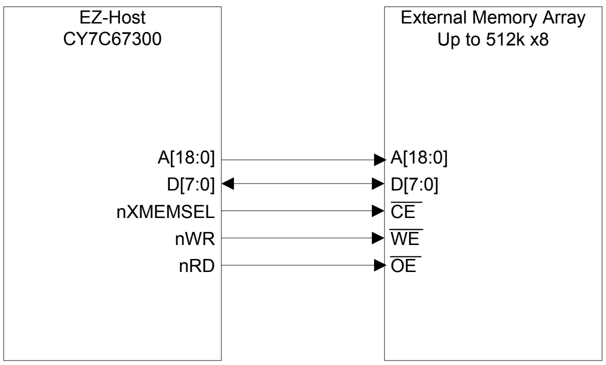


Figure 4 illustrates the interface for connecting an 8-bit ROM or 8-bit RAM to the EZ-Host external memory interface. In 8-bit mode, up to 512K bytes of external ROM or RAM are supported.

Figure 4. Interfacing up to 512k × 8 for External Code/Data

Up to 512k x 8 External Code/Data (Page Mode)



General Purpose IO Interface (GPIO)

EZ-Host has up to 32 GPIO signals available. Several other optional interfaces use GPIO pins as well and may reduce the overall number of available GPIOs.

GPIO Description

All Inputs are sampled asynchronously with state changes occurring at a rate of up to two 48 MHz clock cycles. GPIO pins are latched directly into registers, a single flip-flop.

Unused Pin Descriptions

Ensure to tristate unused USB pins with the D+ line pulled high through the internal pull up resistor and the D– line pulled low through the internal pull down resistor.

Configure unused GPIO pins as outputs so they are driven low.

UART Interface [3]

EZ-Host has a built in UART interface. The UART interface supports data rates from 900 to 115.2K baud. It can be used as a development port or for other interface requirements. The UART interface is exposed through GPIO pins.

UART Features

- Supports baud rates of 900 to 115.2K
- 8-N-1

UART Pins.

Table 7. UART Interface Pins

Pin Name	Pin Number
TX	42
RX	43

I²C EEPROM Interface [4]

EZ-Host provides a master-only I²C interface for external serial EEPROMs. The serial EEPROM can be used to store application specific code and data. Use the I²C interface for loading code out of EEPROM, it is not a general I²C interface. The I²C EEPROM interface is a BIOS implementation and is exposed through GPIO pins. Refer to the BIOS documentation for additional details on this interface.

I²C EEPROM Features

- Supports EEPROMs up to 64 KB (512K bit)
- Auto-detection of EEPROM size

I²C EEPROM Pins

Table 8. I²C EEPROM Interface Pins

Pin Name	Pin Number	GPIO Number
SMALL EEPROM		
SCK	39	GPIO31
SDA	40	GPIO30
LARGE EEPROM		
SCK	40	GPIO30
SDA	39	GPIO31

Serial Peripheral Interface

EZ-Host provides a SPI interface for added connectivity. EZ-Host may be configured as either an SPI master or SPI slave. The SPI interface can be exposed through GPIO pins or the External Memory port.

SPI Features

- Master or slave mode operation
- DMA block transfer and PIO byte transfer modes
- Full duplex or half duplex data communication
- 8-byte receive FIFO and 8-byte transmit FIFO
- Selectable master SPI clock rates from 250 kHz to 12 MHz
- Selectable master SPI clock phase and polarity
- Slave SPI signaling synchronization and filtering
- Slave SPI clock rates up to 2 MHz
- Maskable interrupts for block and byte transfer modes
- Individual bit transfer for non-byte aligned serial communication in PIO mode
- Programmable delay timing for the active/inactive master SPI clock
- Auto or manual control for master mode slave select signal
- Complete access to internal memory

Notes

3. Errata: The UART is not designed to recognize framing errors. When the UART is enabled, the GPIO Control Register still has control over GPIO 27 (UART RX pin). When enabled, the UART should override the GPIO Control Register, which defaults to setting the pin as an input. Please refer to Errata on page 107 for details and workaround.
4. Errata: If, while the BIOS is loading fi rmware, the part is reset and at that time the EEPROM is drivi ng the SDA line low, the BIOS will configure the part for co-processor mode instead of standalone mode. Please refer to Errata on page 107 for details and workaround.

SPI Pins

The SPI port has a few different pin location options as shown in Table 9. The port location is selectable via the GPIO control register [0xC006].

Table 9. SPI Interface Pins

Pin Name	Pin Number
Default Location	
nSSI	56 or 65
SCK	61
MOSI	60
MISO	66
Alternate Location	
nSSI	73
SCK	72
MOSI	71
MISO	74

High-Speed Serial Interface

EZ-Host provides an HSS interface. The HSS interface is a programmable serial connection with baud rate from 9600 baud to 2.0M baud. The HSS interface supports both byte and block mode operations and also hardware and software handshaking. Complete control of EZ-Host can be accomplished through this interface via an extensible API and communication protocol. The HSS interface can be exposed through GPIO pins or the External Memory port.

HSS Features

- 8 bits, no parity code
- Programmable baud rate from 9600 baud to 2M baud
- Selectable 1- or 2-stop bit on transmit
- Programmable inter-character gap timing for Block Transmit
- 8-byte receive FIFO
- Glitch filter on receive
- Block mode transfer directly to/from EZ-Host internal memory (DMA transfer)
- Selectable CTS/RTS hardware signal handshake protocol
- Selectable XON/XOFF software handshake protocol
- Programmable Receive interrupt, Block Transfer Done interrupts
- Complete access to internal memory

HSS Pins

The HSS port has a few different pin location options as shown in Table 10. The port location is selectable via the GPIO control register [0xC006].

Table 10. HSS Interface Pins

Pin Name	Pin Number
Default Location	
CTS	44
RTS	53
RXD	54
TXD	55
Alternate Location	
CTS	67
RTS	68
RXD	69
TXD	70

Programmable Pulse/PWM Interface

EZ-Host has four built in PWM output channels. Each channel provides a programmable timing generator sequence that can be used to interface to various image sensors or other applications. The PWM interface is exposed through GPIO pins.

Programmable Pulse/PWM Features

- Four independent programmable waveform generators
- Programmable predefined frequencies ranging from 5.90 KHz to 48 MHz
- Configurable polarity
- Continuous and one-shot mode available

Programmable Pulse/PWM Pins.

Table 11. PWM Interface Pins

Pin Name	Pin Number
PWM3	44
PWM2	53
PWM1	54
PWM0	55

Host Port Interface

EZ-Host has an HPI interface. The HPI interface provides DMA access to the EZ-Host internal memory by an external host, plus a bidirectional mailbox register for supporting high level communication protocols. This port is designed to be the primary high-speed connection to a host processor. Complete control of EZ-Host can be accomplished through this interface via an extensible API and communication protocol. Other than the hardware communication protocols, a host processor has identical control over EZ-Host whether connecting to the HPI or HSS port. The HPI interface is exposed through GPIO pins.

HPI Features

- 16-bit data bus interface
- 16 MB/s throughput
- Auto-increment of address pointer for fast block mode transfers
- Direct memory access (DMA) to internal memory
- Bidirectional Mailbox register
- Byte swapping
- Complete access to internal memory
- Complete control of SIEs through HPI
- Dedicated HPI status register

HPI Pins

Table 12. HPI Interface Pins [5, 6]

Pin Name	Pin Number
INT	46
nRD	47
nWR	48
nCS	49
A1	50
A0	52
D15	56
D14	57
D13	58
D12	59
D11	60
D10	61
D9	65
D8	66
D7	86
D6	87
D5	89
D4	90
D3	91
D2	92
D1	93
D0	94

The two HPI address pins are used to address one of four possible HPI port registers as shown in Table 13.

Table 13. HPI Addressing

HPI A[1:0]	A1	A0
HPI Data	0	0
HPI Mailbox	0	1
HPI Address	1	0
HPI Status	1	1

IDE Interface

EZ-Host has an IDE interface. The IDE interface supports PIO mode 0-4 as specified in the Information Technology-AT Attachment–4 with Packet Interface Extension (ATA/ATAPI-4) Specification, T13/1153D Rev 18. There is no need for firmware to use programmable wait states. The CPU read/write cycle is automatically extended as needed for direct CPU to IDE read/write accesses.

The EZ-Host IDE interface also has a BLOCK transfer mode that allows EZ-Host to read/write large blocks of data to/from the IDE data register and move it to/from the EZ-Host on-chip memory directly without intervention of the CPU. The IDE interface is exposed through GPIO pins. Table 14 on page 12 lists the achieved throughput for maximum block mode data transfer rate (with IDE_IORDY true) for the various IDE PIO modes.

Notes
5. HPI_INT is for the Outgoing Mailbox interrupt.
6. HPI strobes are negative logic sampled on rising edge.

Table 14. IDE Throughput

Mode	ATA/ATAPI-4 Min Cycle Time	Actual Min Cycle Time	ATA/ATPI-4 Max Transfer Rate	Actual Max Transfer Rate
PIO Mode 0	600 ns	30T = 625 ns	3.33 MB/s	3.2 MB/s
PIO Mode 1	383 ns	20T = 416.7 ns	5.22 MB/s	4.8 MB/s
PIO Mode 2	240	13T = 270.8 ns	8.33 MB/s	7.38 MB/s
PIO Mode 3	180 ns	10T = 208.3 ns	11.11 MB/s	9.6 MB/s
PIO Mode 4	120 ns	8T = 166.7 ns	16.67 MB/s	12.0 MB/s

T = System clock period = 1/48 MHz.

IDE Features

- Programmable IO mode 0–4
- Block mode transfers
- Direct memory access to/from internal memory through the IDE data register

IDE Pins

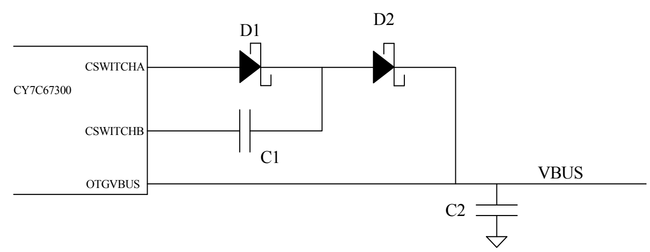
Table 15. IDE Interface Pins

Pin Name	Pin Number
IORDY	46
IOR	47
IOW	48
CS1	50
CS0	52
A2	53
A1	54
A0	55
D15	56
D14	57
D13	58
D12	59
D11	60
D10	61
D9	65
D8	66
D7	86
D6	87
D5	89
D4	90
D3	91
D2	92
D1	93
D0	94

Charge Pump Interface

VBUS for the USB OTG port can be produced by EZ-Host using its built in charge pump and some external components. Ensure the circuit connections look similar to the following diagram.

Figure 5. Charge Pump



Component details:

- D1 and D2: Schottky diodes with a current rating greater than 60 mA
- C1: Ceramic capacitor with a capacitance of 0.1 µF
- C2: Make capacitor value no more that 6.5 µF since that is the maximum capacitance allowed by the USB OTG specifications for a dual role device. The minimum value of C2 is 1 µF. There are no restrictions on the type of capacitor for C2.

If the VBUS charge pump circuit is not to be used, CSWITCHA, CSWITCHB, and OTGVBUS can be left unconnected.

Charge Pump Features

- Meets OTG Supplement Requirements, see Table 134 on page 91 for details.

Charge Pump Pins

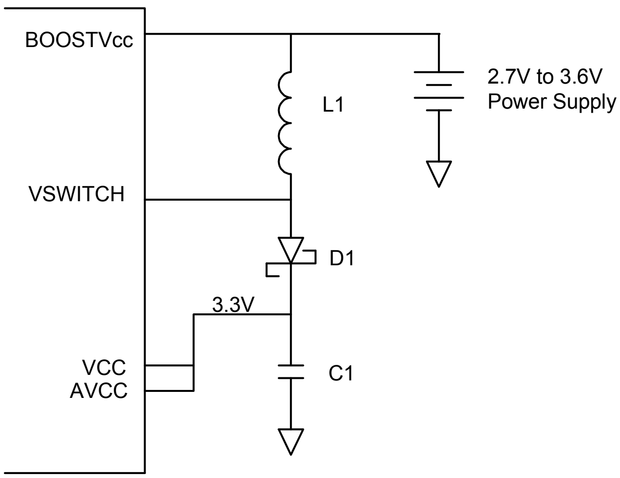
Table 16. Charge Pump Interface Pins

Pin Name	Pin Number
OTGVBUS	11
CSwitchA	13
CSwitchB	12

Booster Interface

EZ-Host has an on chip power booster circuit for use with power supplies that range between 2.7V and 3.6V. The booster circuit boosts the power to 3.3V nominal to supply power for the entire chip. The booster circuit requires an external inductor, diode, and capacitor. During power down mode, the circuit is disabled to save power. Figure 6 shows how to connect the booster circuit.

Figure 6. Power Supply Connection With Booster

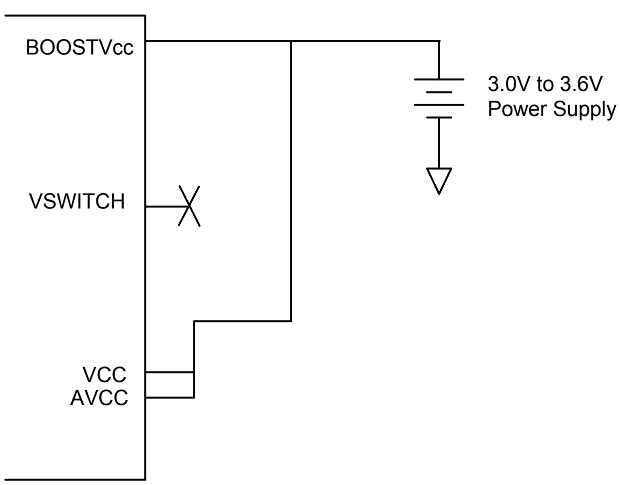


Component details:

- L1: Inductor with inductance of 10 µH and a current rating of at least 250 mA
- D1: Schottky diode with a current rating of at least 250 mA
- C1: Tantalum or ceramic capacitor with a capacitance of at least 2.2 µF

Figure 7 shows how to connect the power supply when the booster circuit is not being used.

Figure 7. Power Supply Connection Without Booster



Booster Pins

Table 17. Charge Pump Interface Pins

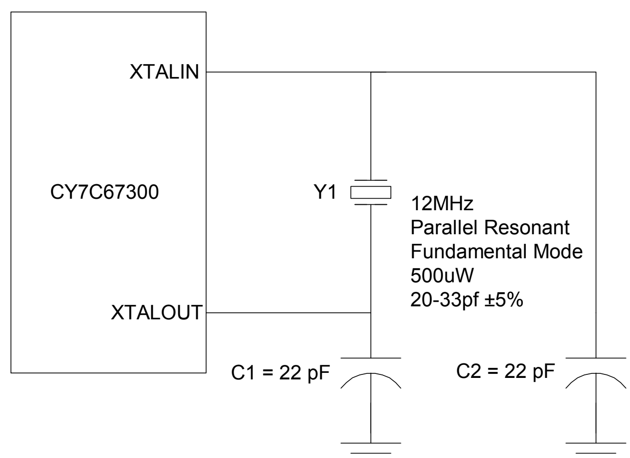
Pin Name	Pin Number
BOOSTVcc	16
VSWITCH	14

Crystal Interface

The recommended crystal circuit to be used with EZ-Host is shown in Figure 8 If an oscillator is used instead of a crystal circuit, connect it to XTALIN and leave XTALOUT unconnected. For further information about the crystal requirements, see Table 132 on page 90.

Noted that the CLKSEL pin (pin 38) is sampled after reset to determine what crystal or clock source frequency is used. For normal operation, 12 MHz is required so the CLKSEL pin must have a 47K ohm pull up resistor to V_{CC}.

Figure 8. Crystal Interface



Crystal Pins

Table 18. Crystal Pins

Pin Name	Pin Number
XTALIN	29
XTALOUT	28

Boot Configuration Interface

EZ-Host can boot into any one of four modes. The mode it boots into is determined by the TTL voltage level of GPIO[31:30] at the time nRESET is deasserted. Table 19 shows the different boot pin combinations possible. After a reset pin event occurs, the BIOS bootup procedure executes for up to 3 ms. GPIO[31:30] are sampled by the BIOS during bootup only. After bootup these pins are available to the application as GPIOs.

Table 19. Boot Configuration Interface

GPIO31 (Pin 39)	GPIO30 (Pin 40)	Boot Mode
0	0	Host Port Interface (HPI)
0	1	High-Speed Serial (HSS)
1	0	Serial Peripheral Interface (SPI, slave mode)
1	1	I^2C EEPROM (Standalone Mode)

Ensure that GPIO[31:30] is pulled high or low as needed using resistors tied to V_{CC} or GND with resistor values between 5K ohms and 15K ohms. Do not tie GPIO[31:30] directly to V_{CC} or GND. Note that in standalone mode, the pull ups on those two pins are used for the serial I2C EEPROM (if implemented). Make sure that the resistors used for these pull ups conform to the serial EEPROM manufacturer's requirements.

If any mode other then standalone is chosen, EZ-Host is in coprocessor mode. The device powers up with the appropriate communication interface enabled according to its boot pins and waits idle until a coprocessor communicates with it. See the BIOS documentation for greater detail of the boot process.

Operational Modes

The operational modes are discussed in the following sections.

Coprocessor Mode

EZ-Host can act as a coprocessor to an external host processor. In this mode, an external host processor drives EZ-Host and is the main processor rather then EZ-Host's own 16-bit internal CPU. An external host processor may interface to EZ-Host through one of the following three interfaces in coprocessor mode:

- HPI mode, a 16 bit parallel interface with up to 16 MB transfer rate
- HSS mode, a serial interface with up to 2M baud transfer rate
- SPI mode, a serial interface with up to 2 Mb/s transfer rate

At bootup GPIO[31:30] determine which of these three interfaces are used for coprocessor mode. See Table 19 for details. Bootloading begins from the selected interface after POR + 3 ms of BIOS bootup.

Standalone Mode

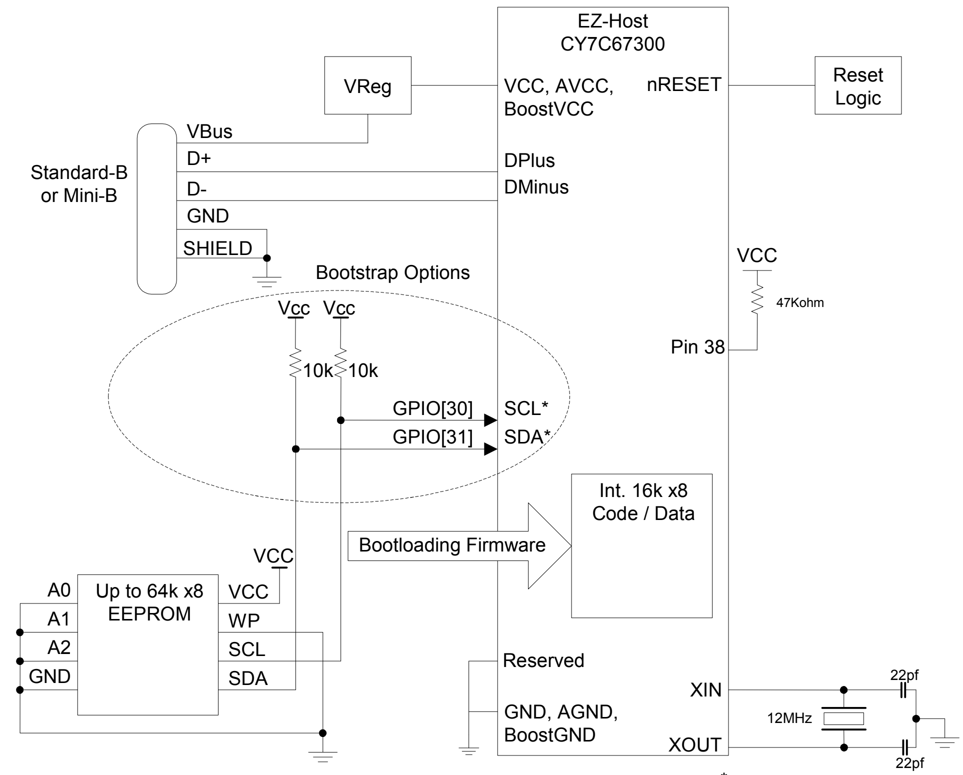
In standalone mode, there is no external processor connected to EZ-Host. Instead, EZ-Host's own internal 16-bit CPU is the main processor and firmware is typically downloaded from an EEPROM. Optionally, firmware may also be downloaded via USB. See Table 19 for booting into standalone mode.

After booting into standalone mode (GPIO[31:30] = ‘11’), the following pins are affected:

- GPIO[31:30] are configured as output pins to examine the EEPROM contents
- GPIO[28:27] are enabled for debug UART mode
- GPIO[29] is configured for as OTGID for OTG applications on PORT1A
  - If OTGID is logic 1 then PORT1A (OTG) is configured as a USB peripheral
  - If OTGID is logic 0 then PORT1A (OTG) is configured as a USB host
- Ports 1B, 2A, and 2B default as USB peripheral ports
- All other pins remain INPUT pins.

Minimum Hardware Requirements for Standalone Mode – Peripheral Only

Figure 9. Minimum Standalone Hardware Configuration – Peripheral Only



*Bootloading begins after POR + 3ms BIOS bootup

*GPIO[31:30]	31	30
Up to 2k x8	SCL	SDA
>2k x8 to 64k x8	SDA	SCL

*Parallel Resonant
Fundamental Mode
500uW
20-33pf ±5%

Power Savings and Reset Description

This sections describes the different modes for resetting the chip and ways to save power.

Power Saving Mode Description

EZ-Host has one main power saving mode, Sleep. For detailed information about Sleep mode, see the Sleep section that follows.

Sleep mode is used for USB applications to support USB suspend and non USB applications as the main chip power down mode.

In addition, EZ-Host is capable of slowing down the CPU clock speed through the CPU Speed register [0xC008] without affecting other peripheral timing. Reducing the CPU clock speed from 48 MHz to 24 MHz reduces the overall current draw by around 8 mA while reducing it from 48 MHz to 3 MHz reduces the overall current draw by approximately 15 mA.

Sleep

Sleep mode is the main chip power down mode and is also used for USB suspend. Sleep mode is entered by setting the Sleep Enable (bit 1) of the Power control register [0xC00A]. During Sleep mode (USB Suspend) the following events and states are true:

- GPIO pins maintain their configuration during sleep (in suspend)
- External Memory address pins are driven low
- XTALOUT is turned off
- Internal PLL is turned off
- Ensure that firmware disables the charge pump (OTG Control register [0xC098]) thereby causing OTGVBUS to drop below 0.2V. Otherwise OTGVBUS only drops to V_{CC} – (2 schottky diode drops).
- Booster circuit is turned off
- USB transceivers is turned off
- CPU goes into suspend mode until a programmable wakeup event

External (Remote) Wakeup Source

There are several possible events available to wake EZ-Host from Sleep mode as shown in Table 20. These may also be used as remote wakeup options for USB applications. See the Power Control Register [0xC00A] [R/W] on page 21 for details.

Upon wakeup, code begins executing within 200 µs, the time it takes the PLL to stabilize.

Table 20. Wakeup Sources [7, 8]

Wakeup Source (if enabled)	Event
USB Resume	D+/D– Signaling
OTGVBUS	Level
OTGID	Any Edge
HPI	Read
HSS	Read
SPI	Read
IRQ1 (GPIO 25)	Any Edge
IRQ0 (GPIO 24)	Any Edge

Power-On-Reset Description

The length of the power-on-reset event can be defined by (V_{CC} ramp to valid) + (Crystal startup). A typical application might use a 12 ms power-on-reset event = ~7 ms + ~5 ms, respectively.

Reset Pin

The Reset pin is active low and requires a minimum pulse duration of sixteen 12 MHz clock cycles (1.3 µs). A reset event restores all registers to their default POR settings. Code execution then begins 200 µs later at 0xFF00 with an immediate jump to 0xE000, the start of BIOS. Refer to BIOS documentation for additional details.

USB Reset

A USB Reset affects registers 0xC090 and 0xC0B0, all other registers remain unchanged.

Memory Map

The memory map is discussed in the following sections.

Mapping

The total memory space directly addressable by the CY16 processor is 64K (0x0000-0xFFFF). Program, data, and IO are contained within this 64K space. This memory space is byte addressable. Figure 10 on page 17 shows the various memory region address locations.

Internal Memory

Of the internal memory, 15K bytes are allocated for user's program and data. The lower memory space from 0x0000 to 0x04A2 is reserved for interrupt vectors, general purpose registers, USB control registers, stack, and other BIOS variables. The upper internal memory space contains EZ-Host control registers from 0xC000 to 0xC0FF and the BIOS ROM itself from 0xE000 to 0xFFFF. For more information about the reserved lower memory or the BIOS ROM, refer to the Programmer's documentation and/or the BIOS documentation.

During development with the EZ-Host toolset, leave the lower area of user's space (0x04A4 to 0x1000) available to load the GDB stub. The GDB stub is required to allow the toolset debug access into EZ-Host.

The chip select pins are not active during accesses to internal memory.

External Memory

Up to 32 KB of external memory from 0x4000 - 0xBFFF is available via one chip select line (nXRAMSEL) with RAM Merge enabled (BIOS default). Additionally, another 8 KB region from 0xC100 - 0xDFFF is available via a second chip select line (nXROMSEL) giving 40 KB of total available external memory. Together with the internal 15 KB, this gives a total of either ~48 KB (one chip select) or ~56 KB (two chip selects) of available memory for either code or data.

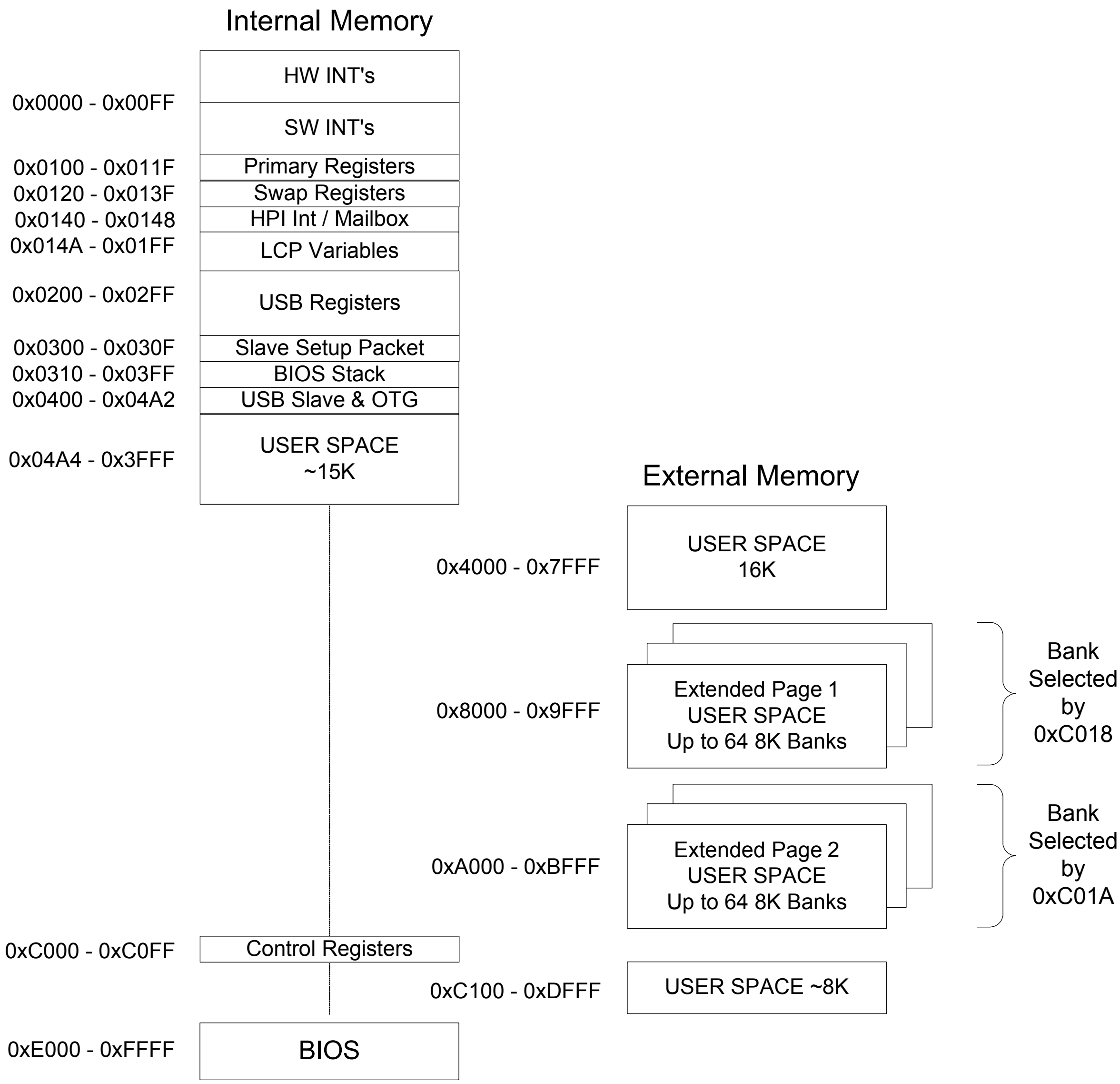
Note that the memory map and pin names (nXRAMSEL/ nXROMSEL) define specific memory regions for RAM vs. ROM. This allows the BIOS to look in the upper external memory space at 0xC100 for SCAN vectors (enabling code to be loaded/ executed from ROM). If no SCAN vectors are required in the design (external memory is used exclusively for data), then all external memory regions can be used for RAM. Similarly, the external memory can be used exclusively for code space (ROM).

If more external memory is required, EZ-Host has enough address lines to support up to 512 KB. However, this requires complex code banking/paging schemes via the Extended Page registers.

For further information about setting up the external memory, see the External Memory Interface on page 6.

Notes
7. Read data is discarded (dummy data).
8. HPI_INT asserts on a USB Resume.

Figure 10. Memory Map



Registers

Some registers have different functions for a read vs. a write access or USB host vs. USB device mode. Therefore, registers of this type have multiple definitions for the same address.

The default register values listed in this data sheet may be altered to some other value during the BIOS initialization. Refer to the BIOS documentation for register initialization information.

Processor Control Registers

There are nine registers dedicated to general processor control. Each of these registers are covered in this section and are summarized in Table 21.

Table 21. Processor Control Registers

Register Name	Address	R/W
CPU Flags Register	0xC000	R
Register Bank Register	0xC002	R/W
Hardware Revision Register	0xC004	R
CPU Speed Register	0xC008	R/W
Power Control Register	0xC00A	R/W
Interrupt Enable Register	0xC00E	R/W
Breakpoint Register	0xC014	R/W
USB Diagnostic Register	0xC03C	W
Memory Diagnostic Register	0xC03E	W

CPU Flags Register [0xC000] [R]

Table 22. CPU Flags Register

Bit #	15	14	13	12	11	10	9	8
Field	Reserved...							
Read/Write	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Field	...Reserved			Global Interrupt Enable	Negative Flag	Overflow Flag	Carry Flag	Zero Flag
Read/Write	-	-	-	R	R	R	R	R
Default	0	0	0	X	X	X	X	X

Register Description

The CPU Flags register is a read only register that gives processor flags status.

Global Interrupt Enable (Bit 4)

The Global Interrupt Enable bit indicates if the Global Interrupts are enabled.

1: Enabled

0: Disabled

Negative Flag (Bit 3)

The Negative Flag bit indicates if an arithmetic operation results in a negative answer.

1: MS result bit is ‘1’

0: MS result bit is not ‘1’

Overflow Flag (Bit 2)

The Overflow Flag bit indicates if an overflow condition occurred. An overflow condition can occur if an arithmetic result was either larger than the destination operand size (for addition) or smaller than the destination operand must allow for subtraction.

1: Overflow occurred

0: Overflow did not occur

Carry Flag (Bit 1)

The Carry Flag bit indicates if an arithmetic operation resulted in a Carry for addition, or Borrow for subtraction.

1: Carry/Borrow occurred

0: Carry/Borrow did not occur

Zero Flag (Bit 0)

The Zero Flag bit indicates if an instruction execution resulted in a ‘0’.

1: Zero occurred

0: Zero did not occur

Bank Register [0xC002] [R/W]

Table 23. Bank Register

Bit #	15	14	13	12	11	10	9	8
Field	Address...							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	1

Bit #	7	6	5	4	3	2	1	0
Field	...Address			Reserved				
Read/Write	R/W	R/W	R/W	-	-	-	-	-
Default	0	0	0	X	X	X	X	X

Register Description

The Bank register maps registers R0–R15 into RAM. The eleven MSBs of this register are used as a base address for registers R0–R15. A register address is automatically generated by:

1. Shifting the four LSBs of the register address left by 1.
2. ORing the four shifted bits of the register address with the twelve MSBs of the Bank register.
3. Forcing the LSB to zero.

For example, if the Bank register is left at its default value of 0x0100, and R2 is read, then the physical address 0x0102 is read. Refer to Table 24 for details.

Table 24. Bank Register Example

Register	Hex Value	Binary Value
Bank	0x0100	0000 0001 0000 0000
R14	0x000E << 1 = 0x001C	0000 0000 0001 1100
RAM Location	0x011C	0000 0001 0001 1100

Address (Bits [15:4])

The Address field is used as a base address for all register addresses to start from.

Reserved

Write all reserved bits with ’0’.

Hardware Revision Register [0xC004] [R]

Table 25. Revision Register

Bit #	15	14	13	12	11	10	9	8
Field	Revision...							
Read/Write	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

Bit #	7	6	5	4	3	2	1	0
Field	...Revision							
Read/Write	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

Register Description

The Hardware Revision register is a read only register that indicates the silicon revision number. The first silicon revision is represented by 0x0101. This number is increased by one for each new silicon revision.

Revision (Bits [15:0])

The Revision field contains the silicon revision number.

CPU Speed Register [0xC008] [R/W]

Table 26. CPU Speed Register

Bit #	15	14	13	12	11	10	9	8
Field	Reserved...							
Read/Write	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Field	...Reserved				CPU Speed			
Read/Write	-	-	-	-	R/W	R/W	R/W	R/W
Default	0	0	0	0	1	1	1	1

Register Description

The CPU Speed register allows the processor to operate at a user selected speed. This register only affects the CPU, all other peripheral timing is still based on the 48 MHz system clock (unless otherwise noted).

CPU Speed (Bits[3:0])

The CPU Speed field is a divisor that selects the operating speed of the processor as defined in Table 27.

Table 27. CPU Speed Definition

CPU Speed [3:0]	Processor Speed
0000	48 MHz/1
0001	48 MHz/2
0010	48 MHz/3
0011	48 MHz/4
0100	48 MHz/5
0101	48 MHz/6
0110	48 MHz/7
0111	48 MHz/8
1000	48 MHz/9
1001	48 MHz/10
1010	48 MHz/11
1011	48 MHz/12
1100	48 MHz/13
1101	48 MHz/14
1110	48 MHz/15
1111	48 MHz/16

Reserved

Write all reserved bits with '0'.

Power Control Register [0xC00A] [R/W]

Table 28. Power Control Register

Bit #	15	14	13	12	11	10	9	8
Field	Host/Device 2B Wake Enable	Host/Device 2A Wake Enable	Host/Device 1B Wake Enable	Host/Device 1A Wake Enable	OTG Wake Enable	Reserved	HSS Wake Enable	SPI Wake Enable
Read/Write	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Field	HPI Wake Enable	Reserved		GPI Wake Enable	Reserved	Boost 3V OK	Sleep Enable	Halt Enable
Read/Write	R/W	-	-	R/W	-	R	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register Description

The Power Control register controls the power down and wakeup options. Either the sleep mode or the halt mode options can be selected. All other writable bits in this register can be used as a wakeup source while in sleep mode.

Host/Device 2B Wake Enable (Bit 15)

The Host/Device 2B Wake Enable bit enables or disables a wakeup condition to occur on a Host/Device 2B transition. This wakeup from the SIE port does not cause an interrupt to the on-chip CPU.

1: Enable wakeup on Host/Device 2B transition

0: Disable wakeup on Host/Device 2B transition

Host/Device 2A Wake Enable (Bit 14)

The Host/Device 2A Wake Enable bit enables or disables a wakeup condition to occur on an Host/Device 2A transition. This wakeup from the SIE port does not cause an interrupt to the on-chip CPU.

1: Enable wakeup on Host/Device 2A transition

0: Disable wakeup on Host/Device 2A transition

Host/Device 1B Wake Enable (Bit 13)

The Host/Device 1B Wake Enable bit enables or disables a wakeup condition to occur on an Host/Device 1B transition. This wakeup from the SIE port does not cause an interrupt to the on-chip CPU.

1: Enable wakeup on Host/Device 1B transition

0: Disable wakeup on Host/Device 1B transition

Host/Device 1A Wake Enable (Bit 12)

The Host/Device 1A Wake Enable bit enables or disables a wakeup condition to occur on an Host/Device 1A transition. This wakeup from the SIE port does not cause an interrupt to the on-chip CPU.

1: Enable wakeup on Host/Device 1A transition

0: Disable wakeup on Host/Device 1A transition

OTG Wake Enable (Bit 11)

The OTG Wake Enable bit enables or disables a wakeup condition to occur on either an OTG VBUS_Valid or OTG ID transition (IRQ20).

1: Enable wakeup on OTG VBUS valid or OTG ID transition

0: Disable wakeup on OTG VBUS valid or OTG ID transition

HSS Wake Enable (Bit 9)

The HSS Wake Enable bit enables or disables a wakeup condition to occur on an HSS Rx serial input transition. The processor may take several hundreds of microseconds before being operational after wakeup. Therefore, the incoming data byte that causes the wakeup is discarded.

1: Enable wakeup on HSS Rx serial input transition

0: Disable wakeup on HSS Rx serial input transition

SPI Wake Enable (Bit 8)

The SPI Wake Enable bit enables or disables a wakeup condition to occur on a falling SPI_nSS input transition. The processor may take several hundreds of microseconds before being operational after wakeup. Therefore, the incoming data byte that causes the wakeup is discarded.

1: Enable wakeup on falling SPI nSS input transition

0: Disable SPI_nSS interrupt

HPI Wake Enable (Bit 7)

The HPI Wake Enable bit enables or disables a wakeup condition to occur on an HPI interface read.

1: Enable wakeup on HPI interface read

0: Disable wakeup on HPI interface read

GPI Wake Enable (Bit 4)

The GPI Wake Enable bit enables or disables a wakeup condition to occur on a GPIO(25:24) transition.

1: Enable wakeup on GPIO(25:24) transition

0: Disable wakeup on GPIO(25:24) transition

Boost 3V OK (Bit 2)

The Boost 3V OK bit is a read only bit that returns the status of the OTG Boost circuit.

1: Boost circuit not ok and internal voltage rails are below 3.0V

0: Boost circuit ok and internal voltage rails are at or above 3.0V

Sleep Enable (Bit 1)

Setting this bit to ‘1’ immediately initiates SLEEP mode. While in SLEEP mode, the entire chip is paused, achieving the lowest standby power state. All operations are paused, the internal clock is stopped, the booster circuit and OTG VBUS charge pump are all powered down, and the USB transceivers are powered down. All counters and timers are paused but retain their values; enabled PWM outputs freeze in their current states. SLEEP mode exits by any activity selected in this register. When SLEEP mode ends, instruction execution resumes within 0.5 ms.

1: Enable Sleep mode

0: No function

Halt Enable (Bit 0)

Setting this bit to ‘1’ immediately initiates HALT mode. While in HALT mode, only the CPU is stopped. The internal clock still runs and all peripherals still operate, including the USB engines. The power saving using HALT in most cases is minimal, but in applications that are very CPU intensive the incremental savings may provide some benefit.

The HALT state is exited when any enabled interrupt is triggered. Upon exiting the HALT state, one or two instructions immediately following the HALT instruction may be executed before the waking interrupt is serviced (you may want to follow the HALT instruction with two NOPs).

1: Enable Halt mode

0: No function

Reserved

Write all reserved bits with ’0’.

Interrupt Enable Register [0xC00E] [R/W] [9]

Table 29. Interrupt Enable Register

Bit #	15	14	13	12	11	10	9	8
Field	Reserved			OTG Interrupt Enable	SPI Interrupt Enable	Reserved	Host/Device 2 Interrupt Enable	Host/Device 1 Interrupt Enable
Read/Write	-	-	-	R/W	R/W	-	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Field	HSS Interrupt Enable	In Mailbox Interrupt Enable	Out Mailbox Interrupt Enable	Reserved	UART Interrupt Enable	GPIO Interrupt Enable	Timer 1 Interrupt Enable	Timer 0 Interrupt Enable
Read/Write	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
Default	0	0	0	1	0	0	0	0

Register Description

The Interrupt Enable register allows control of the hardware interrupt vectors.

OTG Interrupt Enable (Bit 12)

The OTG Interrupt Enable bit enables or disables the OTG ID/OTG4.4V Valid hardware interrupt.

1: Enable OTG interrupt

0: Disable OTG interrupt

SPI Interrupt Enable (Bit 11)

The SPI Interrupt Enable bit enables or disables the following three SPI hardware interrupts: SPI TX, SPI RX, and SPI DMA Block Done.

1: Enable SPI interrupt

0: Disable SPI interrupt

Host/Device 2 Interrupt Enable (Bit 9)

The Host/Device 2 Interrupt Enable bit enables or disables all of the following Host/Device 2 hardware interrupts: Host 2 USB Done, Host 2 USB SOF/EOP, Host 2 Wakeup/Insert/Remove, Device 2 Reset, Device 2 SOF/EOP or WakeUp from USB, Device 2 Endpoint n.

1: Enable Host 2 and Device 2 interrupt

0: Disable Host 2 and Device 2 interrupt

Host/Device 1 Interrupt Enable (Bit 8)

The Host/Device 1 Interrupt Enable bit enables or disables all of the following Host/Device 1 hardware interrupts: Host 1 USB Done, Host 1 USB SOF/EOP, Host 1 Wakeup/Insert/Remove, Device 1 Reset, Device 1 SOF/EOP or WakeUp from USB, Device 1Endpoint n.

1: Enable Host 1 and Device 1 interrupt

0: Disable Host 1 and Device 1 interrupt

Note

9. Errata: Host/Device 1 SIE events will still trigger an interrupt when only the Host/Device 2 SIE Interrupt Enable is set and vise versa. Please refer to Errata on page 107 for details and workaround.

HSS Interrupt Enable (Bit 7)

The HSS Interrupt Enable bit enables or disables the following High-speed Serial Interface hardware interrupts: HSS Block Done and HSS RX Full.

1: Enable HSS interrupt

0: Disable HSS interrupt

In Mailbox Interrupt Enable (Bit 6)

The In Mailbox Interrupt Enable bit enables or disables the HPI: Incoming Mailbox hardware interrupt.

1: Enable MBXI interrupt

0: Disable MBXI interrupt

Out Mailbox Interrupt Enable (Bit 5)

The Out Mailbox Interrupt Enable bit enables or disables the HPI: Outgoing Mailbox hardware interrupt.

1: Enable MBXO interrupt

0: Disable MBXO interrupt

UART Interrupt Enable (Bit 3)

The UART Interrupt Enable bit enables or disables the following UART hardware interrupts: UART TX, and UART RX.

1: Enable UART interrupt

0: Disable UART interrupt

GPIO Interrupt Enable (Bit 2)

The GPIO Interrupt Enable bit enables or disables the General Purpose IO pins interrupt (see the GPIO Control Register [0xC006] [R/W] on page 56). When the GPIO bit is reset, all pending GPIO interrupts are also cleared

1: Enable GPIO interrupt

0: Disable GPIO interrupt

Timer 1 Interrupt Enable (Bit 1)

The Timer 1 Interrupt Enable bit enables or disables the TImer1 Interrupt Enable. When this bit is reset, all pending Timer 1 interrupts are cleared.

1: Enable TM1 interrupt

0: Disable TM1 interrupt

Timer 0 Interrupt Enable (Bit 0)

The Timer 0 Interrupt Enable bit enables or disables the TImer0 Interrupt Enable. When this bit is reset, all pending Timer 0 interrupts are cleared.

1: Enable TM0 interrupt

0: Disable TM0 interrupt

Reserved

Write all reserved bits with ’0’.

Breakpoint Register [0xC014] [R/W]

Table 30. Breakpoint Register

Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	Address...							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	...Address							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register Description

The Breakpoint register holds the breakpoint address. When the program counter matches this address, the INT127 interrupt occurs. To clear this interrupt, write a zero value to this register.

Address (Bits [15:0])

The Address field is a 16-bit field containing the breakpoint address.

USB Diagnostic Register [0xC03C] [R/W]

Table 31. USB Diagnostic Register

Bit #	15	14	13	12	11	10	9	8
Field	Port 2B Diagnostic Enable	Port 2A Diagnostic Enable	Port 1B Diagnostic Enable	Port 1A Diagnostic Enable	Reserved...			
Read/Write	R/W	R/W	R/W	R/W	-	-	-	-
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Field	...Reserved	Pull-down Enable	LS Pull-up Enable	FS Pull-up Enable	Reserved	Force Select		
Read/Write	-	R/W	R/W	R/W	-	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register Description

The USB Diagnostic register provides control of diagnostic modes. It is intended for use by device characterization tests, not for normal operations. This register is read/write by the on-chip CPU but is write-only via the HPI port.

Port 2B Diagnostic Enable (Bit 15)

The Port 2B Diagnostic Enable bit enables or disables Port 2B for the test conditions selected in this register.

1: Apply any of the following enabled test conditions: J/K, DCK, SE0, RSF, RSL, PRD

0: Do not apply test conditions

Port 2A Diagnostic Enable (Bit 14)

The Port 2A Diagnostic Enable bit enables or disables Port 2A for the test conditions selected in this register.

1: Apply any of the following enabled test conditions: J/K, DCK, SE0, RSF, RSL, PRD

0: Do not apply test conditions

Port 1B Diagnostic Enable (Bit 13)

The Port 1B Diagnostic Enable bit enables or disables Port 1B for the test conditions selected in this register.

1: Apply any of the following enabled test conditions: J/K, DCK, SE0, RSF, RSL, PRD

0: Do not apply test conditions

Port 1A Diagnostic Enable (Bit 12)

The Port 1A Diagnostic Enable bit enables or disables Port 1A for the test conditions selected in this register.

1: Apply any of the following enabled test conditions: J/K, DCK, SE0, RSF, RSL, PRD

0: Do not apply test conditions

Pull-down Enable (Bit 6)

The Pull-down Enable bit enables or disables full-speed pull down resistors (pull down on both D+ and D–) for testing.

1: Enable pull down resistors on both D+ and D–

0: Disable pull down resistors on both D+ and D–

LS Pull-up Enable (Bit 5)

The LS Pull-up Enable bit enables or disables a low-speed pull up resistor (pull up on D–) for testing.

1: Enable low-speed pull up resistor on D–

0: Pull-up resistor is not connected on D–

FS Pull-up Enable (Bit 4)

The FS Pull-up Enable bit enables or disables a full-speed pull up resistor (pull up on D+) for testing.

1: Enable full-speed pull up resistor on D+

0: Pull up resistor is not connected on D+

Force Select (Bits [2:0])

The Force Select field bit selects several different test condition states on the data lines (D+/D–). Refer to Table 32 for details.

Table 32. Force Select Definition

Force Select [2:0]	Data Line State
1xx	Assert SE0
01x	Toggle JK
001	Assert J
000	Assert K

Reserved

Write all reserved bits with ’0’.

Memory Diagnostic Register [0xC03E] [W]

Table 33. Memory Diagnostic Register

Bit #	15	14	13	12	11	10	9	8
Field	Reserved					Memory Arbitration Select		
Read/Write	-	-	-	-	-	W	W	W
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Field	Reserved							Monitor Enable
Read/Write	-	-	-	-	-	-	-	W
Default	0	0	0	0	0	0	0	0

Register Description

The Memory Diagnostic register provides control of diagnostic modes.

Memory Arbitration Select (Bits[10:8])

The Memory Arbitration Select field is defined in Table 34.

Table 34. Memory Arbitration Select

Memory Arbitration Select [3:0]	Memory Arbitration Timing
111	1/8, 7 of every 8 cycles dead
110	2/8, 6 of every 8 cycles dead
101	3/8, 5 of every 8 cycles dead
100	4/8, 4 of every 8 cycles dead
011	5/8, 3 of every 8 cycles dead
010	6/8, 2 of every 8 cycles dead
001	7/8, 1 of every 8 cycles dead
000	8/8, all cycles available

Monitor Enable (Bit 0)

The Monitor Enable bit enables or disables monitor mode. In monitor mode the internal address bus is echoed to the external address pins.

1: Enable monitor mode

0: Disable monitor mode

Reserved

Write all reserved bits with ’0’.

External Memory Registers

There are four registers dedicated to controlling the external memory interface. Each of these registers are covered in this section and are summarized in Table 35.

Table 35. External Memory Control Registers

Register Name	Address	R/W
Extended Page 1 Map Register	0xC018	R/W
Extended Page 2 Map Register	0xC01A	R/W
Upper Address Enable Register	0xC038	R/W
External Memory Control Register	0xC03A	R/W