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CY7C68003

MoBL-USB™ TX2UL USB 2.0 ULPI Transceiver

Features

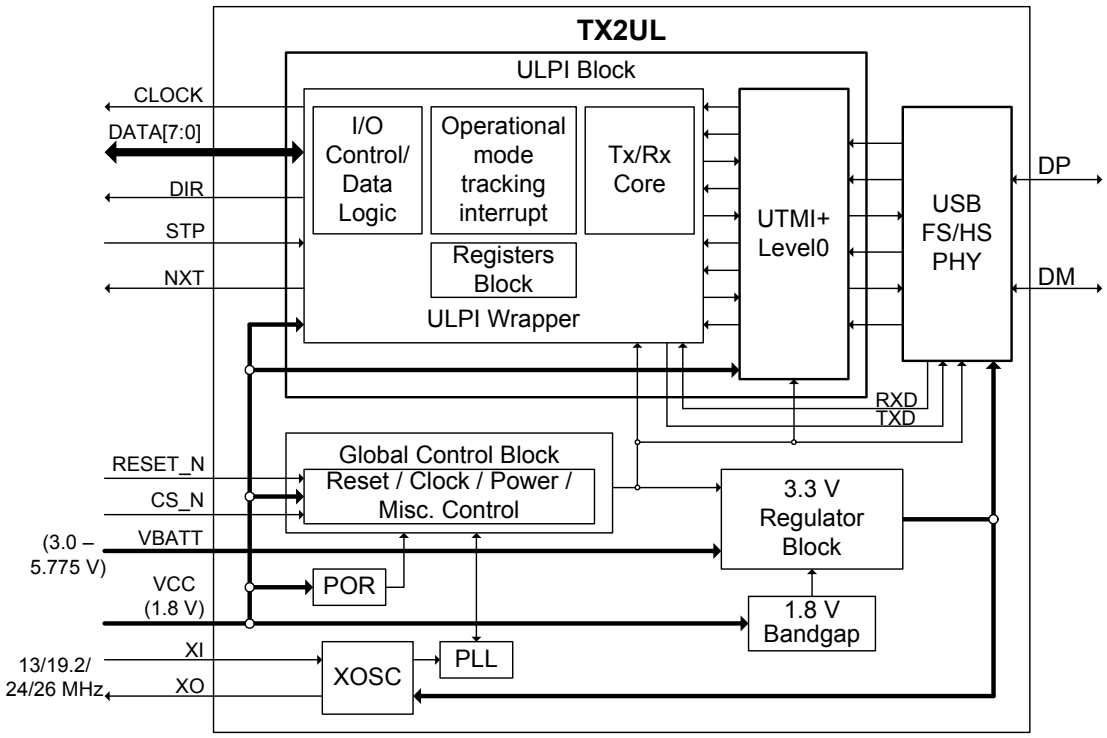
The Cypress MoBL-USB™ TX2UL is a low voltage high speed (HS) USB 2.0 UTMI+ Low Pin Interface (ULPI) Transceiver. The TX2UL is specifically designed for mobile handset applications by offering tiny package options and low power consumption.

- USB 2.0 Full Speed and High Speed compliant transceiver
- Multi range (1.8 V to 3.3 V) I/O voltages
- Fully compliant ULPI link interface
- 8-bit SDR ULPI data path
- UTMI+ level 0 support
- Support USB device mode only
- Integrated oscillator
- Integrated phase locked loop (PLL) – 13, 19.2, 24, or 26 MHz reference
- Integrated USB pull-up and termination resistors
- 3.0 V to 5.775 V VBATT input
- Chip select pin
- Single ended device RESET input
- UART pass through mode
- ESD compliance:
  - JESD22-A114D 8 kV Contact human body model (HBM) for DP, DM, and V_{SS} pins
  - IEC61000 - 4-2 8 kV contact discharge
  - IEC61000 - 4-2 15 kV air discharge
- Support for industrial temperature range: (-40 °C to 85 °C)
- Low power consumption for mobile applications:
  - 5 µA nominal sleep mode
  - 30 mA nominal active HS transfer
- Small package for mobile applications:
  - 2.14 x 1.76 mm 20-pin WLCSP 0.4 mm pitch
  - 4 x 4 mm 24-pin QFN

Applications

- Mobile phones
- PDAs
- Portable media players (PMPs)
- DTV applications
- Portable GPS units

TX2UL Block Diagram



Contents

Functional Overview

UTMI+ Low Pin Interface (ULPI)

This block conforms to the ULPI specification. It supports the 8-bit wide SDR data path. The primary I/Os of this block support multi-range LVCMOS signaling from 1.8 V to 3.3 V (±5%). The level used is automatically selected by the voltage applied to V_{CCIO} and is set at any voltage between 1.8 V and 3.3 V.

Oscillator (OSC)

This block meets the requirements of both the on-chip PLL and the USB-IF requirements for clock parameters. It is a fundamental mode parallel resonant oscillator with a maximum ESR of 60 Ω. It supports the following:

- Integrated Crystal Oscillator – 13, 19.2, 24, or 26 MHz crystal
- 13, 19.2, 24, or 26 MHz LVCMOS single ended input clock on XI

Phase Locked Loop (PLL)

The PLL meets all clock stability requirements imposed by this device and the USB standard. It supports all requirements to make the device compliant to the USB 2.0 specifications. It also has a fractional multiplier that enables it to supply the correct frequency to the device when it is presented with a 13, 19.2, 24, or 26 MHz reference clock.

Power On Reset (POR)

This block provides a POR signal (internal) based on the input supply. An internal POR is generated when V_{CC} input rises above VPOR(trip).

Reset (RESET_N)

The three major functions of RESET_N pin are as follows:

- Reset TX2UL
- Place TX2UL into Sleep Mode
- Place TX2UL into Configuration Mode

When the RESET_N pin is asserted (low) for tSTATE (tSTATE is specified in Table 21 on page 21), the TX2UL enters either Sleep Mode or Configuration Mode depending on the CS_N state. When RESET_N is asserted while CS_N is asserted, TX2UL enters Sleep Mode. When RESET_N is asserted for tSTATE while CS_N is deasserted, TX2UL enters Configuration Mode. In these modes, all the pins in the ULPI interface are tristated. If the RESET_N pin is not used, it must be pulled high. For information about different modes of configuration, see Table 5 on page 5.

DP and DM pins

The DP and DM pins are the differential pins for the USB. They must be connected to the corresponding DP and DM pins of the USB receptacle.

Chip Select (CS_N)

This signal pin is available only in 24-pin QFN package. The two major functions of CS_N are as follows:

- Tristate the ULPI bus output pins
- Associate with RESET_N to place TX2UL in the Sleep mode

When the CS_N pin is deasserted (high), all the pins in the ULPI interface are tristated.

USB2 Transceiver Macrocell Interface (UTMI+)

This block conforms to the UTMI+ Level 0 standard. It performs all the UTMI to USB translation.

Global Control

This block is the digital control logic that ties the blocks of the device together. Its functions include pull up control, over current protect control, and more.

Full Speed and High Speed USB Transceivers (FS/HS)

The FS and HS Transceivers comply fully with the USB 2.0 specifications.

USB Pull up and Intr Detect, Termination Resistors (Pull up/TERM)

These blocks contain the USB pull-up and termination resistors as specified by the USB 2.0 specification.

UART Pass Through Mode

TX2UL supports Carkit UART Pass Through Mode. When the Carkit Mode bit in the Interface Control register is set, it enables the Link to communicate through the DP/DM to a remote system using UART signaling. By default, the clock is powered down when the TX2UL enters Carkit Mode. Entering and exiting the Carkit Mode is identical to the Serial Mode. Table 1, Table 2, and Figure 1 show the UART Signal Mapping between the DP/DM and DATA[1:0] at ULPI interface.

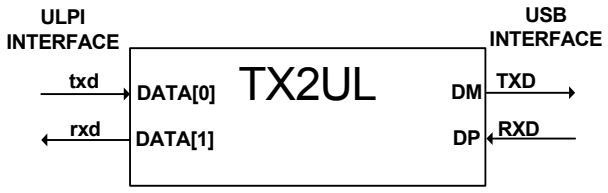
Table 1. UART Signal Mapping at ULPI Interface

Signal	Maps to	Direction	Description
txd	DATA[0]	IN	UART TXD signal routed to DM pin
rxd	DATA[1]	OUT	UART RXD signal routed to DP pin
Reserved	DATA[7:2]	-	Reserved

Table 2. UART Signal Mapping at USB Interface

Signal	Maps to	Direction	Description
TXD	DM	OUT	UART TXD signal
RXD	DP	INT	UART RXD signal

Figure 1. UART Signal Mapping in Pass Through Mode



Clocking

TX2UL supports external crystal and clock inputs at the 13, 19.2, 24, and 26 MHz frequencies. The internal PLL applies the proper clock multiply option depending on the input frequency. For applications that use an external clock source to drive XI, the XO pin (in the 24-pin QFN package) is left floating. TX2UL has an on-chip oscillator circuit that uses an external 13, 19.2, 24, or 26 MHz (±100 ppm) crystal with the following characteristics:

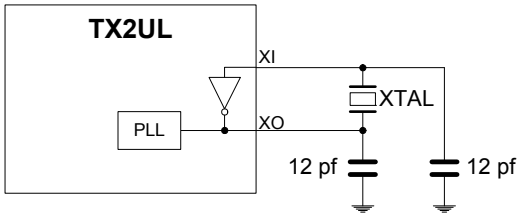
- Parallel resonant
- Fundamental mode
- 750 µW drive level
- 12 pF (5 percent tolerance) load capacitors
- 150 ppm

TX2UL operates on one of two primary clock sources:

- LVCMOS square wave clock input driven on the XI pin
- Crystal generated sine wave clock on the XI and XO pins

The selection between input clock source and frequency on the XI pin is determined by the *Chip Configuration* register loaded through the RESET_N during Configuration Mode. The external clock source requirements are shown in Figure 3 on page 5.

Figure 2. Crystal Configuration



* 12 pF capacitor values assumes a trace capacitance of 3 pF per side on a four layer FR4 PCA

Table 3. External Clock Requirements

Parameter	Description	Specification		Unit
		Min	Max	
Vn	Supply voltage noise at frequencies < 50 MHz	–	20	mV p-p
PN_100	Input phase noise at 100 Hz	–	75	dBc/Hz
PN_1k	Input phase noise at 1 kHz offset	–	104	dBc/Hz
PN_10k	Input phase noise at 10 kHz offset	–	120	dBc/Hz
PN_100k	Input phase noise at 100 kHz offset	–	128	dBc/Hz
PN_1M	Input phase noise at 1 MHz offset	–	130	dBc/Hz
	Duty cycle	30	70	%
	Maximum frequency deviation	–	150	ppm

Power Domains

The TX2UL has three power supply domains:

- V_{CC}
- V_{IO}
- V_{BATT}

TX2UL has two grounds:

- V_{SS}
- V_{SSBATT}

V_{CC}

This is the core 1.8 V power supply for the TX2UL. It can range anywhere from 1.7 V to 1.9 V during actual operation.

V_{IO}

This is the 1.8 V to 3.3 V multi range supply to the I/O ring. It can range anywhere from 1.7 V to 3.6 V during actual operation.

V_{BATT}

This is the battery input supply that powers the 3.3 V regulator block. It can range anywhere from 3.0 to 5.775 V during actual operation.

Voltage Regulator

The internal 3.3 V regulator block regulates the VBATT supply to the internal 3.3 V supply for the USBIO and XOSC blocks. If the supply voltage at VBATT is below 3.3 V, the regulator block switches the VBATT supply directly for the USBIO and XOSC blocks.

Power Supply Sequence

TX2UL does not require a power supply sequence. All power supplies are independently sequenced without damaging the part. All supplies are up and stable for the device to function properly. The analog block contains circuitry that senses the power supply to determine when all supplies are valid.

Operation Modes

There are six operation modes available in TX2UL. They are:

- Normal operation mode
- Configuration mode
- ULPI low power mode
- Sleep mode
- Carkit UART pass through mode
- Tristate ULPI interface output mode (only available in 24-pin QFN package)

When changing the operation modes, if the current and changing modes are not the normal operation Mode, TX2UL first changes to the normal operation mode. For example, to change from ULPI low power mode to Sleep mode, TX2UL changes to normal operation mode first, and then to Sleep mode. The Mode Change State diagram in Figure 3 shows the mode change path of TX2UL. The entries of the six operations modes (20-pin CSP package has five operation modes) are listed in Table 4 and Table 5. There are three mode change transactions that require the RESET_N assert or deassert with tSTATE (see Table 21 on page 21 for tSTATE). The three mode change transactions are:

- Change from normal operation mode to configuration mode; RESET_N is required to assert with tSTATE
- Change from configuration mode to normal operation mode; RESET_N is required to de-assert with tSTATE
- Change from normal operation mode to sleep mode; RESET_N is required to assert with tSTATE

Figure 3. Mode Change State Diagram

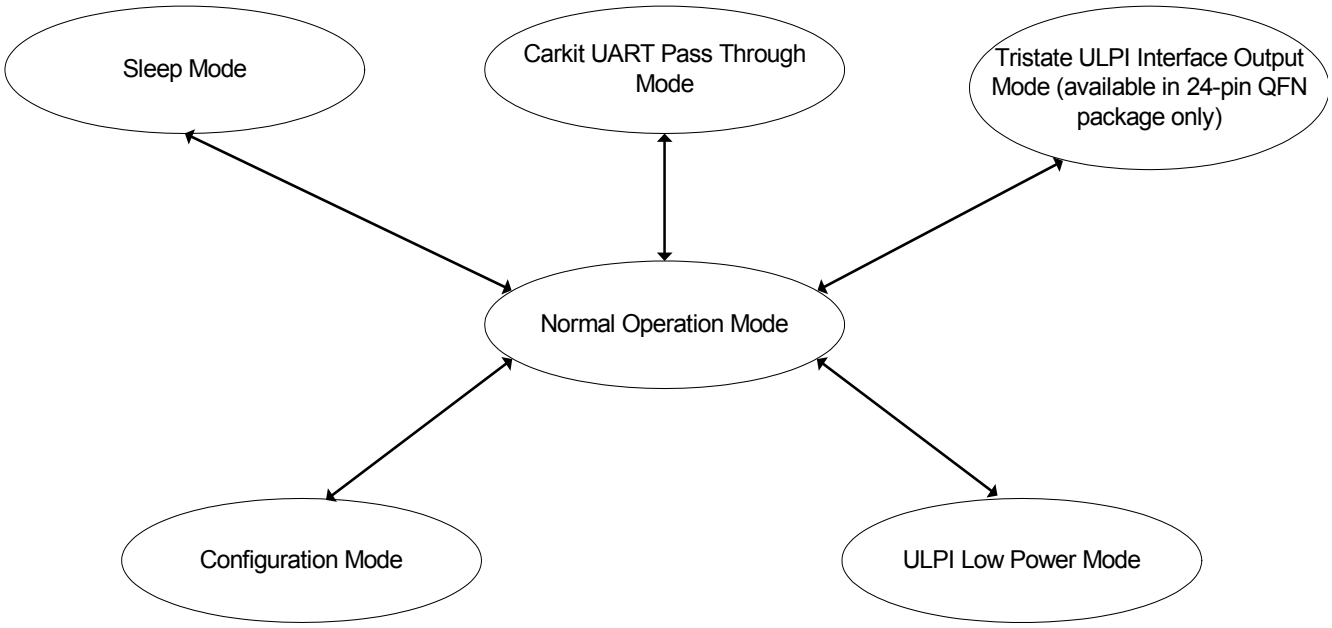


Table 4. TX2UL 20-Pin CPS Package Operation Modes

RESET_N	Mode
0 (Low)	Sleep mode
1 (High)	Normal operation mode
1 (High)	Enter into ULPI low power mode by setting SuspendM register bit (in Function Control Register) to 0 during the normal operation mode.
1 (High)	Enter into Carkit UART pass through mode by setting Carkit mode register bit (in Interface Control Register) to 1 during the normal operation mode.
0 (Low) when Power On (VCC On)	Enter into Configuration Mode

Table 5. TX2UL 24-Pin QFN Package Operation Modes

CS_N	RESET_N	Mode
0 (Low)	0 (Low)	Sleep mode
0 (Low)	1 (High)	Normal operation mode
0 (Low)	1 (High)	Enter into ULPI low power mode by setting SuspendM register bit (in Function Control Register) to 0 during the normal operation mode.
0 (Low)	1 (High)	Enter into Carkit UART pass through mode by setting Carkit Mode register bit (in Interface Control Register) to 1 during the normal operation mode.
1 (High)	0 (Low)	Configuration mode
1 (High)	1 (High)	Tristate ULPI interface output pins

The operation and configuration modes are described in the sections Operation Modes on page 5 and Configuration Mode on page 16 respectively. The ULPI low power mode and Sleep mode are described in the following sections.

ULPI Low Power Mode

In this mode, the link optionally places the TX2UL in low power mode when the USB is suspended. TX2UL powers down all the circuitry except for the interface pins and full speed receiver. To enter low power mode, the link must set SuspendM in the Function Control register to 0b. The TX2UL clock is stopped for a minimum of five cycles after TX2UL accepts the register write. To exit low power mode, the link signals TX2UL to exit the mode by asynchronously asserting a signal, STP. The TX2UL wakes up its internal circuitry and when it meets the ULPI timing requirements, it deasserts DIR. The SuspendM register is set to 1b.

Sleep Mode

Sleep mode is entered by asserting RESET_N during the Normal Operation Mode. When RESET_N is driven low for tSTATE (see Table 21 on page 21 for tSTATE requirement) while CS_N is low, TX2UL enters Sleep Mode. VCC must remain supplied (ON) during the sleep mode. This mode powers down all internal circuitry except the RESET_N pin and the chip_config register. The ULPI interface bus is tristated.

During the Sleep Mode ensure that:

- The ULPI interface I/Os are either floating or driven high by the link
- DP and DM are either floating or pull to 0 V
- Deassert RESET_N to exit the Sleep Mode

VID and PID

The VID and PID are hard coded into Product ID and Vendor ID registers (read only) as shown in Table 6.

Table 6. Immediate Register Values for VID and PID

Field Name	Size (bit)	Address (6 bits)				Value
		Rd	Wr	Set	Clr	
Vendor ID (VID) Low	8	00h	-	-	-	B4h
Vendor ID (VID) High	8	01h	-	-	-	04h
Product ID (PID) Low	8	02h	-	-	-	03h
Product ID (PID) High	8	03h	-	-	-	68h

Pinouts

TX2UL is available in 20-ball WLCSP and 24-pin QFN package. The pin assignment is shown in Figure 4 and Figure 5

Figure 4. Pin Assignment - TX2UL 20-Ball WLCSP (Top View)

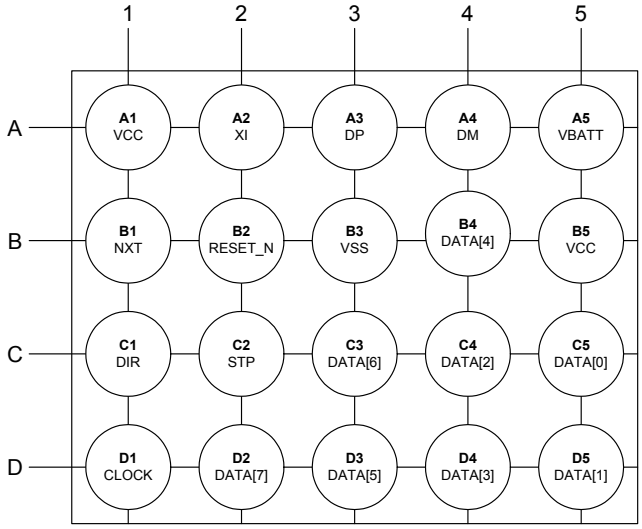


Table 7. Pin Definitions - TX2UL 20-Ball WLCSP

Name	Ball No.	Type	Voltage	Description
ULPI Link Interface				
DATA[0]	C5	I/O	1.8 V	ULPI data to/from link
DATA[1]	D5	I/O	1.8 V	ULPI data to/from link
DATA[2]	C4	I/O	1.8 V	ULPI data to/from link
DATA[3]	D4	I/O	1.8 V	ULPI data to/from link
DATA[4]	B4	I/O	1.8 V	ULPI data to/from link
DATA[5]	D3	I/O	1.8 V	ULPI data to/from link
DATA[6]	C3	I/O	1.8 V	ULPI data to/from link
DATA[7]	D2	I/O	1.8 V	ULPI data to/from link
CLOCK	D1	O	1.8 V	ULPI clock
NXT	B1	O	1.8 V	ULPI next signal
STP	C2	I	1.8 V	ULPI stop signal
DIR	C1	O	1.8 V	ULPI direction
USB				
DP	A3	I/O	USB	USB D-plus signal
DM	A4	I/O	USB	USB D-minus signal
Miscellaneous				
RESET_N	B2	I	1.8 V	Global reset. When RESET_N is asserted during the VCC power on, TX2UL enters configuration mode. During normal operation mode, asserting RESET_N resets the TX2UL and enter into the power saving mode.
XI	A2	I	1.8 V	LVCMOS single ended clock of frequency 13, 19.2, 24, or 26 MHz
POWER and GROUND				
VCC	B5, A1	Power	1.8 V	Low voltage supply for the digital core and I/O
VBATT	A5	Power	3.0 - 5.775 V	High voltage supply for USB
VSS	B3	GND	0 V	Common ground

Figure 5. Pin Assignment - TX2UL 24-Pin QFN (Top View)

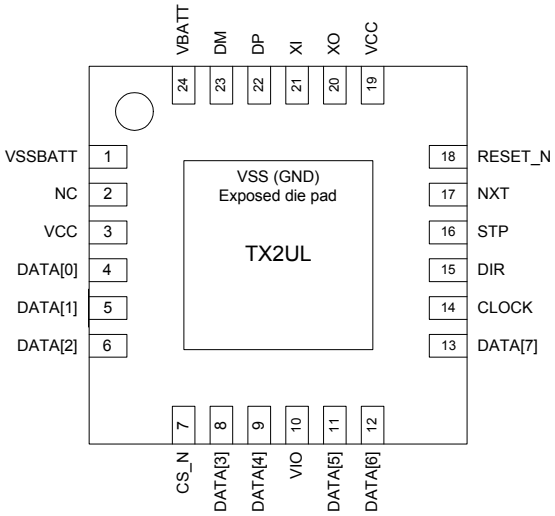


Table 8. Pin Definitions - TX2UL 24-Pin QFN

Name	Pin No.	Type	Voltage	Description
ULPI Link Interface				
DATA[0]	4	I/O	1.8 - 3.3 V	ULPI data to/from link
DATA[1]	5	I/O	1.8 - 3.3 V	ULPI data to/from link
DATA[2]	6	I/O	1.8 - 3.3 V	ULPI data to/from link
DATA[3]	8	I/O	1.8 - 3.3 V	ULPI data to/from link
DATA[4]	9	I/O	1.8 - 3.3 V	ULPI data to/from link
DATA[5]	11	I/O	1.8 - 3.3 V	ULPI data to/from link
DATA[6]	12	I/O	1.8 - 3.3 V	ULPI data to/from link
DATA[7]	13	I/O	1.8 - 3.3 V	ULPI data to/from link
CLOCK	14	O	1.8 - 3.3 V	ULPI clock
NXT	17	O	1.8 - 3.3 V	ULPI next signal
STP	16	I	1.8 - 3.3 V	ULPI stop signal
DIR	15	O	1.8 - 3.3 V	ULPI direction
USB				
DP	22	I/O	USB	USB D-plus signal
DM	23	I/O	USB	USB D-minus signal
Misc				
CS_N	7	I	1.8 - 3.3 V	When CS_N is de-asserted, all pins at ULPI interface are tristated
RESET_N	18	I	1.8 - 3.3 V	Device chip global reset. When RESET_N is asserted, TX2UL is in reset and enters into the power saving mode.
XI	21	I	1.8 V	Crystal or LVCMOS single ended clock of frequency 13, 19.2, 24, or 26 MHz
XO	20	O	1.8 - 3.3 V	Crystal
NC	2	-	-	No connect
POWER and GROUND				
VCC	3, 19	Power	1.8 V	Low voltage supply for the digital core
VIO	10	Power	1.8 - 3.3 V	Power for multi-range I/Os
VBATT	24	Power	3.0 - 5.775 V	High voltage supply for USB
VSSBATT	1	GND	0	USB ground
VSS	Die Paddle	GND	0	Digital ground (core and I/O)

Synchronous Operation Modes

This section describes the synchronous mode of TX2UL ULPI interface protocol.

ULPI Transmit Command Byte (TX CMD)

The Link initiates transfers to TX2UL by sending the Transmit Command Byte as shown in Table 9. TX CMD byte consists of a 2-bit command code and a 6-bit payload.

Table 9. Transmit Command (TX CMD) Byte Format

Byte Name	Command Code Data (7:6)	Command Payload Data (5:0)		Command Description
Special	00b	000000b	(NOOP)	No operation. 00h is the idle value of the data bus. The Link drives NOOP by default.
		XXXXXXb	(RSVD)	Reserved command space. Values other than those mentioned give undefined behavior.
Transmit	01b	000000b	(NOPID)	Transmit USB data that does not have a PID, such as chirp and resume signalling. The TX2UL starts transmitting on the USB beginning with the next byte.
		00XXXXb	(PID)	Transmit USB packet. data (3:0) indicates USB packet identifier PID (3:0)
		XXXXXXb	(RSVD)	Reserved Command space. Values other than those mentioned give undefined behavior.
RegWrite	10b	101111b	(EXTW)	Extended register write command. 8-bit address available in the next cycle.
		XXXXXXb	(REGW)	Register write command with 6-bit immediate address.
RegRead	11b	101111b	(EXTR)	Extended register read command. 8-bit address available in the next cycle.
		XXXXXXb	(REGR)	Register read command with 6-bit immediate address.

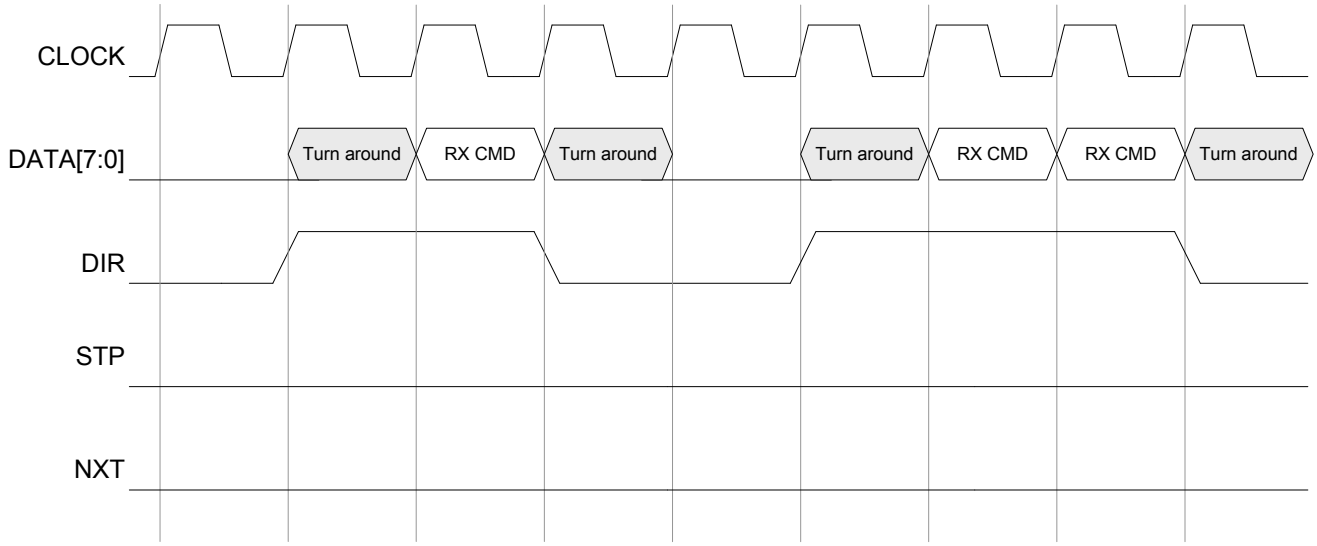
ULPI Receive Command Byte (RX CMD)

The Receive Command Byte, as shown in Table 10, is sent by TX2UL to update the link with LineState and USB receive information. The USB receive information includes LineState, RxActive, and RxError. After a USB transmit, TX2UL sends RX CMD with LineState indicating EOP to the link. For High Speed, EOP is the squelch to squelch transition on LineState. Figure 7 on page 10 shows how TX2UL sends RX CMD information to the link. The first packet shows a single RX CMD. If back to back changes are detected, TX2UL keeps DIR asserted and sends back to back RX CMDs as shown in the second packet.

Table 10. Receive Command (RX CMD) Byte Format

Data	Name	Description and Value		
1:0	LineState	ULPI LineState signals. DATA[0] = LineState (0) DATA[1] = LineState (1)		
3:2	Reserved			
5:4	RxEvent	Encoded UTMI event signals		
		Value	**RxActive**	**RxError**
		00	0	0
		01	1	0
		11	1	1
		10	X	X
7:6	Reserved			

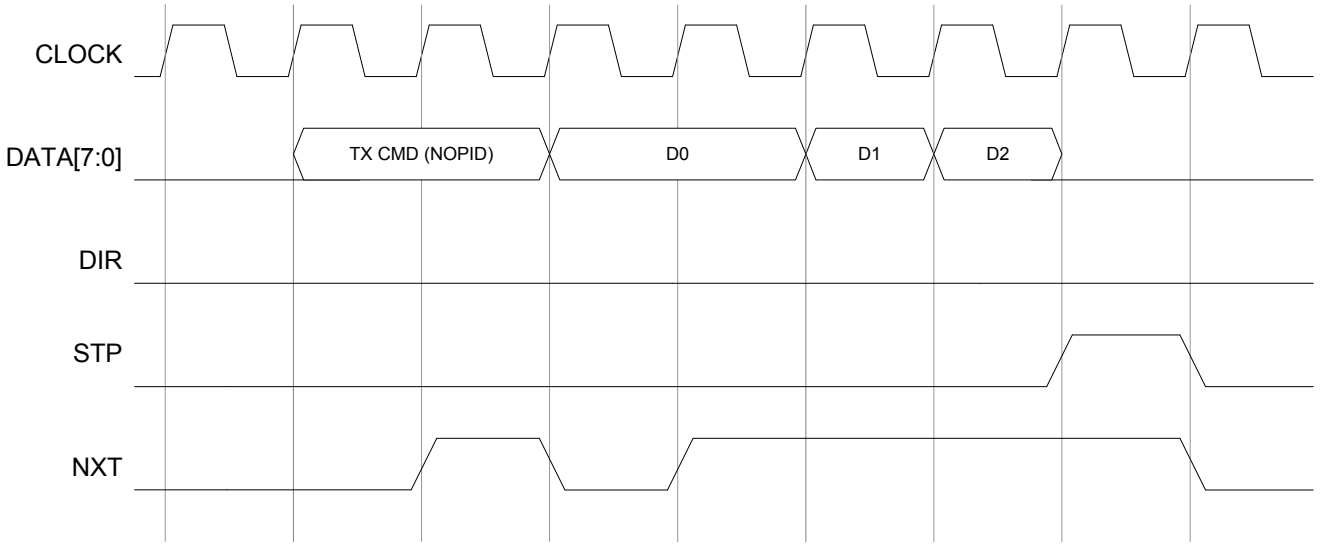
Figure 6. Sending RX CMD



USB Data Transmit (NOPID)

In this mode, the Link transmits data on the USB without a Packet Identifier (PID) by sending a TX CMD byte of the NOPID type. TX2UL asserts NXT (see Figure 8 on page 11) in the first cycle of TX CMD and deasserts NXT when it detects STP to be high. Because this command does not contain PID data, TX2UL waits for the next data byte before beginning transmission on the USB. When the last byte is transferred by the TX2UL, the link asserts STP for one cycle and drives data to 00h if no transmit errors occur. The link does not assert STP before the first byte is transferred by the TX2UL.

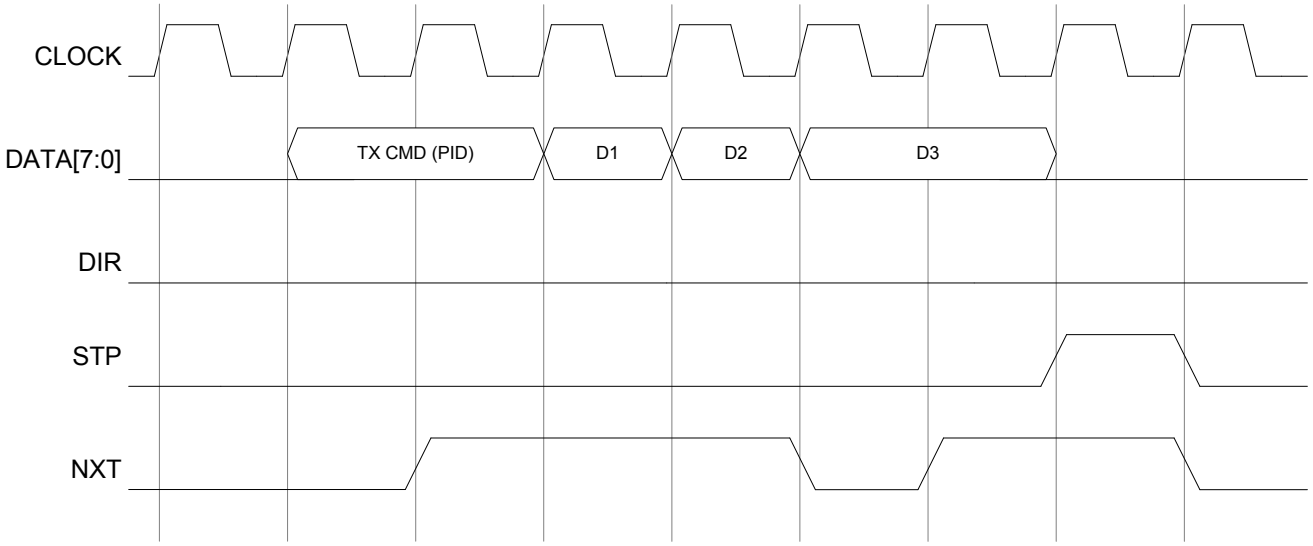
Figure 7. USB Data Transmit (NOPID)



USB Data Transmit (PID)

In this mode, the link transmits data on the USB with a PID. The link first drives a TX CMD byte as illustrated in Figure 9 on page 11 to transmit a USB packet. The link sets the Command Code to 01b (Transmit) and places the USB Packet Identifier (PID) on DATA[3:0] (see Table 9 on page 9). TX2UL throttles the data using NXT such that the link provides the next byte in the cycle after NXT is detected as high.

Figure 8. USB Data Transmit (PID)



USB Packet Receive

As shown in Figure 10 on page 12, when TX2UL receives the USB data it gains ownership of the data bus by asserting DIR. The DIR is previously either high or low. If DIR is low (see Figure 9), TX2UL asserts both DIR and NXT so that the link knows immediately that this is a USB receive packet. If DIR is high (see Figure 10 on page 12), TX2UL deasserts NXT and drives an RX CMD with the RxEvent field set to the RxActive state. The TX2UL starts driving data in the following cycle or outputs RX CMD until USB data is available. Valid USB packet data is presented to the link by asserting NXT and placing a byte on the bus. When NXT is low, TX2UL drives the RX CMD byte. All RX CMD changes during the USB packet receive are signaled when NXT is low. If NXT is never low during the packet receive, all RX CMD changes are replaced with a single RX CMD update. This update is sent at the end of the USB packet receive, when the ULPI bus is available. The RX CMD update always conveys the current RX CMD values and not the previous one.

Figure 9. USB Receive While DIR is Previously Low

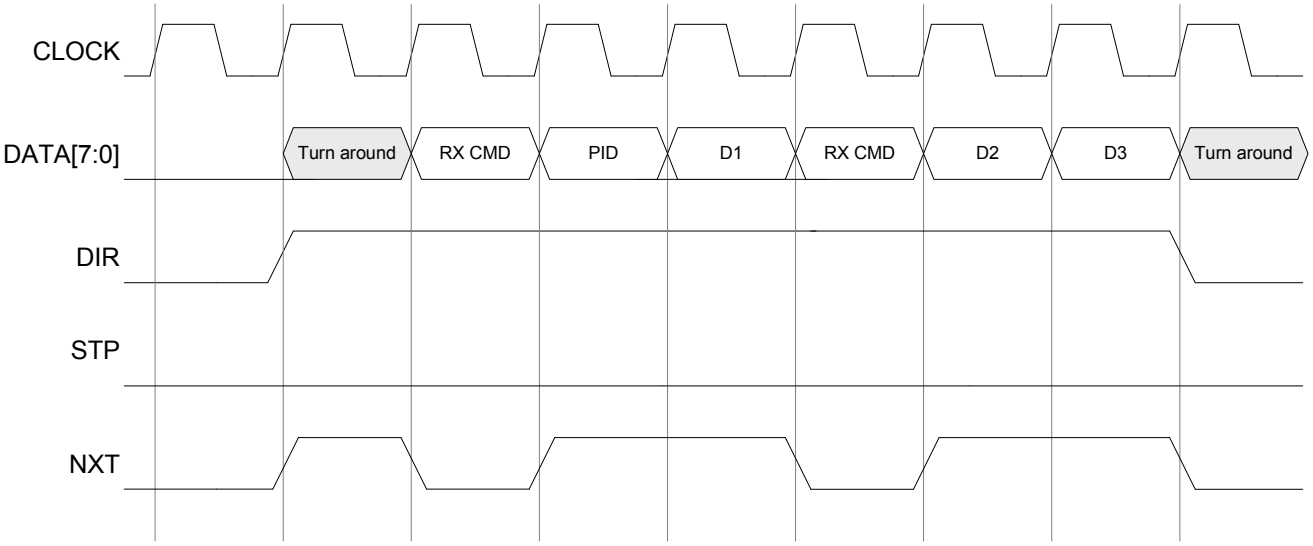
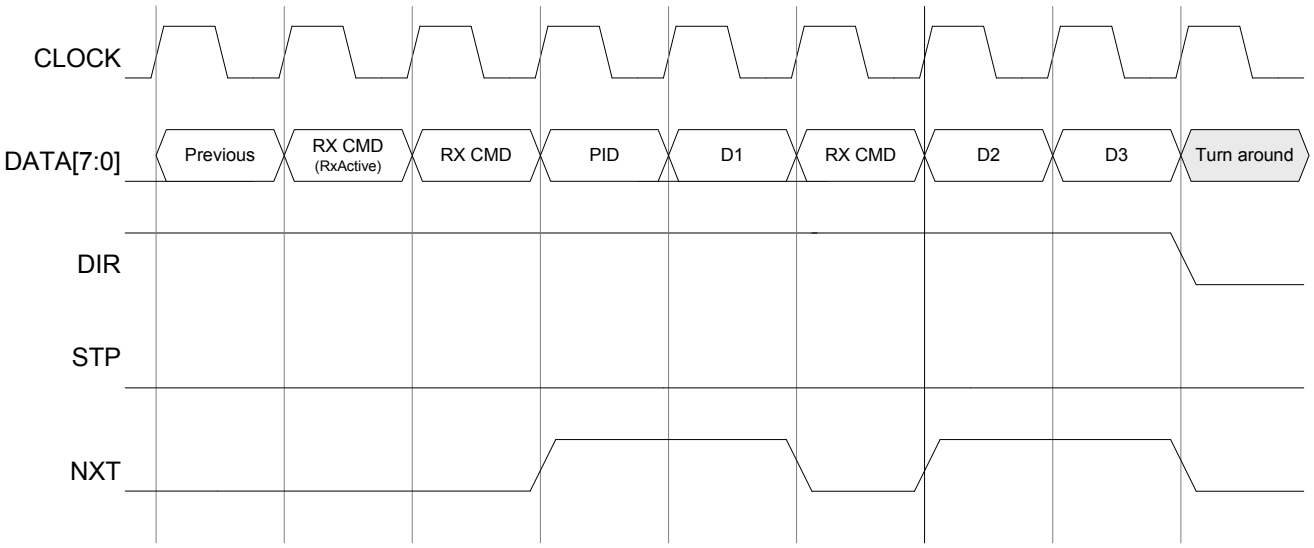


Figure 10. USB Receive While DIR is Previously High



Immediate Register Read and Write

An immediate register is accessed by sending the TX CMD byte first (see Figure 11 and Figure 12 on page 13). This byte is sent as a regread or regwrite command, depending on the intended operation.

For a register write (see Figure 11), the link first sends a register write TX CMD byte and waits for NXT to assert. After NXT asserts, the link sends the register write data and waits for NXT to assert again. After the second assertion is detected, the link asserts STP in the following cycle to complete the operation. The TX2UL detects this STP assertion before it can accept another transmit command. If the TX2UL aborts rewrite by asserting DIR, the link repeats the entire process again when the bus is idle.

For a register read (see Figure 12 on page 13), the link sends a register read command and waits for NXT to assert. In the cycle after NXT asserts, the TX2UL asserts DIR to gain control of the data bus. In the cycle, after DIR asserts the TX2UL returns the register read data. The TX2UL does not assert NXT when DIR is asserted during the register read operation, even during the cycle when the register read data is returned. If the TX2UL aborts the regread by asserting DIR earlier than shown in Figure 12 on page 13, the link retries the regread when the bus is idle.

Figure 11. Register Write

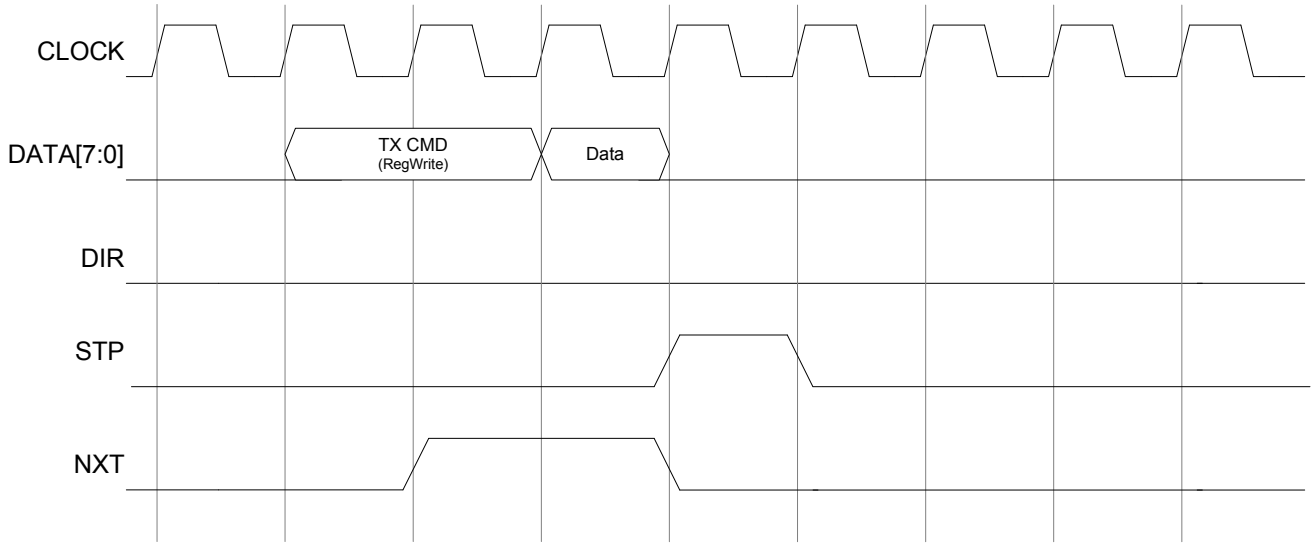
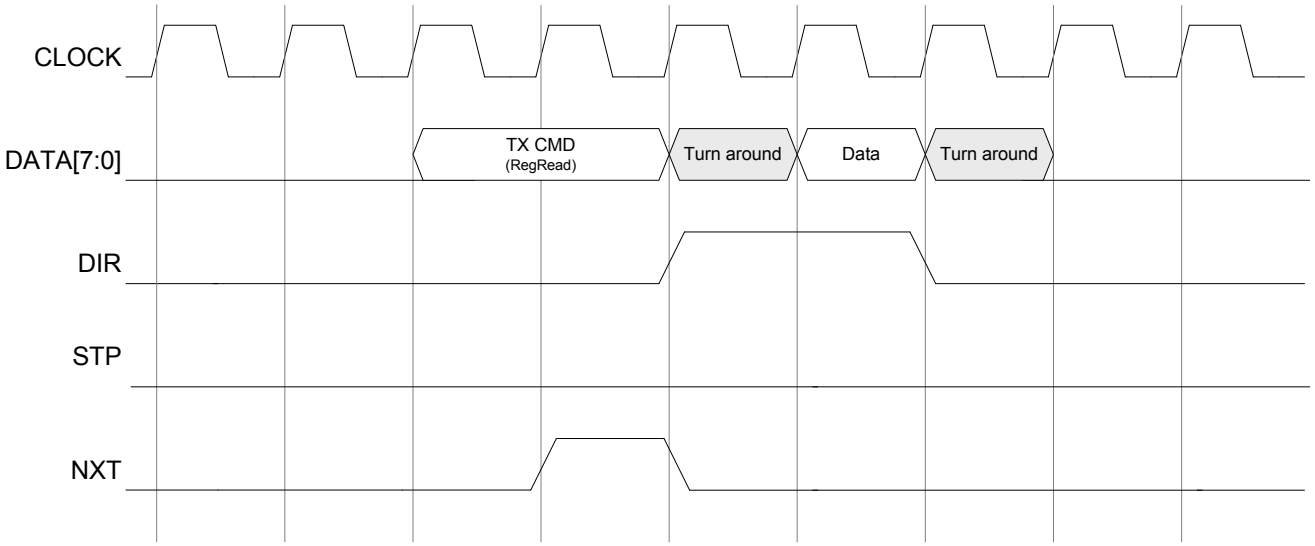


Figure 12. Register Read



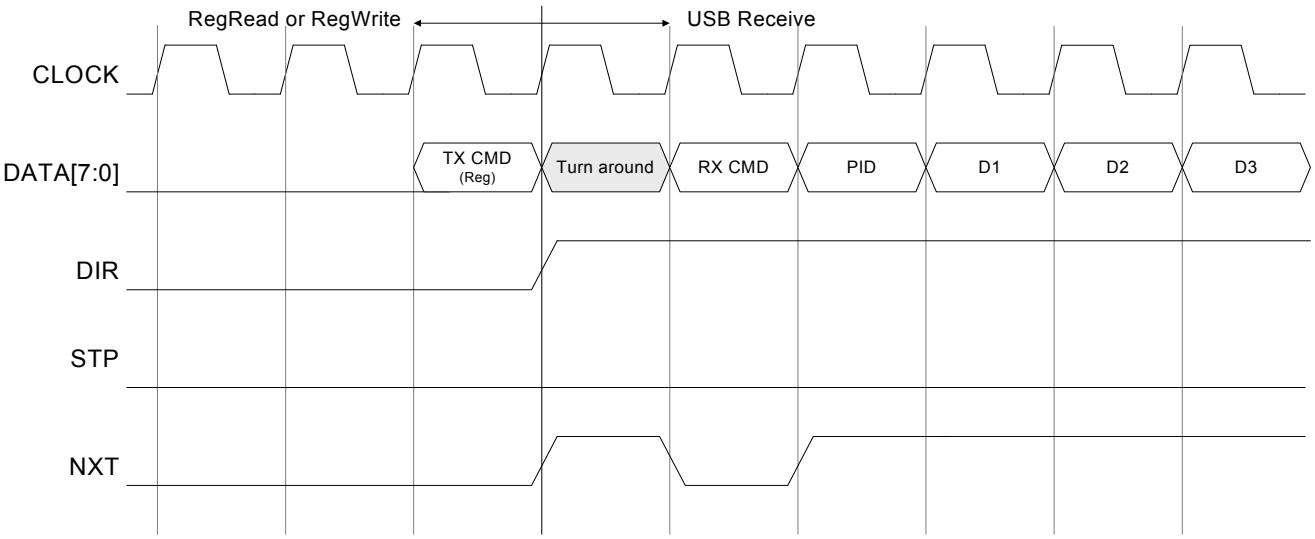
Immediate Register Read and Write Aborted by USB Receive

A register read is the only instance where ULPI does not use NXT to acquire data. The NXT signal is asserted only during USB receive to distinguish this type of receive from other types of data transfers.

Register read and write operations are aborted when the TX2UL sends a RX CMD, except during the cycle where register read data is returned to the link.

TX2UL asserts both DIR and NXT whenever a register read or write is aborted by a USB receive during the initial transmit command byte or in the same cycle that the register read data returned to the link.

Figure 13. Register Read or Write Aborted by USB Receive During TX CMD Byte



Back to Back Immediate Register Read and Write and USB Receive

When a USB receive occurs in the same cycle that the register read data is returned to the link, the TX2UL first returns the register read data, not a RX CMD byte (see Figure 14).

When a USB receive occurs in the cycle immediately after a register read completes, the TX2UL places the USB receive data back-to-back with the register read (see Figure 15). The link accepts back-to-back packets where DIR does not deassert between packets. If DIR asserts during the same cycle that STP is asserted at the end of a register write, then the TX2UL considers the register write to have successfully executed (see Figure 16 on page 15).

When a USB receive starts in the cycle after the register read data is returned to the link, it results in two cycles of bus turnaround when DIR deasserts for a single cycle (see Figure 17 on page 15).

Figure 14. USB Receive in Same Cycle as Register Read Data. USB Receive is Delayed

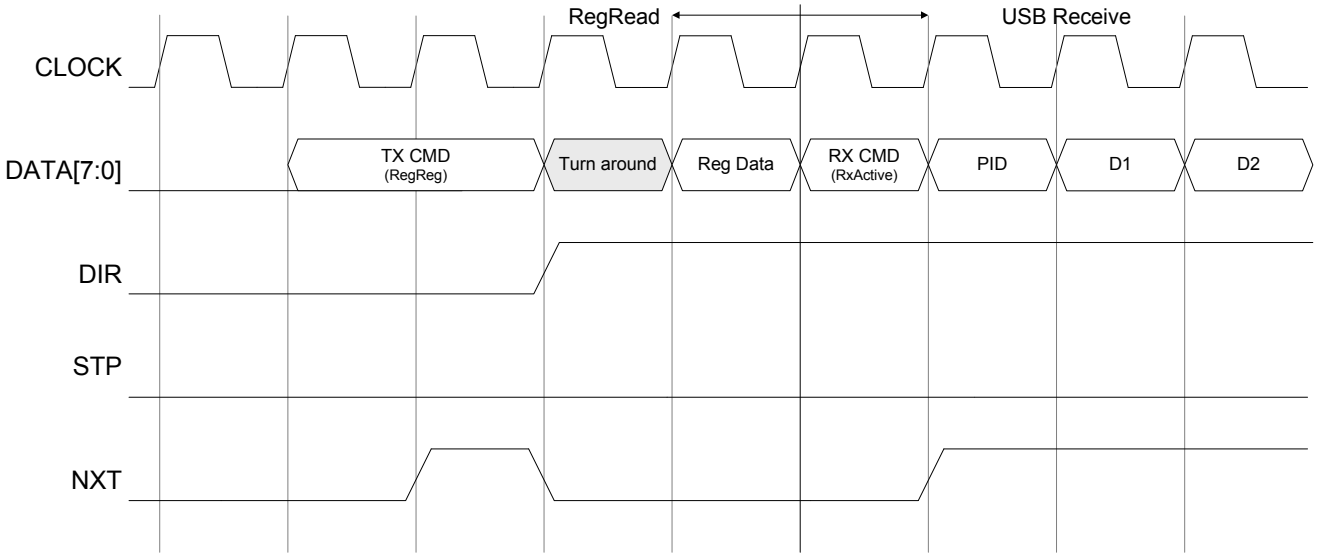


Figure 15. Register Read Followed Immediately by a USB Receive

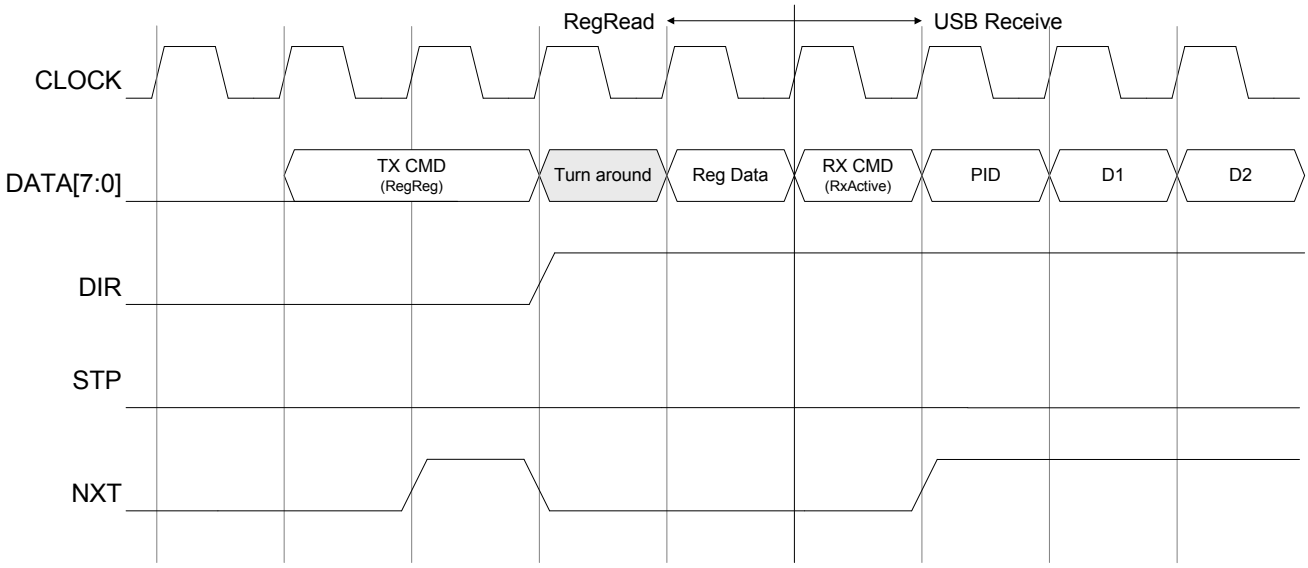


Figure 16. Register Write Followed Immediately by a USB Receive During STP Assertion

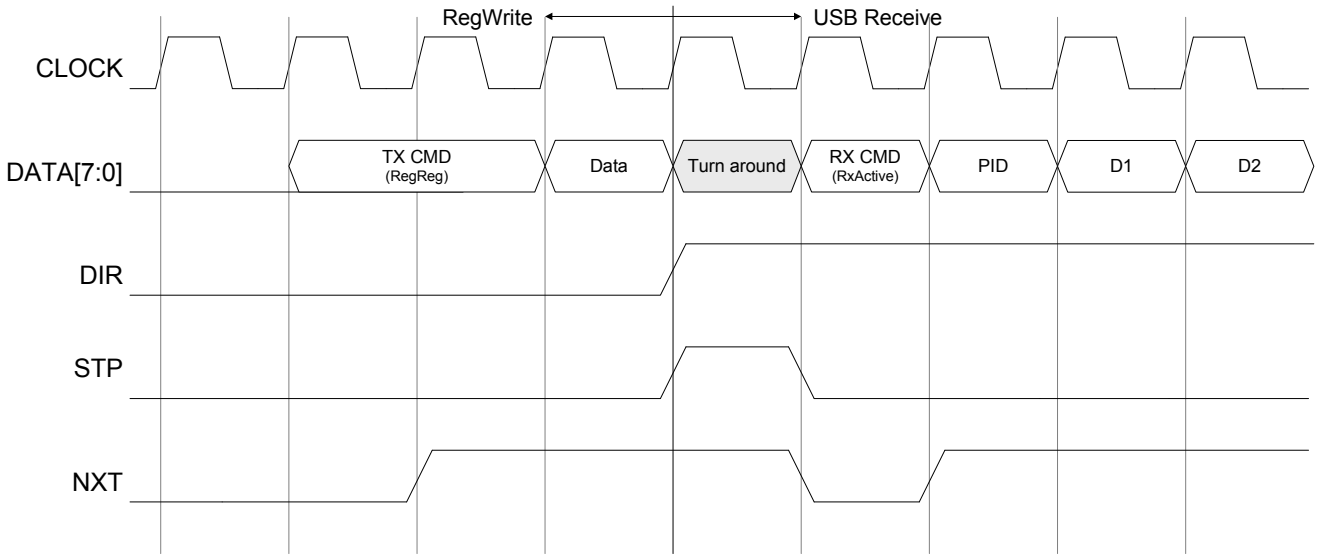
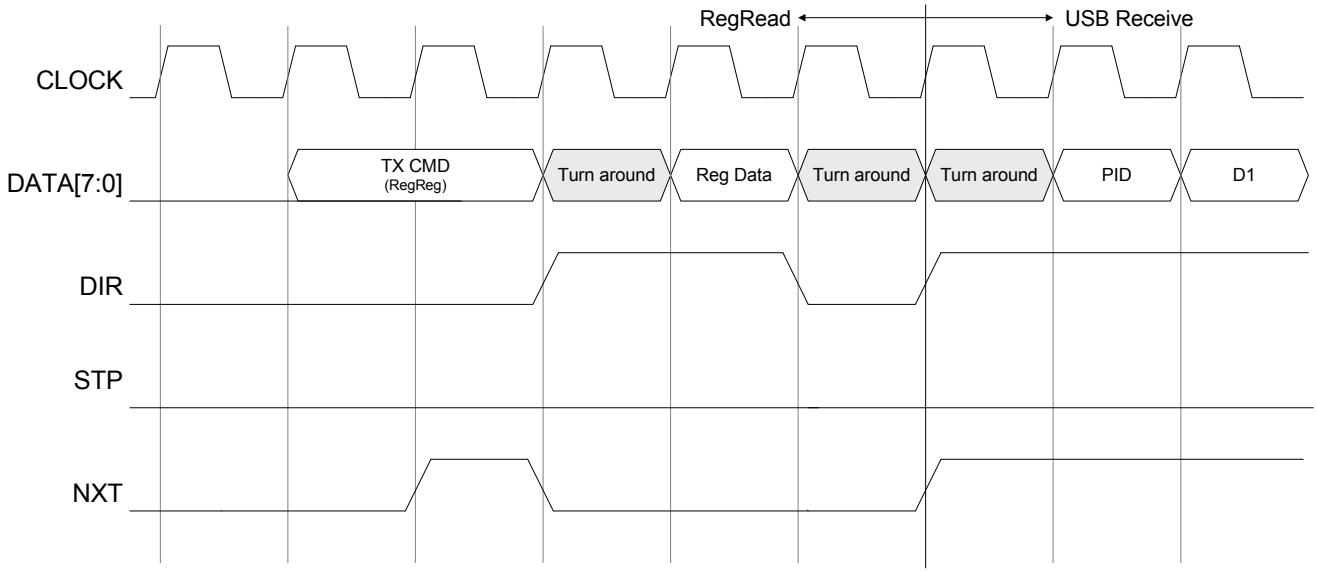


Figure 17. Register Read Followed by a USB Receive



Configuration Mode

TX2UL is configured in the input clock type and frequency for the XI and XO in Configuration Mode. The 20-pin CSP package and the 24-pin QFN package have different procedures to enter configuration mode.

Configuration Mode in 20-Pin CSP package

To enter configuration mode, keep the RESET_N low during V_{CC} Power On for tSTATE (see Figure 19 on page 22 for the timing diagraming and Table 21 on page 21 for the tSTATE timing requirement). When TX2UL enters configuration mode, the peripheral controller (link device) generates the pulses (falling edge) at the RESET_N pin to configure TX2UL. TX2UL configures its internal oscillator base on number of received pulses at the RESET_N pin. When the configuration is completed, deassert RESET_N (high) for tSTATE to exit the Configuration. If the TX2UL needs to enter the Configuration Mode again, it must go through the following power cycle: V_{CC} Off ℜ→ RESET_N Low ℜ→ V_{CC} On.

Configuration Mode in 24-Pin QFN package

To enter configuration mode keep the RESET_N pin pulled low for tSTATE (see Figure 20 on page 22 for the timing diagraming and Table 21 on page 21 for the tSTATE timing requirement) while deasserting CS_N (high). When TX2UL enters configuration mode, the peripheral controller (link device) generates the pulses (falling edge) at the RESET_N pin to configure TX2UL. TX2UL configures its internal oscillator base on number of received pulses at the RESET_N pin. When the configuration is completed, assert the CS_N (low) for tSTATE (see Figure 21 on page 21 for the timing) to exit the configuration mode. Figure 19 on page 22 shows the timing diagram of entering and exiting configuration mode. The configuration options are listed in Table 11. The TX2UL is defaulted to 26 MHz with single end clock input (to XI).

Table 11. TX2UL Configuration Options

Number of Pulses at RESET_N Pin during Configuration Mode	Configuration Description
0 pulses	26 MHz clock input on XI (default)
1 pulses	19.2 MHz clock input on XI
2 pulses	24.0 MHz clock input on XI
3 pulses	13.0 MHz clock input on XI
4 pulses	26 MHz crystal on XI/XO
5 pulses	19.2 MHz crystal on XI/XO
6 pulses	24.0 MHz crystal on XI/XO
7 pulses	13.0 MHz crystal on XI/XO

Power On Reset (POR)

TX2UL has an internal power on reset (POR) block that provides power on reset and power management control functionality. This POR function complies with all the parameters required by the ULPI specification.

Register

TX2UL provides an immediate register set that is defined by the ULPI specification for control and configuration functions.

Register Map

The ULPI specifications define an immediate register set with a 6-bit address that forms a part of the transmit command byte,as shown in shown in Table 12.

Table 12. Register Map

Field Name	Size (bits)	Address (6bits)			
		Rd	Wr	Set	Clr
Immediate Register Set					
Vendor ID Low	8	00h	-	-	-
Vendor ID High	8	01h	-	-	-
Product ID Low	8	02h	-	-	-
Product ID High	8	03h	-	-	-
Function Control	8	04-06h	04h	05h	06h
Interface Control	8	07-09h	07h	08h	09h
Debug	8	15h	-	-	-
Scratch Register	8	16-18h	16h	17h	18h
Carkit Control (Optional)	8	19-1Bh	19h	1Ah	1Bh
Vendor Specific Register Set					
Drive Strength and Slew Rate	8	31h	31h	-	-
USB Interface Control Register	8	35h	35h	-	-

Table 13 to Table 17 on page 18 define the read, write, set, and clear register options. The following are the conventions:

- Rd or rd = Read
- Wr or wr = Write
- Set or s = Set
- Clr or c = Clear

Immediate Register Set

The details of all immediate registers of TX2UL are shown in Table 6 on page 6, Table 18 on page 19, and Table 20 on page 21.

Function Control Register

Control ULPI Function Setting of TX2UL

Table 13. Function Control Register (Address: 04h - 06h [read], 04h [write], 05h [set], 06h [clear])

Bit	Field Name	Description	Access	Reset Value
1:0	XcvrSelect	Selects the required transceiver speed. 00b: Enable HS transceiver 01b: Enable FS transceiver 10b: Reserved 11b: Enable FS transceiver for LS packets.	rd/wr/s/c	01b
2	TermSelect	Controls the internal 1.5 K pull up resistor and 45 HS terminations.	rd/wr/s/c	0b
4:3	OpMode	Selects the required bit encording style during transmit. 00b: Normal operation 01b: Non-driving 10b: Disable bit stuff and NRZI encoding 11b: Do not automatically add SYNC and EOP when transmitting. It is used only for HS packets.	rd/wr/s/c	00b
5	Reset	Active high transceiver reset. After the link sets this bit, TX2UL asserts DIR and resets ULPI core. When the reset is completed, DIR is de-asserted and automatically clears this bit. After de-asserting DIR, TX2UL re-asserts DIR and sends and RX CMD update to the link. The link waits for DIR to de-assert before using ULPI bus. It does not reset the ULPI interface or ULPI register set.	rd/wr/s/c	0b
6	SuspendM	Active low. Put TX2UL into Low Power Mode. TX2UL powers down all blocks except the full speed receiver and ULPI interface pins. TX2UL sets this bit to ‘1’ when it exits from low power mode. 0b: Enter into low power mode 1b: Normal operation mode	rd/wr/s/c	1b
7	Reserved		rd	x

Interface Control Register

This register enables alternative interface and TX2UL features.

Table 14. Interface Control Register (Address: 07h - 09h [read], 07h [write], 08h [set], 09h [clear])

Bit	Field Name	Description	Access	Reset Value
1:0	Reserved		rd	xxb
2	CarkitMode	Changes the ULPI interface to carkit interface that support UART pass through mode. This bit is cleared when it exits from carkit UART pass through mode. 0b: Disable serial carkit mode 1b: Enable serial carkit mode	rd/wr/s/c	0b
6:3	Reserved		rd	xxxxb
7	Interface Protect Disable	Controls circuitry built into TX2UL for protecting the ULPI interface when the link tristates STP and DATA[7:0]. Any pull ups or pull downs employed by this feature are disabled 0b: Enable the interface Protect Circuit 1b: Disable the Interface Protect Circuit	rd/wr/s/c	0b

Debug Register

This register indicates the current value of various signals useful for debugging.

Table 15. Debug Register (Address: 15h [read only])

Bit	Field Name	Description	Access	Reset Value
0	LineState0	Contains the current value of LineState(0)	rd	0b
1	LineState1	Contains the current value of LineState(1)	rd	0b
7:2	Reserved		rd	000000b

Scratch Register

This register is for testing purpose only. The link can read, write, set and clear this register.

Table 16. Scratch Register (Address: 16h - 18h [read], 16h [write], 17h [set], 18h [clear])

Bit	Field Name	Description	Access	Reset Value
7:0	Scratch	Empty register byte for testing purposes. The link software reads, writes, sets, and clears this register.	rd/wr/s/c	00000000b

Carkit Control Register

This register controls the TXD and RXD in carkit UART pass through mode. It has no control function if the CarkitMode bit in Interface Control Register is not set.

Table 17. Carkit Control Register (Address: 19h - 1Bh [read], 19h [write], 1Ah [set], 1Bh [clear])

Bit	Field Name	Description	Access	Reset Value
1:0	Reserved		rd	xxb
2	TxdEn	Routes TXD signal from DATA[0] pin to DM pin	rd/wr/s/c	0b
3	RxdEn	Routes RXD signal from DP pin to DATA[1] pin	rd/wr/s/c	0b
7:4	Reserved		rd	xxxxb

Drive Strength and Slew Rate Configuration Register

This register is mapped to the vendor specific registers address. This register configures the drive strength and slew rate of the outputs.

Table 18. Drive Strength and Slew Rate Configuration Register (Address: 31h [read], 31h [write])

Bit	Field Name	Description	Access	Reset Value
1:0	DriveStrength	Configure the drive strength on the output pins 00b: Full drive strength 01b: Three quarter drive strength 10b: half drive strength 11b: Quarter drive strength	rd/wr	00b
2	SlewRate	Configure the slew rate on the output pins 0b: slow slew rate 1b: fast slew rate	rd/wr	0b
7:3	Reserved		rd	00000b

USB Interface Control Register

This register is mapped to the vendor specific registers address. This register enables or disables the USB interface.

Table 19. USB Interface Control Register (Address: 35h [read], 35h [write])

Bit	Field Name	Description	Access	Reset Value
1:0	Reserved	When write to this register, this field must be filled in 0s	rd	00b
2	UsbEnable	USB interface control 0b: Disable USB interface 1b: Enable USB interface	rd/wr	0b
7:3	Reserved	When write to this register, this field must be filled in 0s	rd	00000b

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power supplied (Industrial) ..... –40 °C to +85 °C

Supply voltage to ground potential

V_{CC} .....–0.5 V to +2.0 V

V_{IO} .....–0.5 V to +4.0 V

V_{BATT} .....–0.5 V to +5.775 V

DC input voltage to any input pin.....1.89 V to 3.6 V

Depends on I/O supply voltage. Inputs are not over voltage tolerant.

DC voltage applied to outputs in high Z state ..... –0.5 V to VCC + 0.5 V

Static discharge voltage (ESD) from JESD22-A114 ..... > 2000 V

Latch up current..... > 200 mA

Maximum output short circuit current for all I/O configurations. (Vout = 0 V) ..... –100 mA

Operating Conditions

Ambient temperature under bias (T_A) Industrial ..... –40 °C to +85 °C

V_{CC} supply voltage .....1.7 V to 1.9 V

V_{IO} supply voltage .....1.7 V to 3.6 V

V_{BATT} supply voltage .....3.0 V to 5.775 V

DC Characteristics

Table 20. DC Specifications for All Voltage Supplies

Parameter	Description	Conditions	Min	Typ	Max	Unit
VCC	Core voltage supply		1.7	1.8	1.9	V
VIO	ULPI interface I/O voltage supply (this I/O supply is not available on 20-Ball WLCSP package)		1.7	1.8, 2.5, 3.3	3.6	V
VBATT	Crystal voltage supply		3.0	–	5.775	V
$V_{POR(trip)}$	Power on reset trip voltage		1.0	–	1.5	V
V_{IH1}	Input HIGH voltage 1	All ports except USB, 2.0 V ≤ VIO < 3.6 V	0.625 × VIO	–	VIO + 0.3	V
V_{IH2}	Input HIGH voltage 2	All ports except USB, 1.7 V ≤ VIO < 2.0 V	VIO, 0.4	–	VIO + 0.3	V
V_{IL}	Input LOW voltage		–0.3	–	0.25 × VIO	V
V_{OH}	Output HIGH voltage	I_{OH}(MAX) = 0.1 mA	0.9 × VIO	–	–	V
V_{OL}	Output LOW voltage	I_{OL}(MIN) = 0.1 mA	–	–	0.1 × VIO	V
I_{IX}	Input leakage current	All I/O signals held at VDDQ	1	–	1	µA
I_{OZ}	Output leakage current	All I/O signals held at VDDQ	1	–	1	µA
ICC	Supply current	Continuous Receive	–	30	65	mA
		Continuous Transmit	–	30	65	mA
		ULPI Low Power Mode (Suspend) VCC = 1.8 V	–	300	750	µA
		Sleep Mode - ULPI interface bus is either Hz or drive High - DP and DM must be Hz or pull low	–	5	40	µA
I_{PU}	Pull up current	Interface protect enabled; STP pin only; V_I = 0 V	–13	–	–80	µA
I_{PD}	Pull down current	Interface protect enabled; DATA[7:0] only; V_I = VIO	16	–	90	µA

AC Characteristics

Table 21. ULPI Timing Parameters

Parameter	Description	Min	Max	Unit
tCS	Setup time for control input	5.8	–	ns
tDS	Setup time for data input	5.8	–	ns
tCH	Hold time for control input	0	–	ns
tDH	Hold time for data input	0	–	ns
tCD	Output delay time for control output	7.6	9.0	ns
tDD	Output delay time for data output	7.6	9.0	ns
tSTATE	Mode state change time	500	–	µs
tPW	Pulse width	200	10000	ns

Figure 18. ULPI Timing Diagram

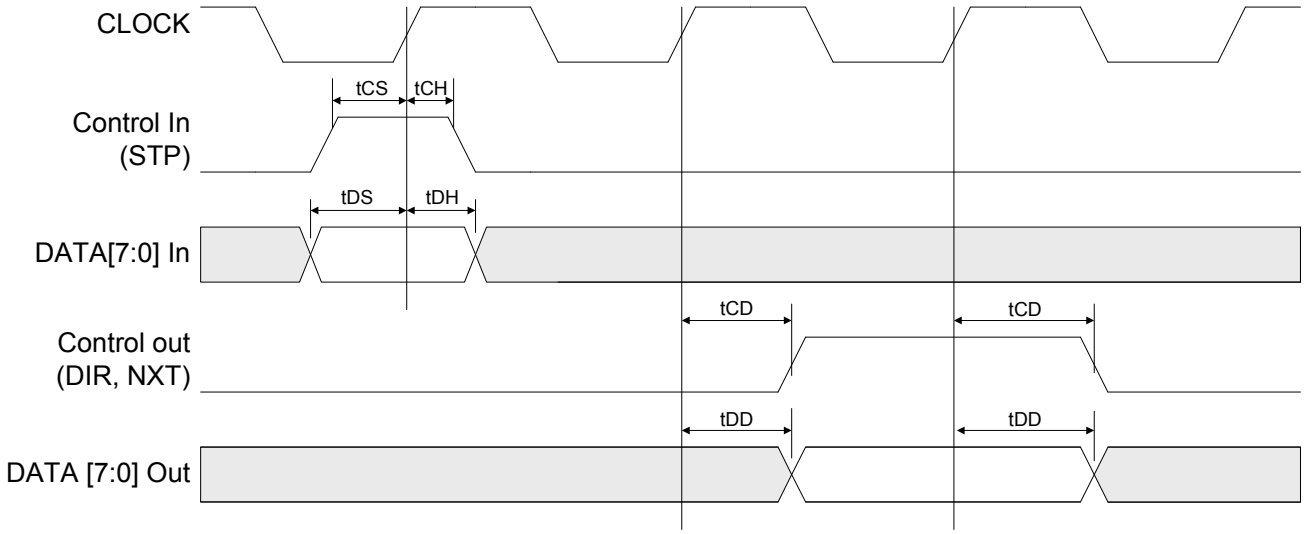


Figure 19. 20-Pin CSP Package Configuration Mode Entry Timing Diagram

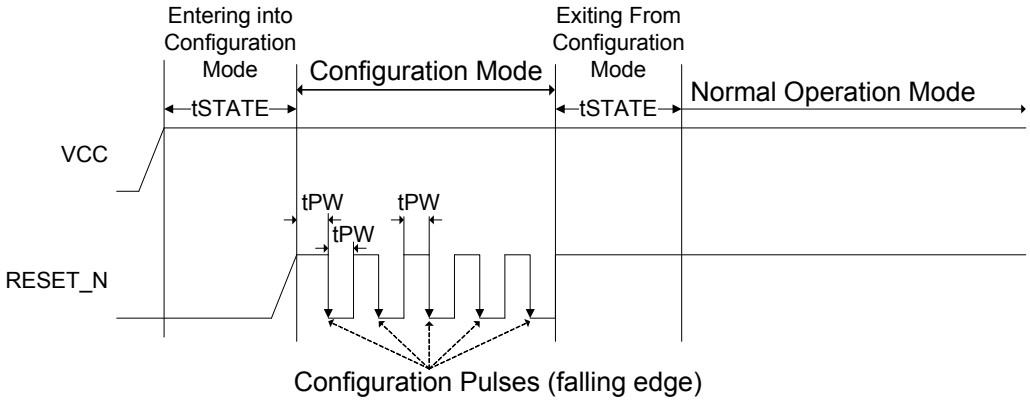


Figure 20. 24-Pin QFN Package Configuration Mode Entry Timing Diagram

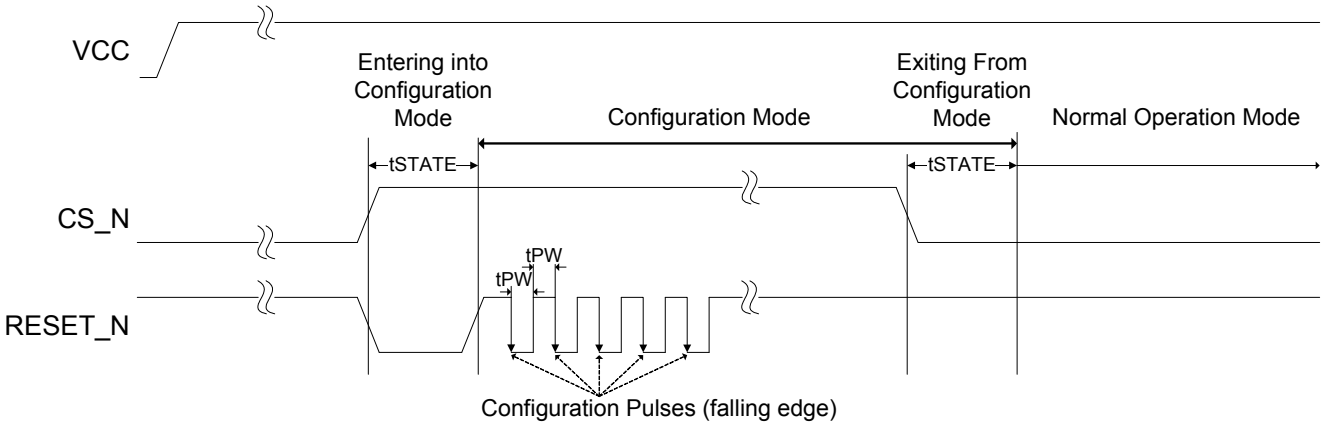
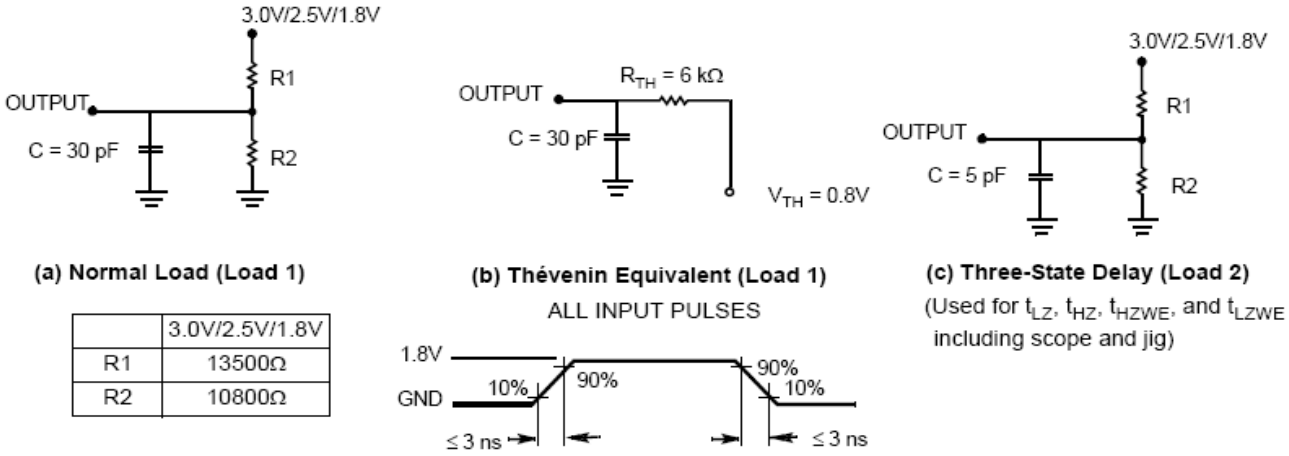
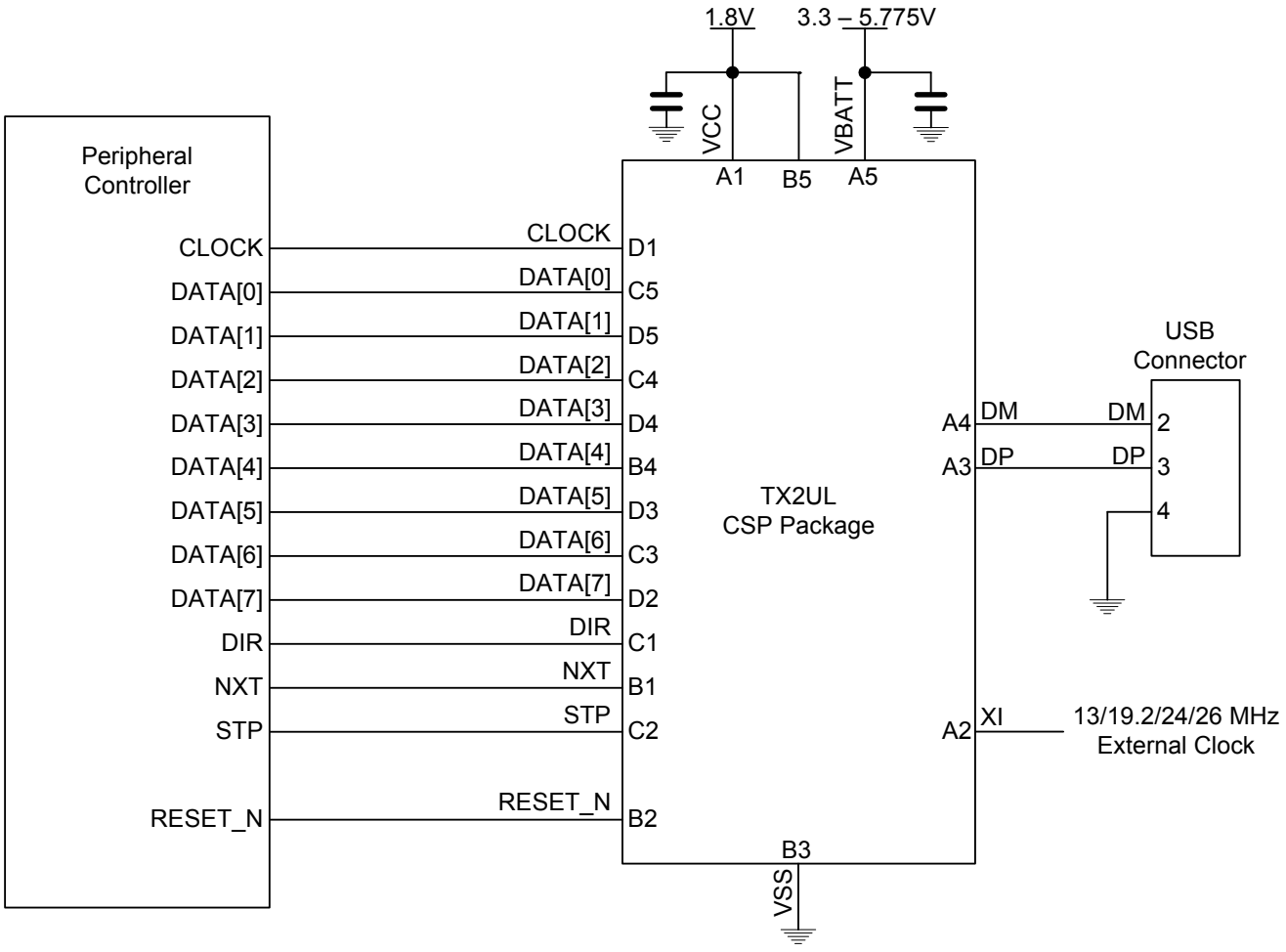


Figure 21. AC Test Loads and Waveforms



	3.0V/2.5V/1.8V
R1	13500Ω
R2	10800Ω

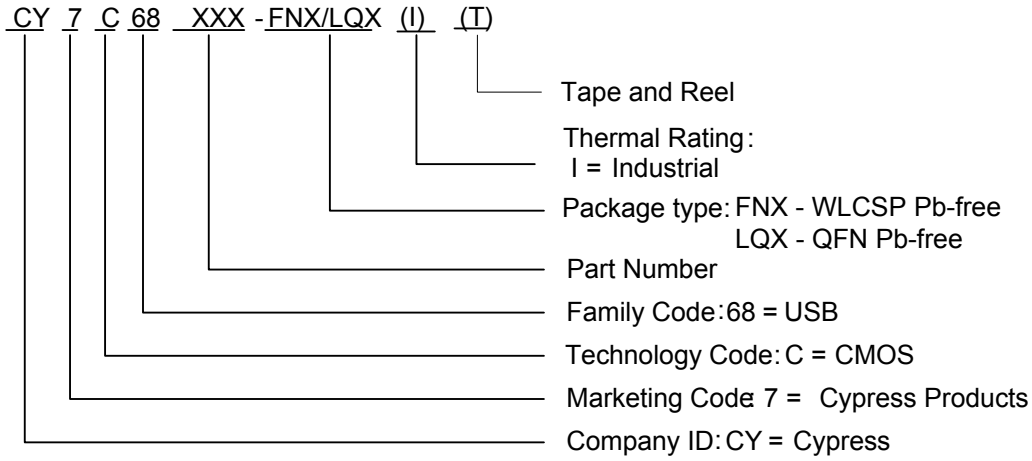
Figure 22. Connecting 20-Ball WLCSP Package TX2UL with a Standard Peripheral Controller with External Clock



Ordering Information

Ordering Code	Package Type	Support Clock Input Frequencies (MHz)
CY7C68003-20FNXIT	20-ball WLCSP – Tape and Reel	13, 19.2, 24, 26
CY7C68003-24LQXI	24-pin QFN	13, 19.2, 24, 26
CY7C68003-24LQXIT	24-pin QFN – Tape and Reel	13, 19.2, 24, 26

Ordering Code Definitions



Package Diagram

Figure 23. 20-Pin WLCSP Package Outline