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CY7C68013
EZ-USB FX2™ USB Microcontroller
High-speed USB Peripheral Controller

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1.0 EZ-USB FX2™ Features

Cypress's EZ-USB FX2™ is the world's first USB 2.0 integrated microcontroller. By integrating the USB 2.0 transceiver, SIE, enhanced 8051 microcontroller, and a programmable peripheral interface in a single chip, Cypress has created a very cost-effective solution that provides superior time-to-market advantages. The ingenious architecture of FX2 results in data transfer rates of 56 Mbytes per second, the maximum allowable USB 2.0 bandwidth, while still using a low-cost 8051 microcontroller in a package as small as a 56 SSOP. Because it incorporates the USB 2.0 transceiver, the FX2 is more economical, providing a smaller footprint solution than USB 2.0 SIE or external transceiver implementations. With EZ-USB FX2, the Cypress Smart SIE handles most of the USB 1.1 and 2.0 protocol in hardware, freeing the embedded microcontroller for application-specific functions and decreasing development time to ensure USB compatibility. The General Programmable Interface (GPIF) and Master/Slave Endpoint FIFO (8- or 16-bit data bus) provides an easy and glueless interface to popular interfaces such as ATA, UTOPIA, EPP, PCMCIA, and most DSP/processors.

Four packages are defined for the family: 56 SSOP, 56 QFN, 100 TQFP, and 128 TQFP.

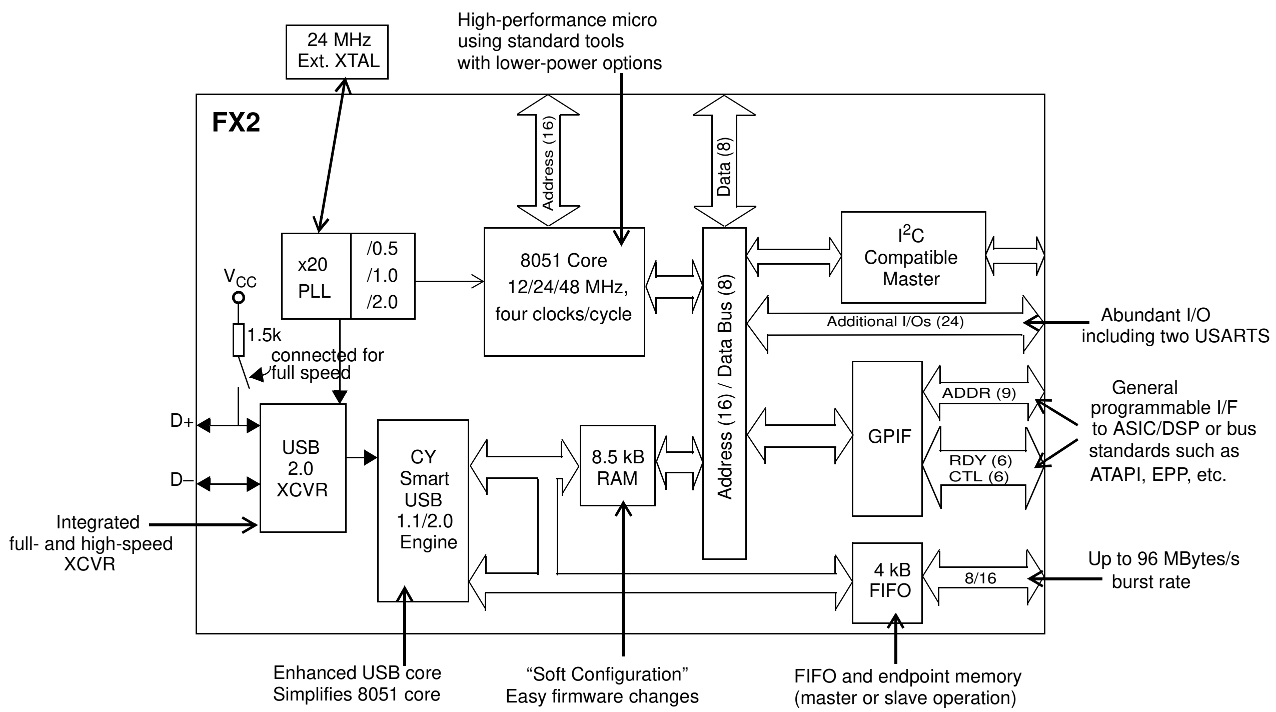


Figure 1-1. Block Diagram

- **Single-chip integrated USB 2.0 Transceiver, SIE, and Enhanced 8051 Microprocessor**
- **Software: 8051 runs from internal RAM, which is:**
  - **— Downloaded via USB, or**
  - **— Loaded from EEPROM**
  - **— External memory device (128-pin configuration only)**
- **Four programmable BULK/INTERRUPT/ISOCHRONOUS endpoints**
  - **— Buffering options: double, triple and quad**
- **8- or 16-bit external data interface**
- **GPIF**
  - **— Allows direct connection to most parallel interfaces; 8- and 16-bit**
  - **— Programmable waveform descriptors and configuration registers to define waveforms**
  - **— Supports multiple Ready (RDY) inputs and Control (CTL) outputs**
- **Integrated, industry standard 8051 with enhanced features:**
  - **— Up to 48-MHz clock rate**
  - **— Four clocks per instruction cycle**
  - **— Two USARTS**

— **Three counter/timers**
— **Expanded interrupt system**
— **Two data pointers**

- **Supports bus powered applications by using renumeration**
- **3.3V operation**
- **Smart Serial Interface Engine**
- **Vectored USB interrupts**
- **Separate data buffers for the SETUP and DATA portions of a CONTROL transfer**
- **Integrated I^2C-compatible controller, runs at 100 or 400 kHz**
- **48-MHz, 24-MHz, or 12-MHz 8051 operation**
- **Four integrated FIFOs**

— **Brings glue and FIFOs inside for lower system cost**
— **Automatic conversion to and from 16-bit buses**
— **Master or slave operation**
— **FIFOs can use externally supplied clock or asynchronous strobes**
— **Easy interface to ASIC and DSP ICs**

- **Special autovectors for FIFO and GPIF interrupts**
- **Up to 40 general purpose I/Os**
- **Four package options—128-pin TQFP, 100-pin TQFP, 56-pin QFN and 56-pin SSOP**.

2.0 Applications

- **DSL modems**
- **ATA interface**
- **Memory card readers**
- **Legacy conversion devices**
- **Cameras**
- **Scanners**
- **Home PNA**
- **Wireless LAN**
- **MP3 players**
- **Networking**.

The “Reference Designs” section of the cypress website provides additional tools for typical USB 2.0 applications. Each reference design comes complete with firmware source and object code, schematics, and documentation. Please visit http://www.cypress.com for more information.

3.0 Functional Overview

3.1 USB Signaling Speed

FX2 operates at two of the three rates defined in the Universal Serial Bus Specification Revision 2.0, dated April 27, 2000:

- Full speed, with a signaling bit rate of 12 Mbps
- High speed, with a signaling bit rate of 480 Mbps

FX2 does not support the low-speed signaling mode of 1.5 Mbps.

3.2 8051 Microprocessor

The 8051 microprocessor embedded in the FX2 family has 256 bytes of register RAM, an expanded interrupt system, three timer/counters, and two USARTs.

3.2.1 8051 Clock Frequency

FX2 has an on-chip oscillator circuit that uses an external 24-MHz (±100 ppm) crystal with the following characteristics:

- Parallel resonant
- Fundamental mode
- 500-µW drive level
- 20–33 pF (5% tolerance) load capacitors.

An on-chip PLL multiplies the 24-MHz oscillator up to 480 MHz, as required by the transceiver/PHY, and internal counters divide it down for use as the 8051 clock. The default 8051 clock frequency is 12 MHz. The clock frequency of the 8051 can be changed by the 8051 through the CPUCS register, dynamically.

The CLKOUT pin, which can be tri-stated and inverted using internal control bits, outputs the 50% duty cycle 8051 clock, at the selected 8051 clock frequency—48, 24, or 12 MHz.

3.2.2 USARTS

FX2 contains two standard 8051 USARTs, addressed via Special Function Register (SFR) bits. The USART interface pins are available on separate I/O pins, and are not multiplexed with port pins.

UART0 and UART1 can operate using an internal clock at 230 KBaud with no more than 1% baud rate error. 230-KBaud operation is achieved by an internally derived clock source that generates overflow pulses at the appropriate time. The internal clock adjusts for the 8051 clock rate (48, 24, 12 MHz) such that it always presents the correct frequency for 230-KBaud operation.

Note. 115-KBaud operation is also possible by programming the 8051 SMOD0 or SMOD1 bits to a “1” for UART0 and/or UART1, respectively.

3.2.3 Special Function Registers

Certain 8051 SFR addresses are populated to provide fast access to critical FX2 functions. These SFR additions are shown in *Table 3-1*. Bold type indicates non-standard, enhanced 8051 registers.

The two SFR rows that end with “0” and “8” contain bit-addressable registers. The four I/O ports A–D use the SFR addresses used in the standard 8051 for ports 0–3, which are not implemented in FX2.

Because of the faster and more efficient SFR addressing, the FX2 I/O ports are not addressable in external RAM space (using the MOVX instruction).

3.3 I^{2}C-compatible Bus

FX2 supports the I^{2}C-compatible bus as a master only at 100/400 kbps. SCL and SDA pins have open-drain outputs and hysteresis inputs. These signals must be pulled up to 3.3V, even if no I^{2}C-compatible device is connected.

3.4 Buses

All packages: 8- or 16-bit “FIFO” bidirectional data bus, multiplexed on I/O ports B and D. 128-pin package: adds 16-bit output-only 8051 address bus, 8-bit bidirectional data bus.

Table 3-1. Special Function Registers

x	8x	9x	Ax	Bx	Cx	Dx	Ex	Fx
0	**IOA**	**IOB**	**IOC**	**IOD**	SCON1	PSW	ACC	B
1	SP	**EXIF**	**INT2CLR**	**IOE**	SBUF1			
2	DPL0	**MPAGE**	**INT4CLR**	**OEA**				
3	DPH0			**OEB**				
4	**DPL1**			**OEC**				
5	**DPH1**			**OED**				
6	**DPS**			**OEE**				
7	PCON							
8	TCON	SCON0	IE	IP	T2CON	**EICON**	**EIE**	**EIP**
9	TMOD	SBUF0						
A	TL0	**AUTOPTRH1**	**EP2468STAT**	**EP01STAT**	RCAP2L			
B	TL1	**AUTOPTRL1**	**EP24FIFOFLGS**	**GPIFTRIG**	RCAP2H			
C	TH0	**reserved**	**EP68FIFOFLGS**		TL2			
D	TH1	**AUTOPTRH2**		**GPIFSGLDATH**	TH2			
E	**CKCON**	**AUTOPTRL2**		**GPIFSGLDATLX**				
F		**reserved**	**AUTOPTRSETUP**	**GPIFSGLDATLNOX**				

3.5 USB Boot Methods

During the power-up sequence, internal logic checks the I^2C-compatible port for the connection of an EEPROM whose first byte is either 0xC0 or 0xC2. If found, it uses the VID/PID/DID values in the EEPROM in place of the internally stored values (0xC0), or it boot-loads the EEPROM contents into internal RAM (0xC2). If no EEPROM is detected, FX2 enumerates using internally stored descriptors. The default ID values for FX2 are VID/PID/DID (0x04B4, 0x8613, 0xxxyy).

Table 3-2. Default ID Values for FX2

Default VID/PID/DID		
Vendor ID	0x04B4	Cypress Semiconductor
Prod ID	0x8613	EZ-USB FX2
Device release	0xXXYY	Depends on revision (0x04 for Rev E)

Note. The I^2C-compatible bus SCL and SDA pins must be pulled up, even if an EEPROM is not connected. Otherwise this detection method does not work properly.

3.6 ReNumeration™

Because the FX2's configuration is soft, one chip can take on the identities of multiple distinct USB devices.

When first plugged into USB, the FX2 enumerates automatically and downloads firmware and USB descriptor tables over the USB cable. Next, the FX2 enumerates again, this time as a device defined by the downloaded information. This patented two-step process, called ReNumeration™, happens instantly when the device is plugged in, with no hint that the initial download step has occurred.

Two control bits in the USBCS (USB Control and Status) register control the ReNumeration process: DISCON and RENUM. To simulate a USB disconnect, the firmware sets DISCON to 1. To reconnect, the firmware clears DISCON to 0.

Before reconnecting, the firmware sets or clears the RENUM bit to indicate whether the firmware or the Default USB Device will handle device requests over endpoint zero: if RENUM = 0, the Default USB Device will handle device requests; if RENUM = 1, the firmware will.

3.7 Bus Powered Applications

Bus powered applications require the FX2 to enumerate in a unconfigured mode with less then 100 mA. To do this, the FX2 must enumerate in the full speed mode and then, when configured, renumerate in high speed mode. For an example of the benefits and limitations of this renumeration process see the application note titled “Bus Powered Enumeration with FX2”.

3.8 Interrupt System

3.8.1 INT2 Interrupt Request and Enable Registers

FX2 implements an autovector feature for INT2 and INT4. There are 27 INT2 (USB) vectors, and 14 INT4 (FIFO/GPIF) vectors. See FX2 TRM for more details.

3.8.2 USB-Interrupt Autovectors

The main USB interrupt is shared by 27 interrupt sources. To save the code and processing time that normally would be required to identify the individual USB interrupt source, the FX2 provides a second level of interrupt vectoring, called Autovectoring. When a USB interrupt is asserted, the FX2 pushes the program counter onto its stack then jumps to address 0x0043, where it expects to find a "jump" instruction to the USB Interrupt service routine.

The FX2 jump instruction is encoded as follows.

Table 3-3. INT2 USB Interrupts

USB INTERRUPT TABLE FOR INT2			
Priority	INT2VEC Value	Source	Notes
1	00	SUDAV	SETUP Data Available
2	04	SOF	Start of Frame (or microframe)
3	08	SUTOK	Setup Token Received
4	0C	SUSPEND	USB Suspend request
5	10	USB RESET	Bus reset
6	14	HISPEED	Entered high speed operation
7	18	EP0ACK	FX2 ACK'd the CONTROL Handshake
8	1C		reserved
9	20	EP0-IN	EP0-IN ready to be loaded with data
10	24	EP0-OUT	EP0-OUT has USB data
11	28	EP1-IN	EP1-IN ready to be loaded with data
12	2C	EP1-OUT	EP1-OUT has USB data
13	30	EP2	IN: buffer available. OUT: buffer has data
14	34	EP4	IN: buffer available. OUT: buffer has data
15	38	EP6	IN: buffer available. OUT: buffer has data
16	3C	EP8	IN: buffer available. OUT: buffer has data
17	40	IBN	IN-Bulk-NAK (any IN endpoint)
18	44		reserved
19	48	EP0PING	EP0 OUT was Pinged and it NAK'd
20	4C	EP1PING	EP1 OUT was Pinged and it NAK'd
21	50	EP2PING	EP2 OUT was Pinged and it NAK'd
22	54	EP4PING	EP4 OUT was Pinged and it NAK'd
23	58	EP6PING	EP6 OUT was Pinged and it NAK'd
24	5C	EP8PING	EP8 OUT was Pinged and it NAK'd
25	60	ERRLIMIT	Bus errors exceeded the programmed limit
26	64		reserved
27	68		reserved
28	6C		reserved
29	70	EP2ISOERR	ISO EP2 OUT PID sequence error
30	74	EP4ISOERR	ISO EP4 OUT PID sequence error
31	78	EP6ISOERR	ISO EP6 OUT PID sequence error
32	7C	EP8ISOERR	ISO EP8 OUT PID sequence error

If Autovectoring is enabled (AV2EN = 1 in the INTSETUP register), the FX2 substitutes its INT2VEC byte. Therefore, if the high byte (“page”) of a jump-table address is preloaded at location 0x0044, the automatically-inserted INT2VEC byte at 0x0045 will direct the jump to the correct address out of the 27 addresses within the page.

3.8.3 FIFO/GPIF Interrupt (INT4)

Just as the USB Interrupt is shared among 27 individual USB-interrupt sources, the FIFO/GPIF interrupt is shared among 14 individual FIFO/GPIF sources. The FIFO/GPIF Interrupt, like the USB Interrupt, can employ autovectoring. *Table 3-4* shows the priority and INT4VEC values for the 14 FIFO/GPIF interrupt sources

Table 3-4. Individual FIFO/GPIF Interrupt Sources

Priority	INT4VEC Value	Source	Notes
1	80	EP2PF	Endpoint 2 Programmable Flag
2	84	EP4PF	Endpoint 4 Programmable Flag
3	88	EP6PF	Endpoint 6 Programmable Flag
4	8C	EP8PF	Endpoint 8 Programmable Flag
5	90	EP2EF	Endpoint 2 Empty Flag
6	94	EP4EF	Endpoint 4 Empty Flag
7	98	EP6EF	Endpoint 6 Empty Flag
8	9C	EP8EF	Endpoint 8 Empty Flag
9	A0	EP2FF	Endpoint 2 Full Flag
10	A4	EP4FF	Endpoint 4 Full Flag
11	A8	EP6FF	Endpoint 6 Full Flag
12	AC	EP8FF	Endpoint 8 Full Flag
13	B0	GPIFDONE	GPIF Operation Complete
14	B4	GPIFWF	GPIF Waveform

If Autovectoring is enabled (AV4EN = 1 in the INTSETUP register), the FX2 substitutes its INT4VEC byte. Therefore, if the high byte (“page”) of a jump-table address is preloaded at location 0x0054, the automatically-inserted INT4VEC byte at 0x0055 will direct the jump to the correct address out of the 14 addresses within the page. When the ISR occurs, the FX2 pushes the program counter onto its stack then jumps to address 0x0053, where it expects to find a “jump” instruction to the ISR Interrupt service routine.

3.9 Reset and Wakeup

3.9.1 Reset Pin

An input pin (RESET#) resets the chip. This pin has hysteresis and is active LOW. The internal PLL stabilizes approximately 200 µs after V_{CC} has reached 3.3V. Typically, an external RC network (R = 100k, C = 0.1 µF) is used to provide the RESET# signal.

3.9.2 Wakeup Pins

The 8051 puts itself and the rest of the chip into a power-down mode by setting PCON.0 = 1. This stops the oscillator and PLL. When WAKEUP is asserted by external logic, the oscillator restarts and after the PLL stabilizes, and the 8051 receives a wakeup interrupt. This applies whether or not FX2 is connected to the USB.

The FX2 exits the power down (USB suspend) state using one of the following methods:

- USB bus signals resume
- External logic asserts the WAKEUP pin
- External logic asserts the PA3/WU2 pin.

The second wakeup pin, WU2, can also be configured as a general purpose I/O pin. This allows a simple external R-C network to be used as a periodic wakeup source.

3.10 Program/Data RAM

3.10.1 Size

The FX2 has eight kbytes of internal program/data RAM, where PSEN#/RD# signals are internally ORed to allow the 8051 to access it as both program and data memory. No USB control registers appear in this space.

Two memory maps are shown in the following diagrams:

Figure 3-1 Internal Code Memory, EA = 0

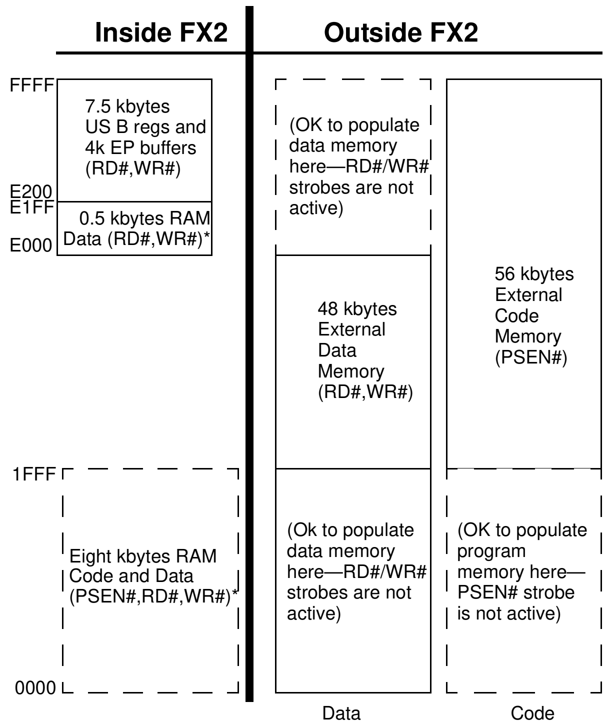
Figure 3-2 External Code Memory, EA = 1.

3.10.2 Internal Code Memory, EA = 0

This mode implements the internal eight-kbyte block of RAM (starting at 0) as combined code and data memory. When external RAM or ROM is added, the external read and write strobes are suppressed for memory spaces that exist inside the chip. This allows the user to connect a 64-kbyte memory without requiring address decodes to keep clear of internal memory spaces.

Only the **internal** eight kbytes and **scratch pad** 0.5 kbytes RAM spaces have the following access:

- USB download
- USB upload
- Setup data pointer
- I^{2}C-compatible interface boot load.

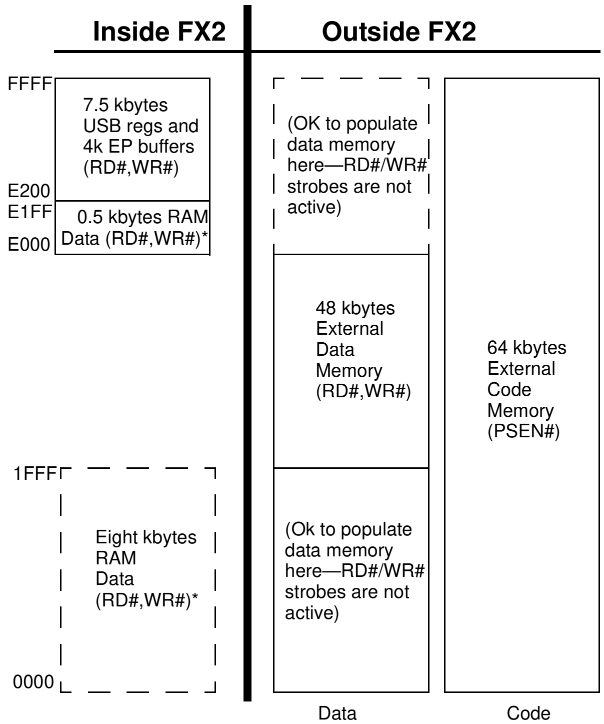


*SUDPTR, USB upload/download, I^{2}C-compatible interface boot access

Figure 3-1. Internal Code Memory, EA = 0

3.10.3 External Code Memory, EA = 1

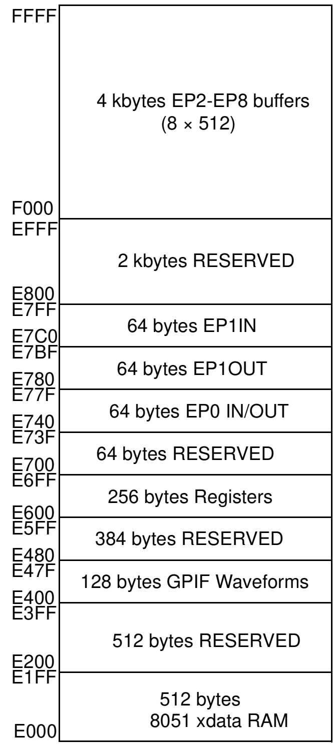
The bottom eight kbytes of program memory is external, and therefore the bottom eight kbytes of internal RAM is accessible only as data memory.



*SUDPTR, USB upload/download, I^{2}C-compatible interface boot access

Figure 3-2. External Code Memory, EA = 1

3.11 Register Addresses



3.12 Endpoint RAM

3.12.1 Size

- 3 × 64 bytes (Endpoints 0 and 1)
- 8 × 512 bytes (Endpoints 2, 4, 6, 8)

3.12.2 Organization

- EP0 Bidirectional endpoint zero, 64-byte buffer
- EP1IN, EP1OUT 64-byte buffers, bulk or interrupt
- EP2,4,6,8 Eight 512-byte buffers, bulk, interrupt, or isochronous. EP2 and 6 can be either double, triple, or quad buffered. For high-speed endpoint configuration options, see *Figure 3-3*.

3.12.3 Setup Data Buffer

A separate eight-byte buffer at 0xE6B8-0xE6BF holds the SETUP data from a CONTROL transfer.

3.12.4 Endpoint Configurations (High-speed Mode)

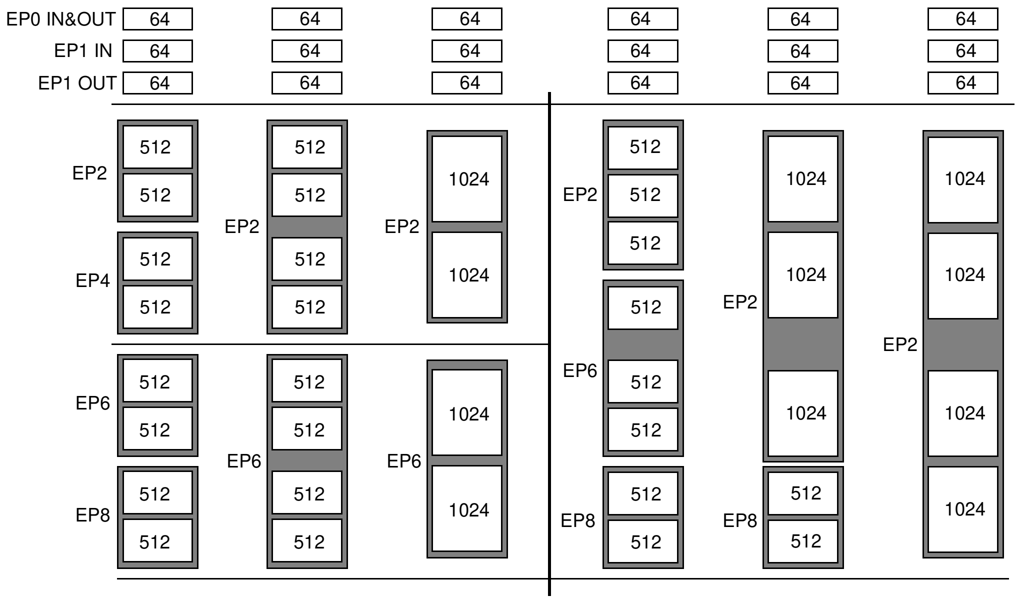


Figure 3-3. Endpoint Configuration

Endpoints 0 and 1 are the same for every configuration. Endpoint 0 is the only CONTROL endpoint, and endpoint 1 can be either BULK or INTERRUPT. To the left of the vertical line, the user may pick different configurations for EP2&4 and EP6&8, since none of the 512-byte buffers are combined between these endpoint groups. An example endpoint configuration would be:

EP2—1024 double buffered; EP6—512 quad buffered.

To the right of the vertical line, buffers are shared between EP2–8, and therefore only entire columns may be chosen.

3.12.5 Default Full-Speed Alternate Settings

Table 3-5. Default Full-Speed Alternate Settings[1, 2]

Alternate Setting	0	1	2	3
ep0	64	64	64	64
ep1out	0	64 bulk	64 int	64 int
ep1in	0	64 bulk	64 int	64 int
ep2	0	64 bulk out (2×)	64 int out (2×)	64 iso out (2×)
ep4	0	64 bulk out (2×)	64 bulk out (2×)	64 bulk out (2×)
ep6	0	64 bulk in (2×)	64 int in (2×)	64 iso in (2×)
ep8	0	64 bulk in (2×)	64 bulk in (2×)	64 bulk in (2×)

Notes:
1. “0” means “not implemented.”
2. “2x” means “double buffered.”

3.12.6 Default High-Speed Alternate Settings

Table 3-6. Default High-Speed Alternate Settings[1, 2]

Alternate Setting	0	1	2	3
ep0	64	64	64	64
ep1out	0	512 bulk[3]	64 int	64 int
ep1in	0	512 bulk[3]	64 int	64 int
ep2	0	512 bulk out (2×)	512 int out (2×)	512 iso out (2×)
ep4	0	512 bulk out (2×)	512 bulk out (2×)	512 bulk out (2×)
ep6	0	512 bulk in (2×)	512 int in (2×)	512 iso in (2×)
ep8	0	512 bulk in (2×)	512 bulk in (2×)	512 bulk in (2×)

Note:

3. Even though these buffers are 64 bytes, they are reported as 512 for USB 2.0 compliance. The user must never transfer packets larger than 64 bytes to EP1.

3.13 External FIFO interface

3.13.1 Architecture

The FX2 slave FIFO architecture has eight 512-byte blocks in the endpoint RAM that directly serve as FIFO memories, and are controlled by FIFO control signals (such as IFCLK, SLCS#, SLRD, SLWR, SLOE, PKTEND, and flags).

In operation, some of the eight RAM blocks fill or empty from the SIE, while the others are connected to the I/O transfer logic. The transfer logic takes two forms, the GPIF for internally generated control signals, or the slave FIFO interface for externally controlled transfers.

3.13.2 Master/Slave Control Signals

The FX2 endpoint FIFOS are implemented as eight physically distinct 256x16 RAM blocks. The 8051/SIE can switch any of the RAM blocks between two domains, the USB (SIE) domain and the 8051-I/O Unit domain. This switching is done virtually instantaneously, giving essentially zero transfer time between "USB FIFOS" and "Slave FIFOS." Since they are physically the same memory, no bytes are actually transferred between buffers.

At any given time, some RAM blocks are filling/emptying with USB data under SIE control, while other RAM blocks are available to the 8051 and/or the I/O control unit. The RAM blocks operate as single-port in the USB domain, and dual-port in the 8051-I/O domain. The blocks can be configured as single, double, triple, or quad buffered as previously shown.

The I/O control unit implements either an internal-master (M for master) or external-master (S for Slave) interface.

In Master (M) mode, the GPIF internally controls FIFOADR[1..0] to select a FIFO. The RDY pins (two in the 56-pin package, six in the 100-pin and 128-pin packages) can be used as flag inputs from an external FIFO or other logic if desired. The GPIF can be run from either an internally derived clock or externally supplied clock (IFCLK), at a rate that transfers data up to 96 Megabytes/s (48 MHz).

In Slave (S) mode, the FX2 accepts either an internally derived clock or externally supplied clock (IFCLK, max. frequency 48 MHz) and SLCS#, SLRD, SLWR, SLOE, PKTEND signals from external logic. Each endpoint can individually be selected for byte or word operation by an internal configuration bit, and a Slave FIFO Output Enable signal SLOE enables data of the selected width. External logic must insure that the output enable signal is inactive when writing data to a slave FIFO. The slave interface can also operate asynchronously, where the SLRD and SLWR signals act directly as strobes, rather than a clock qualifier as in synchronous mode. The signals SLRD, SLWR, SLOE and PKTEND are gated by the signal SLCS#.

3.13.3 GPIF and FIFO Clock Rates

An 8051 register bit selects one of two frequencies for the internally supplied interface clock: 30 MHz and 48 MHz. Alternatively, an externally supplied clock of 5 MHz – 48 MHz feeding the IFCLK pin can be used as the interface clock. IFCLK can be configured to function as an output clock when the GPIF and FIFOs are internally clocked. An output enable bit in the IFCONFIG register turns this clock output off, if desired. Another bit within the IFCONFIG register will invert the IFCLK signal whether internally or externally sourced.

3.14 GPIF

The GPIF is a flexible 8- or 16-bit parallel interface driven by a user-programmable finite state machine. It allows the CY7C68013 to perform local bus mastering, and can implement a wide variety of protocols such as ATA interface, printer parallel port, and Utopia.

The GPIF has six programmable control outputs (CTL), nine address outputs (GPIFADRx), and six general-purpose ready inputs (RDY). The data bus width can be 8 or 16 bits. Each GPIF vector defines the state of the control outputs, and determines what state a ready input (or multiple inputs) must be before proceeding. The GPIF vector can be programmed to advance a FIFO to the next data value, advance an address, etc. A sequence of the GPIF vectors make up a single waveform that will be executed to perform the desired data move between the CY7C68013 and the external design.

3.14.1 Six Control OUT Signals

The 100- and 128-pin packages bring out all six Control Output pins (CTL0-CTL5). The 8051 programs the GPIF unit to define the CTL waveforms. The 56-pin package brings out three of these signals, CTL0–CTL2. CTLx waveform edges can be programmed to make transitions as fast as once per clock (20.8 ns using a 48-MHz clock).

3.14.2 Six Ready IN Signals

The 100- and 128-pin packages bring out all six Ready inputs (RDY0–RDY5). The 8051 programs the GPIF unit to test the RDY pins for GPIF branching. The 56-pin package brings out two of these signals, RDY0–1.

3.14.3 Nine GPIF Address OUT signals

Nine GPIF address lines are available in the 100- and 128-pin packages, GPIFADR[8..0]. The GPIF address lines allow indexing through up to a 512-byte block of RAM. If more address lines are needed, I/O port pins can be used.

3.14.4 Long Transfer Mode

In master mode, the 8051 appropriately sets GPIF transaction count registers (GPIFTCB3, GPIFTCB2, GPIFTCB1, or GPIFTCB0) for unattended transfers of up to 4,294,967,296 bytes. The GPIF automatically throttles data flow to prevent under or overflow until the full number of requested transactions complete. The GPIF decrements the value in these registers to represent the current status of the transaction.

3.15 USB Uploads and Downloads

The core has the ability to directly edit the data contents of the internal 8-kbyte RAM and of the internal 512-byte scratch pad RAM via a vendor-specific command. This capability is normally used when “soft” downloading user code and is available only to and from internal RAM, whether the 8051 is held in reset or running. The available RAM spaces are 8 kbytes from 0x0000–0x1FFF (code/data) and 512 bytes from 0xE000–0xE1FF (scratch pad RAM).

Note: A “loader” running in internal RAM can be used to transfer downloaded data to external memory.

3.16 Autopointer Access

FX2 provides two identical autopointers. They are similar to the internal 8051 data pointers, but with an additional feature: they can optionally increment a pointer address after every memory access. This capability is available to and from both internal and external RAM. The autopointers are available in external FX2 registers, under control of a mode bit (AUTOPTRSETUP.0). Using the external FX2 autopointer access (at 0xE67B – 0xE67C) allows the autopointer to access all RAM, internal and external to the part. Also, the autopointers can point to any FX2 register or endpoint buffer space. When autopointer access to external memory is enabled, location 0xE67B and 0xE67C in XDATA and PDATA space cannot be used.

3.17 I^2C-compatible Controller

FX2 has one I^2C-compatible port that is driven by two internal controllers, one that automatically operates at boot time to load VID/PID/DID and configuration information, and another that the 8051, once running, uses to control external I^2C-compatible devices. The I^2C-compatible port operates in master mode only.

3.17.1 I^2C-compatible Port Pins

The I^2C-compatible pins SCL and SDA must have external 2.2-kΩ pull-up resistors. External EEPROM device address pins must be configured properly. See *Table 3-7* for configuring the device address pins.

Table 3-7. Strap Boot EEPROM Address Lines to These Values

Bytes	Example EEPROM	A2	A1	A0
16	24LC00[4]	N/A	N/A	N/A
128	24LC01	0	0	0
256	24LC02	0	0	0
4K	24LC32	0	0	1
8K	24LC64	0	0	1

3.17.2 I^{2}C-compatible Interface Boot Load Access

At power-on reset the I^{2}C-compatible interface boot loader will load the VID/PID/DID/a configuration byte and up to 8 kbytes of program/data. The available RAM spaces are 8 kbytes from 0x0000–0x1FFF and 512 bytes from 0xE000–0xE1FF. The 8051 will be in reset. I^{2}C-compatible interface boot loads only occur after power-on reset.

3.17.3 I^{2}C-compatible Interface General Purpose Access

The 8051 can control peripherals connected to the I^{2}C-compatible bus using the I2CTL and I2DAT registers. FX2 provides I^{2}C compatible master control only, it is never an I^{2}C-compatible slave.

4.0 Pin Assignments

Figure 4-1 identifies all signals for the four package types. The following pages illustrate the individual pin diagrams, plus a combination diagram showing which of the full set of signals are available in the 128-, 100-, and 56-pin packages.

The 56-pin package is the lowest-cost version. The signals on the left edge of the 56-pin package in *Figure 4-1* are common to all versions in the FX2 family. Three modes are available in all package versions: Port, GPIF master, and Slave FIFO. These modes define the signals on the right edge of the diagram. The 8051 selects the interface mode using the IFCONFIG[1:0] register bits. Port mode is the power-on default configuration.

The 100-pin package adds functionality to the 56-pin package by adding these pins:

- PORTC or alternate GPIFADR[7...0] address signals
- PORTE or alternate GPIFADR8 address signals and 7 more 8051 signals
- 3 GPIF Control signals
- 4 GPIF Ready signals
- Nine 8051 signals (two USARTs, three timer inputs, INT4,and INT5#)
- BKPT, RD#, WR#

The 128-pin package is the full version, adding the 8051 address and data buses plus control signals. Note that two of the required signals, RD# and WR#, are present in the 100-pin version. In the 100-pin and 128-pin versions, an 8051 control bit can be set to pulse the RD# and WR# pins when the 8051 reads from/writes to PORTC.

Note:

4. This EEPROM does not have address pins.

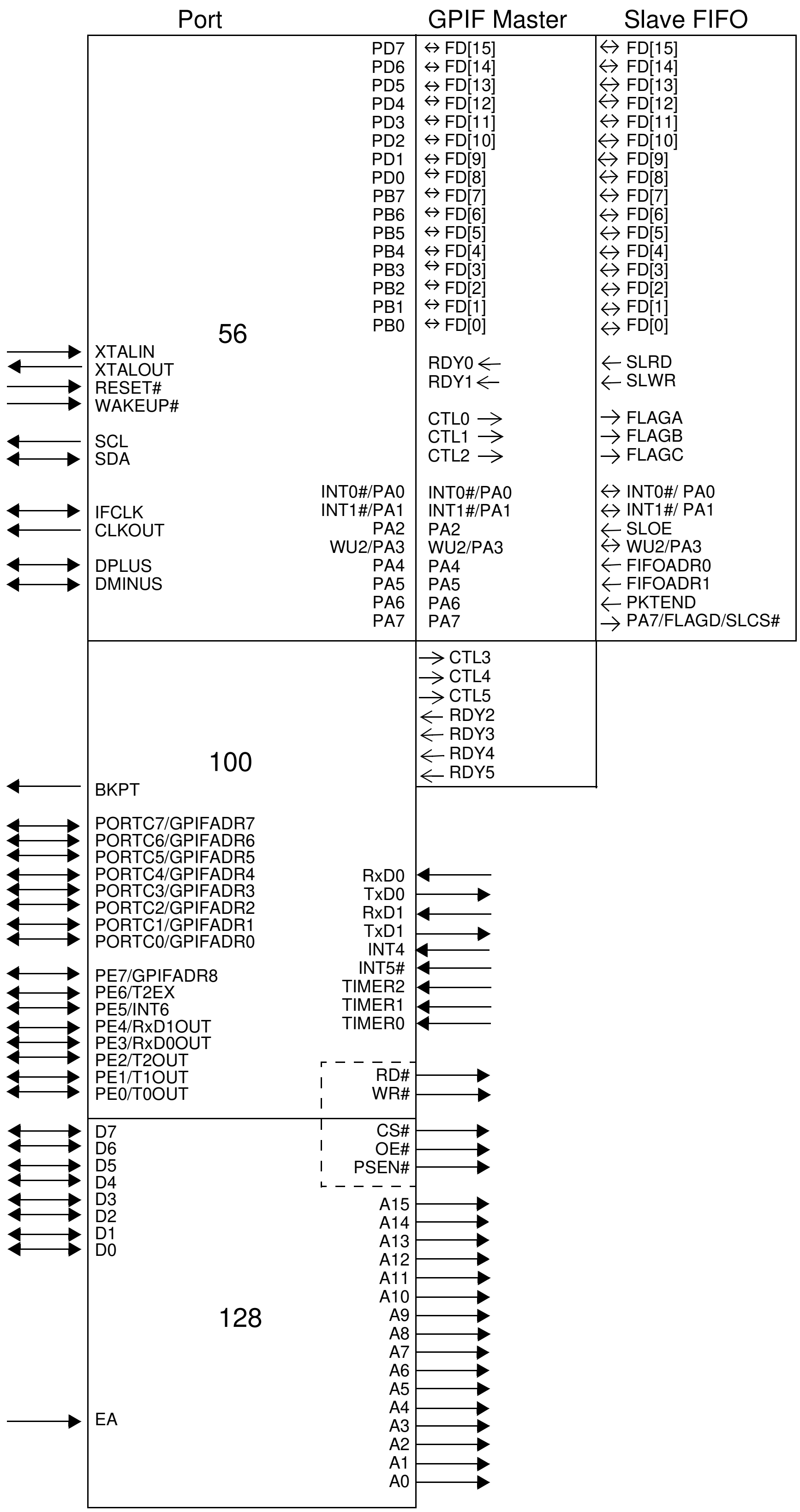


Figure 4-1. Signals

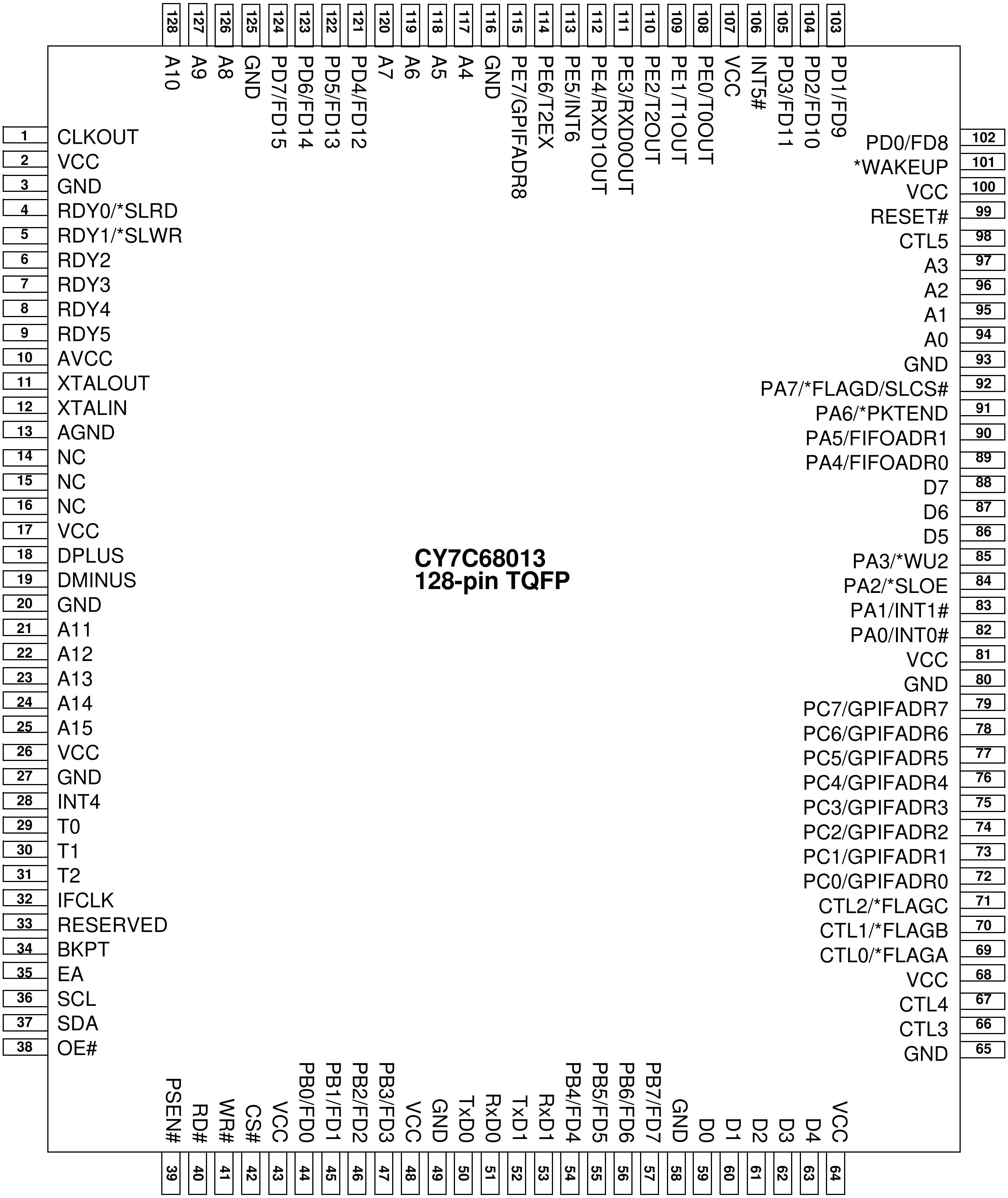


Figure 4-2. CY7C68013 128-pin TQFP Pin Assignment

* denotes programmable polarity

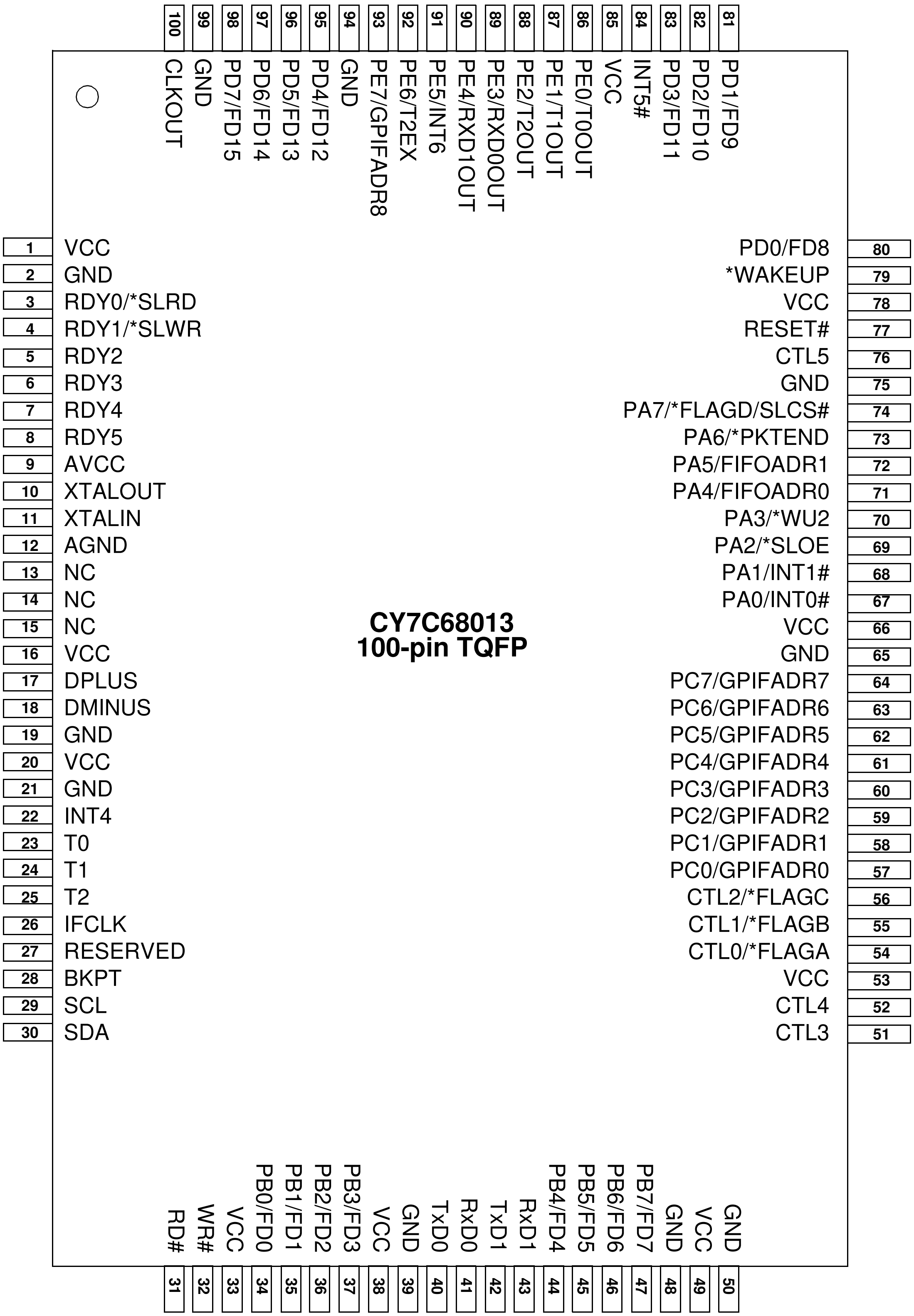


Figure 4-3. CY7C68013 100-pin TQFP Pin Assignment

* denotes programmable polarity

CY7C68013
56-pin SSOP

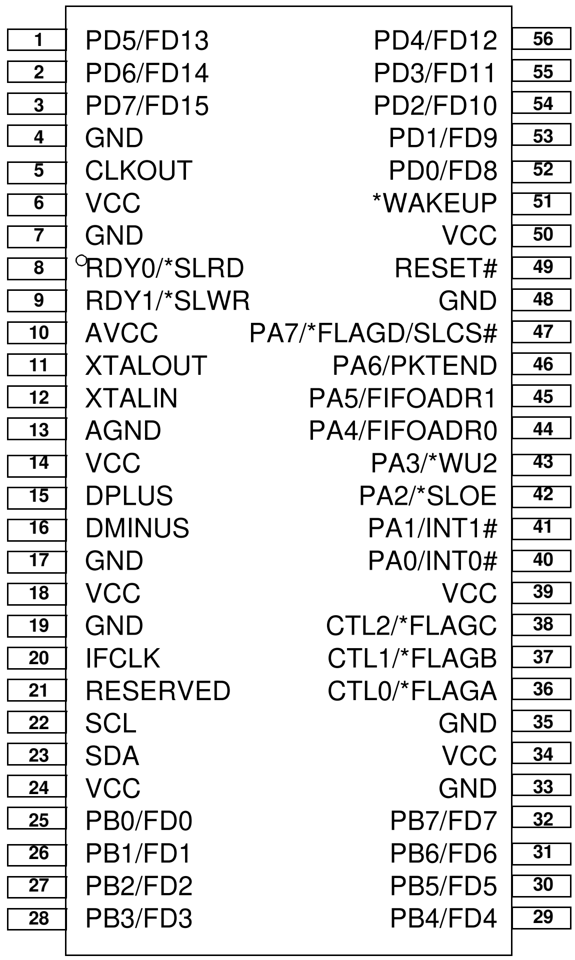


Figure 4-4. CY7C68013 56-pin SSOP Pin Assignment

* denotes programmable polarity

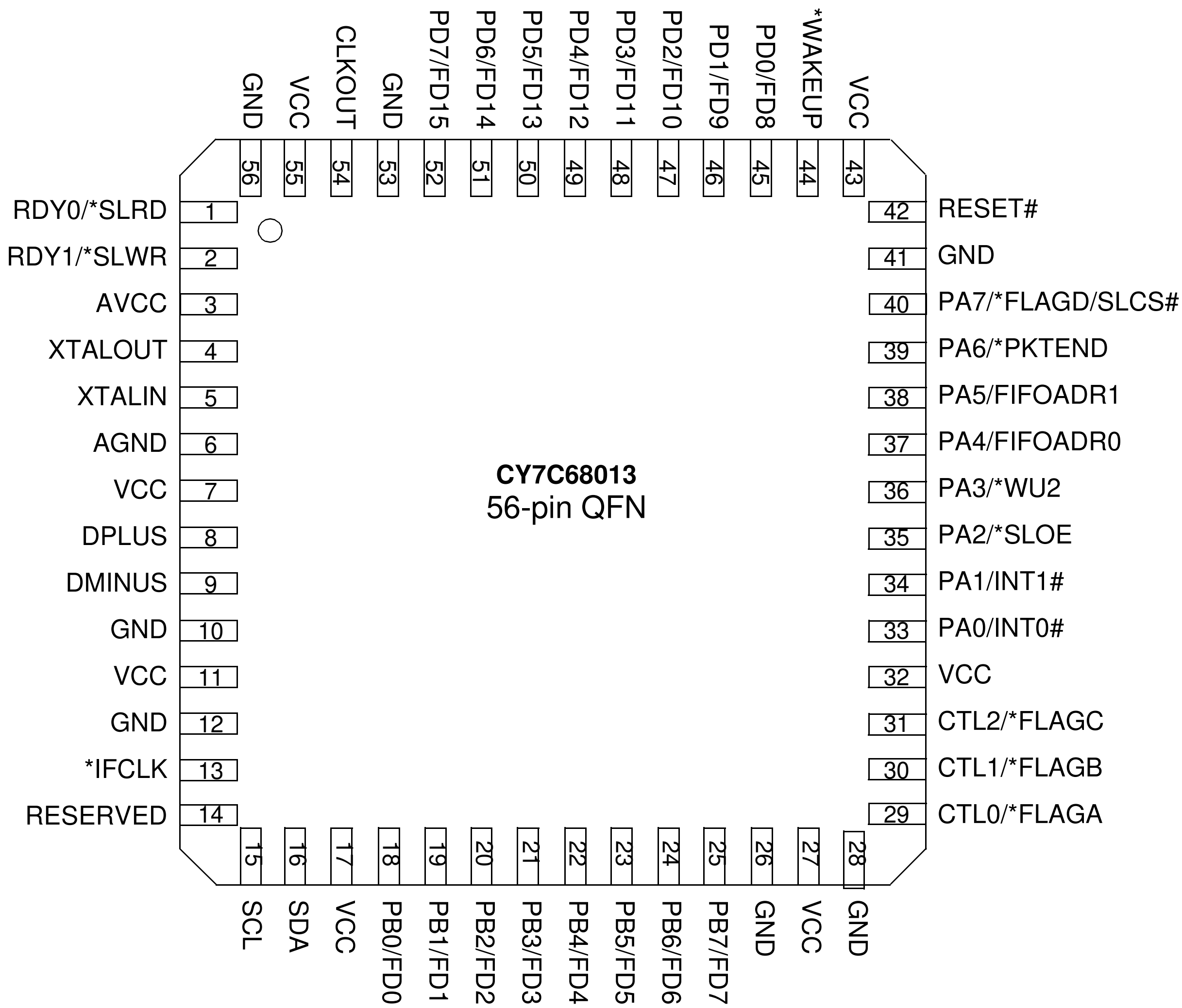


Figure 4-5. CY7C68013 56-pin QFN Pin Assignment

* denotes programmable polarity

4.1 CY7C68013 Pin Descriptions

Table 4-1. FX2 Pin Descriptions [5]

128 TQFP	100 TQFP	56 SSOP	56 QFN	Name	Type	Default	Description
10	9	10	3	AVCC	Power	N/A	**Analog V_{CC}**. This signal provides power to the analog section of the chip.
13	12	13	6	AGND	Power	N/A	**Analog Ground**. Connect to ground with as short a path as possible.
19	18	16	9	DMINUS	I/O/Z	Z	**USB D– Signal**. Connect to the USB D– signal.
18	17	15	8	DPLUS	I/O/Z	Z	**USB D+ Signal**. Connect to the USB D+ signal.
94				A0	Output	L	**8051 Address Bus**. This bus is driven at all times. When the 8051 is addressing internal RAM it reflects the internal address.
95				A1	Output	L	
96				A2	Output	L	
97				A3	Output	L	
117				A4	Output	L	
118				A5	Output	L	
119				A6	Output	L	
120				A7	Output	L	
126				A8	Output	L	
127				A9	Output	L	
128				A10	Output	L	
21				A11	Output	L	
22				A12	Output	L	
23				A13	Output	L	
24				A14	Output	L	
25				A15	Output	L	
59				D0	I/O/Z	Z	**8051 Data Bus**. This bidirectional bus is high-impedance when inactive, input for bus reads, and output for bus writes. The data bus is used for external 8051 program and data memory. The data bus is active only for external bus accesses, and is driven LOW in suspend.
60				D1	I/O/Z	Z	
61				D2	I/O/Z	Z	
62				D3	I/O/Z	Z	
63				D4	I/O/Z	Z	
86				D5	I/O/Z	Z	
87				D6	I/O/Z	Z	
88				D7	I/O/Z	Z	
39				PSEN#	Output	H	**Program Store Enable**. This active-LOW signal indicates an 8051 code fetch from external memory. It is active for program memory fetches from 0x2000–0xFFFF when the EA pin is LOW, or from 0x0000–0xFFFF when the EA pin is HIGH.
34	28			BKPT	Output	L	**Breakpoint**. This pin goes active (HIGH) when the 8051 address bus matches the BPADDRH/L registers and breakpoints are enabled in the BREAKPT register (BPEN = 1). If the BPPULSE bit in the BREAKPT register is HIGH, this signal pulses HIGH for eight 12-/24-/48-MHz clocks. If the BPPULSE bit is LOW, the signal remains HIGH until the 8051 clears the BREAK bit (by writing 1 to it) in the BREAKPT register.
99	77	49	42	RESET#	Input	N/A	**Active LOW Reset**. Resets the entire chip. This pin is normally tied to V_{CC} through a 100K resistor, and to GND through a 0.1-µF capacitor.

Note:
5. Unused inputs should not be left floating. Tie either HIGH or LOW as appropriate. Outputs should only be pulled up or down to ensure signals at power-up and in standby.

Table 4-1. FX2 Pin Descriptions (continued)[5]

128 TQFP	100 TQFP	56 SSOP	56 QFN	Name	Type	Default	Description
35				EA	Input	N/A	**External Access**. This pin determines where the 8051 fetches code between addresses 0x0000 and 0x1FFF. If EA = 0 the 8051 fetches this code from its internal RAM. IF EA = 1 the 8051 fetches this code from external memory.
12	11	12	5	XTALIN	Input	N/A	**Crystal Input**. Connect this signal to a 24-MHz parallel-resonant, fundamental mode crystal and load capacitor to GND. It is also correct to drive XTALIN with an external 24 MHz square wave derived from another clock source.
11	10	11	4	XTALOUT	Output	N/A	**Crystal Output**. Connect this signal to a 24-MHz parallel-resonant, fundamental mode crystal and load capacitor to GND. If an external clock is used to drive XTALIN, leave this pin open.
1	100	5	54	CLKOUT	O/Z	12 MHz	12-, 24- or 48-MHz clock, phase locked to the 24-MHz input clock. The 8051 defaults to 12-MHz operation. The 8051 may tri-state this output by setting CPUCS.1 = 1.
Port A							
82	67	40	33	PA0 or INT0#	I/O/Z	I (PA0)	Multiplexed pin whose function is selected by: PORTACFG.0 **PA0** is a bidirectional IO port pin. **INT0#** is the active-LOW 8051 INT0 interrupt input signal, which is either edge triggered (IT0 = 1) or level triggered (IT0 = 0).
83	68	41	34	PA1 or INT1#	I/O/Z	I (PA1)	Multiplexed pin whose function is selected by: PORTACFG.1 **PA1** is a bidirectional IO port pin. **INT1#** is the active-LOW 8051 INT1 interrupt input signal, which is either edge triggered (IT1 = 1) or level triggered (IT1 = 0).
84	69	42	35	PA2 or SLOE	I/O/Z	I (PA2)	Multiplexed pin whose function is selected by two bits: IFCONFIG[1:0]. **PA2** is a bidirectional IO port pin. **SLOE** is an input-only output enable with programmable polarity (FIFOPOLAR.4) for the slave FIFOs connected to FD[7..0] or FD[15..0].
85	70	43	36	PA3 or WU2	I/O/Z	I (PA3)	Multiplexed pin whose function is selected by: WAKEUP.7 and OEA.3 **PA3** is a bidirectional I/O port pin. **WU2** is an alternate source for **USB Wakeup,** enabled by WU2EN bit (WAKEUP.1) and polarity set by WU2POL (WAKEUP.4). If the 8051 is in suspend and WU2EN = 1, a transition on this pin starts up the oscillator and interrupts the 8051 to allow it to exit the suspend mode. Asserting this pin inhibits the chip from suspending, if WU2EN=1.
89	71	44	37	PA4 or FIFOADR0	I/O/Z	I (PA4)	Multiplexed pin whose function is selected by: IFCONFIG[1..0]. **PA4** is a bidirectional I/O port pin. **FIFOADR0** is an input-only address select for the slave FIFOs connected to FD[7..0] or FD[15..0].
90	72	45	38	PA5 or FIFOADR1	I/O/Z	I (PA5)	Multiplexed pin whose function is selected by: IFCONFIG[1..0]. **PA5** is a bidirectional I/O port pin. **FIFOADR1** is an input-only address select for the slave FIFOs connected to FD[7..0] or FD[15..0].
91	73	46	39	PA6 or PKTEND	I/O/Z	I (PA6)	Multiplexed pin whose function is selected by the IFCONFIG[1:0] bits. **PA6** is a bidirectional I/O port pin. **PKTEND** is an input-only packet end with programmable polarity (FIFOPOLAR.5) for the slave FIFOs connected to FD[7..0] or FD[15..0].