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CY7C68300C/CY7C68301C
CY7C68320C/CY7C68321C

EZ-USB AT2LP™ USB 2.0 to ATA/ATAPI Bridge

Features

- Fixed Function Mass Storage Device - Requires no Firmware
- Two Power Modes: Self Powered and USB Bus Powered to enable Bus Powered CF (CompactFlash) Readers and Truly Portable USB Hard Drives
- Certified Compliant for USB 2.0 (TID# 40490119), the USB Mass Storage Class, and the USB Mass Storage Class Bulk-Only Transport (BOT) Specification
- Operates at High-Speed (480 Mbps) or Full-Speed (12 Mbps) USB
- Complies with ATA/ATAPI-6 Specification
- Supports 48-bit Addressing for Large Hard Drives
- Supports ATA Security Features
- Supports any ATA Command with the ATACB Function
- Supports Mode for BIOS Boot Support
- Supports ATAPI Serial Number VPD Page Retrieval for Digital Rights Management (DRM) Compatibility
- Supports PIO Modes 0, 3, and 4, Multiword DMA Mode 2, and UDMA Modes 2, 3, and 4
- Uses One Small External Serial EEPROM for Storage of USB Descriptors and Device Configuration Data
- ATA Interface IRQ Signal Support
- Supports one or two ATA/ATAPI Devices
- Supports CompactFlash and one ATA/ATAPI Device
- Supports Board-level Manufacturing Test using the USB I/F
- Places the ATA Interface in High Impedance (High Z) to enable Sharing of the ATA Bus with another Controller such as an IEEE-1394 to ATA Bridge Chip or MP3 Decoder)
- Low Power 3.3 V Operation
- Fully Compatible with Native USB Mass Storage Class Drivers
- Cypress Mass Storage Class Drivers available for Windows® (98SE, ME, 2000, XP) and Mac OS X operating systems

Features (CY7C68320C/CY7C68321C only)

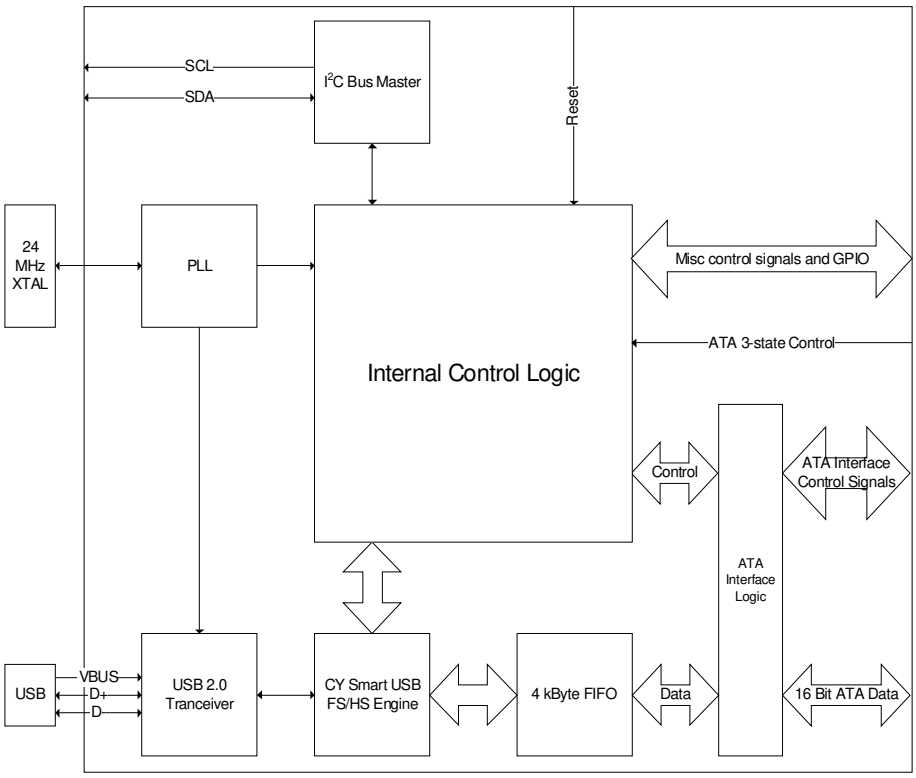
- Supports HID Interface or Custom GPIOs to enable features such as Single Button Backup, Power Off, and LED-based Notification
- 56-pin QFN and 100-pin TQFP Pb-free Packages
- CY7C68321C is Ideal for Battery Powered Designs
- CY7C68320C is Ideal for Self and Bus Powered Designs
- Automotive AEC Grade Option (–40 °C to 85 °C)

Features (CY7C68300C/CY7C68301C only)

- Pin Compatible with CY7C68300A (using Backward Compatibility Mode)
- 56-pin SSOP and 56-pin QFN Pb-free Packages
- CY7C68301C is Ideal for Battery Powered Designs
- CY7C68300C is Ideal for Self and Bus Powered Designs

Errata: For information on silicon errata, see “Errata” on page 43. Details include trigger conditions, devices affected, and proposed workaround.

Logic Block Diagram



Applications

The CY7C68300C/301C and CY7C68320C/321C implement a USB 2.0 bridge for all ATA/ATAPI-6 compliant mass storage devices, such as the following:

- Hard Drives
- CD-ROM, CD-R/W
- DVD-ROM, DVD-RAM, DVD±R/W
- MP3 Players
- Personal Media Players
- CompactFlash
- Microdrives
- Tape Drives
- Personal Video Recorders
- Automotive Applications

The CY7C68300C/301C and CY7C68320C/321A support one or two devices in the following configurations:

- ATA/ATAPI master only
- ATA/ATAPI slave only
- ATA/ATAPI master and ATA/ATAPI slave
- CompactFlash only
- ATA/ATAPI slave and CompactFlash or other removable IDE master

Additional Resources

- CY4615B EZ-USB AT2LP Reference Design Kit
- *USB Specification* Version 2.0
- *ATA Specification* T13/1410D Revision 3B
- USB *Mass Storage Class Bulk-Only Transport Specification* http://www.usb.org/developers/devclass_docs/usbmassbulk_10.pdf

Contents

Introduction

The EZ-USB AT2LP™ (CY7C68300C/CY7C68301C and CY7C68320C/CY7C68321C) implements a fixed-function bridge between one USB port and one or two ATA- or ATAPI-based mass storage device ports. This bridge adheres to the Mass Storage Class Bulk-Only Transport Specification (BOT) and is intended for bus and self powered devices.

The AT2LP is the latest addition to the Cypress USB mass storage portfolio, and is an ideal cost- and power-reduction path for designs that previously used Cypress's ISD-300A1, ISD-300LP, or EZ-USB AT2.

Specifically, the CY7C68300C/CY7C68301C includes a mode that makes it pin-for-pin compatible with the EZ-USB AT2 (CY7C68300A).

The USB port of CY7C68300C/301C and CY7C68320C/321C (AT2LP) is connected to a host computer directly or with the downstream port of a USB hub. Software on the USB host system issues commands and sends data to the AT2LP and receives status and data from the AT2LP using standard USB protocol.

The ATA/ATAPI port of the AT2LP is connected to one or two mass storage devices. A 4 kbyte buffer maximizes ATA/ATAPI data transfer rates by minimizing losses due to device seek times. The ATA interface supports ATA PIO modes 0, 3 [1], and 4, multiword DMA mode 2, and Ultra DMA modes 2, 3, and 4.

The device initialization process is configurable, enabling the AT2LP to initialize ATA/ATAPI devices without software intervention.

CY7C68300A Compatibility

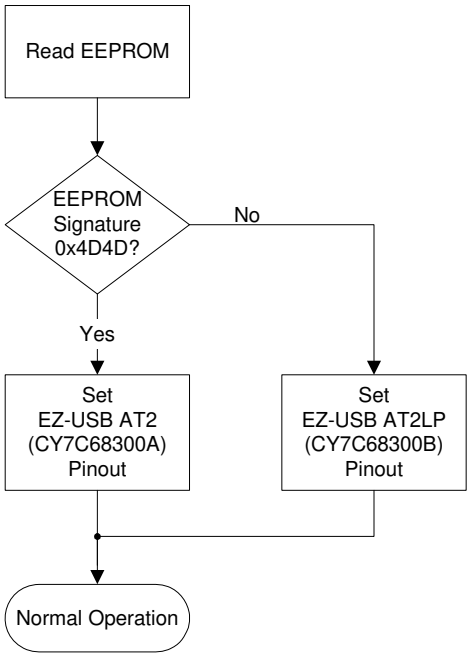
As mentioned in the previous section, the CY7C68300C/301C contains a backward compatibility mode that enables it to be used in existing EZ-USB AT2 (CY7C68300A) designs. The backward compatibility mode is enabled by programming the EEPROM with the CY7C68300A signature.

During startup, the AT2LP checks the I^2C bus for an EEPROM with a valid signature in the first two bytes. If the signature is 0x4D4D, the AT2LP configures itself for pin-to-pin compatibility with the AT2 and begins normal mass storage operation. If the signature is 0x534B, the AT2LP configures itself with the AT2LP pinout and begins normal mass storage operation.

Refer to the logic flow in Figure 1 for more information on the pinout selection process.

Most designs that use the AT2 can migrate to the AT2LP with no changes to either the board layout or EEPROM data. Cypress has published an application note focused on migrating from the AT2 to the AT2LP to help expedite the process. It can be downloaded from the Cypress website (http://www.cypress.com) or obtained through a Cypress representative.

Figure 1. Simplified Pinout Selection Flowchart

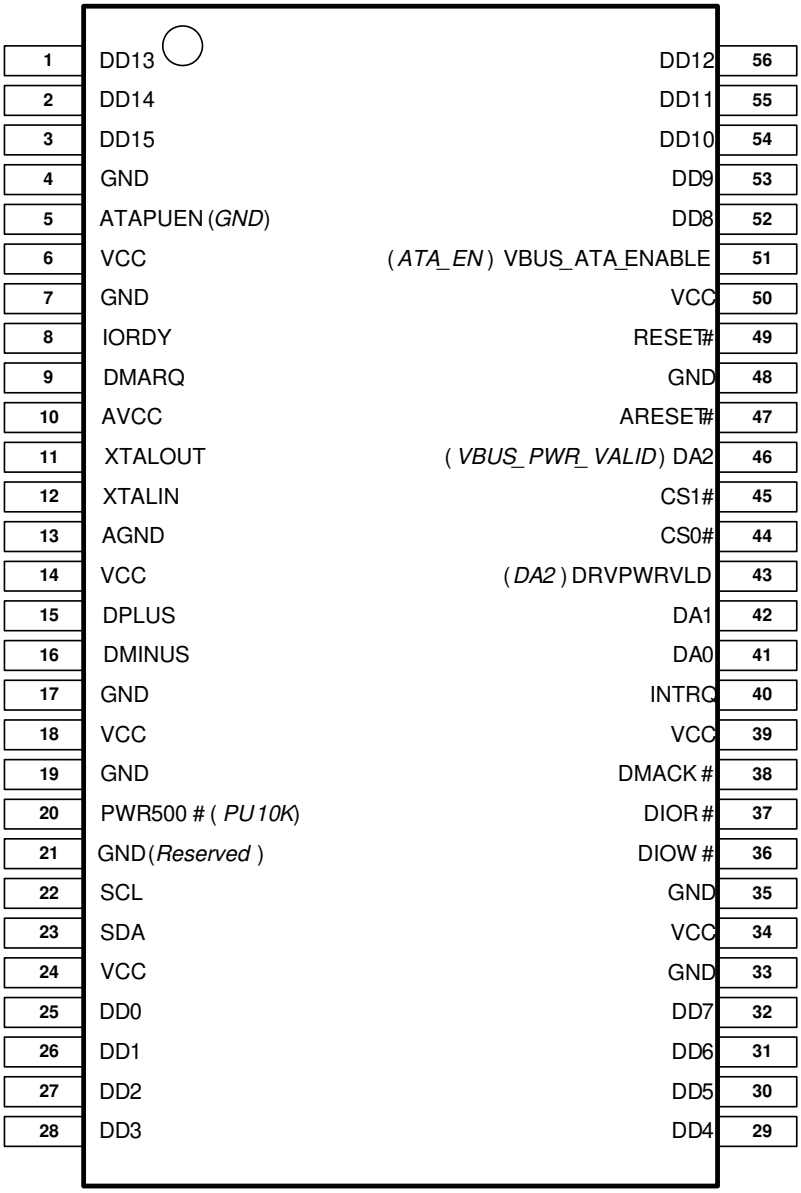


Note
1. Errata: The ATA/ATAPI-6 standard specifies the data recovery timings for each of the Read (DIOR)/Write (DIOW) data transfer modes such as PIO mode-0, 1, 2, 3, 4. As per the standard for PIO mode-3 this timing value is 70 ns. In AT2LP the actual value measured is out of spec limits. Please refer to "Errata" on page 43 for details and workaround.

Pin Diagrams

The AT2LP is available in different package types to meet a variety of design needs. The CY7C68320C/321C is available in 56-pin QFN and 100-pin TQFP packages to provide the greatest flexibility for new designs. The CY7C68300C is available in 56-pin SSOP and QFN package types and CY7C68301C is available in QFN package to ensure backward compatibility with CY7C68300A designs.

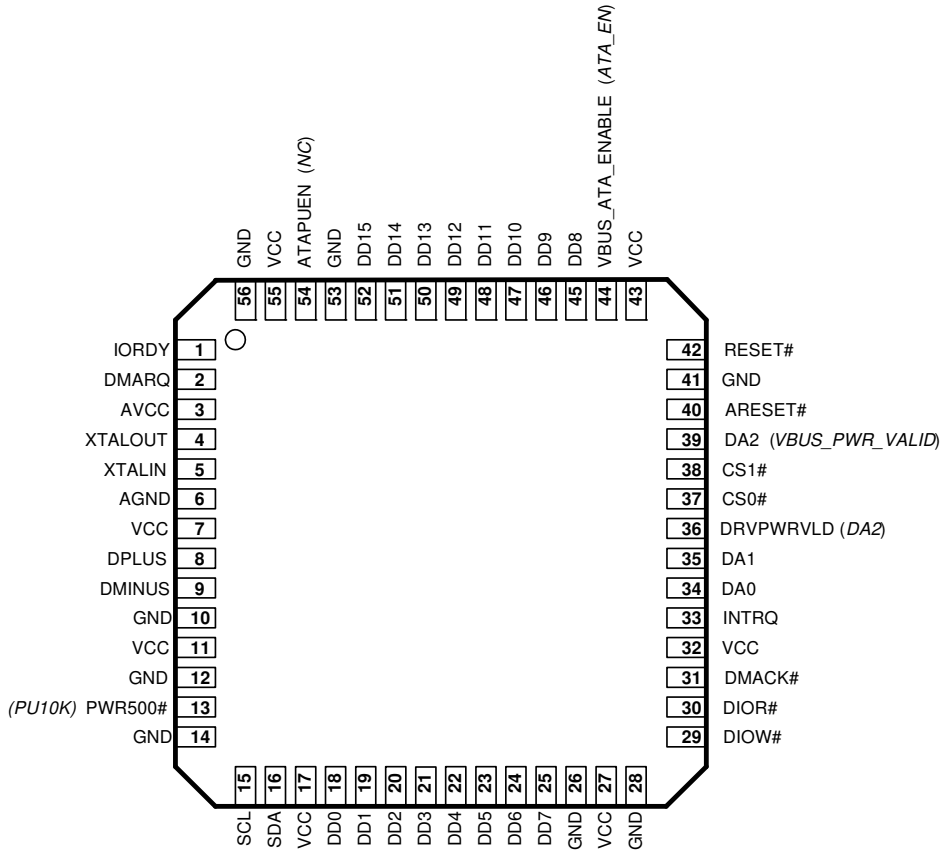
Figure 2. 56-pin SSOP Pinout (CY7C68300C only)



Note Labels in italics denote pin functionality during CY7C68300A compatibility mode.

Pin Diagrams *(continued)*

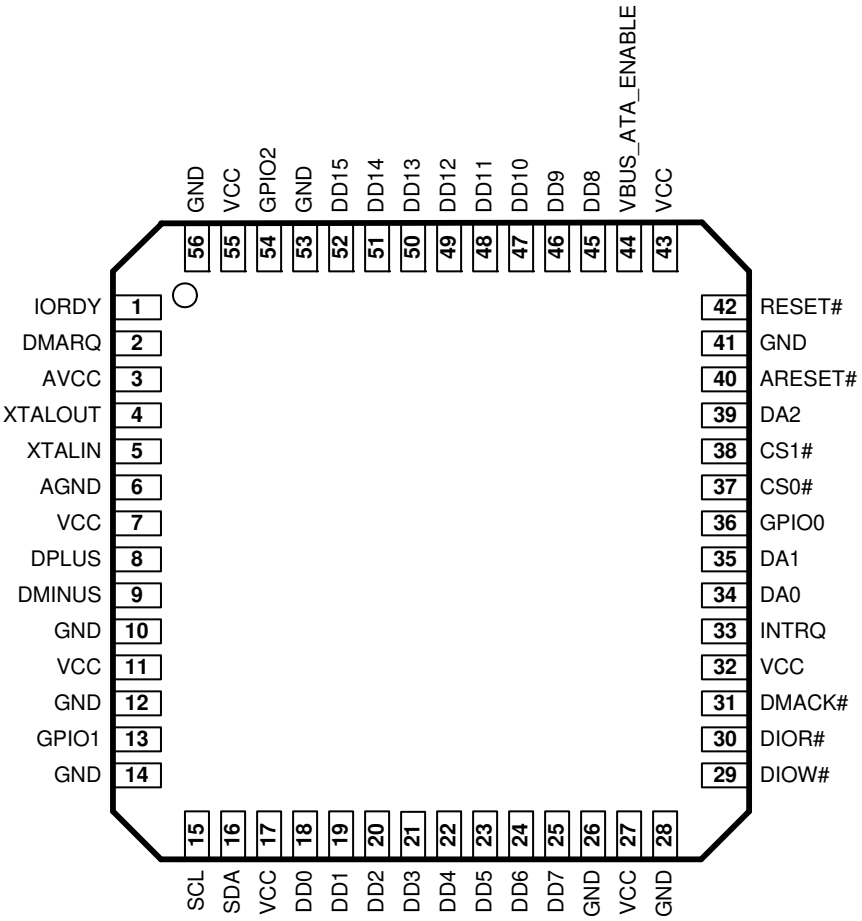
Figure 3. 56-pin QFN Pinout (CY7C68300C/CY7C68301C)



Note Italic labels denote pin functionality during CY7C68300A compatibility mode.

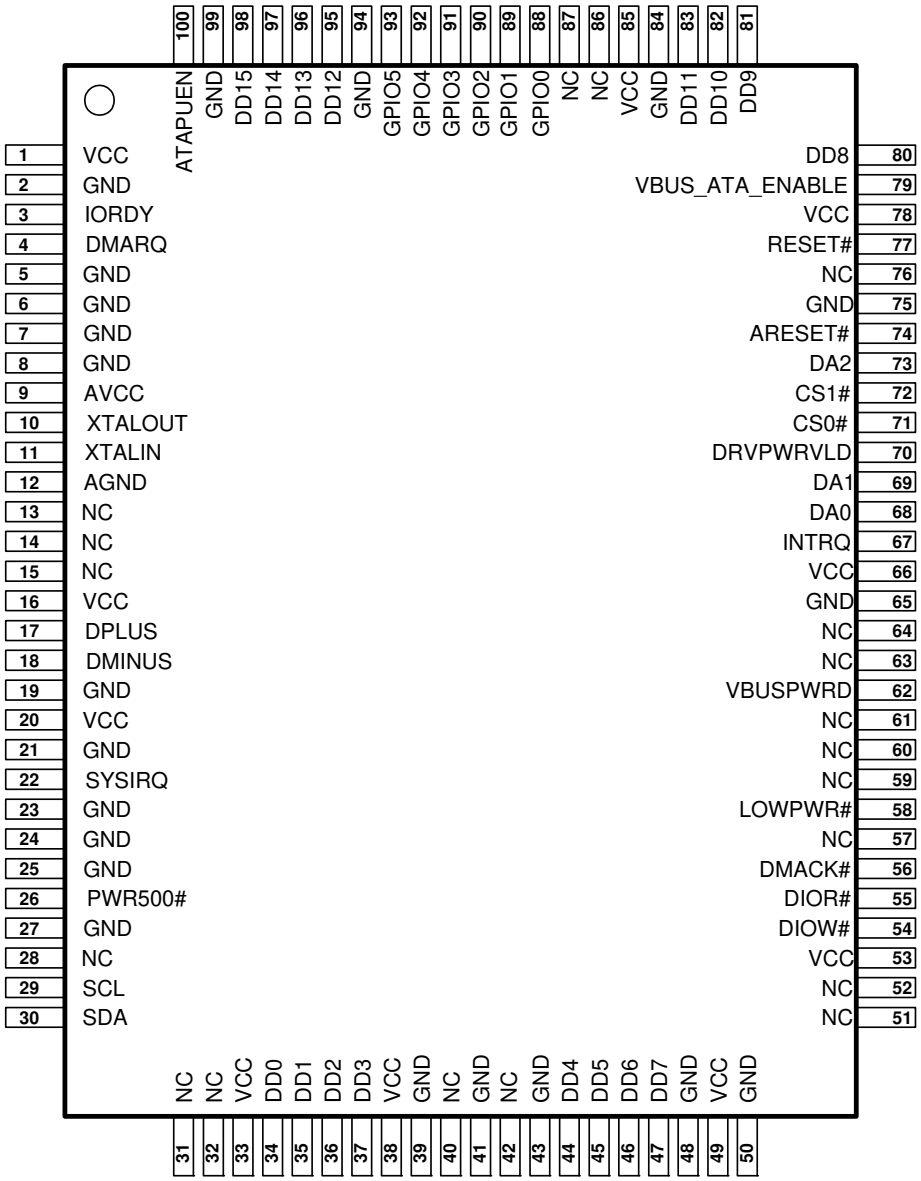
Pin Diagrams *(continued)*

Figure 4. 56-pin QFN Pinout (CY7C68320C/CY7C68321C)



Pin Diagrams *(continued)*

Figure 5. 100-pin TQFP Pinout (CY7C68320C only)



Pin Descriptions

The following table lists the pinouts for the 56-pin SSOP, 56-pin QFN, and 100-pin TQFP package options for the AT2LP. Refer to the Pin Diagrams on page 5 for differences between the 68300C/01C and 68320C/321C pinouts for the 56-pin packages.

Table 1. AT2LP Pin Descriptions

Note Italic pin names denote pin functionality during CY7C68300A compatibility mode

100 TQFP	56 QFN	56 SSOP	Pin Name	Pin Type	Default State at Startup	Pin Description
1	55	6	V_{CC}	PWR		**V_{CC}**. Connect to 3.3 V power source.
2	56	7	GND	GND		**Ground**.
3	1	8	IORDY	I[2]	Input	**ATA control**. Apply a 1 k pull up to 3.3 V.
4	2	9	DMARQ	I[2]	Input	**ATA control**.
5 6 7 8	N/A	N/A	GND			**Ground**.
9	3	10	AV_{CC}	PWR		**Analog V_{CC}**. Connect to V_{CC} through the shortest path possible.
10	4	11	XTALOUT	Xtal	Xtal	**24 MHz crystal output**. (See XTALIN, XTALOUT on page 13).
11	5	12	XTALIN	Xtal	Xtal	**24 MHz crystal input**. (See XTALIN, XTALOUT on page 13).
12	6	13	AGND	GND		**Analog ground**. Connect to ground with as short a path as possible.
13 14 15	N/A	N/A	NC			**No connect**.
16	7	14	V_{CC}	PWR		**V_{CC}**. Connect to 3.3 V power source.
17	8	15	DPLUS	I/O	High Z	**USB D+ signal** (See DPLUS, DMINUS on page 13).
18	9	16	DMINUS	I/O	High Z	**USB D– signal** (See DPLUS, DMINUS on page 13).
19	10	17	GND	GND		**Ground**.
20	11	18	V_{CC}	PWR		**V_{CC}**. Connect to 3.3 V power source.
21	12	19	GND	GND		**Ground**.
22	N/A	N/A	SYSIRQ	I	Input	**USB interrupt request**. (See SYSIRQ on page 13). Active HIGH. Connect to GND if functionality is not used.
23 24 25	N/A	N/A	GND	GND		**Ground**.
26[3]	13[3]	20	PWR500#[4] (*PU 10K*)	O		**bMaxPower request granted indicator**. (See PWR500# on page 15). Active LOW. N/A for CY7C68320C/CY7C68321C 56-pin packages.
27	14	21	GND (*RESERVED*)			**Reserved**. Tie to GND.
28	N/A	N/A	NC			**No connect**.
29	15	22	SCL	O	Active for several ms at startup.	**Clock signal for I^2C interface**. (See SCL, SDA on page 13). Apply a 2.2k pull up resistor.

Notes
2. If byte 8, bit 4 of the EEPROM is set to '0', the ATA interface pins are only active when VBUS_ATA_EN is asserted. See VBUS_ATA_ENABLE on page 15.
3. The General Purpose inputs can be enabled on ATAPUEN, PWR500#, and DRVPWRVLD via EEPROM byte 8, bit 7 on CY7C68320C/CY7C68321C.
4. A '#' sign after the pin name indicates that it is active LOW.

Table 1. AT2LP Pin Descriptions *(continued)*
Note Italic pin names denote pin functionality during CY7C68300A compatibility mode

100 TQFP	56 QFN	56 SSOP	Pin Name	Pin Type	Default State at Startup	Pin Description
30	16	23	SDA	I/O		**Data signal for I^2C interface**. (See SCL, SDA on page 13). Apply a 2.2k pull up resistor.
31 32	N/A	N/A	NC			**No connect**.
33	17	24	V_{CC}	PWR		**V_{CC}**. Connect to 3.3 V power source.
34	18	25	DD0	I/O[5]	High Z	**ATA data bit 0**.
35	19	26	DD1	I/O[5]	High Z	**ATA data bit 1**.
36	20	27	DD2	I/O[5]	High Z	**ATA data bit 2**.
37	21	28	DD3	I/O[5]	High Z	**ATA data bit 3**.
38	N/A	N/A	V_{CC}	PWR		**V_{CC}**. Connect to 3.3 V power source.
39	N/A	N/A	GND	GND		**Ground**.
40	N/A	N/A	NC	NC		**No connect**.
41	N/A	N/A	GND			**Ground**.
42	N/A	N/A	NC	NC		**No connect**.
43	N/A	N/A	GND			**Ground**.
44	22	29	DD4	I/O[5]	High Z	**ATA data bit 4**.
45	23	30	DD5	I/O[5]	High Z	**ATA data bit 5**.
46	24	31	DD6	I/O[5]	High Z	**ATA data bit 6**.
47	25	32	DD7	I/O[5]	High Z	**ATA data bit 7**. Apply a 1k pull down to GND.
48	26	33	GND	GND		**Ground**.
49	27	34	V_{CC}	PWR		**V_{CC}**. Connect to 3.3 V power source.
50	28	35	GND	GND		**Ground**.
51 52	N/A	N/A	NC	NC		**No connect**.
53	N/A	N/A	V_{CC}	PWR		**V_{CC}**. Connect to 3.3 V power source.
54	29	36	DIOW#[6]	O/Z[5]	Driven HIGH (CMOS)	**ATA control**.
55	30	37	DIOR#	O/Z[5]	Driven HIGH (CMOS)	**ATA control**.
56	31	38	DMACK#	O/Z[5]	Driven HIGH (CMOS)	**ATA control**.
57	N/A	N/A	NC	NC		**No connect**.
58	N/A	N/A	LOWPWR#	O		**USB suspend indicator**. (See LOWPWR# on page 14).
59 60 61	N/A	N/A	NC	NC		**No connect**.
62	N/A	N/A	VBUSPWRD	I	Input	**Bus powered mode selector**. (See VBUSPWRD on page 15).
63 64	N/A	N/A	NC	NC		**No connect**.
65	N/A	N/A	GND	GND		**Ground**.
66	32	39	V_{CC}	PWR		**V_{CC}**. Connect to 3.3 V power source.

Notes
5. If byte 8, bit 4 of the EEPROM is set to '0', the ATA interface pins are only active when VBUS_ATA_EN is asserted. See VBUS_ATA_ENABLE on page 15.
6. A '#' sign after the pin name indicates that it is active LOW.

Table 1. AT2LP Pin Descriptions *(continued)*
Note Italic pin names denote pin functionality during CY7C68300A compatibility mode

100 TQFP	56 QFN	56 SSOP	Pin Name	Pin Type	Default State at Startup	Pin Description
67	33	40	INTRQ	I[7]	Input	**ATA interrupt request**.
68	34	41	DA0	O/Z[7]	Driven HIGH after 2 ms delay	**ATA address**.
69	35	42	DA1	O/Z[7]	Driven HIGH after 2 ms delay	**ATA address**.
70[8]	36[8]	43	DRVPWRVLD (*DA2*)	I	Input	**Device presence detect.** (See DRVPWRVLD on page 14). Configurable logical polarity is controlled by EEPROM address 0x08. This pin must be pulled HIGH if functionality is not used. **Alternate function.** Input when the EEPROM configuration byte 8 has bit 7 set to '1'. The input value is reported through EP1IN (byte 0, bit 0).
71	37	44	CS0#	O/Z[7]	Driven HIGH after 2 ms delay	**ATA chip select**.
72	38	45	CS1#	O/Z[7]	Driven HIGH after 2 ms delay	**ATA chip select**.
73	39	46	DA2 (*VBUS_PWR_VALID*)	O/Z[7]	Driven HIGH after 2 ms delay	**ATA address**.
74	40	47	ARESET#	O/Z[7]		**ATA reset**.
75	41	48	GND	GND		**Ground**.
76	N/A	N/A	NC	NC		**No connect**.
77	42	49	RESET#	I	Input	**Chip reset** (See RESET# on page 15).
78	43	50	V_{CC}	PWR		**V_{CC}**. Connect to 3.3 V power source.
79	44	51	VBUS_ATA_ENABLE (*ATA_EN*)	I	Input	**VBUS detection** (See VBUS_ATA_ENABLE on page 15).
80	45	52	DD8	I/O[7]	High Z	**ATA data bit 8**.
81	46	53	DD9	I/O[7]	High Z	**ATA data bit 9**.
82	47	54	DD10	I/O[7]	High Z	**ATA data bit 10**.
83	48	55	DD11	I/O[7]	High Z	**ATA data bit 11**.
84	N/A	N/A	GND			**Ground**.
85	N/A	N/A	V_{CC}	PWR		**V_{CC}**. Connect to 3.3 V power source.
86 87	N/A	N/A	NC	NC		**No connect**.
88 89 90 91 92 93	36[8] 13[8] 54[8]	N/A	GPIO0 GPIO1 GPIO2 GPIO3 GPIO4 GPIO5	I/O[8]		**General Purpose I/O pins** (See GPIO Pins on page 14). The GPIO pins must be tied to GND if functionality is not used.
94	N/A	N/A	GND	GND		**Ground**.

Notes
7. If byte 8, bit 4 of the EEPROM is set to '0', the ATA interface pins are only active when VBUS_ATA_EN is asserted. See VBUS_ATA_ENABLE on page 15.
8. The General Purpose inputs can be enabled on ATAPUEN, PWR500#, and DRVPWRVLD via EEPROM byte 8, bit 7 on CY7C68320C/CY7C68321C.

Table 1. AT2LP Pin Descriptions *(continued)*
Note Italic pin names denote pin functionality during CY7C68300A compatibility mode

100 TQFP	56 QFN	56 SSOP	Pin Name	Pin Type	Default State at Startup	Pin Description
95	49	56	DD12	I/O[9]	High Z	**ATA data bit 12**.
96	50	1	DD13	I/O[9]	High Z	**ATA data bit 13**.
97	51	2	DD14	I/O[9]	High Z	**ATA data bit 14**.
98	52	3	DD15	I/O[9]	High Z	**ATA data bit 15**.
99	53	4	GND	GND		**Ground**.
100[10]	54[10]	5	ATAPUEN (*NC*)	I/O		**Bus powered ATA pull up voltage source** (see ATAPUEN on page 15). **Alternate function**: General purpose input when the EEPROM configuration byte 8 has bit 7 set to '1'. The input value is reported through EP1IN (byte 0, bit 2).

Notes
9. If byte 8, bit 4 of the EEPROM is set to '0', the ATA interface pins are only active when VBUS_ATA_EN is asserted. See VBUS_ATA_ENABLE on page 15.
10. The General Purpose inputs can be enabled on ATAPUEN, PWR500#, and DRVPWRVLD via EEPROM byte 8, bit 7 on CY7C68320C/CY7C68321C.

Additional Pin Descriptions

The following sections provide additional pin information.

DPLUS, DMINUS

DPLUS and DMINUS are the USB signaling pins; they must be tied to the D+ and D– pins of the USB connector. Because they operate at high frequencies, the USB signals require special consideration when designing the layout of the PCB. See General PCB Layout Recommendations for USB Mass Storage Designs on page 40 for PCB layout recommendations.

When RESET# is released, the assertion of the internal pull up on D+ is gated by a combination of the state of the VBUS_ATA_ENABLE pin, the value of configuration address 0x08 bit 0 (DRVPWRVLD Enable), and the detection of a non-removable ATA/ATAPI drive on the IDE bus. See Table 2 for a description of this relationship.

Table 2. D+ Pull Up Assertion Dependencies

VBUS_ATA_EN	1	1	1	1	0	0
DRVPWRVLD Enable Bit	1	1	0	0	1	1
ATA/ATAPI Drive Detected	Yes	No	Yes	No	Yes	No
State of D+ pull up	1	1	1	0	0	0

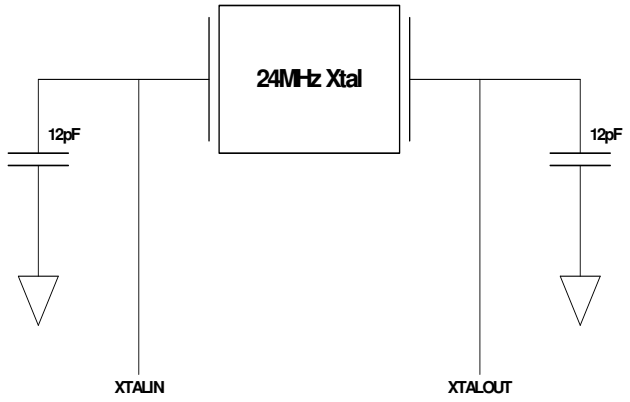
SCL, SDA

The clock and data pins for the I^2C port must be connected to the configuration EEPROM and to 2.2K pull up resistors tied to V_{CC}. If no EEPROM is used in the design, the SCL and SDA pins must still be connected to pull up resistors. The SCL and SDA pins are active for several milliseconds at startup.

XTALIN, XTALOUT

The AT2LP requires a 24 MHz (±100 ppm) signal to derive internal timing. Typically, a 24 MHz (12 pF, 500 µW, parallel-resonant, fundamental mode) crystal is used, but a 24 MHz square wave (3.3 V, 50/50 duty cycle) from another source can also be used. If a crystal is used, connect its pins to XTALIN and XTALOUT, and also through 12 pF capacitors to GND as shown in Figure 6. If an alternate clock source is used, apply it to XTALIN and leave XTALOUT unconnected.

Figure 6. XTALIN/XTALOUT Diagram



SYSIRQ

The SYSIRQ pin provides a way for systems to request service from host software by using the USB interrupt pipe on endpoint 1 (EP1). If the AT2LP has no pending interrupt data to return, USB interrupt pipe data requests are NAK'ed. If pending data is available, the AT2LP returns 16 bits of data. This data indicates whether AT2LP is operating in high speed or full speed, whether the AT2LP is reporting self powered or bus powered operation, and the states of any GPIO pins that are configured as inputs. GPIO pins can be individually set as inputs or outputs, with byte 0x09 of the configuration data. The state of any GPIO pin that is not set as an input is reported as '0' in the EP1 data.

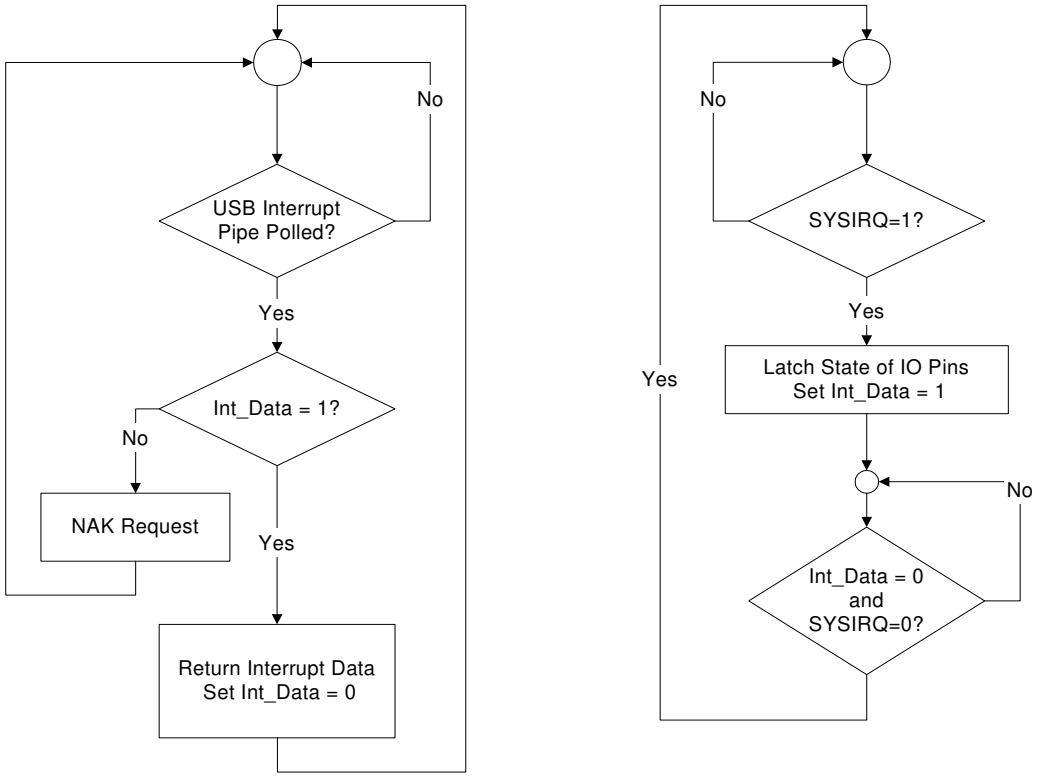
Table 3 gives the bitmap for the data returned on the interrupt pipe and Figure 7 on page 14 depicts the latching algorithm incorporated by the AT2LP.

The SYSIRQ pin must be pulled LOW if HID functionality is used. Refer to HID Functions for Button Controls on page 15 for more details on HID functionality.

Table 3. Interrupt Data Bitmap

EP1 Data Byte 1								EP1 Data Byte 0							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	USB High Speed	VBUS Powered	RESERVED	RESERVED	GPIO[5]	GPIO[4]	GPIO[3]	GPIO[2]	GPIO[1]	GPIO[0]

Figure 7. SYSIRQ Latching Algorithm



DRVPWRVLD

When this pin is enabled with bit 0 of configuration address 0x08 (DRVPWRVLD Enable), the AT2LP informs the host that a removable device, such as a CF card, is present. The AT2LP uses DRVPWRVLD to detect that the removable device is present. Pin polarity is controlled by bit 1 of configuration address 0x08. When DRVPWRVLD is deasserted, the AT2LP reports a “no media present” status (ASC = 0x3A, ASQ = 0x00) when queried by the host. When the media is detected again, the AT2LP reports a “media changed” status to the host (ASC = 0x28, ASQ = 0x00) when queried.

When a removable device is used, it is always considered by the AT2LP to be the IDE master device. Only one removable device may be attached to the AT2LP. If the system only contains a removable device, bit 6 of configuration address 0x08 (Search ATA Bus) must be set to ‘0’ to disable ATA device detection at startup. If a non-removable device is connected in addition to a removable media device, the non removable device must be configured as IDE slave (device address 1).

GPIO Pins

The GPIO pins enable a general purpose input and output interface. There are several different interfaces to the GPIO pins:

- Configuration bytes 0x09 and 0x0A contain the default settings for the GPIO pins upon initial AT2LP configuration.
- The host can modify the settings of the GPIO pins during operation. This is done with vendor-specific commands described in Programming the EEPROM on page 35.
- The status of the GPIO pins is returned on the interrupt endpoint (EP1) in response to a SYSIRQ. See SYSIRQ on page 13 for SYSIRQ details.

LOWPWR#

LOWPWR# is an output pin that is driven to ‘0’ when the AT2LP is not in suspend. LOWPWR# is placed in High Z when the AT2LP is in a suspend state. This pin only indicates the state of the AT2LP and must not be used to determine the status of the USB host because of variations in the behavior of different hosts.

ATA Interface Pins

The ATA Interface pins must be connected to the corresponding pins on an IDE connector or mass storage device. To enable sharing of the IDE bus with other master devices, the AT2LP can place all ATA Interface Pins in a High Z state whenever VBUS_ATA_ENABLE is not asserted. Enabling this feature is done by setting bit 4 of configuration address 0x08 to '1'. Otherwise, the ATA bus is driven by the AT2LP to a default inactive state whenever VBUS_ATA_ENABLE is not asserted.

Design practices for signal integrity as outlined in the ATA/ATAPI-6 specification must be followed with systems that use a ribbon cable interconnect between the AT2LP's ATA interface and the attached mass storage device, especially if Ultra DMA Mode is used.

VBUS_ATA_ENABLE

VBUS_ATA_ENABLE is typically used to indicate to the AT2LP that power is present on VBUS. This pin is polled by the AT2LP at startup and then every 20 ms thereafter. If this pin is '0', the AT2LP releases the pull up on D+ as required by the USB specification.

Also, if bit 4 of configuration address 0x08 is '1', the ATA interface pins are placed in a High Z state when VBUS_ATA_ENABLE is '0'. If bit 4 of configuration address 0x08 is '0', the ATA interface pins are still driven when VBUS_ATA_ENABLE is '0'.

ATAPUEN

This output can be used to control the required host pull up resistors on the ATA interface in a bus powered design to minimize unnecessary power consumption when the AT2LP is in suspend. ATAPUEN is driven to '0' when the ATA bus is inactive. ATAPUEN is driven to '1' when the ATA bus is active. ATAPUEN is set to a High Z state along with all other ATA interface pins if VBUS_ATA_ENABLE is deasserted and the ATA_EN functionality (bit 4 of configuration address 0x08) is enabled (0).

ATAPUEN can also be configured as a GPIO input. See HID Functions for Button Controls on page 15 for more information on HID functionality.

PWR500#

The AT2LP asserts PWR500# to indicate that VBUS current may be drawn up to the limit specified by the bMaxPower field of the USB configuration descriptors. If the AT2LP enters a low-power state, PWR500# is deasserted. When normal operation is resumed, PWR500# is restored. The PWR500# pin must never be used to control power sources for the AT2LP. In the 56-pin package, PWR500# only functions during bus powered operation.

PWR500# can also be configured as a GPIO input. See HID Functions for Button Controls on page 15 for more information on HID functionality.

VBUSPWRD

VBUSPWRD is used to indicate self or bus powered operation. Some designs require the ability to operate in either self- or bus powered modes. The VBUSPWRD input pin enables these devices to switch between self powered and bus powered modes by changing the contents of the bMaxPower field and the self powered bit in the reported configuration descriptors (see Table 4).

Note that current USB host drivers do not poll the device for this information, so the effect of this pin is only seen on a USB or power on reset.

Table 4. Behavior of Descriptor Data that is Dependent Upon VBUSPWRD State

Pin	VBUSPWRD = '1'	VBUSPWRD = '0'	VBUSPWRD N/A (56-pin)
bMaxPower Reported Value	0xFA (500 mA)	0x01 (2 mA)	The value from configuration address 0x34 is used.
bmAttributes Bit 6 Reported Value	'0' (bus powered)	'1' (self powered)	'0' if bMaxPower > 0x01 '1' if bMaxPower ≤ 0x01

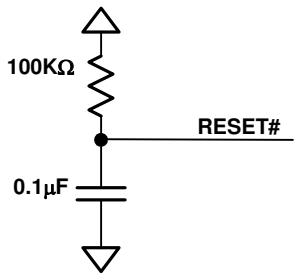
RESET#

Asserting RESET# for 10 ms resets the entire AT2LP. In self powered designs, this pin is normally tied to V_{CC} through a 100k resistor, and to GND through a 0.1 µF capacitor, as shown in Figure 8.

Cypress does not recommend an RC reset circuit for bus powered devices because of the potential for VBUS voltage drop, which may result in a startup time that exceeds the USB limit. Refer to the application note titled *EZ-USB FX2™/AT2™/SX2™ Reset and Power Considerations,* at www.cypress.com, for more information.

While the AT2LP is in reset, all pins are held at their default startup state.

Figure 8. R/C Reset Circuit for Self Powered Designs



HID Functions for Button Controls

Cypress's CY7C68320C/CY7C68321C has the capability of supporting Human Interface Device (HID) signaling to the host.

If there is an HID descriptor in the configuration data, the GPIO pins that are set as inputs are polled by the AT2LP logic approximately every 17 ms (depending on other internal interrupt routines). If a change is detected in the state of any HID-enabled GPIO, an HID report is sent through EP1 to the host. The report format for byte 0 and byte 1 is shown in Table 5.

The ability to add buttons to a mass storage solution opens new applications for data backup and other device-side notification to the host. The AT2LP Blaster software, found in the CY4615B

files, provides an easy way to enable and modify the HID features of the AT2LP.

GPIO pins can be individually set as inputs or outputs, with byte 0x09 of the configuration data, enabling a mix of HID and general purpose outputs. GPIOs that are not configured as inputs are reported with a value of '0' in the HID data. The RESERVED bits' values must be ignored, and Cypress recommends using a bitmask in software to filter out unused HID data.

Note that if using the 56-pin package, the reported GPIO[5:3] values must be ignored because the pins are not actually present.

Table 5. HID Data Bitmap

USB Interrupt Data Byte 1								USB Interrupt Data Byte 0							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	USB High Speed	VBUS Powered	RESERVED	RESERVED	GPIO[5]	GPIO[4]	GPIO[3]	GPIO[2]	GPIO[1]	GPIO[0]

Functional Overview

Chip functionally is described in the subsequent sections.

USB Signaling Speed

AT2LP operates at the following two rates defined in the *USB 2.0 Specification* dated April 27, 2000:

- Full-speed, with a signaling bit rate of 12 Mbits/sec.
- High-speed, with a signaling bit rate of 480 Mbits/sec.

AT2LP does not operate at the low-speed signaling rate of 1.5 Mbits/sec.

ATA Interface

The ATA/ATAPI port on the AT2LP is compatible with the *Information Technology–AT Attachment with Packet Interface–6 (ATA/ATAPI-6) Specification, T13/1410D Revision 2A*. The AT2LP supports both ATAPI packet commands and ATA commands (by use of ATA Command Blocks), as outlined in ATA Command Block (ATACB) on page 16. Refer to the *USB Mass Storage Class (MSC) Bulk-Only Transport (BOT)* Specification for information on Command Block formatting. Additionally, the AT2LP translates *ATAPI SFF-8070i* commands to ATA commands for seamless integration of ATA devices with generic Mass Storage Class BOT drivers.

ATA Command Block (ATACB)

The ATA Command Block (ATACB) functionality provides a means of passing ATA commands and ATA register accesses to the attached device for execution. ATACB commands are transferred in the Command Block Wrapper Command Block (CBWCB) portion of the Command Block Wrapper (CBW). The ATACB is distinguished from other command blocks by having the first two bytes of the command block match the bVSCBSignature and bVSCBSubCommand values that are defined in Table 6. Only command blocks that have a valid bVSCBSignature and bVSCBSubCommand are interpreted as ATA Command Blocks. All other fields of the CBW and restrictions on the CBWCB remain as defined in the USB Mass Storage Class Bulk-Only Transport Specification. The ATACB must be 16 bytes in length. The following table and text defines the fields of the ATACB.

Table 6. ATACB Field Descriptions

Byte	Field Name	Field Description
0	bVSCBSignature	This field indicates to the CY7C68300C/CY7C68301C that the ATACB contains a vendor-specific command block. The value of this field must match the value in EEPROM address 0x04 for the command to be recognized as a vendor-specific ATACB command.
1	bVSCBSubCommand	This field must be set to 0x24 for ATACB commands.

Table 6. ATACB Field Descriptions *(continued)*

Byte	Field Name	Field Description
2	bmATACBActionSelect	This field controls the execution of the ATACB according to the bitfield values: Bit 7 *IdentifyPacketDevice* – This bit indicates that the data phase of the command contains ATAPI (0xA1) or ATA (0xEC) IDENTIFY device data. Setting IdentifyPacketDevice when the data phase does not contain IDENTIFY device data results in unspecified device behavior. 0 = Data phase does not contain IDENTIFY device data 1 = Data phase contains ATAPI or ATA IDENTIFY device data Bit 6 *UDMACommand* – This bit enables supported UDMA device transfers. Setting this bit when a non-UDMA capable device is attached results in undetermined behavior. 0 = Do not use UDMA device transfers (only use PIO mode) 1 = Use UDMA device transfers Bit 5 *DEVOverride* – This bit determines whether the DEV bit value is taken from the value assigned to the LUN during startup or from the ATACB. 0 = The DEV bit is taken from the value assigned to the LUN during startup 1 = The DEV bit is taken from the ATACB field 0x0B, bit 4 Bit 4 *DErrorOverride* – This bit controls the device error override feature. This bit must not be set during a bmATACBActionSelect TaskFileRead. 0 = Data accesses are halted if a device error is detected 1 = Data accesses are not halted if a device error is detected Bit 3 *PErrorOverride* – This bit controls the phase error override feature. This bit must not be set during a bmATACBActionSelect TaskFileRead. 0 = Data accesses are halted if a phase error is detected 1 = Data accesses are not halted if a phase error is detected Bit 2 *PollAltStatOverride* – This bit determines whether or not the Alternate Status register is polled and the BSY bit is used to qualify the ATACB operation. 0 = The AltStat register is polled until BSY=0 before proceeding with the ATACB operation 1 = The ATACB operation is executed without polling the AltStat register. Bit 1 *DeviceSelectionOverride* – This bit determines when the device selection is performed in relation to the command register write accesses. 0 = Device selection is performed before command register write accesses 1 = Device selection is performed following command register write accesses Bit 0 *TaskFileRead* – This bit determines whether or not the TaskFile register data selected in bmATACBRegisterSelect is returned. If this bit is set, the dCBWDataTransferLength field must be set to 8. 0 = Execute ATACB command and data transfer (if any) 1 = Only read TaskFile registers selected in bmATACBRegisterSelect and return 0x00h for all others. The format of the 8 bytes of returned data is as follows: ❒ Address offset 0x00 (0x3F6) – Alternate Status ❒ Address offset 0x01 (0x1F1) – Features/Error ❒ Address offset 0x02 (0x1F2) – Sector Count ❒ Address offset 0x03 (0x1F3) – Sector Number ❒ Address offset 0x04 (0x1F4) – Cylinder Low ❒ Address offset 0x05 (0x1F5) – Cylinder High ❒ Address offset 0x06 (0x1F6) – Device/Head ❒ Address offset 0x07 (0x1F7) – Command/Status

Table 6. ATACB Field Descriptions *(continued)*

Byte	Field Name	Field Description
3	bmATACBRegisterSelect	This field controls which of the TaskFile register read or write accesses occur. TaskFile read data is always 8 bytes in length, and unselected register data are returned as 0x00. Register accesses occur in sequential order as outlined here (0 to 7): Bit 0 *(0x3F6)* Device Control/Alternate Status Bit 1 *(0x1F1)* Features/Error Bit 2 *(0x1F2)* Sector Count Bit 3 *(0x1F3)* Sector Number Bit 4 *(0x1F4)* Cylinder Low Bit 5 *(0x1F5)* Cylinder High Bit 6 *(0x1F6)* Device/Head Bit 7 *(0x1F7)* Command/Status
4	bATACBTransferBlockCount	This value indicates the maximum requested block size be in 512-byte increments. This value must be set to the last value used for the 'Sectors per block' in the SET_MULTIPLE_MODE command. Legal values are 0, 1, 2, 4, 8, 16, 32, 64, and 128 where '0' indicates 256 sectors per block. A command failed status is returned if an illegal value is used in the ATACB.
5–12	bATACBTaskFileWriteData	These bytes contain ATA register data used with ATA command or PIO write operations. Only registers selected in bmATACBRegisterSelect are required to hold valid data when accessed. The registers are as follows. ATACB Address Offset 0x05 *(0x3F6)* – Device Control ATACB Address Offset 0x06 *(0x1F1)* – Features ATACB Address Offset 0x07 *(0x1F2)* – Sector Count ATACB Address Offset 0x08 *(0x1F3)* – Sector Number ATACB Address Offset 0x09 *(0x1F4)* – Cylinder Low ATACB Address Offset 0x0A *(0x1F5)* – Cylinder High ATACB Address Offset 0x0B *(0x1F6)* – Device ATACB Address Offset 0x0C *(0x1F7)* – Command
13–15	Reserved	These bytes must be set to 0x00 for ATACB commands.

Operating Modes

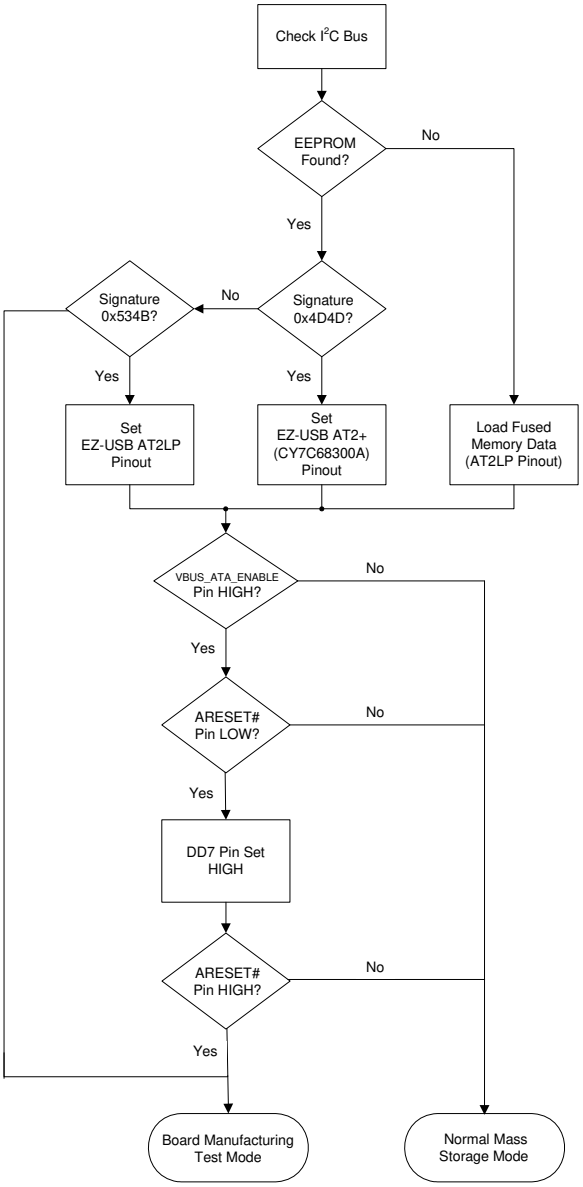
The different modes of operation and EEPROM information are presented in the following sections.

Operational Mode Selection Flow

During the power up sequence, the AT2LP queries the I^2C bus for an EEPROM. The AT2LP then selects a pinout configuration as shown here, and checks to see if ARESET# is configured for Board Manufacturing Test Mode.

- If no EEPROM is detected, the AT2LP uses the values in the factory-programmable (fused) memory space. See Fused Memory Data on page 20 for more information. This is not a valid mode of operation if no factory programming has been done.
- If an EEPROM signature of 0x4D4D is found, the CY7C68300C/CY7C68301C uses the same pinout and EEPROM format as the CY7C68300A (EZ-USB AT2+).
- If an EEPROM signature of 0x534B is found, the AT2LP uses the values stored in the EEPROM to configure the USB descriptors for normal operation.
- If an EEPROM is detected, but an invalid signature is read, the AT2LP defaults into Board Manufacturing Test Mode.

Figure 9. Operational Mode Selection Flow



Fused Memory Data

When no EEPROM is detected at startup, the AT2LP enumerates with the VID/PID/DID values that are stored in the fused memory space. These values can be programmed into the AT2LP during chip manufacturing for high volume applications to avoid the need for an external EEPROM in some designs. Contact your local Cypress Semiconductor sales office for more information on this feature.

If no factory programming has been done, the values returned from the fused memory space would all be 0x00, which is not a valid mode of operation. In this case the chip uses the manufacturing mode and return the default descriptors (VID/PID of 0x4B4/0x6830). An EEPROM must be used with designs that do not use factory-programmed chips to identify the device as your company's product.

Normal Mass Storage Mode

In Normal Mass Storage Mode, the chip behaves as a USB 2.0 to ATA/ATAPI Bridge. This includes all typical USB device states such as powered and configured. The USB descriptors are returned according to the values stored in the external EEPROM or fused memory space. A unique serial number is required for Mass Storage Class Bulk-Only Transport compliance, which is one reason why an EEPROM or factory-programmed part is needed.

Board Manufacturing Test Mode

In Board Manufacturing Test Mode the AT2LP behaves as a USB 2.0 device but the ATA/ATAPI interface is not fully active. This mode must not be used for mass storage operation in a finished design. In this mode, the AT2LP enable reading from and writing to the EEPROM, and for board level testing, through vendor- specific ATAPI commands utilizing the CBW Command Block as described in the USB *Mass Storage Class Bulk-Only Transport Specification*. There is a vendor-specific ATAPI command for EEPROM accesses (CfgCB) and one for board level testing (MfgCB), as described in the following sections.

There is a convenient method available for starting the AT2LP in Board Manufacturing Test Mode to enable reprogramming of EEPROMs without a mass storage device attached. If the ATA Reset (ARESET#) line is LOW on power up, the AT2LP enters Board Manufacturing Test Mode. It is recommended that a 10k resistor be used to pull ARESET# to LOW. An easy way to pull the ARESET# line LOW is to short pins 1 and 3 on the 40-pin ATA connector with a 10k resistor, that ties the ARESET# line to the required pull down on DD7.

CfgCB

The cfg_load and cfg_read vendor-specific commands are passed down through the bulk pipe in the CBWCB portion of the CBW. The format of this CfgCB is shown as follows. Byte 0 is a vendor-specific command designator whose value is configurable and set in the configuration data (address 0x04). Byte 1 must be set to 0x26 to identify it as a CfgCB command. Byte2 is reserved and must be set to zero. Byte 3 is used to determine the memory source to write/read. For the AT2LP, this byte must be set to 0x02, indicating the EEPROM is present. Bytes 4 and 5 are used to determine the start address, which must always be 0x0000. Bytes 6 through 15 are reserved and must be set to zero.

The data transferred to the EEPROM must be in the format specified in Table 11 on page 23 of this data sheet. Maximum data transfer size is 255 bytes.

The data transfer length is determined by the CBW Data Transfer Length specified in bytes 8 through 11 (dCBWDataTransferLength) of the CBW (refer to Table 7). The type/direction of the command is determined by the direction bit specified in byte 12, bit 7 (bmCBWFlags) of the CBW (refer to Table 7).

Table 7. Command Block Wrapper

	Bits							
Offset	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0–3	DCBWSignature							
4–7	dCBWTag							
8–11 (08h–0Bh)	dCBWDataTransferLength							
12 (0Ch)	bwCBWFLAGS							
	Dir	Obsolete	Reserved (0)					
13 (0Dh)	Reserved (0)				bCBWLUN			
14 (0Eh)	Reserved (0)			bCBWCBLength				
15–30 (0Fh1Eh)	CBWCB (CfgCB or MfgCB)							

Table 8. Example CfgCB

Offset	CfgCB Byte Description	Bits							
		7	6	5	4	3	2	1	0
0	bVSCBSignature (set in configuration bytes)	0	0	1	0	0	1	0	0
1	bVSCBSubCommand (must be 0x26)	0	0	1	0	0	1	1	0
2	Reserved (must be set to zero)	0	0	0	0	0	0	0	0
3	Data Source (must be set to 0x02)	0	0	0	0	0	0	1	0
4	Start Address (LSB) (must be set to zero)	0	0	0	0	0	0	0	0
5	Start Address (MSB) (must be set to zero)	0	0	0	0	0	0	0	0
6–15	Reserved (must be set to zero)	0	0	0	0	0	0	0	0

MfgCB

The mfg_load and mfg_read vendor-specific commands are passed down through the bulk pipe in the CBWCB portion of the CBW. The format of this MfgCB is shown as follows. Byte0 is a vendor-specific command designator whose value is configurable and set in the AT2LP configuration data. Byte 1 must be 0x27 to identify a MfgCB. Bytes 2 through 15 are reserved and must be set to zero.

The data transfer length is determined by the CBW Data Transfer Length specified in bytes 8 through 11 (dCBWDataTransferLength) of the CBW. The type and direction of the command is determined by the direction bit specified in byte 12, bit 7 (bmCBWFlags) of the CBW.

Table 9. Example MfgCB

Offset	MfgCB Byte Description	Bits							
		7	6	5	4	3	2	1	0
0	0 bVSCBSignature (set in configuration bytes)	0	0	1	0	0	1	0	0
1	1 bVSCBSubCommand (hardcoded 0x27)	0	0	1	0	0	1	1	1
2–15	2–15 Reserved (must be zero)	0	0	0	0	0	0	0	0

Mfg_load

During a Mfg_load, the AT2LP enters into Manufacturing Test Mode. Manufacturing Test Mode is provided as a means to implement board or system level interconnect tests. During Manufacturing Test Mode operation, all outputs not directly associated with USB operation are controllable. Normal control of the output pins are disabled. Control of the select AT2LP I/O pins and their tri-state controls are mapped to the ATAPI data packet associated with this request. (See Table 10 for an explanation of the required Mfg_load data format.) Any data length can be specified, but only bytes 0 through 3 are mapped to pins, so a length of 4 bytes is recommended. To exit Manufacturing Test Mode, a hard reset (toggle RESET#) is required.

Mfg_read

This USB request returns a 'snapshot' of select AT2LP input pins. AT2LP input pins not directly associated with USB operation can be sampled at any time during Manufacturing Test Mode operation. See Table 10 for an explanation of the Mfg_read data format. Any data length can be specified, but only bytes 0 through 3 contain usable information, so a length of 4 bytes is recommended.

Table 10. Mfg_read and Mfg_load Data Format

Byte	Bits	Read/Load	Function
0	7	R/L	ARESET#
	6	R	DA2
	5:4	R/L	CS#[1:0]
	3	R/L	DRVPWRVLD
	2:1	R/L	DA[1:0]
	0	R	INTRQ
1	7	L	DD[15:0] High Z Status 0 = High Z all DD pins 1 = Drive DD pins
	6	R	MFG_SEL 0 = Mass Storage Mode 1 = Manufacturing Mode
	5	R	VBUS_ATA_ENABLE
	4	R	DMARQ
	3	R	IORDY
	2	R/L	DMACK#
	1	R/L	DIOR#
	0	R/L	DIOW#
2	7:0	R/L	DD[7:0]
3	7:0	R/L	DD[15:8]

EEPROM Organization

The contents of the recommended 256-byte (2048-bit) I^2C EEPROM are arranged as follows. In Table 11, the column labeled 'Required Contents' contains the values that must be used for proper operation of the AT2LP. The column labeled 'Variable Contents' contains suggested entries and values that may vary (such as string lengths) according to the EEPROM data. Some values, such as the Vendor ID, Product ID and device serial number, must be customized to meet USB compliance. The 'AT2LP Blaster' tool in the CY4615B kit can be used to edit and program these values into an AT2LP-based product (refer to Figure 10). The 'AT2LP Primer' tool can be used to program AT2LP-based products in a manufacturing environment and provides for serial number randomization. See Board Manufacturing Test Mode on page 20 for details on how to use vendor-specific ATAPI commands to read and program the EEPROM.

The address pins on the serial EEPROM must be set such that the EEPROM is at physical address 2 (A0 = 0, A1 = 1, A2 = 0) or address 4 (A0 = 0, A1 = 0, A2 = 1) for EEPROM devices that are internally byte-addressed memories. It is recommended that the address pins be set this way even on EEPROMs that may indicate that the address pins are internal no-connects.

Figure 10. Snapshot of 'AT2LP Blaster' Utility

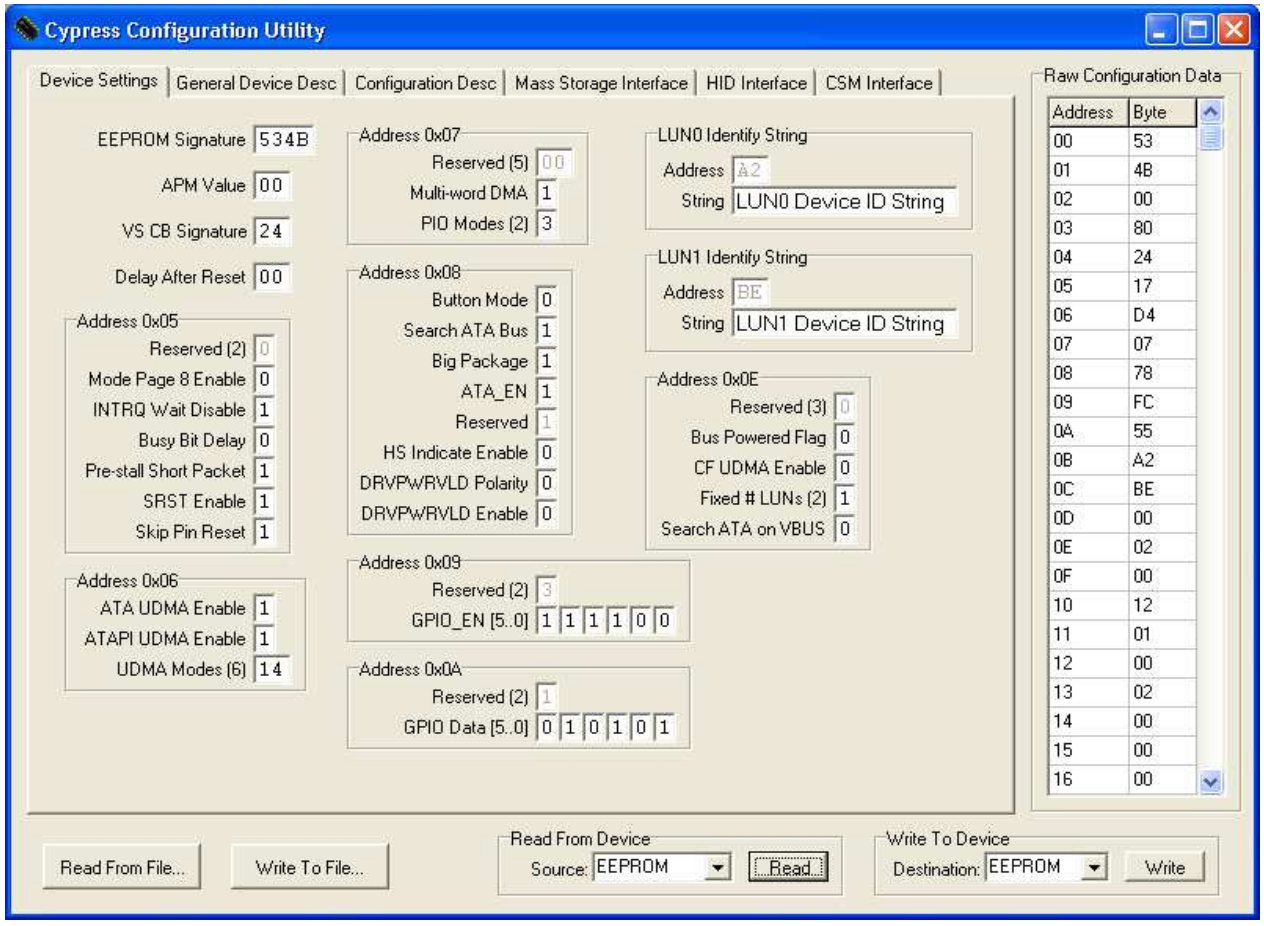


Table 11. Configuration Data Organization

Byte Address	Configuration Item Name	Configuration Item Description	Required Contents	Variable Contents
Note Devices running in Backward Compatibility (CY7C68300A) Mode must use the CY7C68300A EEPROM organization, and not the format shown in this document. Refer to the *CY7C68300A data sheet* for the CY7C68300A EEPROM format.				
AT2LP Configuration				
0x00	EEPROM signature byte 0	I^2C EEPROM signature byte 0. This byte must be 0x53 for proper AT2LP pin configuration.	0x53	
0x01	EEPROM signature byte 1	I^2C EEPROM signature byte 1. This byte must be 0x4B for proper AT2LP pin configuration.	0x4B	
0x02	APM Value	ATA Device Automatic Power Management Value. If an attached ATA device supports APM and this field contains other than 0x00, the AT2LP issues a SET_FEATURES command to enable APM with this value during the drive initialization process. Setting APM value to 0x00 disables this functionality. This value is ignored with ATAPI devices.		0x00
0x03	Reserved	Must be set to 0x00.		0x00
0x04	bVSCBSignature Value	Value in the first byte of the CBW CB field that designates that the CB is to be decoded as vendor-specific ATA commands instead of the ATAPI command block. See Functional Overview on page 16 for more detail on how this byte is used.		0x24
0x05	Reserved	Bits 7:6		0x07
	Enable mode page 8	Bit 5 Enable the write caching mode page (page 8). If this page is enabled, Windows disables write caching by default, which limits write performance. 0 = Disable mode page 8. 1 = Enable mode page 8.		
	Disable wait for INTRQ	Bit 4 Poll status register rather than waiting for INTRQ. Setting this bit to '1' improves USB BOT test results but may introduce compatibility problems with some devices. 0 = Wait for INTRQ. 1 = Poll status register instead of using INTRQ.		
	BUSY Bit Delay	Bit 3 Enable a delay of up to 120 ms at each read of the DRQ bit where the device data length does not match the host data length. This enables the CY7C68300C/CY7C68301C to work with most devices that incorrectly clear the BUSY bit before a valid status is present. 0 = No BUSY bit delay. 1 = Use BUSY bit delay.		
	Short Packet Before Stall	Bit 2 Determines if a short packet is sent before the STALL of an IN endpoint. The USB *Mass Storage Class Bulk-Only Specification* enables a device to send a short or zero-length IN packet before returning a STALL handshake for certain cases. Certain host controller drivers may require a short packet before STALL. 0 = Do not force a short packet before STALL. 1 = Force a short packet before STALL.		

Table 11. Configuration Data Organization *(continued)*

Byte Address	Configuration Item Name	Configuration Item Description	Required Contents	Variable Contents
	SRST Enable	Bit 1 Determines if the AT2LP is to do an SRST reset during drive initialization. At least one reset must be enabled. Do not set SRST to '0' and Skip Pin Reset to '1' at the same time. 0 = Do not perform SRST during initialization. 1 = Perform SRST during initialization.		
	Skip Pin Reset	Bit 0 Skip ARESET# assertion. When this bit is set, the AT2LP bypasses ARESET# during any initialization other than power up. Do not set SRST Enable to '0' and Skip Pin Reset to '1' at the same time. 0 = Allow ARESET# assertion for all device resets. 1 = Disable ARESET# assertion except for chip reset cycles.		
0x06	ATA UDMA Enable	Bit 7 Enable Ultra DMA data transfer support for ATA devices. If enabled, and if the ATA device reports UDMA support for the indicated modes, the AT2LP uses UDMA data transfers at the highest negotiated rate possible. 0 = Disable ATA device UDMA support. 1 = Enable ATA device UDMA support.		0xD4
	ATAPI UDMA Enable	Bit 6 Enable Ultra DMA data transfer support for ATAPI devices. If enabled, and if the ATAPI device reports UDMA support for the indicated modes, the AT2LP uses UDMA data transfers at the highest negotiated rate possible. 0 = Disable ATAPI device UDMA support. 1 = Enable ATAPI device UDMA support.		
	UDMA Modes	Bits 5:0 These bits select which UDMA modes are enabled. The AT2LP operates in the highest enabled UDMA mode supported by the device. The AT2LP supports UDMA modes 2, 3, and 4 only. Bit 5 = Reserved. Must be set to '0'. Bit 4 = Enable UDMA mode 4. Bit 3 = Enable UDMA mode 3. Bit 2 = Enable UDMA mode 2. Bit 1 = Reserved. Must be set to '0'. Bit 0 = Reserved. Must be set to '0'.		
0x07	Reserved	Bits 7:3 Must be set to '0'.		0x07
	Multiword DMA mode	Bit 2 This bit enables multiword DMA support. If this bit is set and the drive supports it, multiword DMA is used.		
	PIO Modes	Bits 1:0 These bits select which PIO modes are enabled. Setting to '1' enables use of that mode with the attached drive, if the drive supports it. Multiple bits may be set. The AT2LP operates in the highest enabled PIO mode supported by the device. The AT2LP supports PIO modes 0, 3, and 4 only. PIO mode 0 is always enabled and has no corresponding configuration bit. Bit 1 = Enable PIO mode 4. Bit 0 = Enable PIO mode 3.		

Table 11. Configuration Data Organization *(continued)*

Byte Address	Configuration Item Name	Configuration Item Description	Required Contents	Variable Contents
0x08	BUTTON_MODE	Bit 7 Button mode (100-pin package only). Sets ATAPUEN, PWR500# and DRVPWRVLD to become button inputs returned on bits 2, 1, and 0 of EP1IN. This bit must be set to '0' if the 56-pin packages are used. 0 = Disable button mode. 1 = Enable button mode.		0x78
	SEARCH_ATA_BUS	Bit 6 Search ATA bus after RESET to detect non-removable ATA and ATAPI devices. Systems with only a removable device (such as CF readers) must set this bit to '0'. Systems with at least one non-removable device must set this bit to '1'. 0 = Do not search for ATA devices. 1 = Search for ATA devices.		
	BIG_PACKAGE	Bit 5 Selects the 100- or 56-pin package pinout configuration. Using the wrong pinout may result in unpredictable behavior. 0 = Use 56-pin package pinout. 1 = Use 100-pin package pinout.		
	ATA_EN	Bit 4 Drive ATA bus when AT2LP is in suspend. For designs in which the ATA bus is shared between the AT2LP and another ATA master (such as an MP3 player), the AT2LP can place the ATA interface pins in a High Z state when it enters suspend. For designs that do not share the ATA bus, the ATA signals must be driven while the AT2LP is in suspend to avoid floating signals. 0 = Drive ATA signals when AT2LP is in suspend. 1 = Set ATA signals to High Z when AT2LP is in suspend.		
	Reserved	Bit 3 Reserved. This bit must be set to '0'.		
	Reserved	Bit 2 Reserved. This bit must be set to '0'		
	Drive Power Valid Polarity	Bit 1 Configure the logical polarity of the DRVPWRVLD input pin. 0 = Active LOW ('connector ground' indication) 1 = Active HIGH (power indication from device)		
	Drive Power Valid Enable	Bit 0 Enable the DRVPWRVLD pin. When this pin is enabled, the AT2LP enumerates a removable ATA device, such as CompactFlash or MicroDrive, as the IDE master device. Enabling this pin also affects other pins related to removable device operation. 0 = Disable removable ATA device support. 1 = Enable removable ATA device support.		